

# MOSFET - Power, Single P-Channel, SOT-23

**-60 V, 230 mΩ, -1.1 A**

## NVR5124PL

### Features

- Trench Technology
- NVR Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	-60	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2, 3)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub> -1.1 A
		T <sub>A</sub> = 100°C	-0.67
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)		T <sub>A</sub> = 25°C	P <sub>D</sub> 0.47 W
		T <sub>A</sub> = 100°C	0.19
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub> 25	A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)	I <sub>S</sub>	-0.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

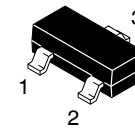
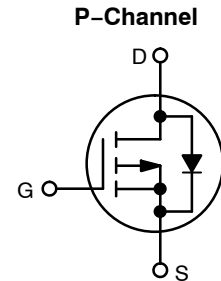
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 2)	R <sub>θJA</sub>	268	°C/W

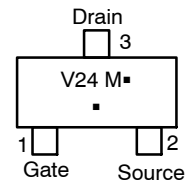
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
-60 V	230 mΩ @ -10 V	-1.1 A
	365 mΩ @ -4.5 V	



SOT-23  
CASE 318  
STYLE 21

### MARKING DIAGRAM/ PIN ASSIGNMENT



V24 = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NVR5124PLT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NVR5124PL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60	-	-	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -60 V	T <sub>J</sub> = 25°C	-	-	-1.0	μA
			T <sub>J</sub> = 125°C	-	-	-10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA	

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1.5	-	-2.5	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3 A	-	183	230	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3 A	-	280	365	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -5 A	4	-	-	S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = -25 V	-	240	-	pF
Output Capacitance	C <sub>oss</sub>		-	27.6	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	18.5	-	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -48 V, I <sub>D</sub> = -3 A	-	2.3	-	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>		-	0.5	-	
Gate-to-Source Charge	Q <sub>GS</sub>		-	0.9	-	
Gate-to-Drain Charge	Q <sub>GD</sub>		-	1.0	-	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -48 V, I <sub>D</sub> = -3 A	-	4.3	-	

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -48 V, I <sub>D</sub> = -3 A, R <sub>G</sub> = 2.5 Ω	-	6.6	-	ns
Rise Time	t <sub>r</sub>		-	10.6	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	12.2	-	
Fall Time	t <sub>f</sub>		-	3.5	-	

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -3 A	T <sub>J</sub> = 25°C	-	-0.88	-1.0	V
			T <sub>J</sub> = 125°C	-	-0.76	-	
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = -3 A	-	15	-	ns	
Charge Time	t <sub>a</sub>		-	13	-		
Discharge Time	t <sub>b</sub>		-	2.4	-		
Reverse Recovery Charge	Q <sub>RR</sub>		-	10	-	nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

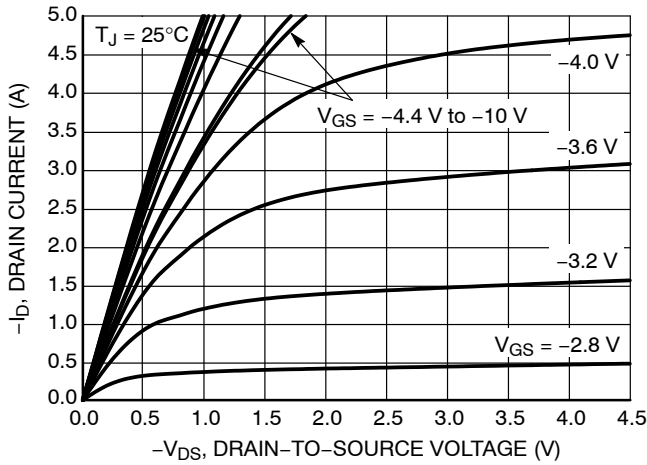


Figure 1. On-Region Characteristics

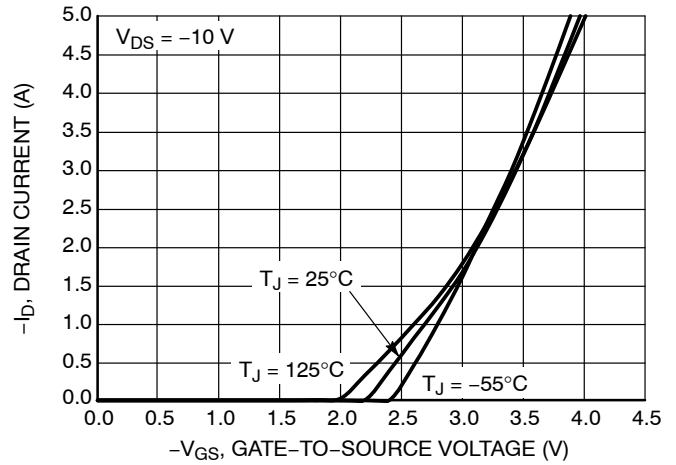


Figure 2. Transfer Characteristics

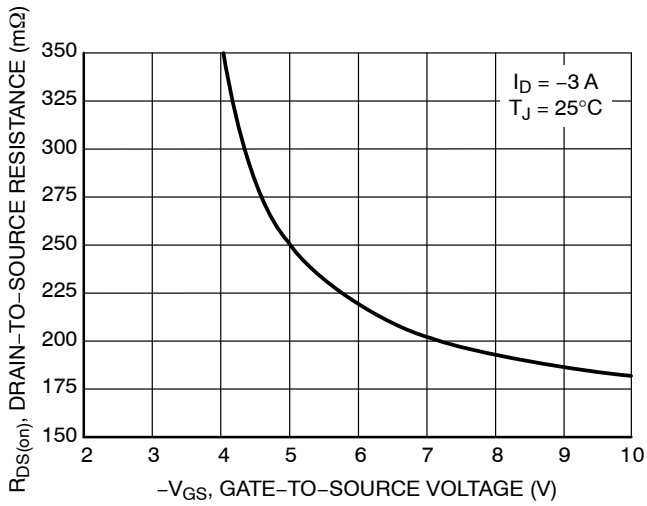


Figure 3. On-Resistance vs. Gate-to-Source Voltage

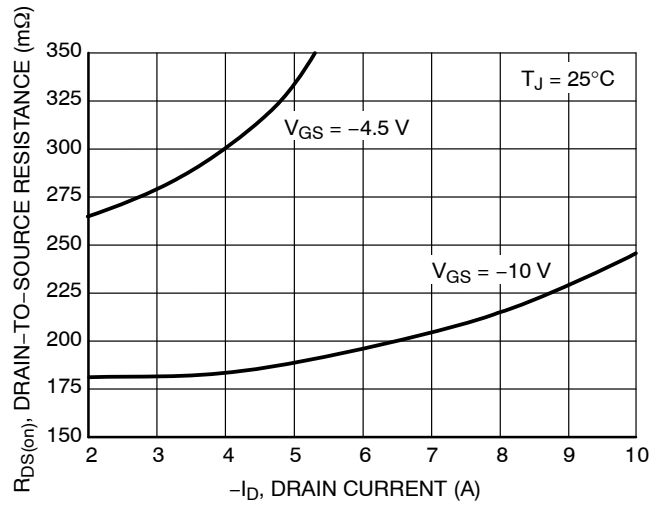


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

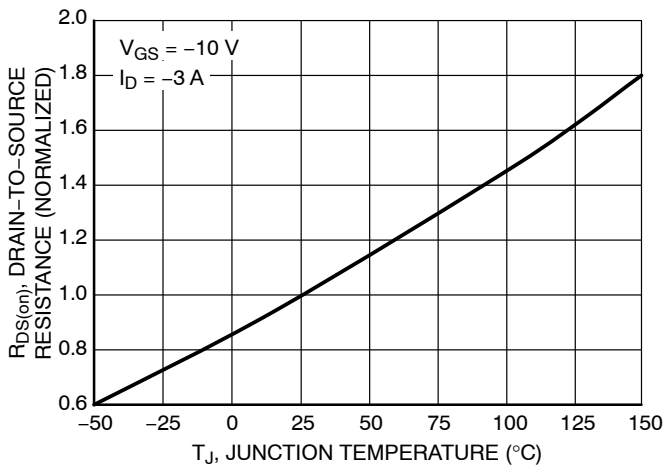


Figure 5. On-Resistance Variation with Temperature

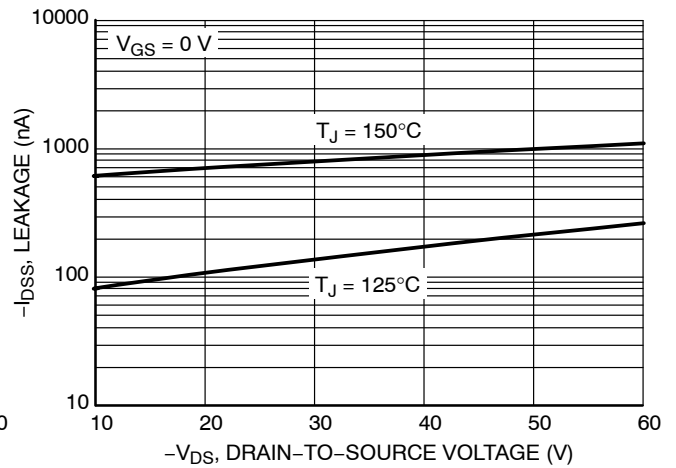


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

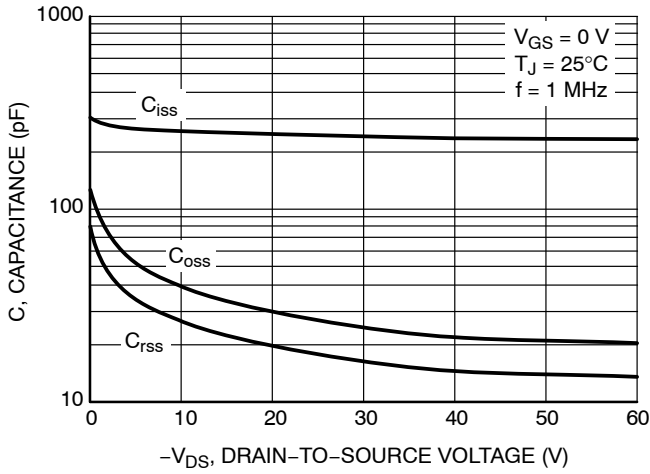


Figure 7. Capacitance Variation

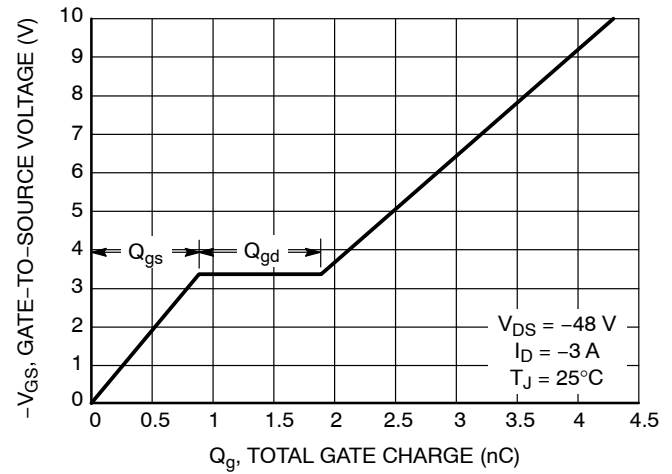


Figure 8. Gate-to-Source Voltage vs. Total Charge

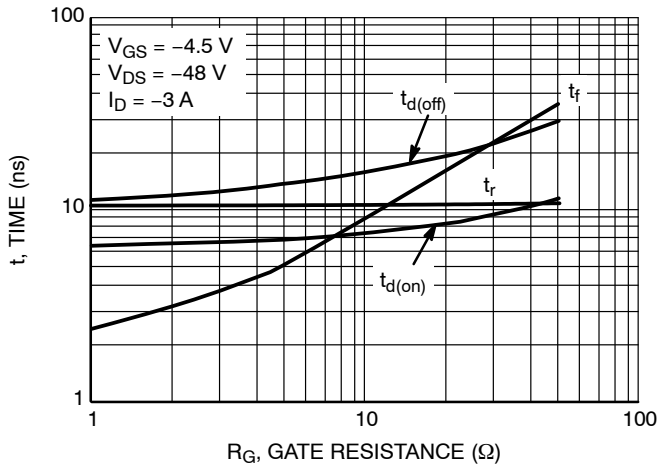


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

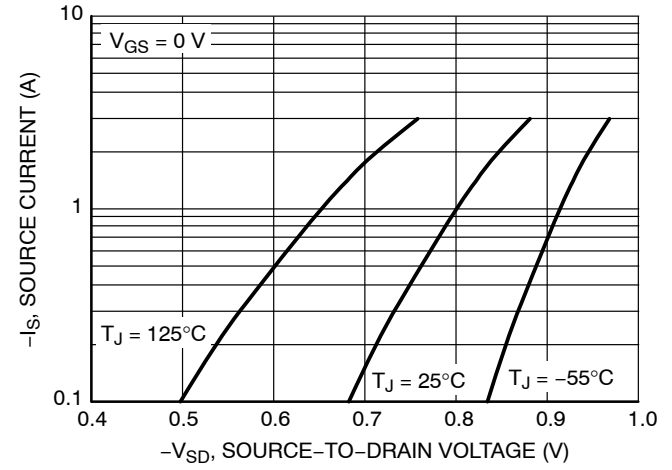


Figure 11. Diode Forward Voltage vs. Current

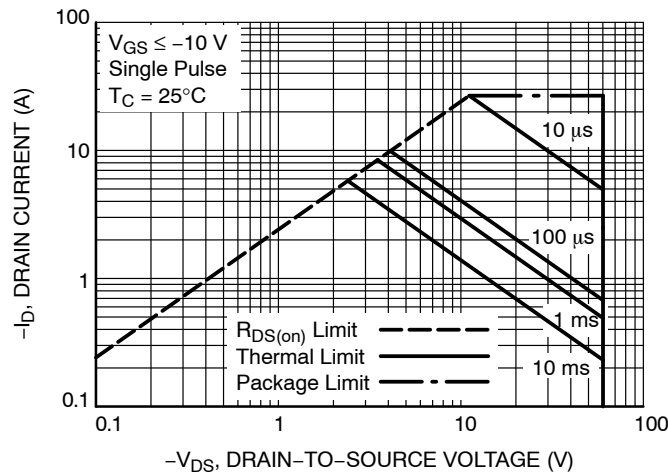


Figure 10. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL CHARACTERISTICS

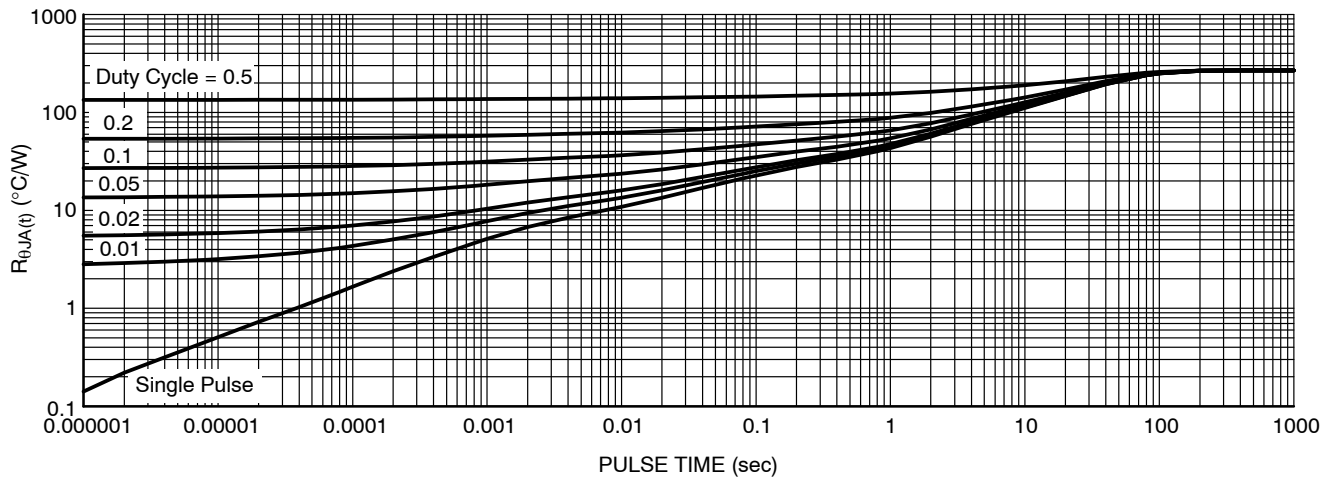
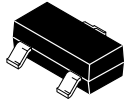


Figure 12. Thermal Response

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

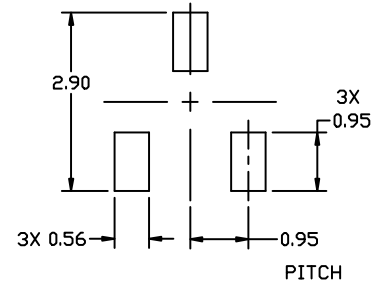
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

- |   |   |   |   |   |   |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |   |   |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |   |   |   |   |

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