# LPC1315/16/17/45/46/47

## 32-bit ARM Cortex-M3 microcontroller; up to 64 kB flash; up to 12 kB SRAM; USB device; USART; EEPROM

Rev. 3 — 20 September 2012 Product data sheet

## 1. General description

The LPC1315/16/17/45/46/47 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC1315/16/17/45/46/47 operate at CPU frequencies of up to 72 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

Equipped with a highly flexible and configurable Full-Speed USB 2.0 device controller available on the LPC1345/46/47, this series brings unparalleled design flexibility and seamless integration to today's demanding connectivity solutions.

The peripheral complement of the LPC1315/16/17/45/46/47 includes up to 64 kB of flash memory, 8 kB or 10 kB of SRAM data memory, one Fast-mode Plus $I^2C$-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, an 8-channel, 12-bit ADC, and up to 51 general purpose I/O pins.

## 2. Features and benefits

- System:
  - ARM Cortex-M3 r2p1 processor, running at frequencies of up to 72 MHz.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non Maskable Interrupt (NMI) input selectable from several input sources.
  - System tick timer.
- Memory:
  - Up to 64 kB on-chip flash program memory with a 256 byte page erase function.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash updates via USB supported.
  - Up to 4 kB on-chip EEPROM data memory with on-chip API support.
  - Up to 12 kB SRAM data memory.
  - 16 kB boot ROM with API support for USB API, power control, EEPROM, and flash IAP/ISP.

- Debug options:
  - Standard JTAG test interface for BSDL.
  - Serial Wire Debug.
  - Support for ETM ARM Cortex-M3 debug time stamping.
- Digital peripherals:
  - Up to 51 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, input inverter, and pseudo open-drain mode. Eight pins support programmable glitch filter.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin (P0_7).
  - High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a internal low-power WatchDog Oscillator (WDO).
  - Repetitive Interrupt Timer (RI Timer).
- Analog peripherals:
  - 12-bit ADC with eight input channels and sampling rates of up to 500 kSamples/s.
- Serial interfaces:
  - USB 2.0 full-speed device controller (LPC1345/46/47) with on-chip ROM-based USB driver library.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - $I^2C$-bus interface supporting the full $I^2C$-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator) with failure detector.
  - 12 MHz high-frequency Internal RC oscillator (IRC) trimmed to 1 % accuracy over the entire voltage and temperature range. The IRC can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB (LPC1345/46/47).
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.

- Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
- Processor wake-up from Deep power-down mode using one special function pin.
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
- Power-On Reset (POR).
- Brownout detect with up to four separate thresholds for interrupt and forced reset.

- Unique device serial number for identification.
- Single 3.3 V power supply (2.0 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, and HVQFN33 package.

## 3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

## 4. Ordering information

**Table 1. Ordering information**

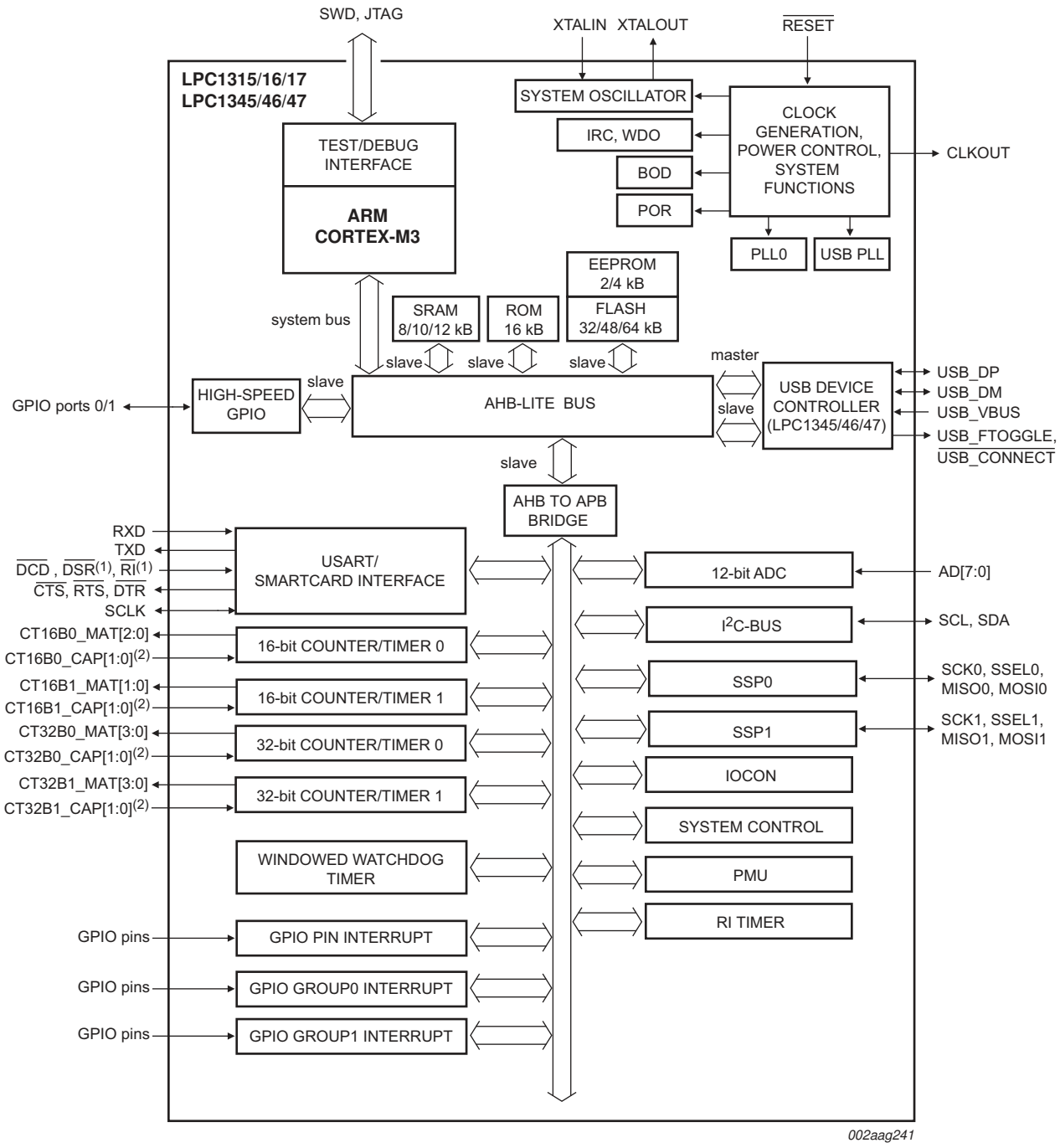
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC1345FHN33 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1345FBD48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1346FHN33 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1346FBD48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1347FHN33 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1347FBD48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1347FBD64 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1315FHN33 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1315FBD48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1316FHN33 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1316FBD48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1317FHN33 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1317FBD48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1317FBD64 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash [kB] | SRAM [kB] | | | EEPROM [kB] | USB device | SSP | I2C/ FM+ | ADC channels | GPIO pins |
|---|---|---|---|---|---|---|---|---|---|---|
| | | SRAM0 | USB SRAM | SRAM1 | | | | | | |
| LPC1345FHN33 | 32 | 8 | 2 | - | 2 | yes | 2 | 1 | 8 | 26 |
| LPC1345FBD48 | 32 | 8 | 2 | - | 2 | yes | 2 | 1 | 8 | 40 |
| LPC1346FHN33 | 48 | 8 | 2 | - | 4 | yes | 2 | 1 | 8 | 26 |
| LPC1346FBD48 | 48 | 8 | 2 | - | 4 | yes | 2 | 1 | 8 | 40 |
| LPC1347FHN33 | 64 | 8 | 2 | 2 | 4 | yes | 2 | 1 | 8 | 26 |
| LPC1347FBD48 | 64 | 8 | 2 | 2 | 4 | yes | 2 | 1 | 8 | 40 |
| LPC1347FBD64 | 64 | 8 | 2 | 2 | 4 | yes | 2 | 1 | 8 | 51 |
| LPC1315FHN33 | 32 | 8 | - | - | 2 | no | 2 | 1 | 8 | 28 |
| LPC1315FBD48 | 32 | 8 | - | - | 2 | no | 2 | 1 | 8 | 40 |
| LPC1316FHN33 | 48 | 8 | - | - | 4 | no | 2 | 1 | 8 | 28 |
| LPC1316FBD48 | 48 | 8 | - | - | 4 | no | 2 | 1 | 8 | 40 |
| LPC1317FHN33 | 64 | 8 | - | 2 | 4 | no | 2 | 1 | 8 | 28 |
| LPC1317FBD48 | 64 | 8 | - | 2 | 4 | no | 2 | 1 | 8 | 40 |
| LPC1317FBD64 | 64 | 8 | - | 2 | 4 | no | 2 | 1 | 8 | 51 |

# 5. Block diagram




(1) Available on LQFP48 and LQFP64 packages only.

(2) CT16B0_CAP1, CT16B1_CAP1, CT32B1_CAP1 inputs available on LQFP64 packages only. CT32B0_CAP0 input available on LQFP48 and LQFP64 packages only.

**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

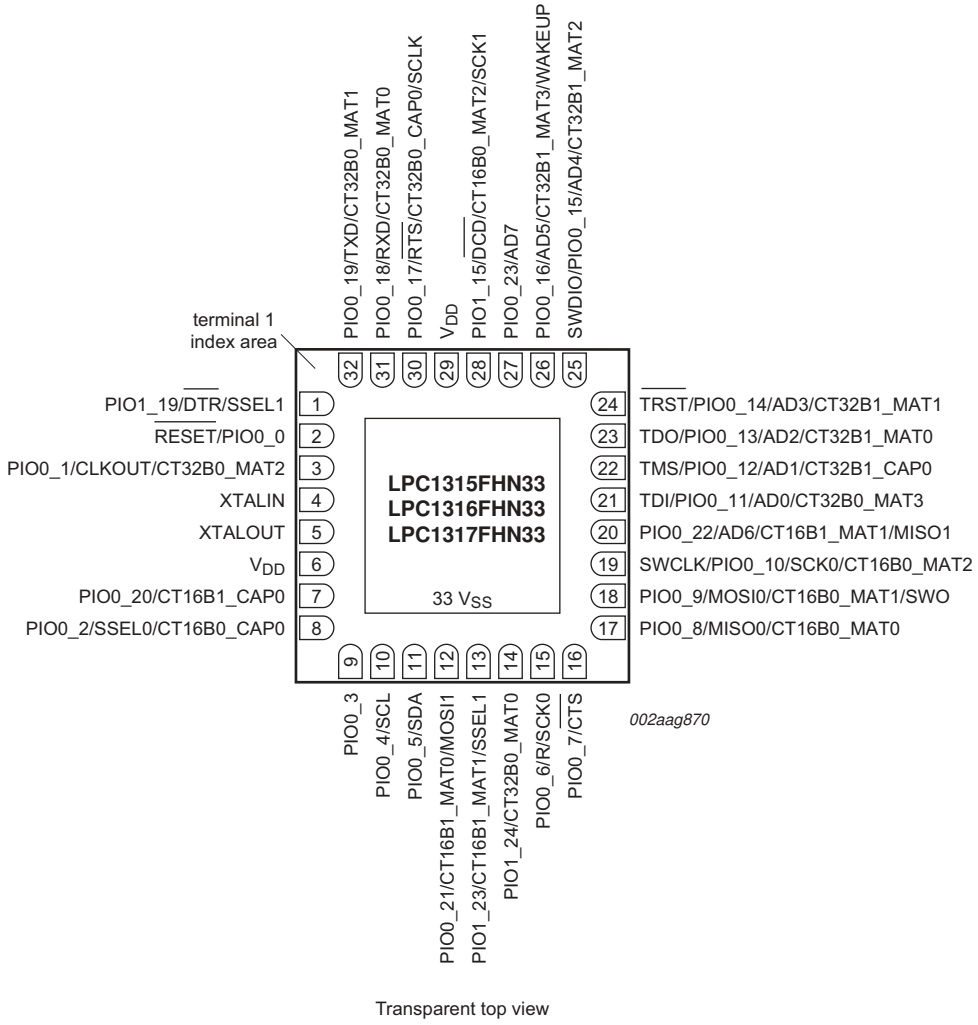



**Fig 2. Pin configuration HVQFN33 package (LPC1315/16/17 - no USB)**

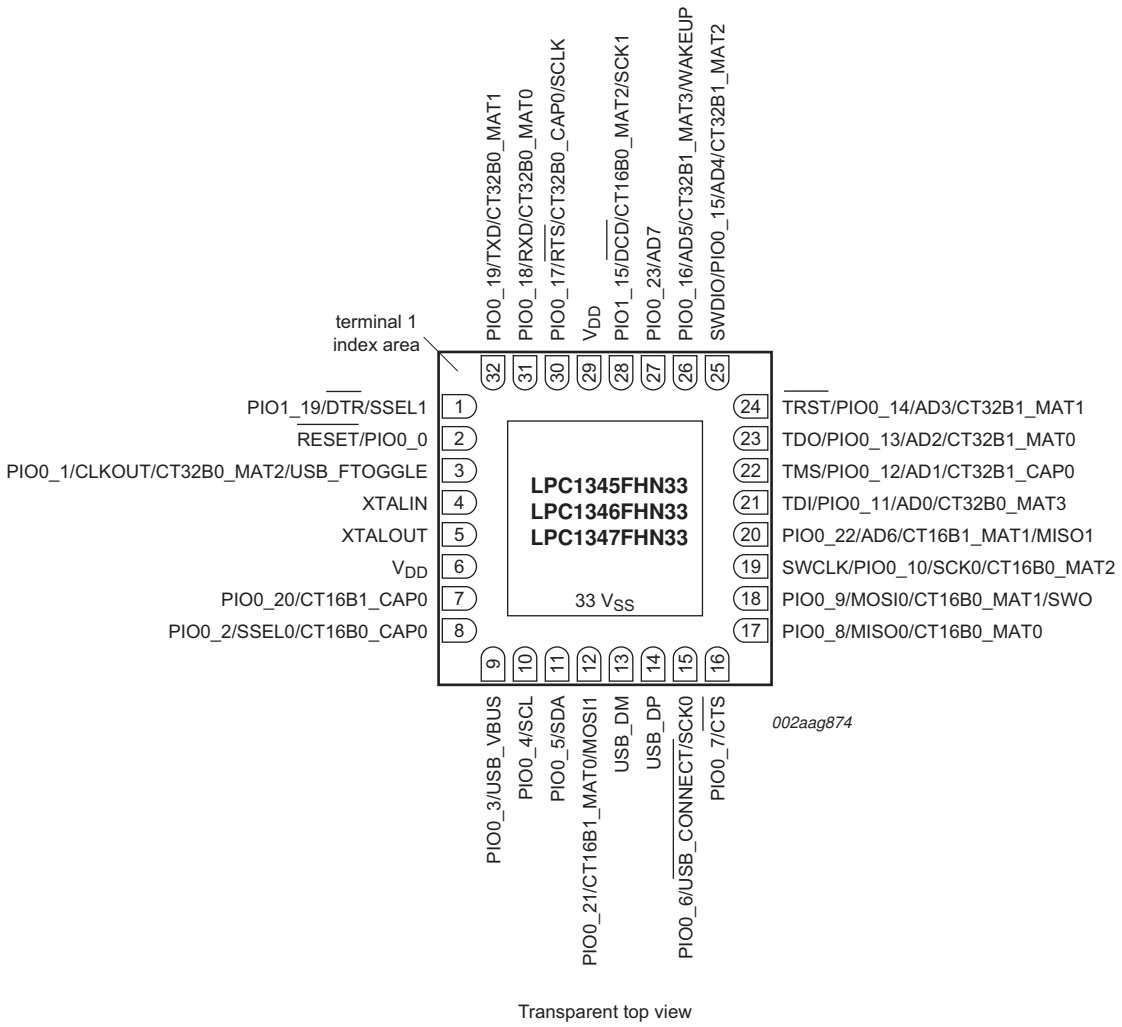



**Fig 3. Pin configuration HVQFN33 package (LPC1345/46/47 - with USB)**

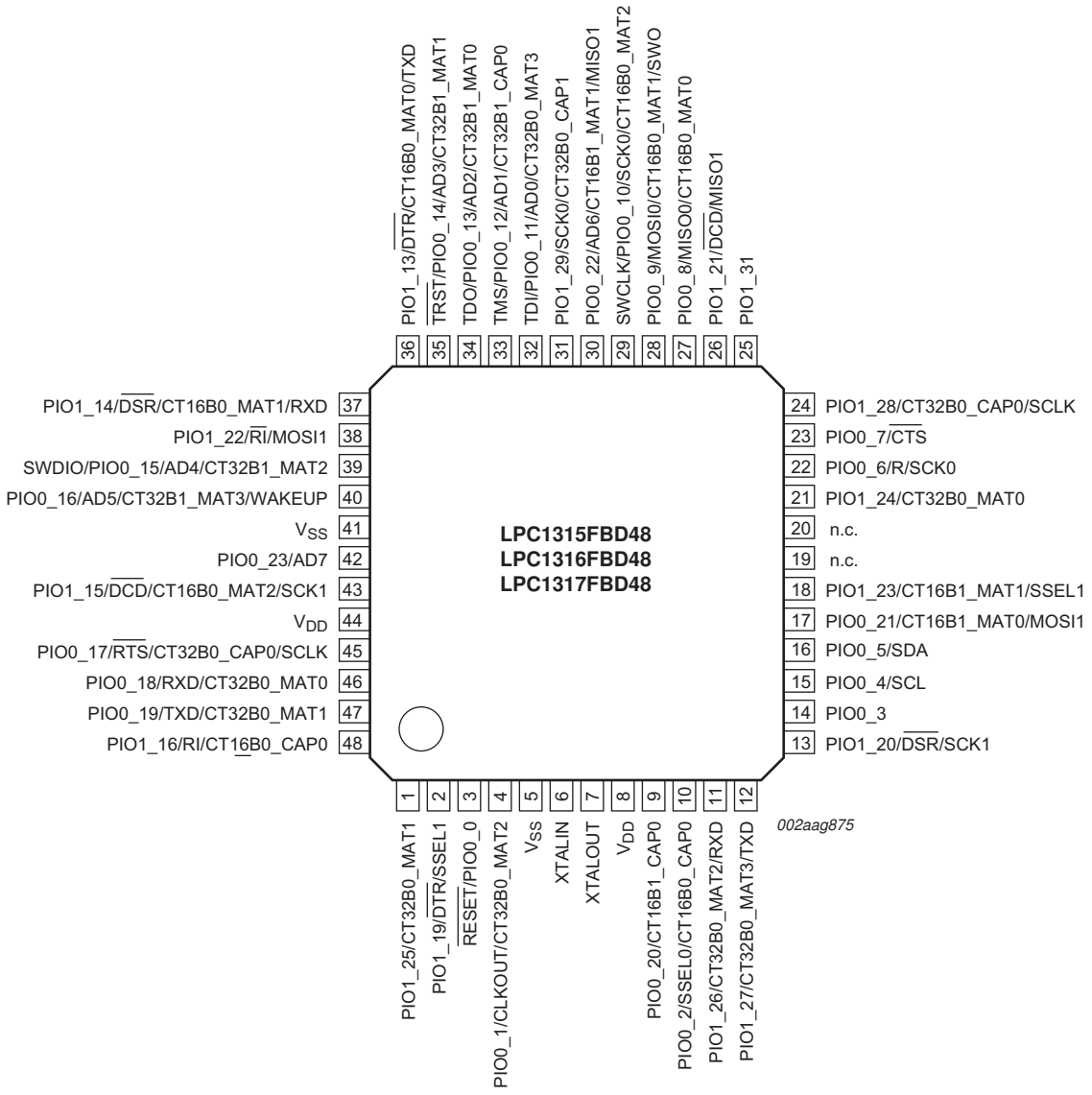



**Fig 4. Pin configuration LQFP48 package (LPC1315/16/17 - no USB)**

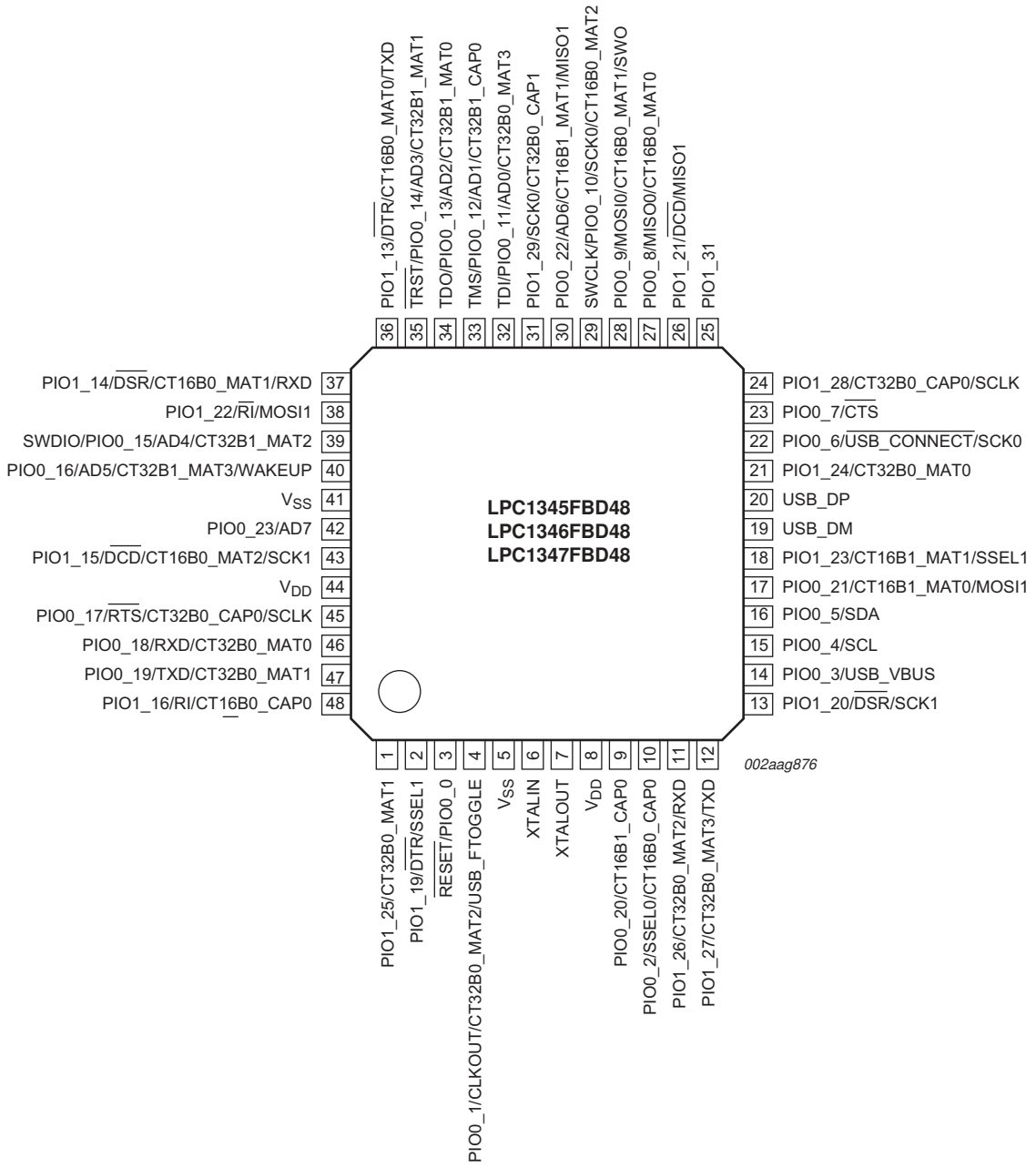
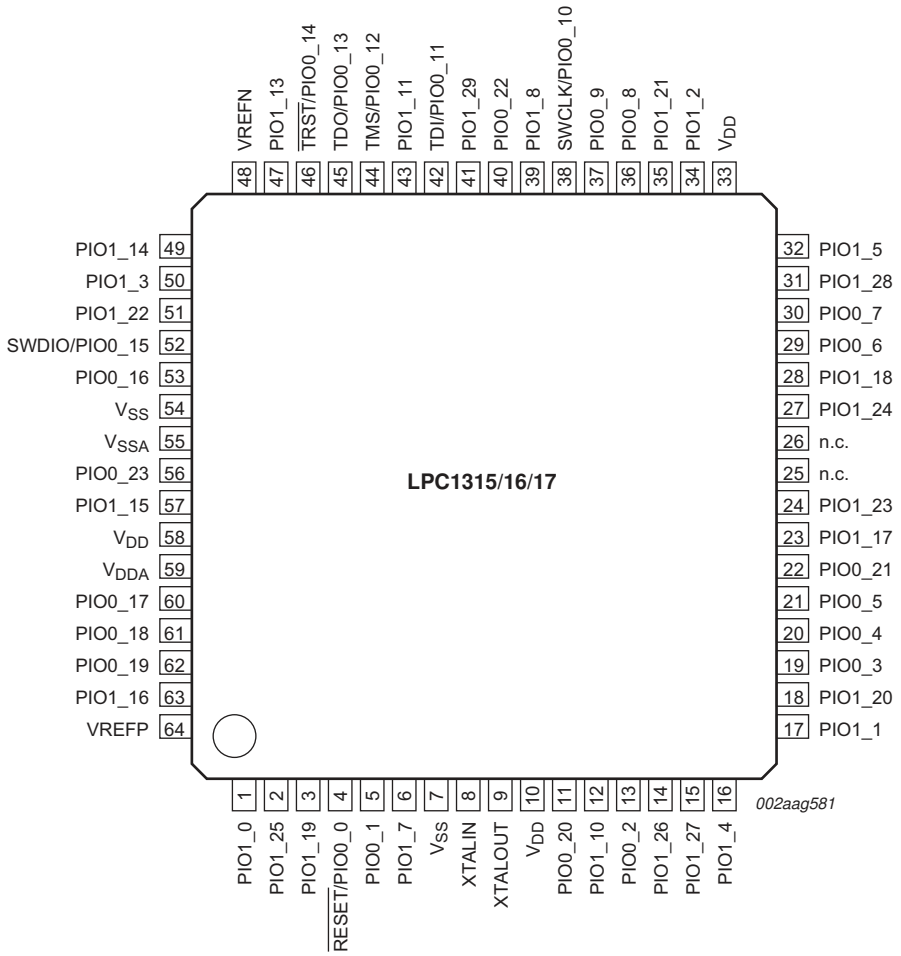



**Fig 5. Pin configuration LQFP48 package (LPC1345/46/47 - with USB)**




See Table 3 for the full pin name.

**Fig 6. Pin configuration LQFP64 package (LPC1315/16/17 - no USB)**

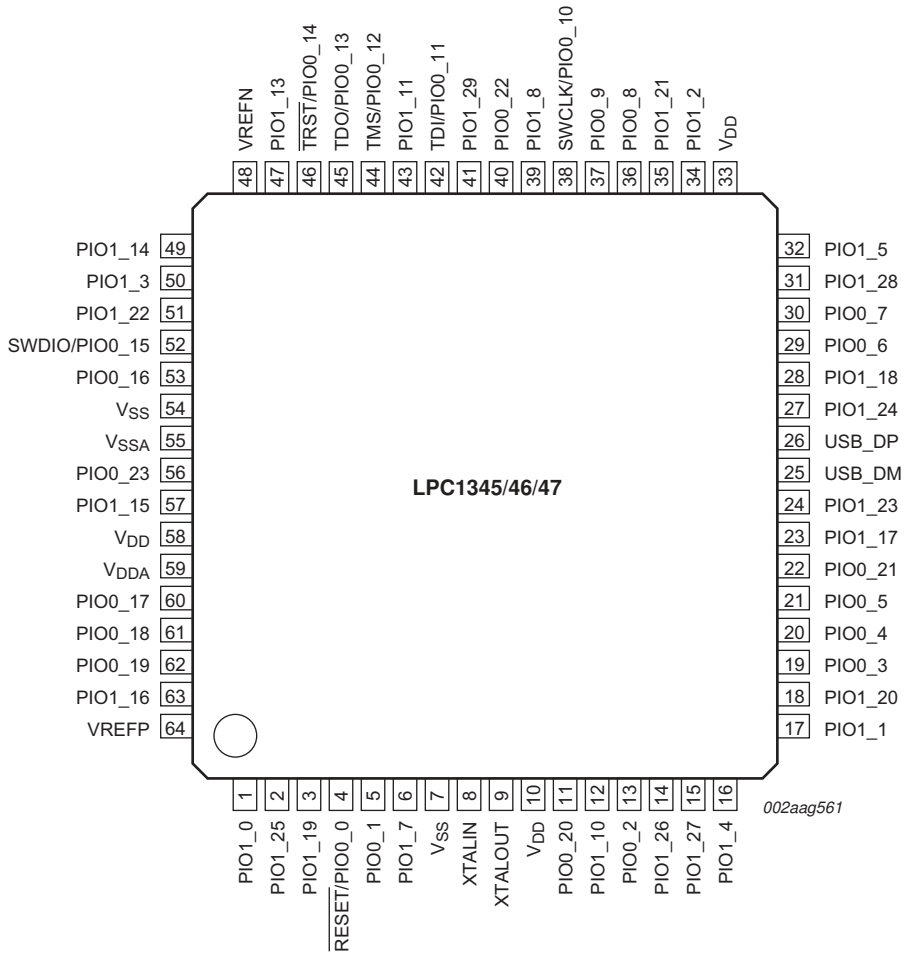



**Fig 7. Pin configuration LQFP64 package (LPC1345/46/47 - with USB)**

## 6.2 Pin description

**Table 3. Pin description (LPC1315/16/17 - no USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RESET}}$/PIO0_0 | 4 | 3 | 2 | [2] | I; PU | I | **$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. |
| | | | | | - | I/O | **PIO0_0 —** General purpose digital input/output pin. |
| PIO0_1/CLKOUT/ CT32B0_MAT2 | 5 | 4 | 3 | [3] | I; PU | I/O | **PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. |
| | | | | | - | O | **CLKOUT —** Clockout pin. |
| | | | | | - | O | **CT32B0_MAT2 —** Match output 2 for 32-bit timer 0. |
| PIO0_2/SSEL0/ CT16B0_CAP0 | 13 | 10 | 8 | [3] | I; PU | I/O | **PIO0_2 —** General purpose digital input/output pin. |
| | | | | | | I/O | **SSEL0 —** Slave select for SSP0. |
| | | | | | | I | **CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0. |
| PIO0_3 | 19 | 14 | 9 | [3] | I; PU | I/O | **PIO0_3 —** General purpose digital input/output pin. |
| PIO0_4/SCL | 20 | 15 | 10 | [4] | IA | I/O | **PIO0_4 —** General purpose digital input/output pin (open-drain). |
| | | | | | - | I/O | **SCL —** $I^2C$-bus clock input/output (open-drain). High-current sink only if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| PIO0_5/SDA | 21 | 16 | 11 | [4] | IA | I/O | **PIO0_5 —** General purpose digital input/output pin (open-drain). |
| | | | | | - | I/O | **SDA —** $I^2C$-bus data input/output (open-drain). High-current sink only if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| PIO0_6/R/ SCK0 | 29 | 22 | 15 | [3] | I; PU | I/O | **PIO0_6 —** General purpose digital input/output pin. |
| | | | | | - | - | **R —** Reserved. |
| | | | | | - | I/O | **SCK0 —** Serial clock for SSP0. |
| PIO0_7/$\overline{\text{CTS}}$ | 30 | 23 | 16 | [5] | I; PU | I/O | **PIO0_7 —** General purpose digital input/output pin (high-current output driver). |
| | | | | | - | I | **$\overline{\text{CTS}}$ —** Clear To Send input for USART. |
| PIO0_8/MISO0/ CT16B0_MAT0 | 36 | 27 | 17 | [3] | I; PU | I/O | **PIO0_8 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **MISO0 —** Master In Slave Out for SSP0. |
| | | | | | - | O | **CT16B0_MAT0 —** Match output 0 for 16-bit timer 0. |
| PIO0_9/MOSI0/ CT16B0_MAT1/ SWO | 37 | 28 | 18 | [3] | I; PU | I/O | **PIO0_9 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **MOSI0 —** Master Out Slave In for SSP0. |
| | | | | | - | O | **CT16B0_MAT1 —** Match output 1 for 16-bit timer 0. |
| | | | | | - | O | **SWO —** Serial wire trace output. |

**Table 3. Pin description (LPC1315/16/17 - no USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| SWCLK/PIO0_10/SCK0/ CT16B0_MAT2 | 38 | 29 | 19 | [3] | I; PU | I | **SWCLK —** Serial wire clock and test clock TCK for JTAG interface. |
| | | | | | - | I/O | **PIO0_10 —** General purpose digital input/output pin. |
| | | | | | - | O | **SCK0 —** Serial clock for SSP0. |
| | | | | | - | O | **CT16B0_MAT2 —** Match output 2 for 16-bit timer 0. |
| TDI/PIO0_11/AD0/ CT32B0_MAT3 | 42 | 32 | 21 | [6] | I; PU | I | **TDI —** Test Data In for JTAG interface. |
| | | | | | - | I/O | **PIO0_11 —** General purpose digital input/output pin. |
| | | | | | - | I | **AD0 —** A/D converter, input 0. |
| | | | | | - | O | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| TMS/PIO0_12/AD1/ CT32B1_CAP0 | 44 | 33 | 22 | [6] | I; PU | I | **TMS —** Test Mode Select for JTAG interface. |
| | | | | | - | I/O | **PIO_12 —** General purpose digital input/output pin. |
| | | | | | - | I | **AD1 —** A/D converter, input 1. |
| | | | | | - | I | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| TDO/PIO0_13/AD2/ CT32B1_MAT0 | 45 | 34 | 23 | [6] | I; PU | O | **TDO —** Test Data Out for JTAG interface. |
| | | | | | - | I/O | **PIO0_13 —** General purpose digital input/output pin. |
| | | | | | - | I | **AD2 —** A/D converter, input 2. |
| | | | | | - | O | **CT32B1_MAT0 —** Match output 0 for 32-bit timer 1. |
| $\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1 | 46 | 35 | 24 | [6] | I; PU | I | **$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. |
| | | | | | - | I/O | **PIO0_14 —** General purpose digital input/output pin. |
| | | | | | - | I | **AD3 —** A/D converter, input 3. |
| | | | | | - | O | **CT32B1_MAT1 —** Match output 1 for 32-bit timer 1. |
| SWDIO/PIO0_15/AD4/ CT32B1_MAT2 | 52 | 39 | 25 | [6] | I; PU | I/O | **SWDIO —** Serial wire debug input/output. |
| | | | | | - | I/O | **PIO0_15 —** General purpose digital input/output pin. |
| | | | | | - | I | **AD4 —** A/D converter, input 4. |
| | | | | | - | O | **CT32B1_MAT2 —** Match output 2 for 32-bit timer 1. |
| PIO0_16/AD5/ CT32B1_MAT3/WAKEUP | 53 | 40 | 26 | [7] | I; PU | I/O | **PIO0_16 —** General purpose digital input/output pin. |
| | | | | | - | I | **AD5 —** A/D converter, input 5. |
| | | | | | - | O | **CT32B1_MAT3 —** Match output 3 for 32-bit timer 1. |
| | | | | | - | I | **WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part. |
| PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK | 60 | 45 | 30 | [3] | I; PU | I/O | **PIO0_17 —** General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{RTS}}$ —** Request To Send output for USART. |
| | | | | | - | I | **CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. |
| | | | | | - | I/O | **SCLK —** Serial clock input/output for USART in synchronous mode. |

**Table 3. Pin description (LPC1315/16/17 - no USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO0_18/RXD/ CT32B0_MAT0 | 61 | 46 | 31 | [3] | I; PU | I/O | **PIO0_18** — General purpose digital input/output pin. |
| | | | | | - | I | **RXD** — Receiver input for USART. Used in UART ISP mode. |
| | | | | | - | O | **CT32B0_MAT0** — Match output 0 for 32-bit timer 0. |
| PIO0_19/TXD/ CT32B0_MAT1 | 62 | 47 | 32 | [3] | I; PU | I/O | **PIO0_19** — General purpose digital input/output pin. |
| | | | | | - | O | **TXD** — Transmitter output for USART. Used in UART ISP mode. |
| | | | | | - | O | **CT32B0_MAT1** — Match output 1 for 32-bit timer 0. |
| PIO0_20/CT16B1_CAP0 | 11 | 9 | 7 | [3] | I; PU | I/O | **PIO0_20** — General purpose digital input/output pin. |
| | | | | | - | I | **CT16B1_CAP0** — Capture input 0 for 16-bit timer 1. |
| PIO0_21/CT16B1_MAT0/ MOSI1 | 22 | 17 | 12 | [3] | I; PU | I/O | **PIO0_21** — General purpose digital input/output pin. |
| | | | | | - | O | **CT16B1_MAT0** — Match output 0 for 16-bit timer 1. |
| | | | | | - | I/O | **MOSI1** — Master Out Slave In for SSP1. |
| PIO0_22/AD6/ CT16B1_MAT1/MISO1 | 40 | 30 | 20 | [6] | I; PU | I/O | **PIO0_22** — General purpose digital input/output pin. |
| | | | | | - | I | **AD6** — A/D converter, input 6. |
| | | | | | - | O | **CT16B1_MAT1** — Match output 1 for 16-bit timer 1. |
| | | | | | - | I/O | **MISO1** — Master In Slave Out for SSP1. |
| PIO0_23/AD7 | 56 | 42 | 27 | [6] | I; PU | I/O | **PIO0_23** — General purpose digital input/output pin. |
| | | | | | - | I | **AD7** — A/D converter, input 7. |
| PIO1_0/CT32B1_MAT0 | 1 | - | - | [3] | I; PU | I/O | **PIO1_0** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT0** — Match output 0 for 32-bit timer 1. |
| PIO1_1/CT32B1_MAT1 | 17 | - | - | [3] | I; PU | I/O | **PIO1_1** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT1** — Match output 1 for 32-bit timer 1. |
| PIO1_2/CT32B1_MAT2 | 34 | - | - | [3] | I; PU | I/O | **PIO1_2** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT2** — Match output 2 for 32-bit timer 1. |
| PIO1_3/CT32B1_MAT3 | 50 | - | - | [3] | I; PU | I/O | **PIO1_3** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT3** — Match output 3 for 32-bit timer 1. |
| PIO1_4/CT32B1_CAP0 | 16 | - | - | [3] | I; PU | I/O | **PIO1_4** — General purpose digital input/output pin. |
| | | | | | - | I | **CT32B1_CAP0** — Capture input 0 for 32-bit timer 1. |
| PIO1_5/CT32B1_CAP1 | 32 | - | - | [3] | I; PU | I/O | **PIO1_5** — General purpose digital input/output pin. |
| | | | | | - | I | **CT32B1_CAP1** — Capture input 1 for 32-bit timer 1. |
| PIO1_7 | 6 | - | - | [3] | I; PU | I/O | **PIO1_7** — General purpose digital input/output pin. |
| PIO1_8 | 39 | - | - | [3] | I; PU | I/O | **PIO1_8** — General purpose digital input/output pin. |
| PIO1_10 | 12 | - | - | [3] | I; PU | I/O | **PIO1_10** — General purpose digital input/output pin. |
| PIO1_11 | 43 | - | - | [3] | I; PU | I/O | **PIO1_11** — General purpose digital input/output pin. |

**Table 3. Pin description (LPC1315/16/17 - no USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD | 47 | 36 | - | [3] | I; PU | I/O | **PIO1_13** — General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{DTR}}$** — Data Terminal Ready output for USART. |
| | | | | | - | O | **CT16B0_MAT0** — Match output 0 for 16-bit timer 0. |
| | | | | | - | O | **TXD** — Transmitter output for USART. |
| PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD | 49 | 37 | - | [3] | I; PU | I/O | **PIO1_14** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DSR}}$** — Data Set Ready input for USART. |
| | | | | | - | O | **CT16B0_MAT1** — Match output 1 for 16-bit timer 0. |
| | | | | | - | I | **RXD** — Receiver input for USART. |
| PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1 | 57 | 43 | 28 | [3] | I; PU | I/O | **PIO1_15** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DCD}}$** — Data Carrier Detect input for USART. |
| | | | | | - | O | **CT16B0_MAT2** — Match output 2 for 16-bit timer 0. |
| | | | | | - | I/O | **SCK1** — Serial clock for SSP1. |
| PIO1_16/$\overline{\text{RI}}$/CT16B0_CAP0 | 63 | 48 | - | [3] | I; PU | I/O | **PIO1_16** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{RI}}$** — Ring Indicator input for USART. |
| | | | | | - | I | **CT16B0_CAP0** — Capture input 0 for 16-bit timer 0. |
| PIO1_17/CT16B0_CAP1/ RXD | 23 | - | - | [3] | I; PU | I/O | **PIO1_17** — General purpose digital input/output pin. |
| | | | | | - | I | **CT16B0_CAP1** — Capture input 1 for 16-bit timer 0. |
| | | | | | - | I | **RXD** — Receiver input for USART. |
| PIO1_18/CT16B1_CAP1/ TXD | 28 | - | - | [3] | I; PU | I/O | **PIO1_18** — General purpose digital input/output pin. |
| | | | | | - | I | **CT16B1_CAP1** — Capture input 1 for 16-bit timer 1. |
| | | | | | - | O | **TXD** — Transmitter output for USART. |
| PIO1_19/$\overline{\text{DTR}}$/SSEL1 | 3 | 2 | 1 | [3] | I; PU | I/O | **PIO1_19** — General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{DTR}}$** — Data Terminal Ready output for USART. |
| | | | | | - | I/O | **SSEL1** — Slave select for SSP1. |
| PIO1_20/$\overline{\text{DSR}}$/SCK1 | 18 | 13 | - | [3] | I; PU | I/O | **PIO1_20** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DSR}}$** — Data Set Ready input for USART. |
| | | | | | - | I/O | **SCK1** — Serial clock for SSP1. |
| PIO1_21/$\overline{\text{DCD}}$/MISO1 | 35 | 26 | - | [3] | I; PU | I/O | **PIO1_21** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DCD}}$** — Data Carrier Detect input for USART. |
| | | | | | - | I/O | **MISO1** — Master In Slave Out for SSP1. |
| PIO1_22/$\overline{\text{RI}}$/MOSI1 | 51 | 38 | - | [3] | I; PU | I/O | **PIO1_22** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{RI}}$** — Ring Indicator input for USART. |
| | | | | | - | I/O | **MOSI1** — Master Out Slave In for SSP1. |
| PIO1_23/CT16B1_MAT1/ SSEL1 | 24 | 18 | 13 | [3] | I; PU | I/O | **PIO1_23** — General purpose digital input/output pin. |
| | | | | | - | O | **CT16B1_MAT1** — Match output 1 for 16-bit timer 1. |
| | | | | | - | I/O | **SSEL1** — Slave select for SSP1. |
| PIO1_24/CT32B0_MAT0 | 27 | 21 | 14 | [3] | I; PU | I/O | **PIO1_24** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT0** — Match output 0 for 32-bit timer 0. |

**Table 3. Pin description (LPC1315/16/17 - no USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO1_25/CT32B0_MAT1 | 2 | 1 | - | [3] | I; PU | I/O | **PIO1_25 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT1 —** Match output 1 for 32-bit timer 0. |
| PIO1_26/CT32B0_MAT2/ RXD | 14 | 11 | - | [3] | I; PU | I/O | **PIO1_26 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT2 —** Match output 2 for 32-bit timer 0. |
| | | | | | - | I | **RXD —** Receiver input for USART. |
| PIO1_27/CT32B0_MAT3/ TXD | 15 | 12 | - | [3] | I; PU | I/O | **PIO1_27 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| | | | | | - | O | **TXD —** Transmitter output for USART. |
| PIO1_28/CT32B0_CAP0/ SCLK | 31 | 24 | - | [3] | I; PU | I/O | **PIO1_28 —** General purpose digital input/output pin. |
| | | | | | - | I | **CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. |
| | | | | | - | I/O | **SCLK —** Serial clock input/output for USART in synchronous mode. |
| PIO1_29/SCK0/ CT32B0_CAP1 | 41 | 31 | - | [3] | I; PU | I/O | **PIO1_29 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **SCK0 —** Serial clock for SSP0. |
| | | | | | - | I | **CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. |
| PIO1_31 | - | 25 | - | [3] | I; PU | I/O | **PIO1_31 —** General purpose digital input/output pin. |
| n.c. | 25 | 19 | - | | - | - | Not connected. |
| n.c. | 26 | 20 | - | | - | - | Not connected. |
| XTALIN | 8 | 6 | 4 | [8] | - | - | Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V. |
| XTALOUT | 9 | 7 | 5 | [8] | - | - | Output from the oscillator amplifier. |
| $V_{DDA}$ | 59 | - | - | | - | - | Analog 3.3 V pad supply voltage: This should be nominally the same voltage as $V_{DD}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC. This pin should be tied to 3.3 V if the ADC is not used. |
| VREFN | 48 | - | - | | - | - | ADC negative reference voltage: This should be nominally the same voltage as $V_{SS}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. |

**Table 3. Pin description (LPC1315/16/17 - no USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|
| VREFP | 64 | - | - | - | - | ADC positive reference voltage: This should be nominally the same voltage as $V_{DDA}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used. |
| $V_{SSA}$ | 55 | - | - | - | - | Analog ground: 0 V reference. This should nominally be the same voltage as $V_{SS}$Product data sheet but should be isolated to minimize noise and error. |
| $V_{DD}$ | 10; 33; 58 | 8; 44 | 6; 29 | - | - | Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage. |
| $V_{SS}$ | 7; 54 | 5; 41 | 33 | - | - | Ground. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 33 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32).

[4] $I^2C$-bus pins compliant with the $I^2C$-bus specification for $I^2C$ standard mode, $I^2C$ Fast-mode, and $I^2C$ Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes programmable digital input glitch filter.

[7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes digital input glitch filter.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

**Table 4. Pin description (LPC1345/46/47 - with USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RESET}}$/PIO0_0 | 4 | 3 | 2 | [2] | I; PU | I | **$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. |
| | | | | | - | I/O | **PIO0_0 —** General purpose digital input/output pin. |
| PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE | 5 | 4 | 3 | [3] | I; PU | I/O | **PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration. |
| | | | | | - | O | **CLKOUT —** Clockout pin. |
| | | | | | - | O | **CT32B0_MAT2 —** Match output 2 for 32-bit timer 0. |
| | | | | | - | O | **USB_FTOGGLE —** USB 1 ms Start-of-Frame signal. |
| PIO0_2/SSEL0/ CT16B0_CAP0 | 13 | 10 | 8 | [3] | I; PU | I/O | **PIO0_2 —** General purpose digital input/output pin. |
| | | | | | | I/O | **SSEL0 —** Slave select for SSP0. |
| | | | | | | I | **CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0. |
| PIO0_3/USB_VBUS | 19 | 14 | 9 | [3] | I; PU | I/O | **PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration. |
| | | | | | - | I | **USB_VBUS —** Monitors the presence of USB bus power. |
| PIO0_4/SCL | 20 | 15 | 10 | [4] | IA | I/O | **PIO0_4 —** General purpose digital input/output pin (open-drain). |
| | | | | | - | I/O | **SCL —** $I^2C$-bus clock input/output (open-drain). High-current sink only if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| PIO0_5/SDA | 21 | 16 | 11 | [4] | IA | I/O | **PIO0_5 —** General purpose digital input/output pin (open-drain). |
| | | | | | - | I/O | **SDA —** $I^2C$-bus data input/output (open-drain). High-current sink only if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| PIO0_6/$\overline{\text{USB_CONNECT}}$/ SCK0 | 29 | 22 | 15 | [3] | I; PU | I/O | **PIO0_6 —** General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{USB_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. |
| | | | | | - | I/O | **SCK0 —** Serial clock for SSP0. |
| PIO0_7/$\overline{\text{CTS}}$ | 30 | 23 | 16 | [5] | I; PU | I/O | **PIO0_7 —** General purpose digital input/output pin (high-current output driver). |
| | | | | | - | I | **$\overline{\text{CTS}}$ —** Clear To Send input for USART. |
| PIO0_8/MISO0/ CT16B0_MAT0 | 36 | 27 | 17 | [3] | I; PU | I/O | **PIO0_8 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **MISO0 —** Master In Slave Out for SSP0. |
| | | | | | - | O | **CT16B0_MAT0 —** Match output 0 for 16-bit timer 0. |

**Table 4. Pin description (LPC1345/46/47 - with USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO0_9/MOSI0/ CT16B0_MAT1/ SWO | 37 | 28 | 18 | [3] | I; PU | I/O | **PIO0_9** — General purpose digital input/output pin. |
| | | | | | - | I/O | **MOSI0** — Master Out Slave In for SSP0. |
| | | | | | - | O | **CT16B0_MAT1** — Match output 1 for 16-bit timer 0. |
| | | | | | - | O | **SWO** — Serial wire trace output. |
| SWCLK/PIO0_10/SCK0/ CT16B0_MAT2 | 38 | 29 | 19 | [3] | I; PU | I | **SWCLK** — Serial wire clock and test clock TCK for JTAG interface. |
| | | | | | - | I/O | **PIO0_10** — General purpose digital input/output pin. |
| | | | | | - | O | **SCK0** — Serial clock for SSP0. |
| | | | | | - | O | **CT16B0_MAT2** — Match output 2 for 16-bit timer 0. |
| TDI/PIO0_11/AD0/ CT32B0_MAT3 | 42 | 32 | 21 | [6] | I; PU | I | **TDI** — Test Data In for JTAG interface. |
| | | | | | - | I/O | **PIO0_11** — General purpose digital input/output pin. |
| | | | | | - | I | **AD0** — A/D converter, input 0. |
| | | | | | - | O | **CT32B0_MAT3** — Match output 3 for 32-bit timer 0. |
| TMS/PIO0_12/AD1/ CT32B1_CAP0 | 44 | 33 | 22 | [6] | I; PU | I | **TMS** — Test Mode Select for JTAG interface. |
| | | | | | - | I/O | **PIO_12** — General purpose digital input/output pin. |
| | | | | | - | I | **AD1** — A/D converter, input 1. |
| | | | | | - | I | **CT32B1_CAP0** — Capture input 0 for 32-bit timer 1. |
| TDO/PIO0_13/AD2/ CT32B1_MAT0 | 45 | 34 | 23 | [6] | I; PU | O | **TDO** — Test Data Out for JTAG interface. |
| | | | | | - | I/O | **PIO0_13** — General purpose digital input/output pin. |
| | | | | | - | I | **AD2** — A/D converter, input 2. |
| | | | | | - | O | **CT32B1_MAT0** — Match output 0 for 32-bit timer 1. |
| $\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1 | 46 | 35 | 24 | [6] | I; PU | I | **$\overline{\text{TRST}}$** — Test Reset for JTAG interface. |
| | | | | | - | I/O | **PIO0_14** — General purpose digital input/output pin. |
| | | | | | - | I | **AD3** — A/D converter, input 3. |
| | | | | | - | O | **CT32B1_MAT1** — Match output 1 for 32-bit timer 1. |
| SWDIO/PIO0_15/AD4/ CT32B1_MAT2 | 52 | 39 | 25 | [6] | I; PU | I/O | **SWDIO** — Serial wire debug input/output. |
| | | | | | - | I/O | **PIO0_15** — General purpose digital input/output pin. |
| | | | | | - | I | **AD4** — A/D converter, input 4. |
| | | | | | - | O | **CT32B1_MAT2** — Match output 2 for 32-bit timer 1. |
| PIO0_16/AD5/ CT32B1_MAT3/WAKEUP | 53 | 40 | 26 | [7] | I; PU | I/O | **PIO0_16** — General purpose digital input/output pin. |
| | | | | | - | I | **AD5** — A/D converter, input 5. |
| | | | | | - | O | **CT32B1_MAT3** — Match output 3 for 32-bit timer 1. |
| | | | | | - | I | **WAKEUP** — Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part. |

**Table 4. Pin description (LPC1345/46/47 - with USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK | 60 | 45 | 30 | [3] | I; PU | I/O | **PIO0_17** — General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{RTS}}$** — Request To Send output for USART. |
| | | | | | - | I | **CT32B0_CAP0** — Capture input 0 for 32-bit timer 0. |
| | | | | | - | I/O | **SCLK** — Serial clock input/output for USART in synchronous mode. |
| PIO0_18/RXD/ CT32B0_MAT0 | 61 | 46 | 31 | [3] | I; PU | I/O | **PIO0_18** — General purpose digital input/output pin. |
| | | | | | - | I | **RXD** — Receiver input for USART. Used in UART ISP mode. |
| | | | | | - | O | **CT32B0_MAT0** — Match output 0 for 32-bit timer 0. |
| PIO0_19/TXD/ CT32B0_MAT1 | 62 | 47 | 32 | [3] | I; PU | I/O | **PIO0_19** — General purpose digital input/output pin. |
| | | | | | - | O | **TXD** — Transmitter output for USART. Used in UART ISP mode. |
| | | | | | - | O | **CT32B0_MAT1** — Match output 1 for 32-bit timer 0. |
| PIO0_20/CT16B1_CAP0 | 11 | 9 | 7 | [3] | I; PU | I/O | **PIO0_20** — General purpose digital input/output pin. |
| | | | | | - | I | **CT16B1_CAP0** — Capture input 0 for 16-bit timer 1. |
| PIO0_21/CT16B1_MAT0/ MOSI1 | 22 | 17 | 12 | [3] | I; PU | I/O | **PIO0_21** — General purpose digital input/output pin. |
| | | | | | - | O | **CT16B1_MAT0** — Match output 0 for 16-bit timer 1. |
| | | | | | - | I/O | **MOSI1** — Master Out Slave In for SSP1. |
| PIO0_22/AD6/ CT16B1_MAT1/MISO1 | 40 | 30 | 20 | [6] | I; PU | I/O | **PIO0_22** — General purpose digital input/output pin. |
| | | | | | - | I | **AD6** — A/D converter, input 6. |
| | | | | | - | O | **CT16B1_MAT1** — Match output 1 for 16-bit timer 1. |
| | | | | | - | I/O | **MISO1** — Master In Slave Out for SSP1. |
| PIO0_23/AD7 | 56 | 42 | 27 | [6] | I; PU | I/O | **PIO0_23** — General purpose digital input/output pin. |
| | | | | | - | I | **AD7** — A/D converter, input 7. |
| PIO1_0/CT32B1_MAT0 | 1 | - | - | [3] | I; PU | I/O | **PIO1_0** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT0** — Match output 0 for 32-bit timer 1. |
| PIO1_1/CT32B1_MAT1 | 17 | - | - | [3] | I; PU | I/O | **PIO1_1** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT1** — Match output 1 for 32-bit timer 1. |
| PIO1_2/CT32B1_MAT2 | 34 | - | - | [3] | I; PU | I/O | **PIO1_2** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT2** — Match output 2 for 32-bit timer 1. |
| PIO1_3/CT32B1_MAT3 | 50 | - | - | [3] | I; PU | I/O | **PIO1_3** — General purpose digital input/output pin. |
| | | | | | - | O | **CT32B1_MAT3** — Match output 3 for 32-bit timer 1. |
| PIO1_4/CT32B1_CAP0 | 16 | - | - | [3] | I; PU | I/O | **PIO1_4** — General purpose digital input/output pin. |
| | | | | | - | I | **CT32B1_CAP0** — Capture input 0 for 32-bit timer 1. |
| PIO1_5/CT32B1_CAP1 | 32 | - | - | [3] | I; PU | I/O | **PIO1_5** — General purpose digital input/output pin. |
| | | | | | - | I | **CT32B1_CAP1** — Capture input 1 for 32-bit timer 1. |
| PIO1_7 | 6 | - | - | [3] | I; PU | I/O | **PIO1_7** — General purpose digital input/output pin. |
| PIO1_8 | 39 | - | - | [3] | I; PU | I/O | **PIO1_8** — General purpose digital input/output pin. |

**Table 4. Pin description (LPC1345/46/47 - with USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO1_10 | 12 | - | - | [3] | I; PU | I/O | **PIO1_10** — General purpose digital input/output pin. |
| PIO1_11 | 43 | - | - | [3] | I; PU | I/O | **PIO1_11** — General purpose digital input/output pin. |
| PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD | 47 | 36 | - | [3] | I; PU | I/O | **PIO1_13** — General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{DTR}}$** — Data Terminal Ready output for USART. |
| | | | | | - | O | **CT16B0_MAT0** — Match output 0 for 16-bit timer 0. |
| | | | | | - | O | **TXD** — Transmitter output for USART. |
| PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD | 49 | 37 | - | [3] | I; PU | I/O | **PIO1_14** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DSR}}$** — Data Set Ready input for USART. |
| | | | | | - | O | **CT16B0_MAT1** — Match output 1 for 16-bit timer 0. |
| | | | | | - | I | **RXD** — Receiver input for USART. |
| PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1 | 57 | 43 | 28 | [3] | I; PU | I/O | **PIO1_15** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DCD}}$** — Data Carrier Detect input for USART. |
| | | | | | - | O | **CT16B0_MAT2** — Match output 2 for 16-bit timer 0. |
| | | | | | - | I/O | **SCK1** — Serial clock for SSP1. |
| PIO1_16/$\overline{\text{RI}}$/CT16B0_CAP0 | 63 | 48 | - | [3] | I; PU | I/O | **PIO1_16** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{RI}}$** — Ring Indicator input for USART. |
| | | | | | - | I | **CT16B0_CAP0** — Capture input 0 for 16-bit timer 0. |
| PIO1_17/CT16B0_CAP1/ RXD | 23 | - | - | [3] | I; PU | I/O | **PIO1_17** — General purpose digital input/output pin. |
| | | | | | - | I | **CT16B0_CAP1** — Capture input 1 for 16-bit timer 0. |
| | | | | | - | I | **RXD** — Receiver input for USART. |
| PIO1_18/CT16B1_CAP1/ TXD | 28 | - | - | [3] | I; PU | I/O | **PIO1_18** — General purpose digital input/output pin. |
| | | | | | - | I | **CT16B1_CAP1** — Capture input 1 for 16-bit timer 1. |
| | | | | | - | O | **TXD** — Transmitter output for USART. |
| PIO1_19/$\overline{\text{DTR}}$/SSEL1 | 3 | 2 | 1 | [3] | I; PU | I/O | **PIO1_19** — General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{DTR}}$** — Data Terminal Ready output for USART. |
| | | | | | - | I/O | **SSEL1** — Slave select for SSP1. |
| PIO1_20/$\overline{\text{DSR}}$/SCK1 | 18 | 13 | - | [3] | I; PU | I/O | **PIO1_20** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DSR}}$** — Data Set Ready input for USART. |
| | | | | | - | I/O | **SCK1** — Serial clock for SSP1. |
| PIO1_21/$\overline{\text{DCD}}$/MISO1 | 35 | 26 | - | [3] | I; PU | I/O | **PIO1_21** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{DCD}}$** — Data Carrier Detect input for USART. |
| | | | | | - | I/O | **MISO1** — Master In Slave Out for SSP1. |
| PIO1_22/$\overline{\text{RI}}$/MOSI1 | 51 | 38 | - | [3] | I; PU | I/O | **PIO1_22** — General purpose digital input/output pin. |
| | | | | | - | I | **$\overline{\text{RI}}$** — Ring Indicator input for USART. |
| | | | | | - | I/O | **MOSI1** — Master Out Slave In for SSP1. |
| PIO1_23/CT16B1_MAT1/ SSEL1 | 24 | 18 | - | [3] | I; PU | I/O | **PIO1_23** — General purpose digital input/output pin. |
| | | | | | - | O | **CT16B1_MAT1** — Match output 1 for 16-bit timer 1. |
| | | | | | - | I/O | **SSEL1** — Slave select for SSP1. |

**Table 4. Pin description (LPC1345/46/47 - with USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO1_24/CT32B0_MAT0 | 27 | 21 | - | [3] | I; PU | I/O | **PIO1_24 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT0 —** Match output 0 for 32-bit timer 0. |
| PIO1_25/CT32B0_MAT1 | 2 | 1 | - | [3] | I; PU | I/O | **PIO1_25 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT1 —** Match output 1 for 32-bit timer 0. |
| PIO1_26/CT32B0_MAT2/ RXD | 14 | 11 | - | [3] | I; PU | I/O | **PIO1_26 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT2 —** Match output 2 for 32-bit timer 0. |
| | | | | | - | I | **RXD —** Receiver input for USART. |
| PIO1_27/CT32B0_MAT3/ TXD | 15 | 12 | - | [3] | I; PU | I/O | **PIO1_27 —** General purpose digital input/output pin. |
| | | | | | - | O | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| | | | | | - | O | **TXD —** Transmitter output for USART. |
| PIO1_28/CT32B0_CAP0/ SCLK | 31 | 24 | - | [3] | I; PU | I/O | **PIO1_28 —** General purpose digital input/output pin. |
| | | | | | - | I | **CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. |
| | | | | | - | I/O | **SCLK —** Serial clock input/output for USART in synchronous mode. |
| PIO1_29/SCK0/ CT32B0_CAP1 | 41 | 31 | - | [3] | I; PU | I/O | **PIO1_29 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **SCK0 —** Serial clock for SSP0. |
| | | | | | - | I | **CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. |
| PIO1_31 | - | 25 | - | [3] | I; PU | I/O | **PIO1_31 —** General purpose digital input/output pin. |
| USB_DM | 25 | 19 | 13 | [8] | F | - | **USB_DM —** USB bidirectional D− line. (LPC1345/46/46 only.) |
| USB_DP | 26 | 20 | 14 | [8] | F | - | **USB_DP —** USB bidirectional D+ line. (LPC1345/46/46 only.) |
| XTALIN | 8 | 6 | 4 | [9] | - | - | Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V. |
| XTALOUT | 9 | 7 | 5 | [9] | - | - | Output from the oscillator amplifier. |
| $V_{DDA}$ | 59 | - | - | | - | - | Analog 3.3 V pad supply voltage: This should be nominally the same voltage as $V_{DD}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC. This pin should be tied to 3.3 V if the ADC are not used. |
| VREFN | 48 | - | - | | - | - | ADC negative reference voltage: This should be nominally the same voltage as $V_{SS}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. |

**Table 4. Pin description (LPC1345/46/47 - with USB)**

| Symbol | LQFP64 | LQFP48 | HVQFN33 | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|
| VREFP | 64 | - | - | - | - | ADC positive reference voltage: This should be nominally the same voltage as $V_{DDA}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used. |
| $V_{SSA}$ | 55 | - | - | - | - | analog ground: 0 V reference. This should nominally be the same voltage as $V_{SS}$, but should be isolated to minimize noise and error. |
| $V_{DD}$ | 10; 33; 58 | 8; 44 | 6; 29 | - | - | Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage. |
| $V_{SS}$ | 7; 54 | 5; 41 | 33 | - | - | Ground. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 33 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32).

[4] $I^2C$-bus pins compliant with the $I^2C$-bus specification for $I^2C$ standard mode, $I^2C$ Fast-mode, and $I^2C$ Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes programmable digital input glitch filter.

[7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes digital input glitch filter.

[8] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[9] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.15

# 7. Functional description

## 7.1 On-chip flash programming memory

The LPC1315/16/17/45/46/47 contain up to 64 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

## 7.2 EEPROM

The LPC1315/16/17/45/46/47 contain 2 kB or 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

## 7.3 SRAM

The LPC1315/16/17/45/46/47 contain a total of 8 kB, 10 kB, or 12 kB on-chip static RAM memory.

## 7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API (HID, CDC, and MSC drivers) (LPC1345/46/47 only)
- Power profiles for configuring power consumption and PLL settings
- Flash updates via USB supported (LPC1345/46/47 only)

## 7.5 Memory map

The LPC1315/16/17/45/46/47 incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

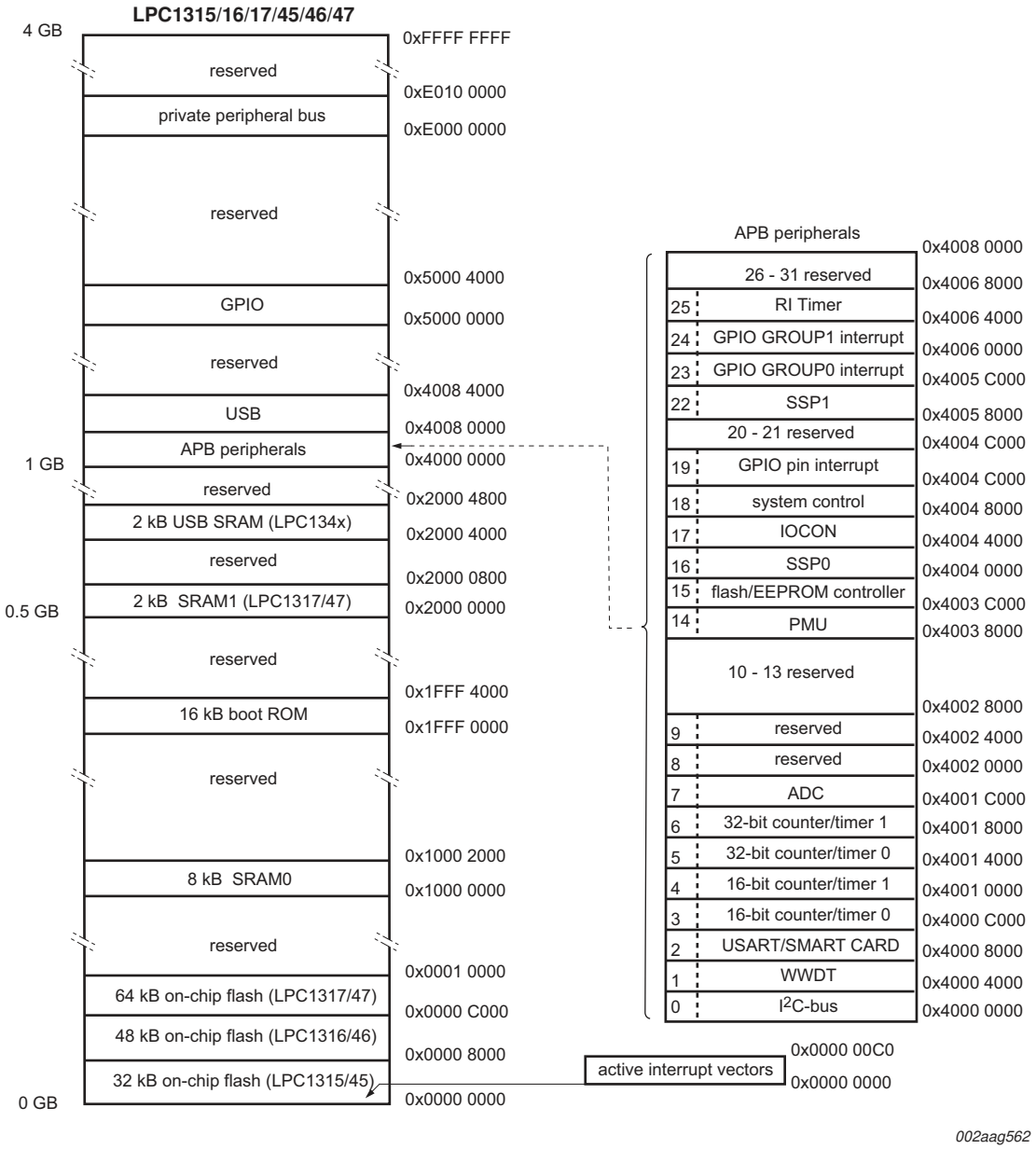



**Fig 8. LPC1315/16/17/45/46/47 memory map**

## 7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

### 7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC1315/16/17/45/46/47, the NVIC supports up to 32 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.

- Software interrupt generation.

### 7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

## 7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

### 7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V ($V_{DD}$ = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10-ns glitch filter on pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16. The glitch filter is turned off by default.
- Programmable hysteresis.
- Programmable input inverter.

## 7.8 General Purpose Input/Output GPIO

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1315/16/17/45/46/47 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

### 7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Port interrupts can be triggered by any pin or pins in each port.

## 7.9 USB interface

**Remark:** The USB interface is available on parts LPC1345/46/47 only.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC1345/46/47 USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

**Remark:** Configure the LPC1345/46/47 in default power mode with the power profiles before using the USB (see Section 7.18.5.1). Do not use the USB with the part in performance, efficiency, or low-power mode.

### 7.9.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

#### 7.9.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.
- Supports Link Power Management (LPM).

## 7.10 USART

The LPC1315/16/17/45/46/47 contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.10.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface (ISO 7816-3).

## 7.11 SSP serial I/O controller

The SSP controllers are capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

### 7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

## 7.12 $I^2C$-bus serial I/O controller

The LPC1315/16/17/45/46/47 contain one $I^2C$-bus controller.

The $I^2C$-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The $I^2C$ is a multi-master bus and can be controlled by more than one bus master connected to it.

### 7.12.1 Features

- The $I^2C$-interface is an $I^2C$-bus compliant interface with open-drain pins. The $I^2C$-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The $I^2C$-bus can be used for test and diagnostic purposes.
- The $I^2C$-bus controller supports multiple address recognition and a bus monitor mode.

## 7.13 12-bit ADC

The LPC1315/16/17/45/46/47 contains one ADC. It is a single 12-bit successive approximation ADC with eight channels.

### 7.13.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among 8 pins and three internal sources.
- Low-power mode.
- 10-bit double-conversion rate mode (conversion rate of up to 1 Msample/s).
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of up to 500 kHz.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- On the LQFP64 package, power and reference pins ($V_{DDA}$, $V_{SSA}$, VREFP, VREFN) are brought out on separate pins for superior noise immunity.

## 7.14 General purpose external event counter/timers

The LPC1315/16/17/45/46/47 includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

### 7.14.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

## 7.15 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

### 7.15.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Support for ETM timestamp generator.

## 7.16 System tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

## 7.17 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

### 7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

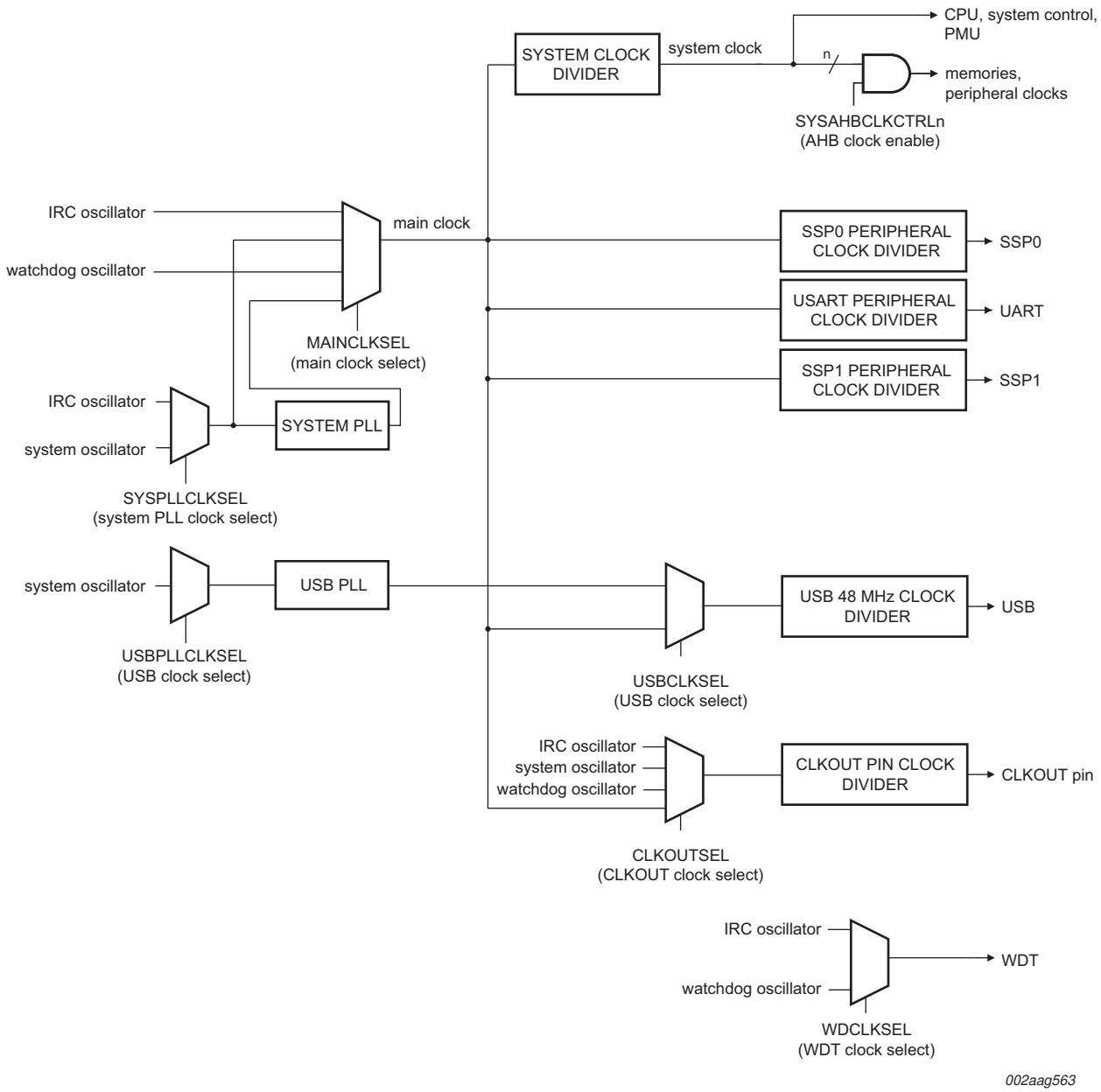
## 7.18 Clocking and power control

### 7.18.1 Integrated oscillators

The LPC1315/16/17/45/46/47 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1315/16/17/45/46/47 will operate from the internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 9 for an overview of the LPC1315/16/17/45/46/47 clock generation.




The USB clock divider is available on parts LPC1345/46/47 only.

**Fig 9. LPC1315/16/17/45/46/47 clocking generation block diagram**

#### 7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC1315/16/17/45/46/47 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

#### 7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC1315/16/17/45/46/47, the system oscillator must be used to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

#### 7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

### 7.18.2 System PLL and USB PLL

The LPC1315/16/17/45/46/47 contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

### 7.18.3 Clock output

The LPC1315/16/17/45/46/47 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

### 7.18.4 Wake-up process

The LPC1315/16/17/45/46/47 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

### 7.18.5 Power control

The LPC1315/16/17/45/46/47 support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be

controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

#### 7.18.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1315/16/17/45/46/47 for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

**Remark:** When using the USB, configure the LPC1345/46/47 in Default mode.

#### 7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

#### 7.18.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC1315/16/17/45/46/47 is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC1315/16/17/45/46/47 can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

#### 7.18.5.4 Power-down mode

In Power-down mode, the LPC1315/16/17/45/46/47 is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the user has the option to keep the BOD circuit running for BOD protection.

The LPC1315/16/17/45/46/47 can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

#### 7.18.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC1315/16/17/45/46/47 can wake up from Deep power-down mode via the WAKEUP pin.

The LPC1315/16/17/45/46/47 can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the user to always keep the watchdog timer or the BOD running.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

### 7.18.6 System control

#### 7.18.6.1 Reset

Reset has four sources on the LPC1315/16/17/45/46/47: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

#### 7.18.6.2 Brownout detection

The LPC1315/16/17/45/46/47 includes up to four levels for monitoring the voltage on the $V_{DD}$ pin. If this voltage falls below one of selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

#### 7.18.6.3 Code security (Code Read Protection - CRP)

This feature of the LPC1315/16/17/45/46/47 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the LPC1315/16/17/45/46/47 *user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the USART.

**CAUTION**

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the LPC1315/16/17/45/46/47 *user manual*.

#### 7.18.6.4 APB interface

The APB peripherals are located on one APB bus.

#### 7.18.6.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M3 to the flash memory, the main static RAM, and the ROM.

#### 7.18.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

## 7.19 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC1315/16/17/45/46/47 is in reset.

**Remark:** Boundary scan operations should not be started until 250 μs after POR, and the test TAP should be reset after the boundary scan. Boundary scan is not affected by Code Read Protection.

**Remark:** The JTAG interface cannot be used for debug purposes.

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (core and external rail) | | | 2.0 | 3.6 | V |
| $V_I$ | input voltage | 5 V tolerant I/O pins; only valid when the $V_{DD}$ supply voltage is present | [2] | −0.5 | +5.5 | V |
| $I_{DD}$ | supply current | per supply pin | | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | | - | 100 | mA |
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C | | - | 100 | mA |
| $T_{stg}$ | storage temperature | non-operating | [3] | −65 | +150 | °C |
| $T_{j(max)}$ | maximum junction temperature | | | - | 150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins | [4] | −5000 | +5000 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

# 9. Static characteristics

**Table 6. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (core and external rail) | | [2] | 2.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | supply current | Active mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C; code `while(1){}` executed from flash; | | | | | |
| | | system clock = 1 MHz | [3][5][6][7][8][9] | - | 0.5 | - | mA |
| | | system clock = 12 MHz | [4][5][6][7][8][9] | - | 2 | - | mA |
| | | system clock = 72 MHz | [5][6][7][8][9][10] | - | 14 | - | mA |
| | | Sleep mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C; system clock = 12 MHz | [4][5][6][7][8][9] | - | 1 | - | mA |
| | | Deep-sleep mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C | [5][8] | - | 280 | - | µA |
| | | Power-down mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C | [5][8] | - | 2.1 | - | µA |
| | | Deep power-down mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C | [11] | - | 220 | - | nA |
| **Standard port pins, $\overline{\text{RESET}}$** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 0.5 | 10 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I$ = $V_{DD}$; on-chip pull-down resistor disabled | | - | 0.5 | 10 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O$ = $V_{DD}$; on-chip pull-up/down resistors disabled | | - | 0.5 | 10 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function | [12][13][14] | 0 | - | 5.0 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-level output voltage | 2.5 V< $V_{DD}$ ≤ 3.6 V; $I_{OH}$ = −4 mA | | $V_{DD}$ − 0.4 | - | - | V |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $I_{OH}$ = −3 mA | | $V_{DD}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OL}$ = 4 mA | | - | - | 0.4 | V |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $I_{OL}$ = 3 mA | | - | - | 0.4 | V |

**Table 6. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ | HIGH-level output current | 2.5 V≤ $V_{DD}$ ≤ 3.6 V; $V_{OH}$ = $V_{DD}$ − 0.4 V | | −4 | - | - | mA |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $V_{OH}$ = $V_{DD}$ − 0.4 V | | −3 | - | - | mA |
| $I_{OL}$ | LOW-level output current | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $V_{OL}$ = 0.4 V | | 4 | - | - | mA |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $V_{OL}$ = 0.4 V | | 3 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V | [15] | - | - | −45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL}$ = $V_{DD}$ | [15] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | | 10 | 50 | 150 | µA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V; 2.0 V < $V_{DD}$ ≤ 3.6 V | | −15 | −50 | −85 | µA |
| | | $V_{DD}$ = 2.0 V | | −10 | −50 | −85 | µA |
| | | $V_{DD}$ < $V_I$ < 5 V | | 0 | 0 | 0 | µA |
| **High-drive output pin (PIO0_7)** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 0.5 | 10 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I$ = $V_{DD}$; on-chip pull-down resistor disabled | | - | 0.5 | 10 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O$ = $V_{DD}$; on-chip pull-up/down resistors disabled | | - | 0.5 | 10 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function | [12][13] [14] | 0 | - | 5.0 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | 0.3$V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | 0.4 | - | - | V |
| $V_{OH}$ | HIGH-level output voltage | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OH}$ = −20 mA | | $V_{DD}$ − 0.4 | - | - | V |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $I_{OH}$ = −12 mA | | $V_{DD}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OL}$ = 4 mA | | - | - | 0.4 | V |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $I_{OL}$ = 3 mA | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $V_{OH}$ = $V_{DD}$ − 0.4 V | | 20 | - | - | mA |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $V_{OH}$ = $V_{DD}$ − 0.4 V; | | 12 | - | - | mA |
| $I_{OL}$ | LOW-level output current | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $V_{OL}$ = 0.4 V | | 4 | - | - | mA |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V; $V_{OL}$ = 0.4 V | | 3 | - | - | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL}$ = $V_{DD}$ | [15] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | | 10 | 50 | 150 | µA |

**Table 6. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{pu}$ | pull-up current | $V_I$ = 0 V | | −15 | −50 | −85 | µA |
| | | 2.0 V < $V_{DD}$ ≤ 3.6 V | | | | | |
| | | $V_{DD}$ = 2.0 V | | −10 | −50 | −85 | µA |
| | | $V_{DD}$ < $V_I$ < 5 V | | 0 | 0 | 0 | µA |
| **$I^2C$-bus pins (PIO0_4 and PIO0_5)** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | 0.3$V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | 0.05$V_{DD}$ | - | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; $I^2C$-bus pins configured as standard mode pins | | 3.5 | - | - | mA |
| | | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V | | | | | |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V | | 3.0 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; $I^2C$-bus pins configured as Fast-mode Plus pins | | 20 | - | - | mA |
| | | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V | | | | | |
| | | 2.0 V ≤ $V_{DD}$ < 2.5 V | | 16 | - | - | |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{DD}$ | [16] | - | 2 | 4 | µA |
| | | $V_I$ = 5 V | | - | 10 | 22 | µA |
| **Oscillator pins** | | | | | | | |
| $V_{i(xtal)}$ | crystal input voltage | | | −0.5 | 1.8 | 1.95 | V |
| $V_{o(xtal)}$ | crystal output voltage | | | −0.5 | 1.8 | 1.95 | V |
| **USB pins** | | | | | | | |
| $I_{OZ}$ | OFF-state output current | 0 V < $V_I$ < 3.3 V | [2] | - | - | ±10 | µA |
| $V_{BUS}$ | bus supply voltage | | [2] | - | - | 5.25 | V |
| $V_{DI}$ | differential input sensitivity voltage | \|(D+) − (D−)\| | [2] | 0.2 | - | - | V |
| $V_{CM}$ | differential common mode voltage range | includes $V_{DI}$ range | [2] | 0.8 | - | 2.5 | V |
| $V_{th(rs)se}$ | single-ended receiver switching threshold voltage | | [2] | 0.8 | - | 2.0 | V |
| $V_{OL}$ | LOW-level output voltage | for low-/full-speed; $R_L$ of 1.5 kΩ to 3.6 V | [2] | - | - | 0.18 | V |
| $V_{OH}$ | HIGH-level output voltage | driven; for low-/full-speed; $R_L$ of 15 kΩ to GND | [2] | 2.8 | - | 3.5 | V |
| $C_{trans}$ | transceiver capacitance | pin to GND | [2] | - | - | 20 | pF |
| $Z_{DRV}$ | driver output impedance for driver which is not high-speed capable | with 33 Ω series resistor; steady state drive | [17][2] | 36 | - | 44.1 | Ω |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD}$ ≤ 3.6 V. Guaranteed by design.

[3] System oscillator enabled; PLL and IRC disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] $I_{DD}$ measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[6] BOD disabled.

[7] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the syscon block.

[8] USB_DP and USB_DM pulled LOW externally.

[9] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[10] IRC disabled; system oscillator enabled; system PLL enabled.

[11] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.

[12] Including voltage on outputs in 3-state mode.

[13] $V_{DD}$ supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To $V_{SS}$.

[17] Includes external resistors of 33 Ω ± 1 % on USB_DP and USB_DM.

## 9.1 BOD static characteristics

**Table 7. BOD static characteristics[1]**

*$T_{amb}$ = 25 °C.*

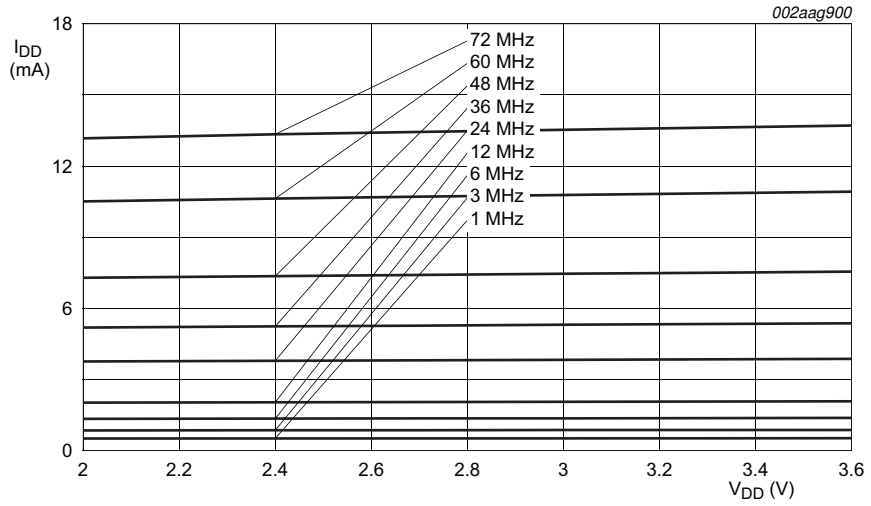
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{th}$ | threshold voltage | interrupt level 1 | | | | |
| | | assertion | - | 2.22 | - | V |
| | | de-assertion | - | 2.35 | - | V |
| | | interrupt level 2 | | | | |
| | | assertion | - | 2.52 | - | V |
| | | de-assertion | - | 2.66 | - | V |
| | | interrupt level 3 | | | | |
| | | assertion | - | 2.80 | - | V |
| | | de-assertion | - | 2.90 | - | V |
| | | reset level 0 | | | | |
| | | assertion | - | 1.46 | - | V |
| | | de-assertion | - | 1.63 | - | V |
| | | reset level 1 | | | | |
| | | assertion | - | 2.06 | - | V |
| | | de-assertion | - | 2.15 | - | V |
| | | reset level 2 | | | | |
| | | assertion | - | 2.35 | - | V |
| | | de-assertion | - | 2.43 | - | V |
| | | reset level 3 | | | | |
| | | assertion | - | 2.63 | - | V |
| | | de-assertion | - | 2.71 | - | V |

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see LPC1315/16/17/45/46/47 *user manual*.

## 9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see LPC1315/16/17/45/46/47 *user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



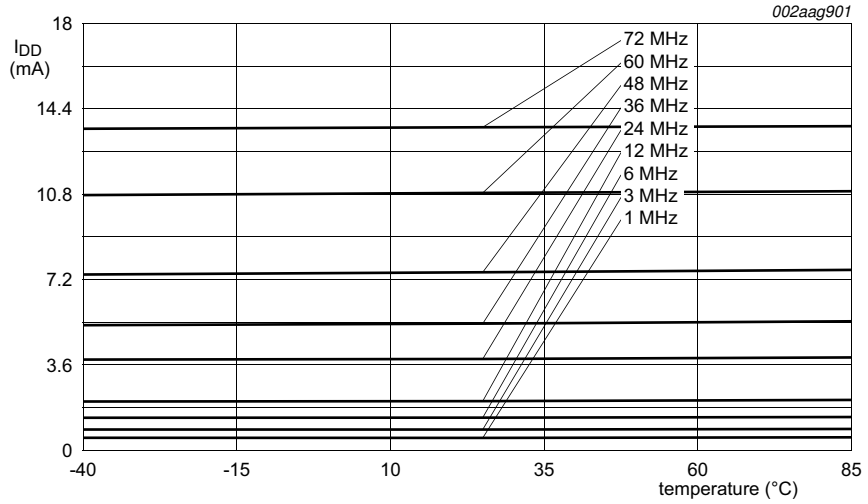

Conditions: $T_{amb}$ = 25 °C; active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally.

1 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz - 72 MHz: IRC disabled; system oscillator, PLL enabled.

**Fig 10. Typical supply current versus regulator supply voltage $V_{DD}$ in active mode**



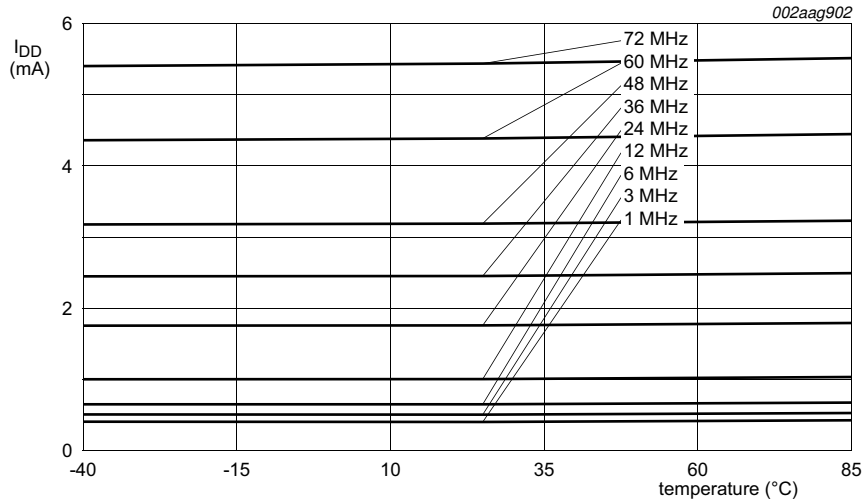

Conditions: $V_{DD}$ = 3.3 V; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally.

1 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz - 72 MHz: IRC disabled; system oscillator, PLL enabled.

**Fig 11. Typical supply current versus temperature in Active mode**



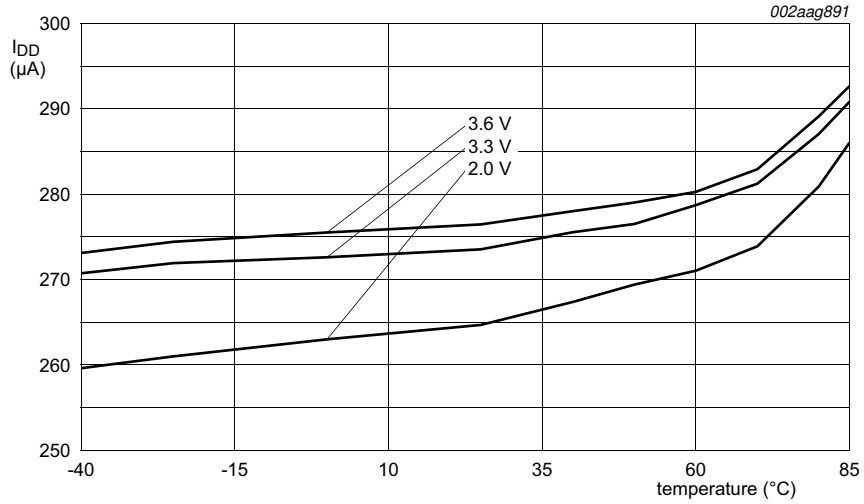

Conditions: $V_{DD}$ = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally.

1 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

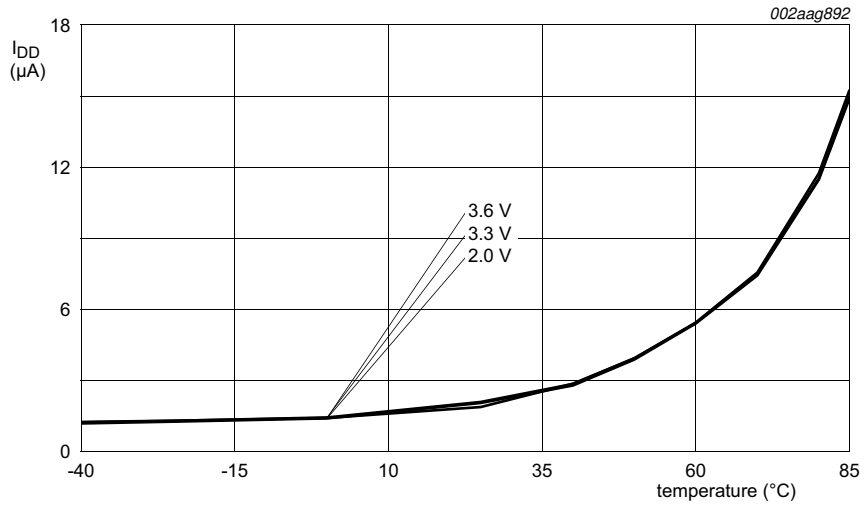
24 MHz - 72 MHz: IRC disabled; system oscillator, PLL enabled.

**Fig 12. Typical supply current versus temperature in Sleep mode**




Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

**Fig 13. Typical supply current versus temperature in Deep-sleep mode**




Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

**Fig 14. Typical supply current versus temperature in Power-down mode**

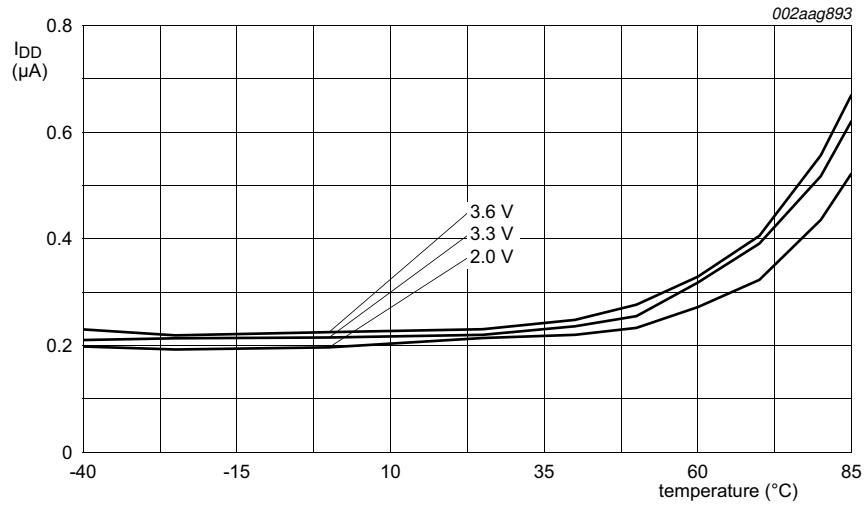



**Fig 15. Typical supply current versus temperature in Deep power-down mode**

**Table 8. Power consumption for individual analog and digital blocks**

*The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCTRL or PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb}$ = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.*

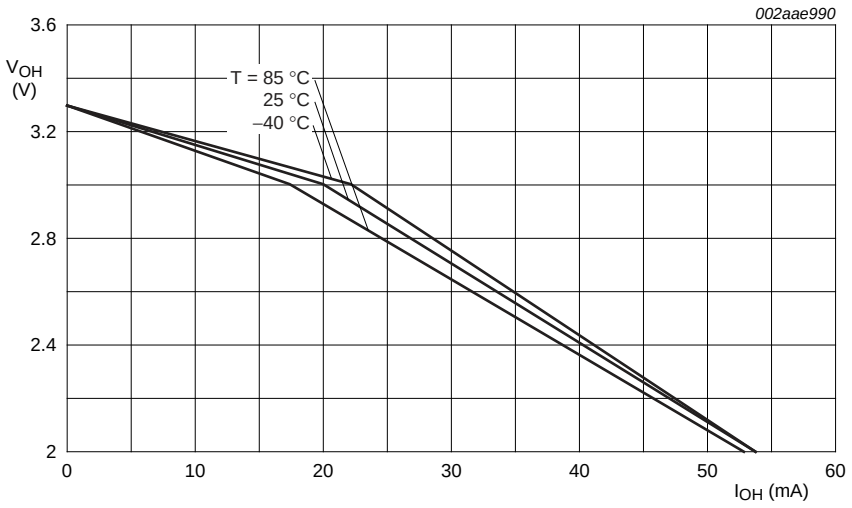
| | Typical supply current per peripheral in mA for different system clock frequencies | | | | Notes |
|---|---|---|---|---|---|
| | n/a | 12 MHz | 48 MHz | 72 MHz | |
| IRC | 0.23 | - | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| System oscillator at 12 MHz | 0.23 | - | - | - | IRC running; PLL off; independent of main clock frequency. |
| Watchdog oscillator at 500 kHz/2 | 0.002 | - | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| BOD | 0.045 | - | - | - | Independent of main clock frequency. |
| Main PLL or USB PLL | - | 0.26 | 0.34 | 0.48 | |
| ADC | - | 0.07 | 0.25 | 0.37 | |
| CLKOUT | - | 0.14 | 0.56 | 0.82 | Main clock divided by 4 in the CLKOUTDIV register. |
| CT16B0 | - | 0.01 | 0.05 | 0.08 | |
| CT16B1 | - | 0.01 | 0.04 | 0.06 | |
| CT32B0 | - | 0.01 | 0.05 | 0.07 | |
| CT32B1 | - | 0.01 | 0.04 | 0.06 | |
| GPIO | - | 0.21 | 0.80 | 1.17 | GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register. |
| IOCON | - | 0.00 | 0.02 | 0.02 | |
| I2C | - | 0.03 | 0.12 | 0.17 | |

**Table 8. Power consumption for individual analog and digital blocks**

*The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCTRL or PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb}$ = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.*

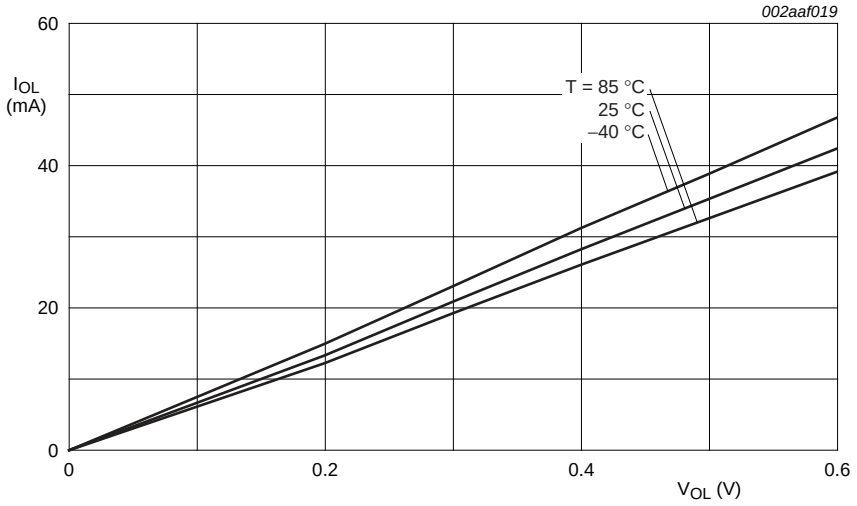
| | Typical supply current per peripheral in mA for different system clock frequencies | | | | Notes |
|---|---|---|---|---|---|
| | n/a | 12 MHz | 48 MHz | 72 MHz | |
| ROM | - | 0.04 | 0.15 | 0.22 | |
| SSP0 | - | 0.11 | 0.41 | 0.60 | |
| SSP1 | - | 0.11 | 0.41 | 0.60 | |
| USART | - | 0.20 | 0.76 | 1.11 | |
| WDT | - | 0.01 | 0.05 | 0.08 | Main clock selected as clock source for the WDT. |
| USB | - | - | 1.2 | - | |

## 9.3 Electrical pin characteristics



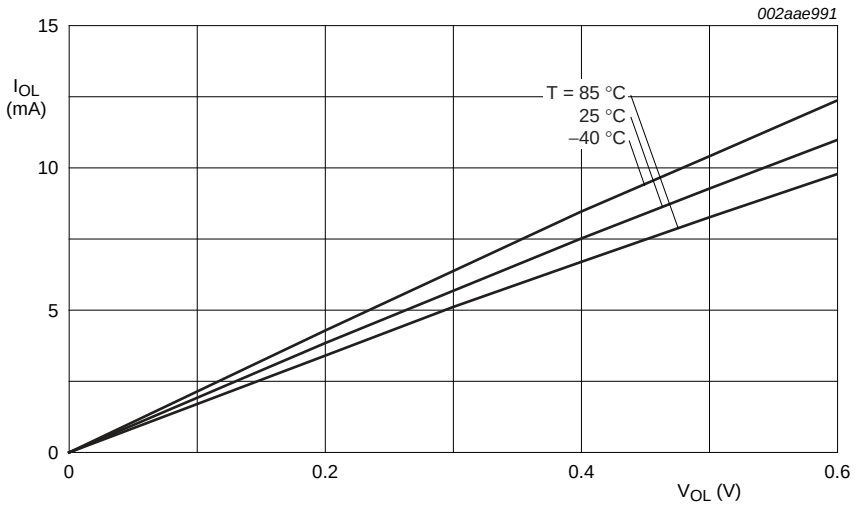

Conditions: $V_{DD}$ = 3.3 V; on pin PIO0_7.

**Fig 16. High-drive output: Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output current $I_{OH}$.**



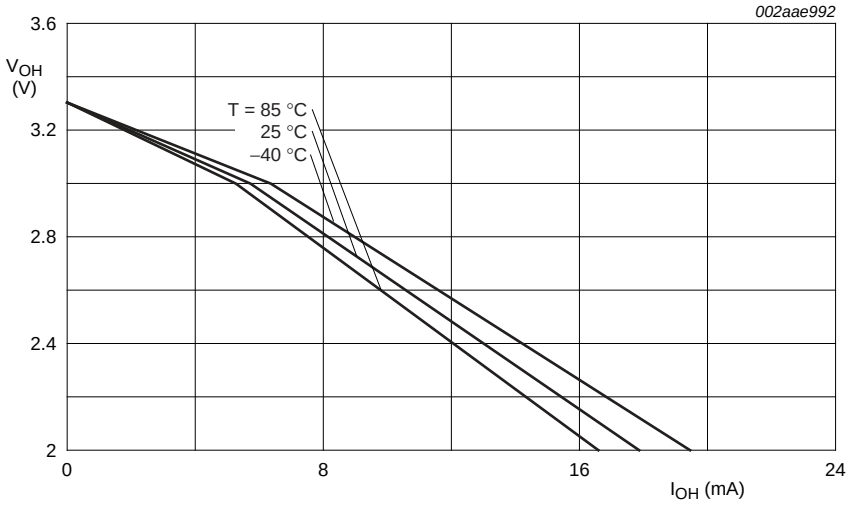

Conditions: $V_{DD}$ = 3.3 V; on pins PIO0_4 and PIO0_5.

**Fig 17. $I^2C$-bus pins (high current sink): Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**



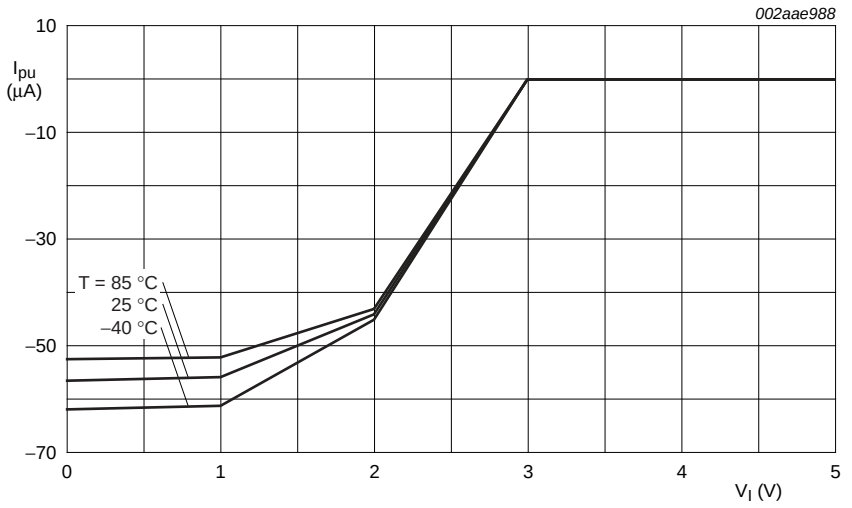

Conditions: $V_{DD}$ = 3.3 V; standard port pins and PIO0_7.

**Fig 18. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**



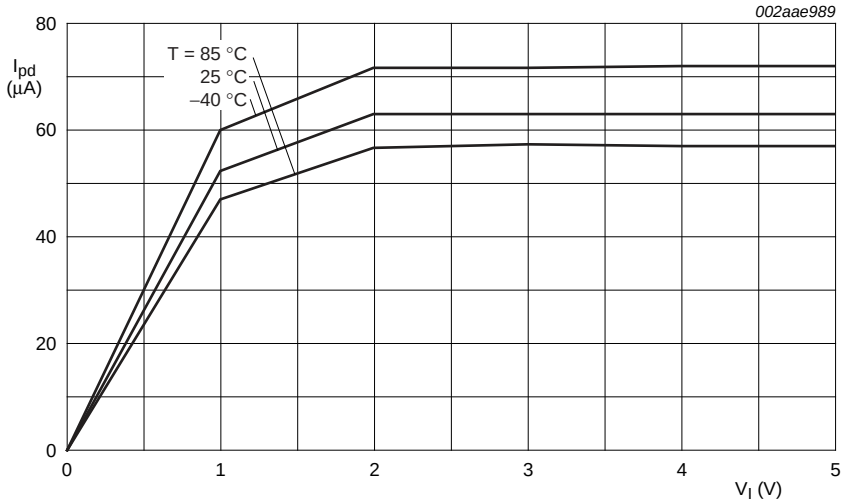

Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 19. Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output source current $I_{OH}$**




Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 20. Typical pull-up current $I_{pu}$ versus input voltage $V_I$**




Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 21. Typical pull-down current $I_{pd}$ versus input voltage $V_I$**

# 10. Dynamic characteristics

## 10.1 Flash/EEPROM memory

**Table 9. Flash characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $N_{endu}$ | endurance | | [1] | 10000 | 100000 | - | cycles |
| $t_{ret}$ | retention time | powered | | 10 | - | - | years |
| | | unpowered | | 20 | - | - | years |
| $t_{er}$ | erase time | sector or multiple consecutive sectors | | 95 | 100 | 105 | ms |
| $t_{prog}$ | programming time | | [2] | 0.95 | 1 | 1.05 | ms |

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

**Table 10. EEPROM characteristics**

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD}$ = 2.7 V to 3.6 V.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | | 200 | 375 | 400 | kHz |
| $N_{endu}$ | endurance | | 100000 | 1000000 | - | cycles |
| $t_{ret}$ | retention time | powered | 100 | 200 | - | years |
| | | unpowered | 150 | 300 | - | years |
| $t_{er}$ | erase time | 64 bytes | - | 1.8 | - | ms |
| $t_{prog}$ | programming time | 64 bytes | - | 1.1 | - | ms |

## 10.2 External clock

**Table 11. Dynamic characteristic: external clock**

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD}$ over specified ranges.*[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | | 1 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | 40 | - | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | | - | - | 5 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

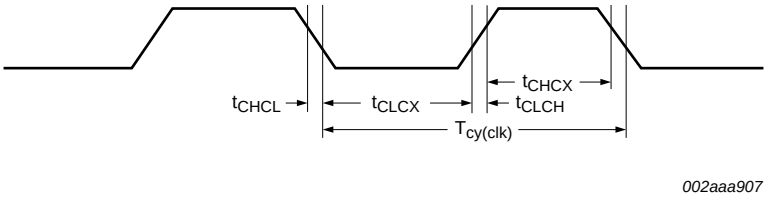



**Fig 22. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

## 10.3 Internal oscillators

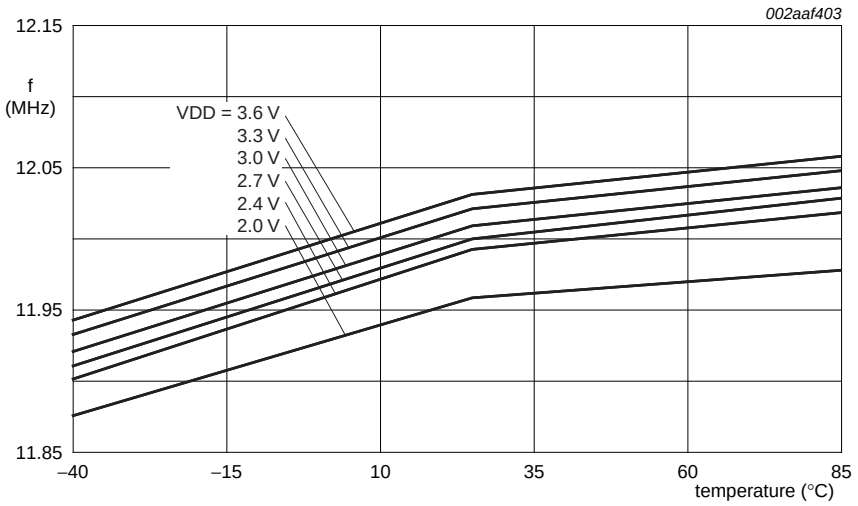
**Table 12. Dynamic characteristics: IRC**

*$T_{amb}$ = −40 °C to +85 °C; 2.7 V ≤ $V_{DD}$ ≤ 3.6 V*[1].

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.88 | 12 | 12.12 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.




Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD}$ ≤ 3.6 V and $T_{amb}$ = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

**Fig 23. Internal RC oscillator frequency versus temperature**

**Table 13. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2][3] | - | 9.4 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2][3] | - | 2300 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

[3] See the LPC1315/16/17/45/46/47 *user manual*.

## 10.4 I/O pins

**Table 14. Dynamic characteristics: I/O pins[1]**
*$T_{amb}$ = −40 °C to +85 °C; 3.0 V ≤ $V_{DD}$ ≤ 3.6 V.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_r$ | rise time | pin configured as output | 3.0 | - | 5.0 | ns |
| $t_f$ | fall time | pin configured as output | 2.5 | - | 5.0 | ns |

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

## 10.5 I²C-bus

**Table 15. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +85 °C.[2]*

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time | [4][5][6][7] | of both SDA and SCL signals | - | 300 | ns |
| | | | Standard-mode | | | |
| | | | Fast-mode | 20 + 0.1 × $C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [3][4][8] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [9][10] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] $C_b$ = total capacitance of one bus line in pF.

[6] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

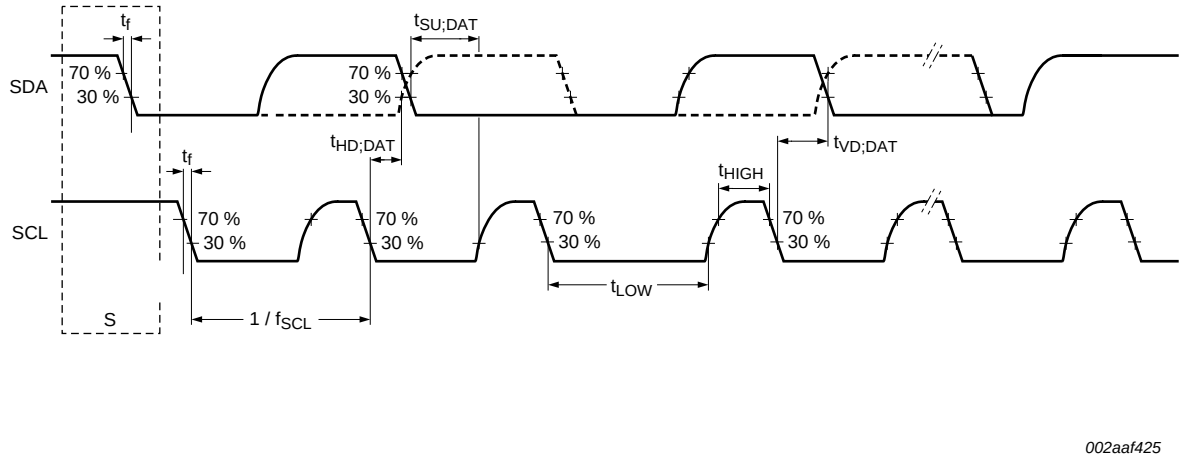



**Fig 24. I²C-bus pins clock timing**

## 10.6 SSP interface

**Table 16. Dynamic characteristics: SSP pins in SPI mode**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **SSP master** | | | | | | |
| $T_{cy(clk)}$ | clock cycle time | full-duplex mode | [1] | 40 | - | ns |
| | | when only transmitting | [1] | 27.8 | - | ns |
| $t_{DS}$ | data set-up time | in SPI mode; $2.4\ V \leq V_{DD} \leq 3.6\ V$ | [2] | 15 | - | ns |
| | | $2.0\ V \leq V_{DD} < 2.4\ V$ | [2] | 20 | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [2] | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [2] | - | 10 | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [2] | 0 | - | ns |
| **SSP slave** | | | | | | |
| $T_{cy(PCLK)}$ | PCLK cycle time | | | 13.9 | - | ns |
| $t_{DS}$ | data set-up time | in SPI mode | [3][4] | 0 | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [3][4] | $3 \times T_{cy(PCLK)} + 4$ | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [3][4] | - | $3 \times T_{cy(PCLK)} + 11$ | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [3][4] | - | $2 \times T_{cy(PCLK)} + 5$ | ns |

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency $f_{main}$, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{amb} = -40\ °C$ to $85\ °C$.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\ °C$; $V_{DD} = 3.3\ V$.

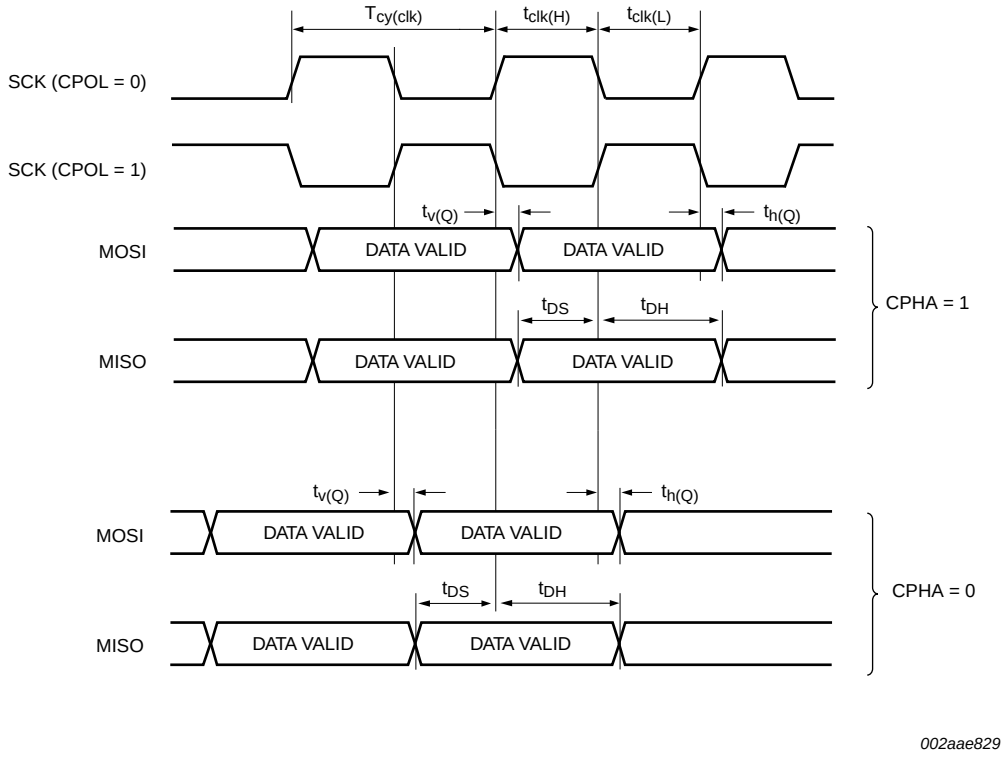



**Fig 25. SSP master timing in SPI mode**

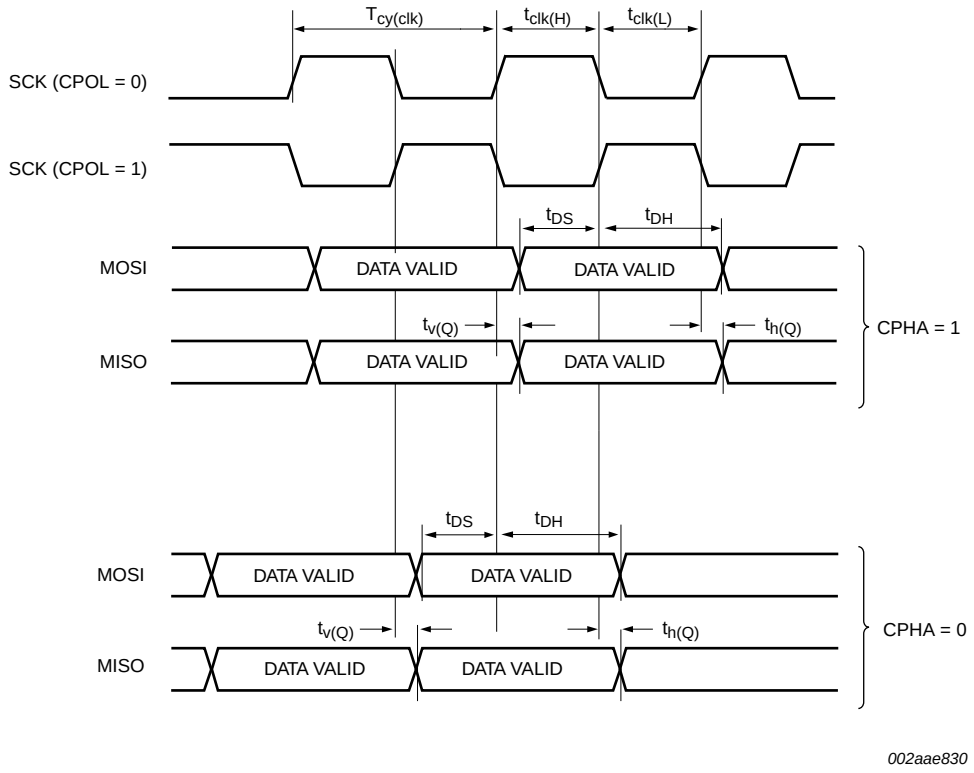



**Fig 26. SSP slave timing in SPI mode**

# 11. ADC electrical characteristics

**Table 17. ADC characteristics**

*$V_{DDA}$ = 2.7 V to 3.6 V; $T_{amb}$ = −40 °C to +85 °C unless otherwise specified; 12-bit resolution.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | | | 0 | - | $V_{DDA}$ | V |
| $C_{ia}$ | analog input capacitance | | | - | 5 | - | pF |
| $I_{DDA(ADC)}$ | ADC analog supply current | on pin $V_{DDA}$ (LQFP64 package only) | [1] | - | 5 | - | μA |
| | | low-power mode | | | | | |
| | | during ADC conversions | | - | 350 | - | μA |
| $E_D$ | differential linearity error | | [2][3] | - | - | ±1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | | [4] | - | - | ±5 | LSB |
| $E_O$ | offset error | | [5][6] | - | - | ±2.5 | LSB |
| $E_G$ | gain error | | [7] | - | - | ±0.3 | % |
| $E_T$ | absolute error | | [8] | - | - | 7 | LSB |
| $R_{vsi}$ | voltage source interface resistance | | [9] | - | 1 | - | kΩ |
| $f_{clk(ADC)}$ | ADC clock frequency | | | - | - | 15.5 | MHz |
| $f_{c(ADC)}$ | ADC conversion frequency | | [10] | - | - | 500 | kHz |

[1] Select the ADC low-power mode by setting the LPWRMODE bit in the ADC CR register. See the *LPC1315/16/17/45/46/47 user manual*.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 27.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 27.

[5] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 27.

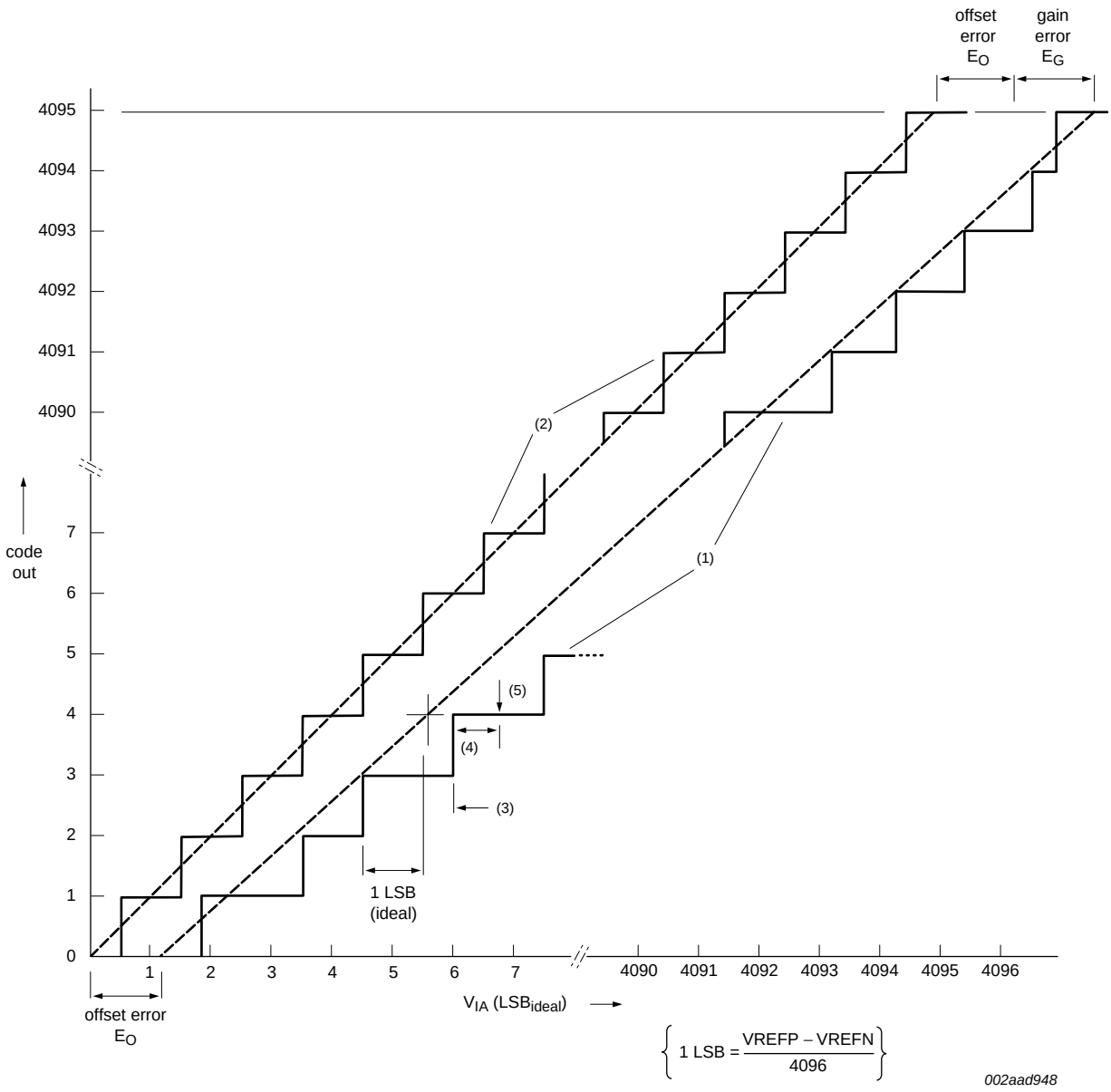
[6] ADCOFFS value (bits 7:4) = 2 in the ADC TRM register. See the *LPC1315/16/17/45/46/47 user manual*.

[7] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 27.

[8] The absolute error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 27.

[9] See Figure 27.

[10] The conversion frequency corresponds to the number of samples per second.




(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 27. 12-bit ADC characteristics**

# 12. Application information

## 12.1 Suggested USB interface solutions

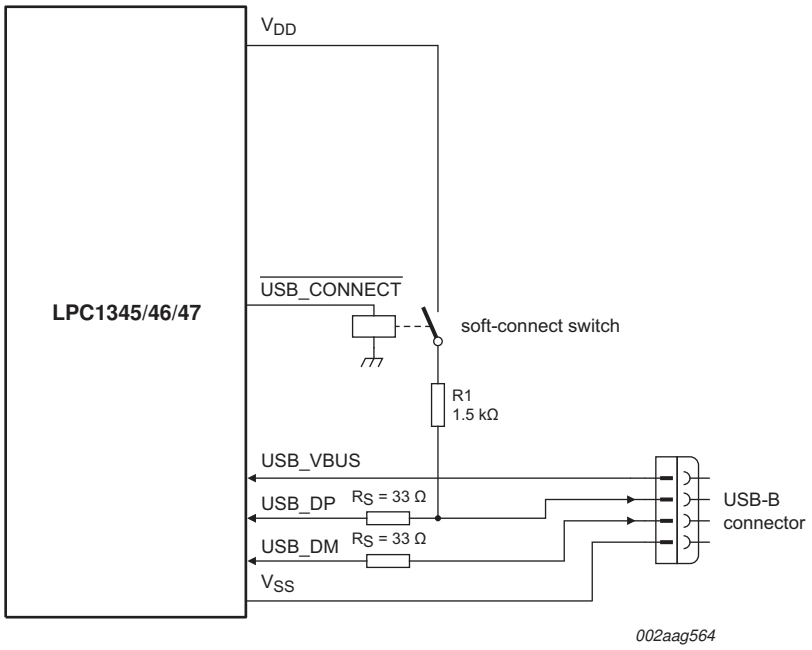



**Fig 28. USB interface on a self-powered device**

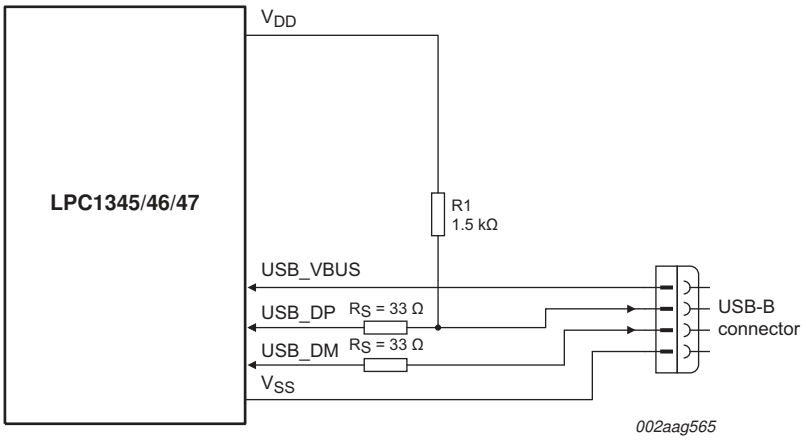



**Fig 29. USB interface on a bus-powered device**

## 12.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i$ = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground $C_g$ which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

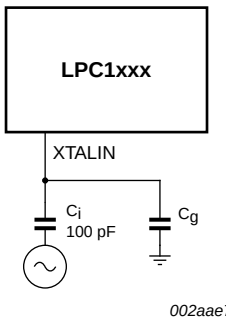



**Fig 30. Slave mode operation of the on-chip oscillator**

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 30), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 31 and in Table 18 and Table 19. Since the feedback resistance is integrated on chip, only a crystal and the capacitances $C_{X1}$ and $C_{X2}$ need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, $C_L$ and $R_S$). Capacitance $C_P$ in Figure 31 represents the parallel package capacitance and should not be larger than 7 pF. Parameters $F_{OSC}$, $C_L$, $R_S$ and $C_P$ are supplied by the crystal manufacturer.

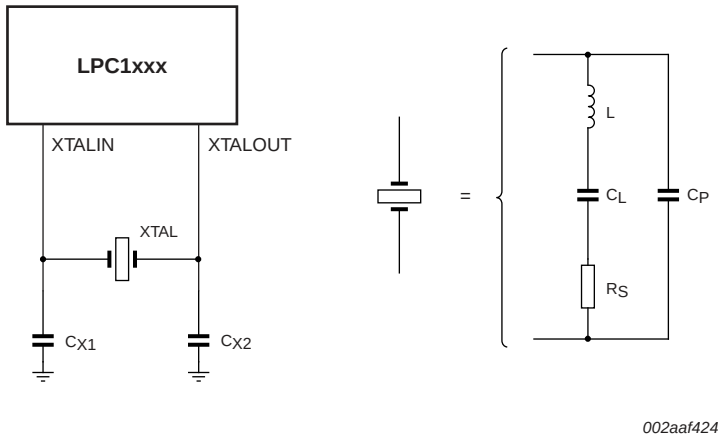



**Fig 31. Oscillator modes and models: oscillation mode of operation and external crystal model used for $C_{X1}/C_{X2}$ evaluation**

**Table 18. Recommended values for $C_{X1}/C_{X2}$ in oscillation mode (crystal and external components parameters) low frequency mode**

| Fundamental oscillation frequency $F_{OSC}$ | Crystal load capacitance $C_L$ | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|---|
| 1 MHz - 5 MHz | 10 pF | < 300 Ω | 18 pF, 18 pF |
| | 20 pF | < 300 Ω | 39 pF, 39 pF |
| | 30 pF | < 300 Ω | 57 pF, 57 pF |

**Table 18. Recommended values for $C_{X1}/C_{X2}$ in oscillation mode (crystal and external components parameters) low frequency mode**

| Fundamental oscillation frequency $F_{OSC}$ | Crystal load capacitance $C_L$ | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|---|
| 5 MHz - 10 MHz | 10 pF | < 300 Ω | 18 pF, 18 pF |
| | 20 pF | < 200 Ω | 39 pF, 39 pF |
| | 30 pF | < 100 Ω | 57 pF, 57 pF |
| 10 MHz - 15 MHz | 10 pF | < 160 Ω | 18 pF, 18 pF |
| | 20 pF | < 60 Ω | 39 pF, 39 pF |
| 15 MHz - 20 MHz | 10 pF | < 80 Ω | 18 pF, 18 pF |

**Table 19. Recommended values for $C_{X1}/C_{X2}$ in oscillation mode (crystal and external components parameters) high frequency mode**

| Fundamental oscillation frequency $F_{OSC}$ | Crystal load capacitance $C_L$ | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|---|
| 15 MHz - 20 MHz | 10 pF | < 180 Ω | 18 pF, 18 pF |
| | 20 pF | < 100 Ω | 39 pF, 39 pF |
| 20 MHz - 25 MHz | 10 pF | < 160 Ω | 18 pF, 18 pF |
| | 20 pF | < 80 Ω | 39 pF, 39 pF |

## 12.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors $C_{x1}$, $C_{x2}$, and $C_{x3}$ in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of $C_{x1}$ and $C_{x2}$ should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

## 12.4 Standard I/O pad configuration

Figure 32 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

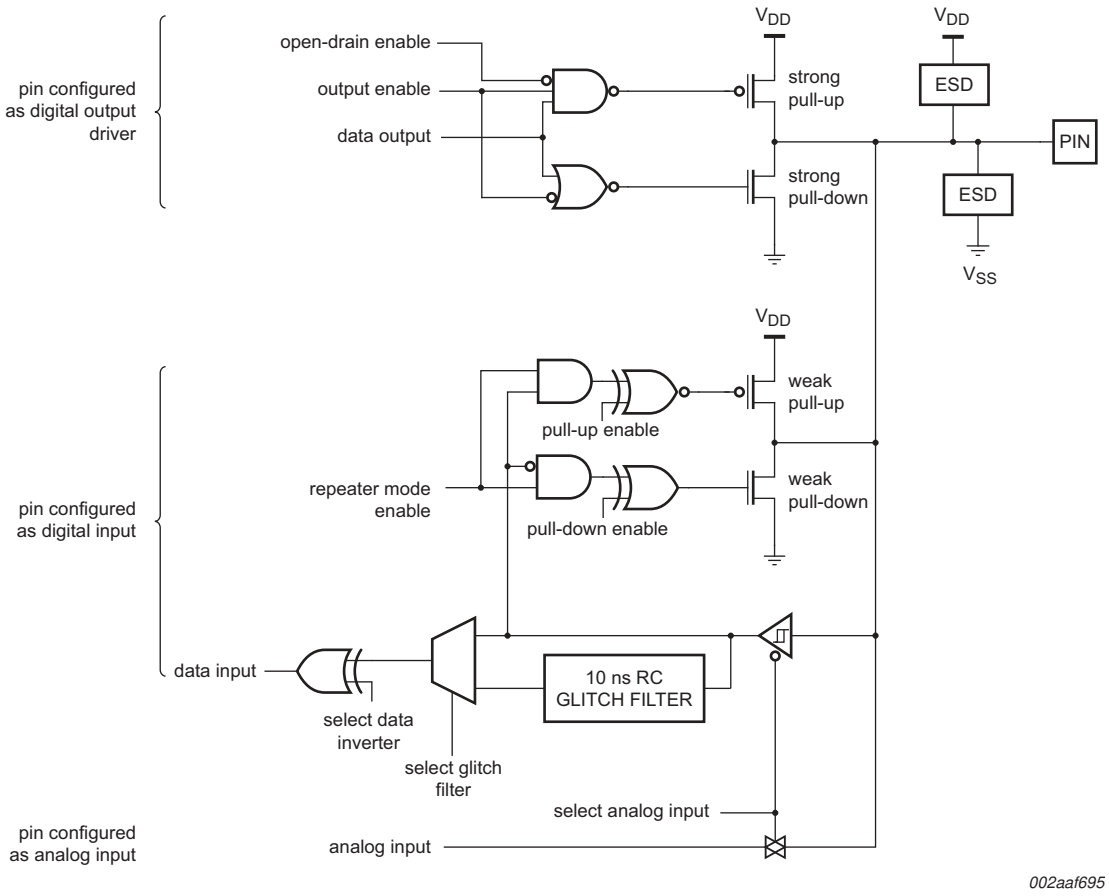



**Fig 32. Standard I/O pad configuration**

## 12.5 Reset pad configuration

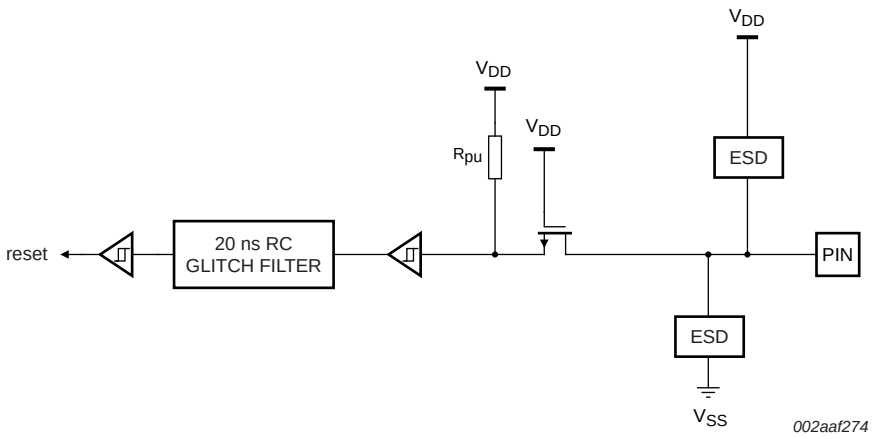



**Fig 33. Reset pad configuration**

## 12.6 ADC usage notes

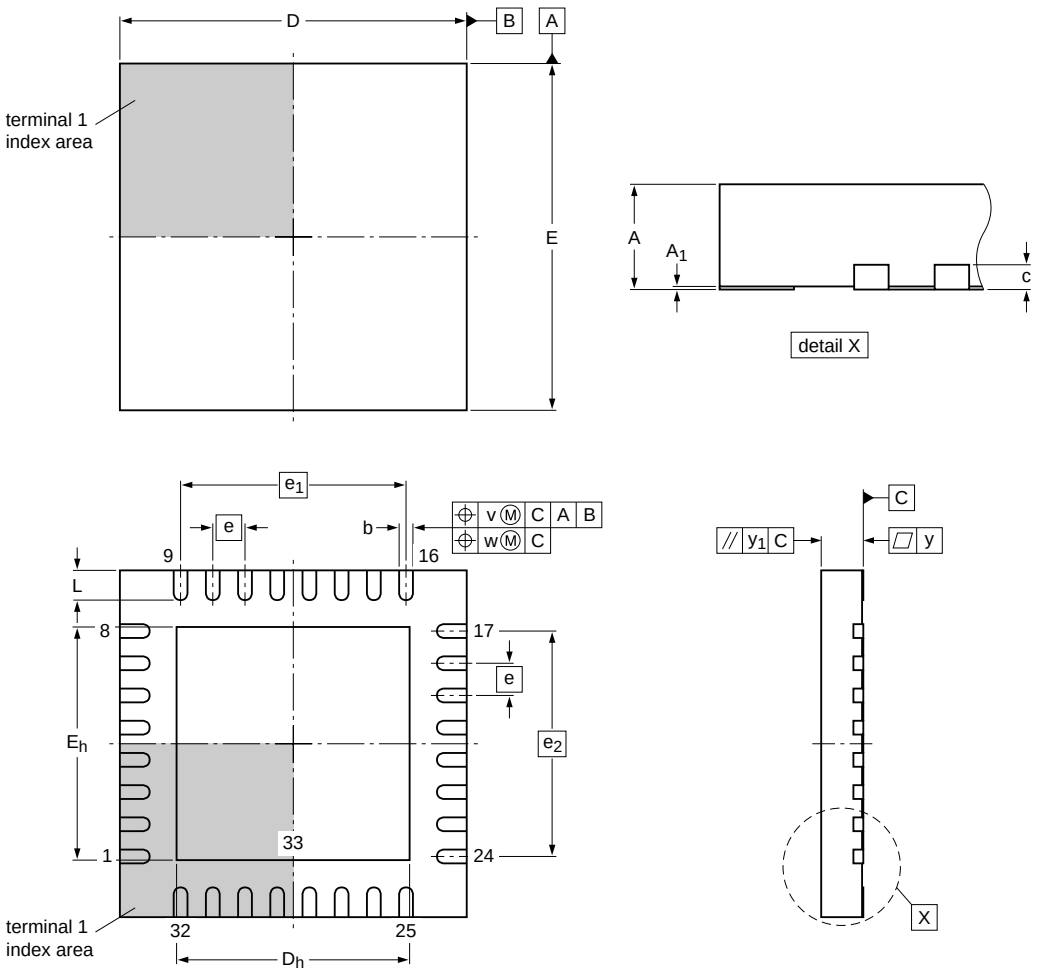
The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 17:

- The ADC input trace must be short and as close as possible to the LPC1315/16/17/45/46/47 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

**Remark:** On the LQFP64 package, the analog power supply and the reference voltage can be connected on separate pins for better noise immunity.

# 13. Package outline

**HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm**




Dimensions

| Unit | | $A^{(1)}$ | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.35 | | 7.1 | 4.85 | 7.1 | 4.85 | | | | 0.75 | | | | |
| mm | nom | 0.85 | 0.02 | 0.28 | 0.2 | 7.0 | 4.70 | 7.0 | 4.70 | 0.65 | 4.55 | 4.55 | 0.60 | 0.1 | 0.05 | 0.08 | 0.1 |
| | min | 0.80 | 0.00 | 0.23 | | 6.9 | 4.55 | 6.9 | 4.55 | | | | 0.45 | | | | |

Note

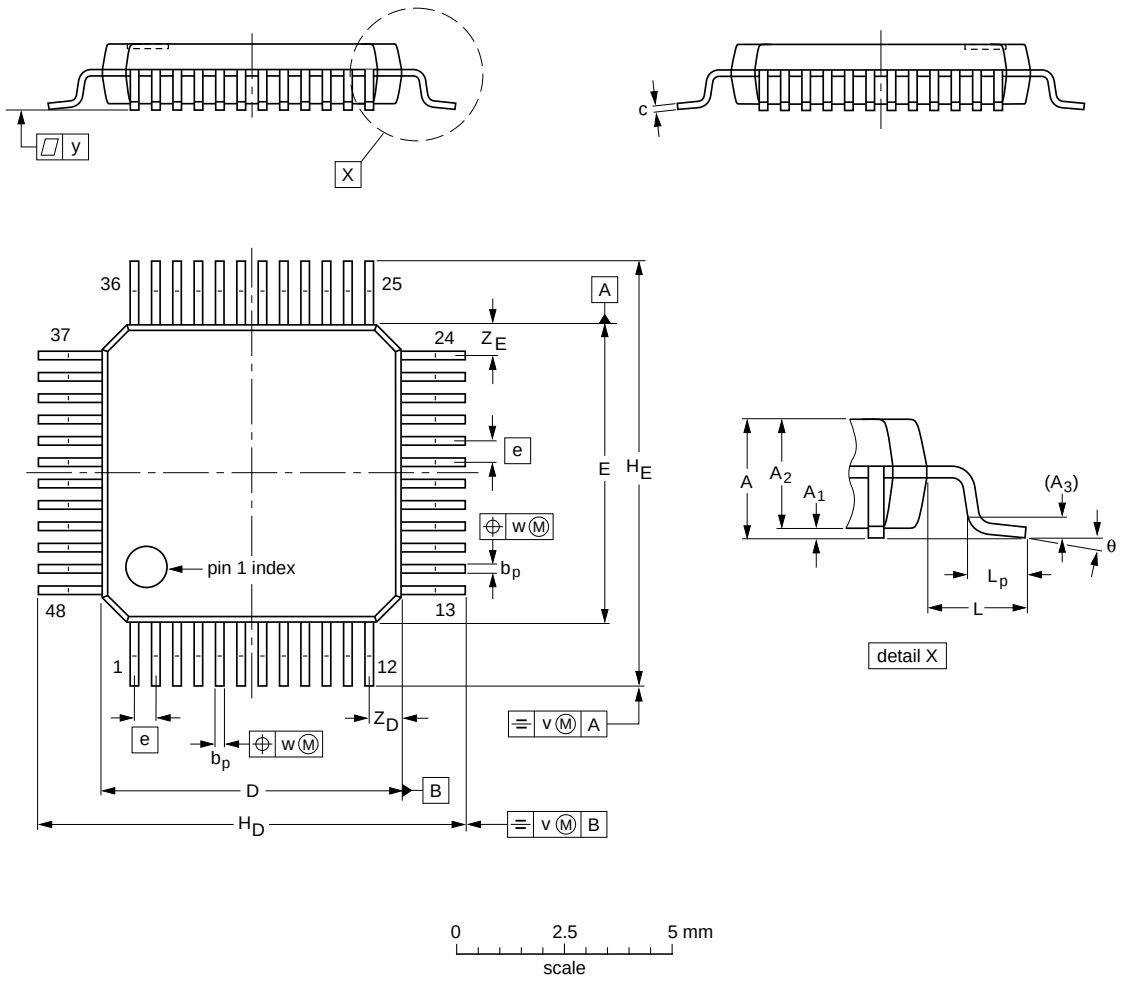
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*hvqfn33_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| | | - - - | | | | ~~09-03-17~~ 09-03-23 |

**Fig 34. Package outline HVQFN33**

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

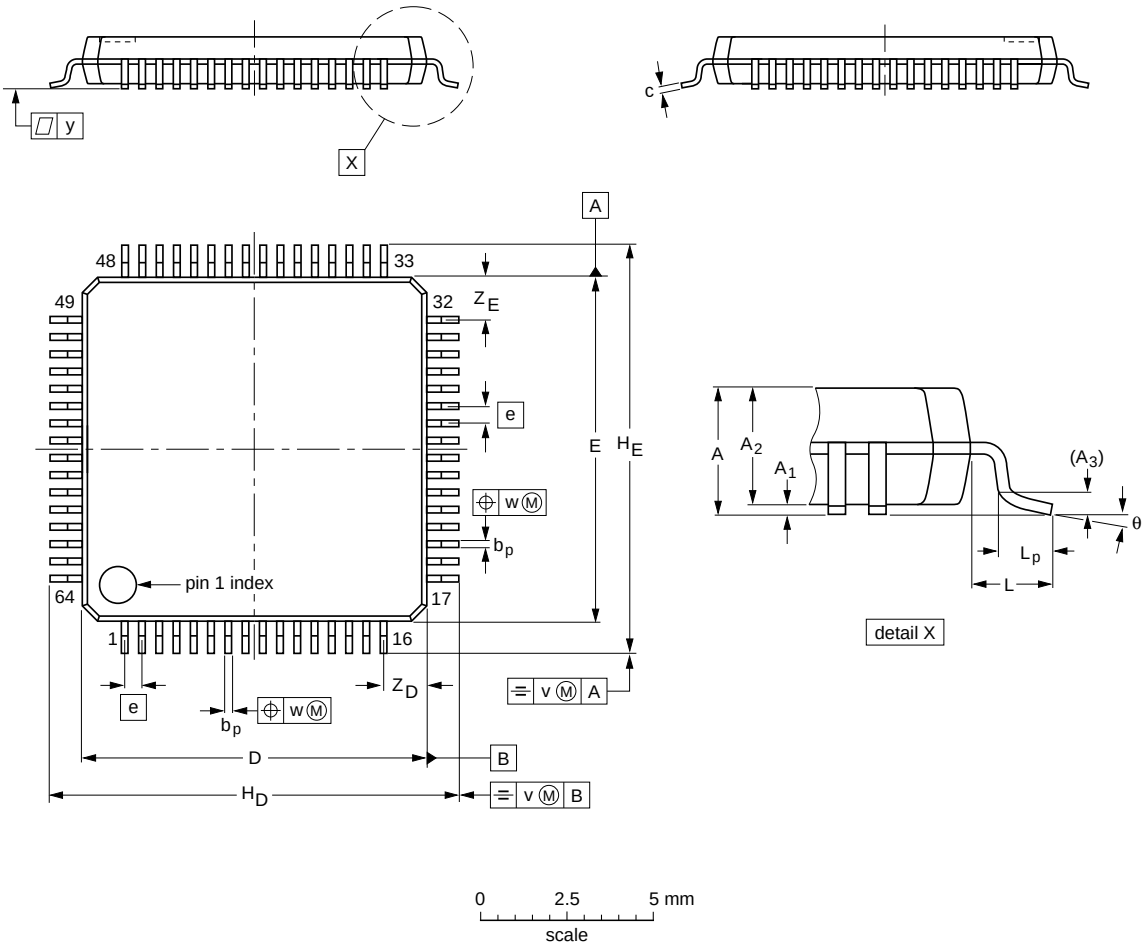
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 35. Package outline LQFP48 (SOT313-2)**

**LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm** **SOT314-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 10.1<br>9.9 | 10.1<br>9.9 | 0.5 | 12.15<br>11.85 | 12.15<br>11.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 1.45<br>1.05 | 1.45<br>1.05 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT314-2 | 136E10 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 36. Package outline LQFP64 (SOT314-2)**

# 14. Soldering

**Footprint information for reflow soldering of HVQFN33 package**

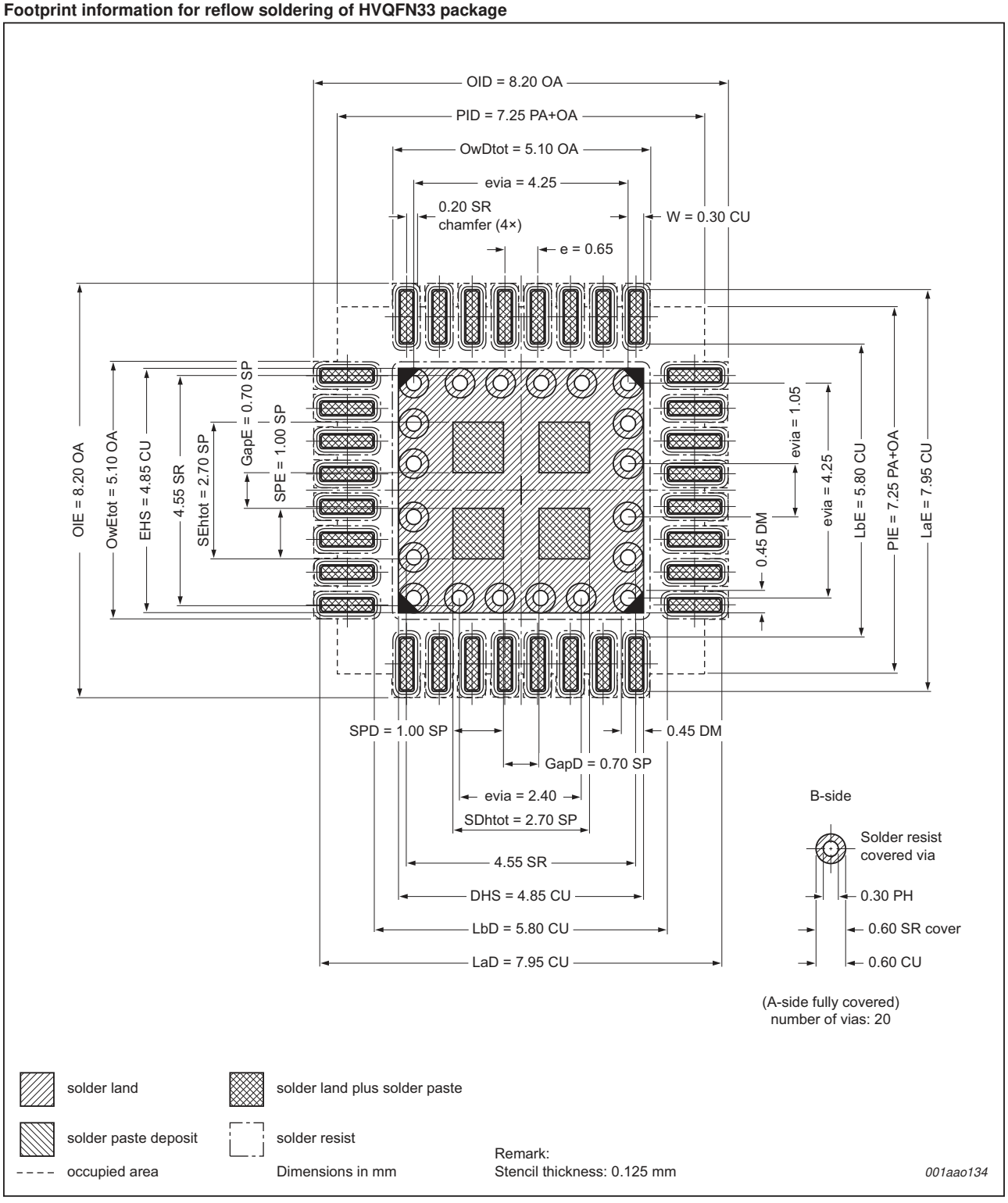
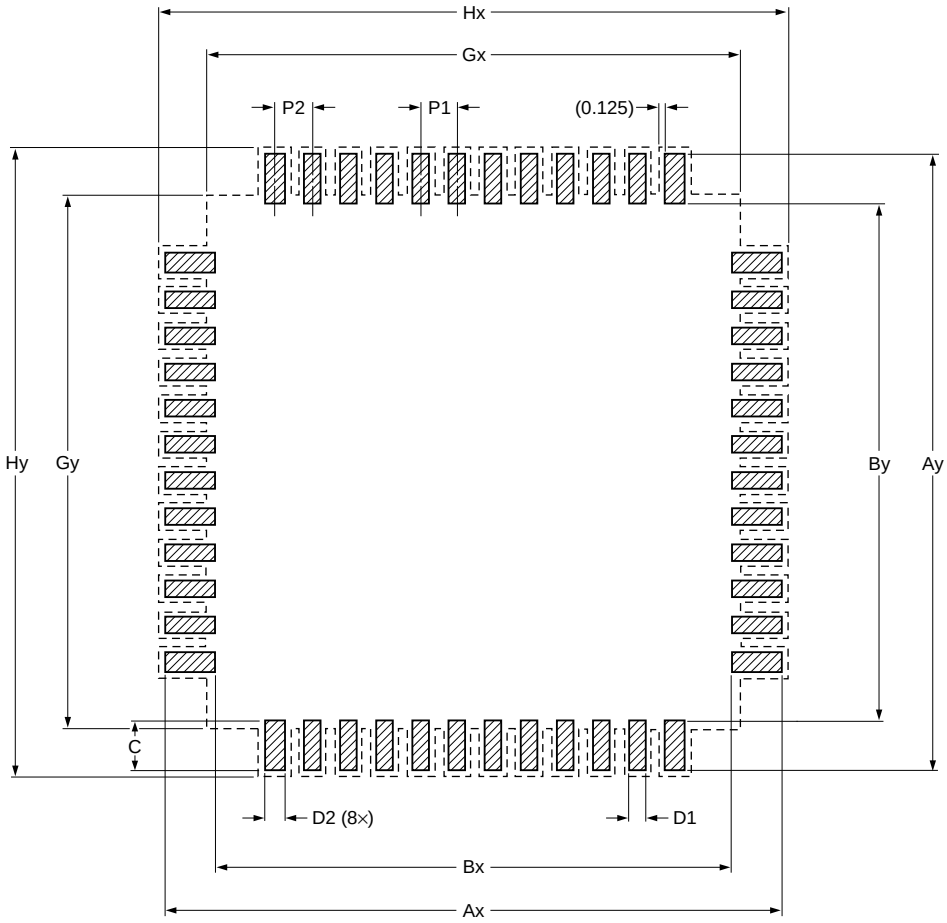



**Fig 37. Reflow soldering of the HVQFN33 package**

**Footprint information for reflow soldering of LQFP48 package** **SOT313-2**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

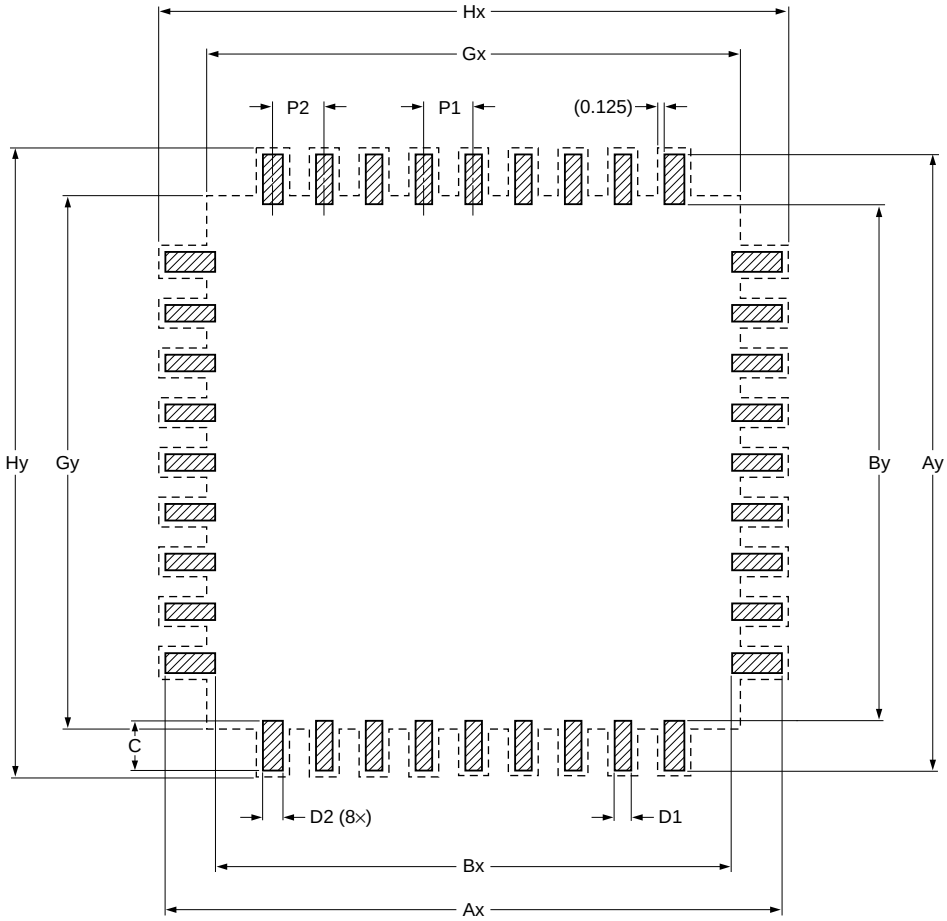
DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 10.350 | 10.350 | 7.350 | 7.350 | 1.500 | 0.280 | 0.500 | 7.500 | 7.500 | 10.650 | 10.650 |

*sot313-2_fr*

**Fig 38. Reflow soldering of the LQFP48 package**

**Footprint information for reflow soldering of LQFP64 package** **SOT314-2**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 13.300 | 13.300 | 10.300 | 10.300 | 1.500 | 0.280 | 0.400 | 10.500 | 10.500 | 13.550 | 13.550 |

*sot314-2_fr*

**Fig 39. Reflow soldering of the LQFP64 package**

# 15. Abbreviations

Table 20. Abbreviations

| Acronym | Description |
|---|---|
| A/D | Analog-to-Digital |
| ADC | Analog-to-Digital Converter |
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CDC | Communication Device Class |
| ETM | Embedded Trace Macrocell |
| GPIO | General Purpose Input/Output |
| HID | Human Interface Device |
| JTAG | Joint Test Action Group |
| MSC | Mass Storage Class |
| PLL | Phase-Locked Loop |
| RC | Resistor-Capacitor |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| TAP | Test Access Port |
| USART | Universal Synchronous Asynchronous Receiver/Transmitter |

# 16. Revision history

**Table 21. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC1315_16_17_45_46_47 v.3 | 20120920 | Product data sheet | - | LPC1315_16_17_45_46_47 v.2 |
| | • Reflow soldering drawing corrected for the HVQFN33 package. See Figure 37.<br>• BOD interrupt trigger level 0 removed. See Table 7.<br>• Pin configuration diagrams updated: Orientation of index sector relative to part marking corrected in Figure 4 to Figure 7. | | | |
| LPC1315_16_17_45_46_47 v.2 | 20120718 | Product data sheet | - | LPC1315_16_17_45_46_47 v.1 |
| Modifications: | • Data sheet status changed to Product data sheet.<br>• Parameters $V_{OL}$, $V_{OH}$, $I_{OL}$, $I_{OH}$ updated for voltage range 2.0 V ≤ $V_{DD}$ < 2.5 V in Table 6.<br>• Condition “The peak current is limited to 25 times the corresponding maximum current.” removed from parameters $I_{DD}$ and $I_{SS}$ in Table 5.<br>• Typical operating frequencies of the watchdog oscillator corrected in Table 13 and Section 7.18.1.3. | | | |
| LPC1315_16_17_45_46_47 v.1 | 20120229 | Preliminary data sheet | - | - |

# 17. Legal information

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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