



## Data brief

## Bluetooth communication board based on BlueNRG-1





Product summary			
Bluetooth communication board based on the BlueNRG-1	AEK-COM- BLEV1		
Firmware for AEK- COM-BLEV1 testing	STSW-AEKBLE		
Bluetooth® low energy system-on-chip	BlueNRG-1		
Setup for BlueNRG kits	STSW- BLUENRG-DK		
$50\ \Omega$ , conjugate match balun to BlueNRG transceiver, with integrated harmonic filter	BALF- NRG-02D3		
Applications	Factory Automation Bluetooth Low Energy Mobility Services		

### **Features**

- Based on the BlueNRG-1 Bluetooth low energy system on chip
- Associated STSW-BLUENRG-DK (BlueNRG-1 development kit software package) including firmware and documentation
- Up to +8 dBm available output power (at antenna connector)
- Excellent receiver sensitivity (-88 dBm)
- Very low power consumption: 7.7 mA RX and 8.2 mA TX at +0 dBm
- Bluetooth<sup>®</sup> low energy compliant: supports master, slave and simultaneous master-and-slave roles
- New integrated balun BALF-NRG-02D3 which integrates a matching network and harmonics filter
- 3 user LEDs
- JTAG debug connector
- Pre-programmed as network processor
- Board size: 60 x 40 mm.
- Part of the AutoDevKit™ initiative
- RoHS and WEEE compliant

## **Description**

The AEK-COM-BLEV1 evaluation board is based on the BlueNRG-1 low power Bluetooth<sup>®</sup> smart system on chip, compliant with the Bluetooth<sup>®</sup> specification.

The evaluation board can be connected to a microcontroller via a 12-pin or alternative 9-pin male connector for SPI, serial interface or I<sup>2</sup>C communication.

The BlueNRG-1 device is supplied with the network processor software loaded and ready to process Bluetooth commands. The software image (DTM\_UART.hex) is available in the BlueNRG design kit.

The STSW-AEKBLE firmware provides a straightforward demonstration of the AEK-COM-BLEV1 board functionality used in conjunction with the AEK-MCU-C4MLIT1 evaluation board with microcontroller.



# 1 Loading firmware onto the BlueNRG-1 chip

Follow the procedure below to restore the factor firmware on the BlueNRG-1 device.

## **1.1** Hardware and software requirements

- ST-LINK/V2 programmer/debugger, which is connected through the evaluation board JTAG port
- STSW-LINK007 ST-LINK/V2 firmware upgrade
- STSW-LINK009 ST-LINK/V2 Windows driver
- STSW-BNRG1STLINK ST-LINK utility required to burn the code in the BlueNRG-1
- STSW-BLUENRG-DK design kit containing the Flash image for the BlueNRG-1. After installing the design kit, go to the installation directory ([Firmware ]>[BLE\_Examples]>[DTM]>[BlueNRG-1]) to find the "DTM\_UART.hex" file

### **1.2** Firmware burning procedure

- Step 1. Connect the ST-LINK/V2 to the PC via USB and to the AEK-COM-BLEV1 evaluation board JTAG port
- Step 2. Run the BlueNRG-1 ST-LINK Utility



#### Step 3. From the top menu, select [Target]>[Settings] and ensure the following parameters are set:

- Frequency: 4.0 MHz
- Mode: Normal
- Port: SWD

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#### Figure 1. BlueNRG-1 ST-LINK Utility settings

Serial Number					
53FF6C0672875	551163613	67		~	Refresh
Firmware	V2J34S7				
arget Information					
Target	BlueNRG-1				
Target Voltage	2.5 V			~	
Connection setting	ļS				
Connection setting Port	IS	Mode			
Port	) SWD	Mode			
Port OJTAG	is ) SWD	Mode Normal			~
Port OJTAG Frequency 4,0 MHz	) SWD	Mode Normal			~
Port OJTAG Frequency 4.0 MHz	) SWD V	Mode Normal			~

- Step 4. Press [OK] to confirm
- Step 5. From the main menu, select [Target]>[Connect] to connect the programmer The ST-LINK/V2 LED starts blinking
- Step 6. From main menu, select [Target]>[Program Verify]



#### Step 7. Press [Browse] and select DTM\_UART.hex from the disk to download it

Figure 2	DTM	_UART.hex file	downloading
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Download [ DTM_UART.hex ]	×
Start address : 0x10040000 File path : C:\Program Files (x86)\STMice	roelectronics\BlueNRG-1_2 Dł
Verification Overify while programming	Overify after programming
Click "Start" to program target.	
Reset after programming	Cancel

#### Step 8. Press [Start] to Flash the image onto the BlueNRG-1 memory

## Figure 3. BlueNRG-1 ST LINK Utility device memory

😼 BlueNRG-1 ST-LINK Utility

Memory displ	ay		Theip		
Address:	0x1004000	00 ~ Si	ze: 0	200C4	Data Width: 32 bits ~
Device Memo	ry @ 0x100	040000 : F	ile : DTM_U	JART.hex	
Target memory, Address range: [0x10040000 0x100600C4]					
Addres	0	4	8	С	ASCII
0x100400	20006	10040	10040	10040	Å!)
0x100400	AA555	00000	00000	00000	<sup>a</sup> U U <sup>a</sup>
0x100400	00000	00000	00000	10040	1
0x100400	00000	00000	10040	10040	;E
0x100400	10040	10040	00000	00000	0
0x100400	10040	10040	10040	10040	wmYc
0x100400	00000	00000	00000	00000	
0x100400	00000	10040	10040	10040	
0x100400	00000	10040	10040	10040	© <sup>3</sup> 1/2
0x100400	10040	10040	10040	10040	ÇÑÛå
0x100400	2008B	80084	9 <mark>1</mark> 014	AB010	.µ. HI.€HI.′A«
0x100400	430BB	60134	400C6	4C45D	> <sup>2</sup> . C F J . ` . h . @ ü Ñ E L
0x100400	60139	400B6	1C5BD	94004	.".`.h.@üÑ[.BL."
0x100400	B2A44	60144	400C6	9C00D	F ¤ <sup>2</sup> . C . ` . h . @ ü Ñ . œ
0x100400	2C050	B2DBD	DBEE2	4A3C4	\$,.ĐÛ²d+îÛ;I <j< td=""></j<>
<					

Step 9. From the main menu, select[]>[Target]>[Disconnect] to disconnect the programmer



# 2 Block diagram





## Schematic diagrams

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AEK-COM-BLEV1 Schematic diagrams

#### Figure 6. AEK-COM-BLEV1 schematic diagram (2 of 4)



#### Figure 7. AEK-COM-BLEV1 schematic diagram (3 of 4)











#### Figure 8. AEK-COM-BLEV1 schematic diagram (4 of 4)



# **Revision history**

#### Table 1. Document revision history

Date	Version	Changes
19-Feb-2020	1	Initial release.



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