HD-6408

CMOS Asynchronous Serial Manchester Adapter (ASMA)

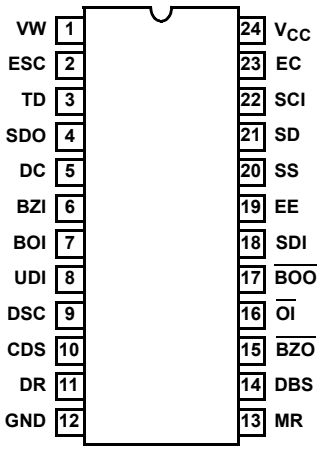
FN2952
Rev 3.00
October 1, 2015

The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data, adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. The Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

The HD-6408 can be used in many commercial applications such as security systems, environmental control systems, serial data links and many others. It utilizes a single 12 x clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

Pinout

HD-6408 (DIP)
TOP VIEW



Features

- Low Bit Error Rate
- Data Rate 1MBit/s
- Sync Identification and Lock-In
- Clock Recovery
- Manchester II Encoder, Decoder
- Separate Encode and Decode
- Low Operating Power. . . . . 50mW at 5V
- Single Power Supply
- 24 Ld Package
- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

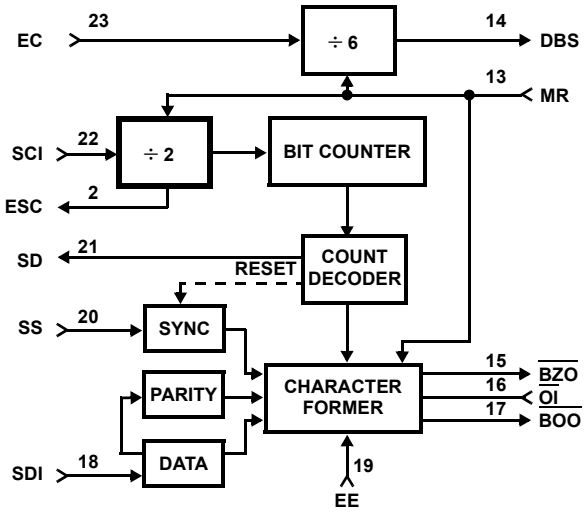
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HD3-6408-9 **No longer available or supported, recommended replacement HD3-6408-9Z**	HD3-6408-9	-40 to +85	24 Ld PDIP	E24.6
HD3-6408-9Z (Note)	HD3-6408-9Z	-40 to +85	24 Ld PDIP* (Pb-Free)	E24.6
HD1-6408-9	HD1-6408-9	-40 to +85	24 Ld CERDIP	F24.6

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

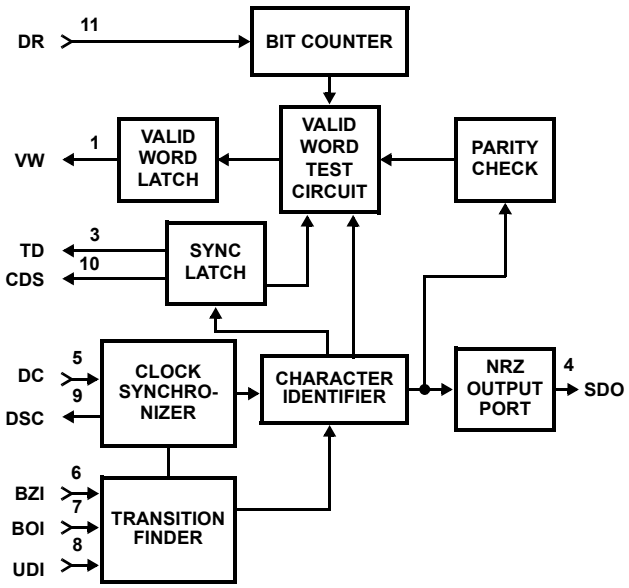
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Block Diagrams

ENCODER



DECODER



Pin Description

PIN	TYPE	SYMBOL	SECTION	DESCRIPTION
1	O	VW	Decoder	Output high indicates receipt of a VALID WORD.
2	O	ESC	Encoder	ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of ESC.
3	O	TD	Decoder	TAKE DATA output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SDO	Decoder	SERIAL DATA OUT delivers received data in correct NRZ format.
5	I	DC	Decoder	DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder. Input a frequency equal to 12X the data rate.
6	I	BZI	Decoder	A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BOI	Decoder	A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	I	UDI	Decoder	With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.
9	O	DSC	Decoder	DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK $^3\div$ 12), synchronized by the recovered serial data stream.
10	O	CDS	Decoder	COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.
11	I	DR	Decoder	A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GND	Both	GROUND supply pin.
13	I	MR	Both	A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder and the $^3 \div 6$ counter.
14	O	DBS	Encoder	DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BZO}}$	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$ is a active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OI}}$	Encoder	A low on $\overline{\text{OUTPUT INHIBIT}}$ forces pin 15 and 17 high, their inactive states.
17	O	$\overline{\text{BOO}}$	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$ is an active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SDI	Encoder	SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	EE	Encoder	A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being completed).
20	I	SS	Encoder	SYNC SELECT actuates a Command sync for an input high and data sync for an input low.
21	O	SD	Encoder	SEND DATA is an active high output which enables the external source of serial data.
22	I	SCI	Encoder	SEND CLOCK IN is 2X the Encoder data rate.
23	I	EC	Encoder	ENCODER CLOCK is the input to the 6:1 divider.
24	I	V_{CC}	Both	V_{CC} is the +5V power supply pin. A 0.1µF decoupling capacitor from V_{CC} (pin 24) to GND (pin 12) is recommended.

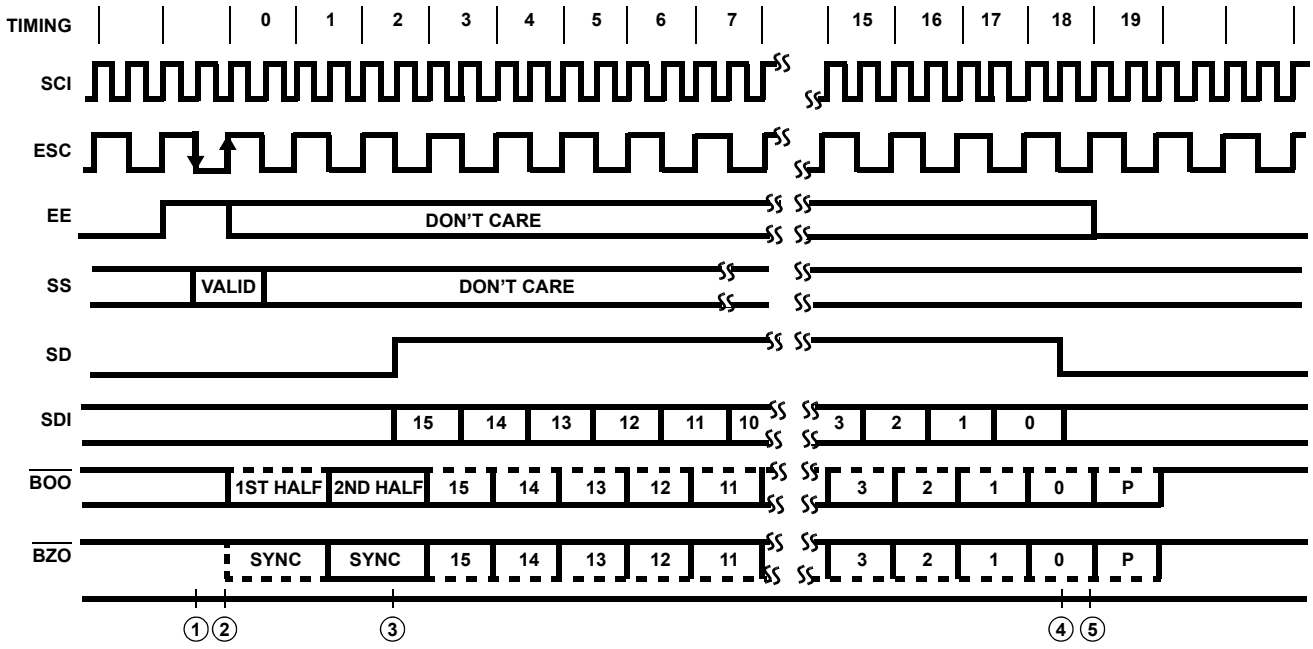
Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC (1). This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word (2). When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods (3) - (4).

During these sixteen periods the data should be clocked into the SD Input with every high-to-low transition of the ESC (3) - (4). After the sync and Manchester II encoded data are transmitted through the $\overline{BOO}$ and $\overline{BZO}$ outputs, the Encoder adds on an additional bit which is the (odd) parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{OI}$ will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To Abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SCI clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

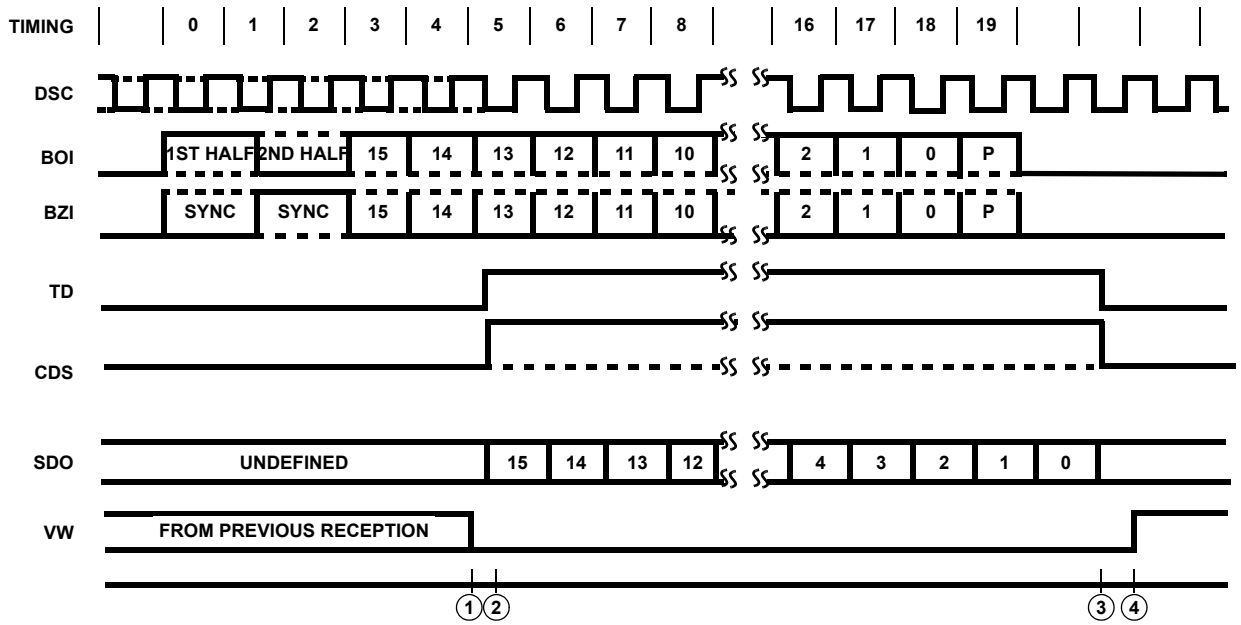
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from $\overline{BOO}$ of an Encoder through an inverter to UDI).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high (2) and remain high for sixteen DSC periods (3), otherwise it will remain low. The TD output will go high and remain high (2) - (3) while the Decoder is transmitting the decoded data through SDO.

The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock (2) - (3). Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VW output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown (1).

At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Gate Count. . . . . 456 Gates
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range. . . . . +4.5V to +5.5V
Operating Temperature Range
HD-6408-9 . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package.	50	11
PDIP Package*	60	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage		70% V_{CC}	-	-	V
V_{IL}	Logical "0" Input Voltage		-	20% V_{CC}	-	V
V_{IHC}	Logical "1" Input Voltage (Clock)		V_{CC} -0.5	-	-	V
V_{ILC}	Logical "0" Input Voltage (Clock)		-	GND +0.5	-	V
II	Input Leakage	V_{IN} = V_{CC} or GND, DIP Pins 5-8, 11, 13, 16, 18, 19, 20, 22, 23	-1.0	-	+1.0	µA
V_{OH}	Logical "1" Output Voltage	I_{OH} = -3mA	2.4	-	-	V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 1.8mA	-	-	0.4	V
I_{CCSB}	Supply Current Standby	V_{IN} = V_{CC} = 5.5V Outputs Open	-	0.5	2	mA
I_{CCOP}	Supply Current Operating (Note 1)	V_{CC} = 5.5V, f = 15MHz	-	8.0	10.0	mA

NOTE:

1. Guaranteed but not 100% tested.

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C

SYMBOL		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENCODER TIMING							
(1)	F_{EC}	Encoder Clock Frequency	C_L = 50pF	0	-	12	MHz
(2)	F_{ESC}	Send Clock Frequency	C_L = 50pF	0	-	2.0	MHz
(3)	T_{ECR}	Encoder Clock Rise Time	C_L = 50pF	-	-	8	ns
(4)	T_{ECF}	Encoder Clock Fall Time	C_L = 50pF	-	-	8	ns
(5)	F_{ED}	Data Rate	C_L = 50pF	0	-	1.0	MHz
(6)	T_{MR}	Master Reset Pulse Width	C_L = 50pF	150	-	-	ns
(7)	T_{E1}	Shift Clock Delay	C_L = 50pF	-	-	125	ns
(8)	T_{E2}	Serial Data Setup	C_L = 50pF	75	-	-	ns
(9)	T_{E3}	Serial Data Hold	C_L = 50pF	75	-	-	ns
(10)	T_{E4}	Enable Setup	C_L = 50pF	90	-	-	ns
(11)	T_{E5}	Enable Pulse Width	C_L = 50pF	100	-	-	ns
(12)	T_{E6}	Sync Setup	C_L = 50pF	55	-	-	ns
(13)	T_{E7}	Sync Pulse Width	C_L = 50pF	150	-	-	ns
(14)	T_{E8}	Send Data Delay	C_L = 50pF	0	-	50	ns
(15)	T_{E9}	Bipolar Output Delay	C_L = 50pF	-	-	130	ns

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C **(Continued)**

SYMBOL		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
(16)	T_{E10}	Enable Hold	C_L = 50pF	10	-	-	ns
(17)	T_{E11}	Sync Hold	C_L = 50pF	95	-	-	ns
DECODER TIMING							
(18)	F_{DC}	Decoder Clock Frequency	C_L = 50pF	0	-	12	MHz
(19)	T_{DCR}	Decoder Clock Rise Time	C_L = 50pF	-	-	8	ns
(20)	T_{DCF}	Decoder Clock Fall Time	C_L = 50pF	-	-	8	ns
(21)	F_{DD}	Data Rate	C_L = 50pF	0	-	1.0	MHz
(22)	T_{DR}	Decoder Reset Pulse Width	C_L = 50pF	150	-	-	ns
(23)	T_{DRS}	Decoder Reset Setup Time	C_L = 50pF	75	-	-	ns
(24)	T_{DRH}	Decoder Reset Hold Time	C_L = 50pF	10	-	-	ns
(25)	T_{MR}	Master Reset Pulse Width	C_L = 50pF	150	-	-	ns
(26)	T_{D1}	Bipolar Data Pulse Width	Note 2, C_L = 50pF	T_{DC} +10	-	-	ns
(27)	T_{D2}	Sync Transition Span	Note 2, C_L = 50pF	-	$18T_{DC}$	-	ns
(28)	T_{D3}	One Zero Overlap	Note 2, C_L = 50pF	-	-	T_{DC} -10	ns
(29)	T_{D4}	Short Data Transition Span	Note 2, C_L = 50pF	-	$6T_{DC}$	-	ns
(30)	T_{D5}	Long Data Transition Span	Note 2, C_L = 50pF	-	$12T_{DC}$	-	ns
(31)	T_{D6}	Sync Delay (ON)	C_L = 50pF	-20	-	110	ns
(32)	T_{D7}	Take Data Delay (ON)	C_L = 50pF	0	-	110	ns
(33)	T_{D8}	Serial Data Out Delay	C_L = 50pF	-	-	80	ns
(34)	T_{D9}	Sync Delay (OFF)	C_L = 50pF	0	-	110	ns
(35)	T_{D10}	Take Data Delay (OFF)	C_L = 50pF	0	-	110	ns
(36)	T_{D11}	Valid Word Delay	C_L = 50pF	0	-	110	ns

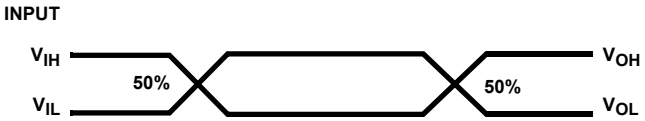
NOTE:

2. T_{DC} = Decoder Clock Period = $^1/F_{DC}$. (These parameters are guaranteed but not 100% tested).

Capacitance T_A = +25°C

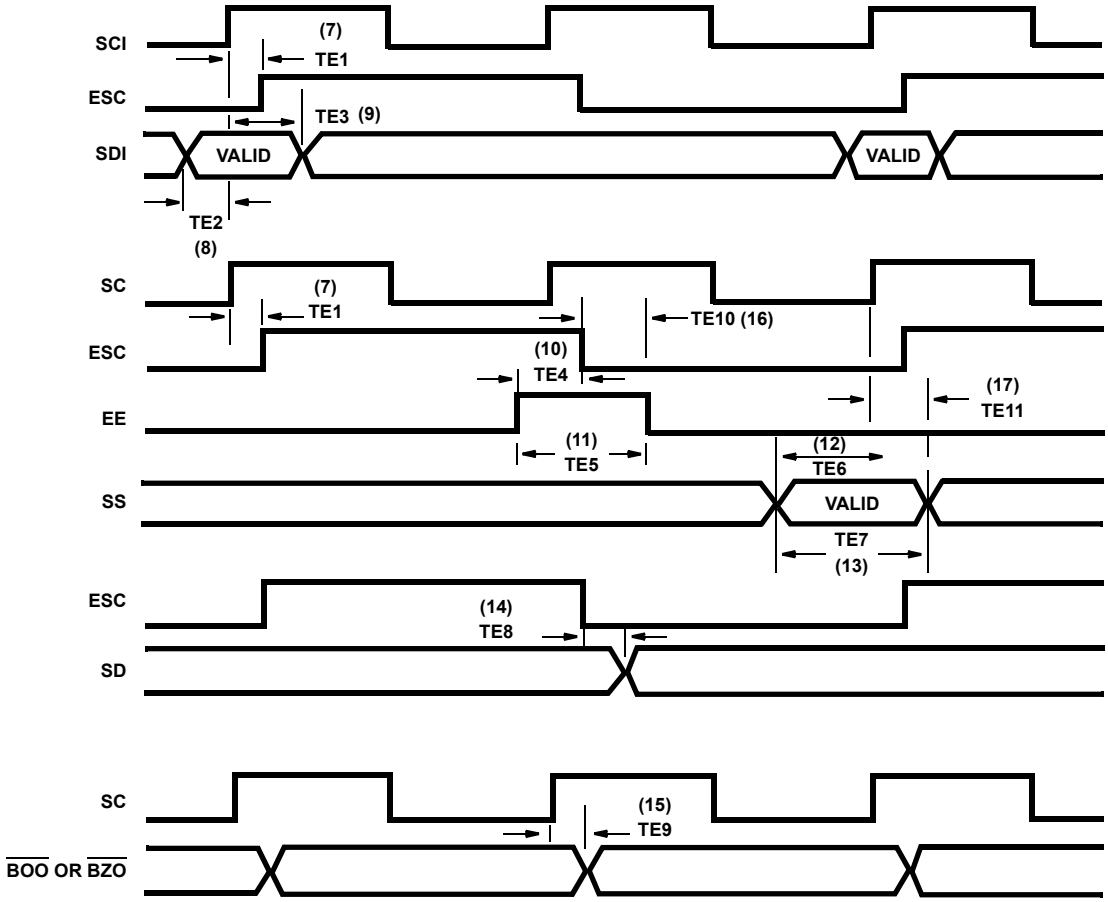
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	FREQ = 1MHz, all measurements are referenced to device GND	-	15	-	pF
C_O	Output Capacitance		-	15	-	pF

AC Testing Input, Output Waveform

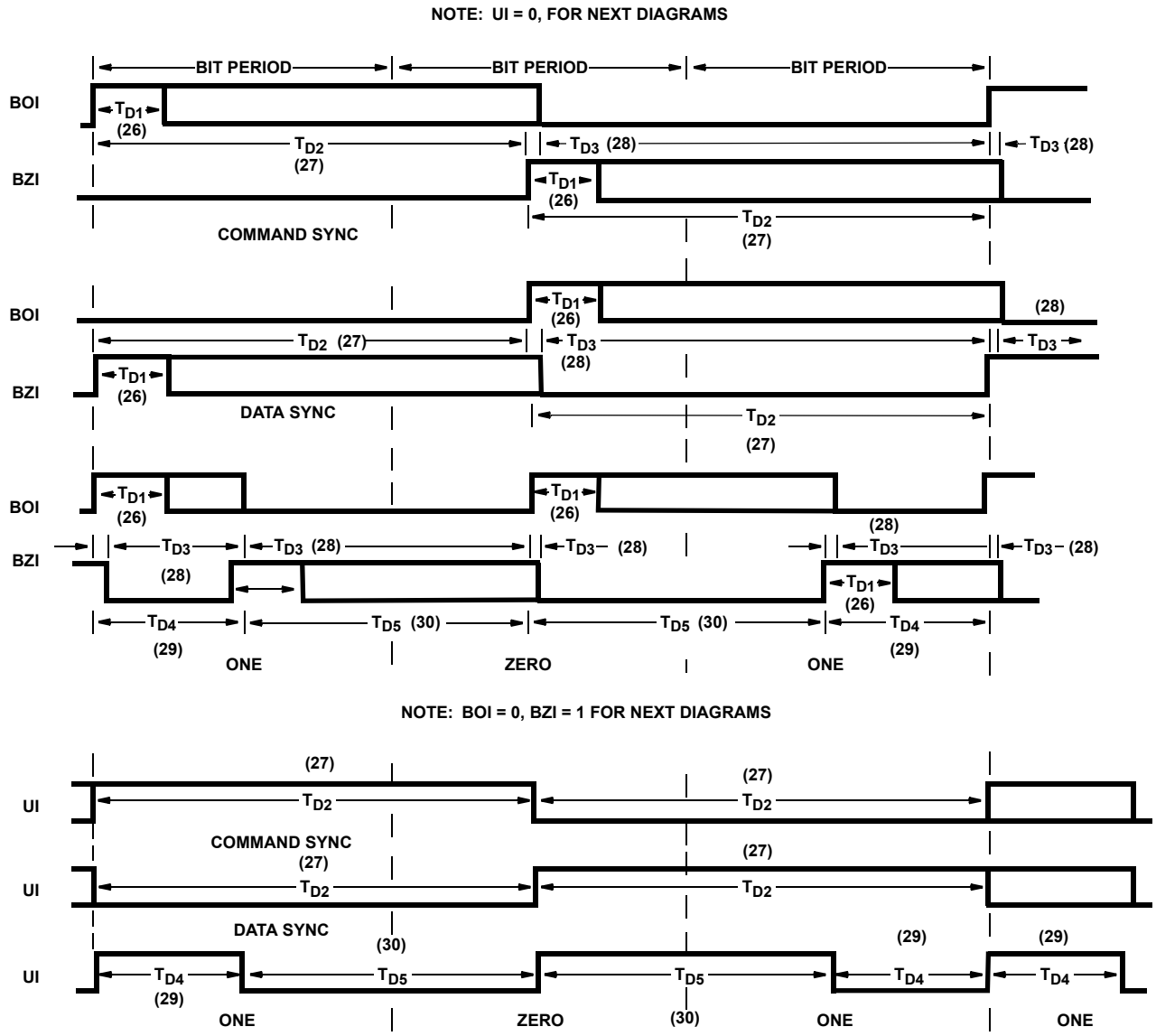


NOTE: AC Testing: All input signals must switch between V_{IL} and V_{IH}. Input rise and fall times are driven at 1ns per volt.

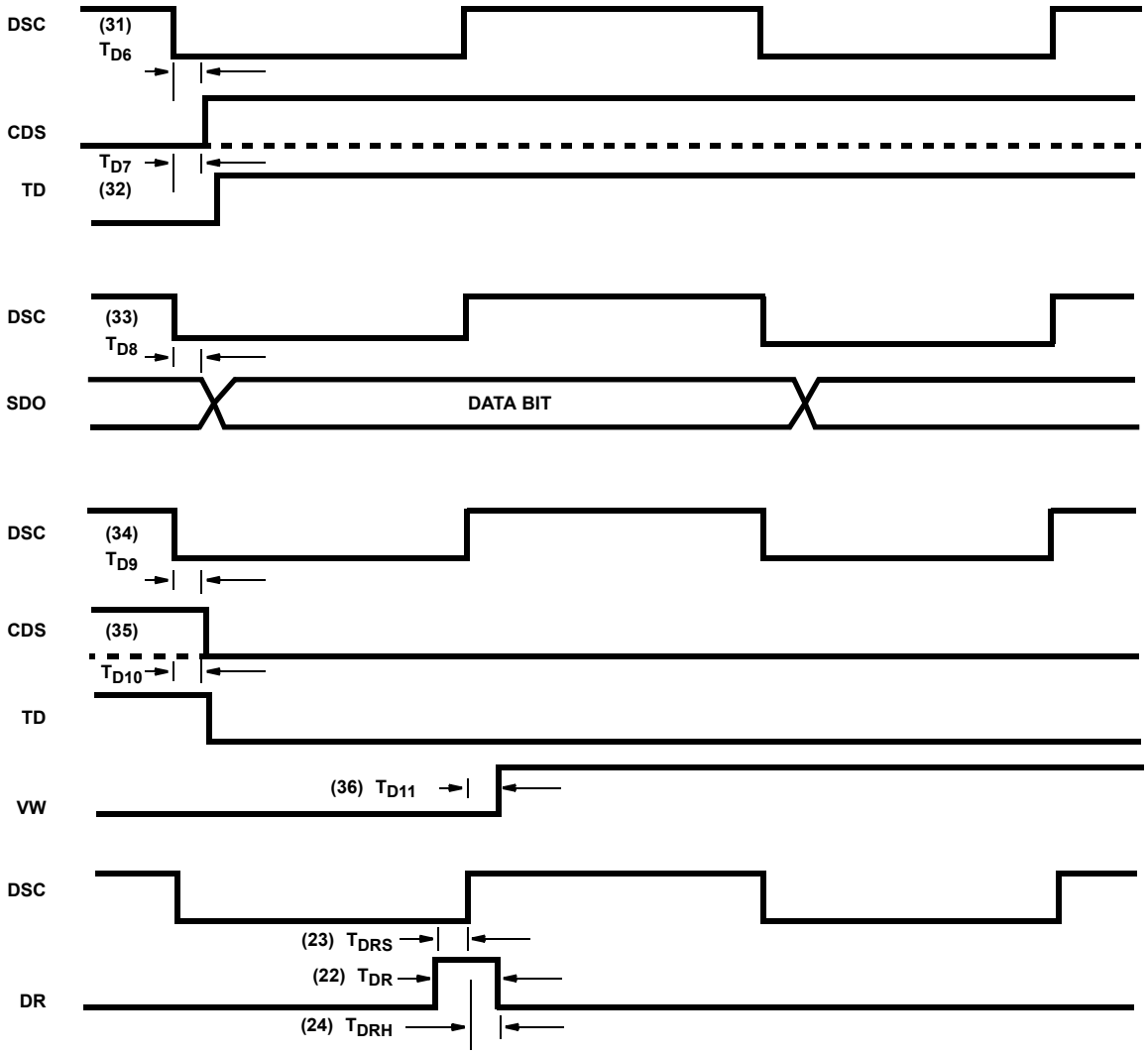
Encoder Timing



Decoder Timing



Decoder Timing (Continued)



Decoder Timing (Continued)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 1, 2015	FN2952.3	Added Rev History beginning with Rev 3. Added About Intersil Verbiage. Updated Ordering Information on page 1

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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