DATA SHEET

74F298
Quad 2-input multiplexer with storage

Product specification

1989 Aug 14

IC15 Data Handbook

Philips
Semiconductors

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Quad 2-input multiplexer with storage 74F298

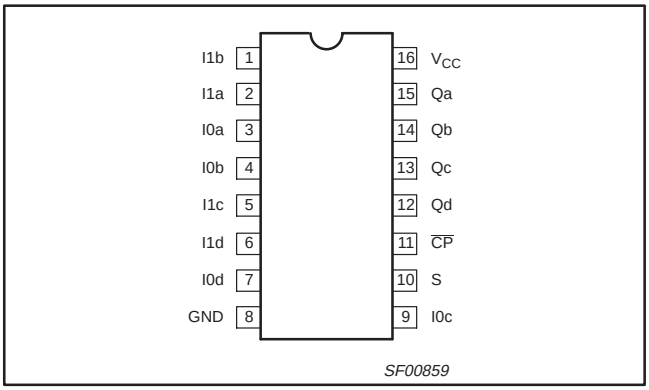
FEATURES

- Fully synchronous operation
- Select from two data sources
- Buffered, negative edge triggered clock
- Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)

DESCRIPTION

The 74F298 is a high speed Quad 2-Input Multiplexer with storage. It selects 4 bits of data from two sources (ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the clock ($\overline{CP}$). The 4-bit register is fully edge triggered. The data inputs (I0 and I1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING INFORMATION

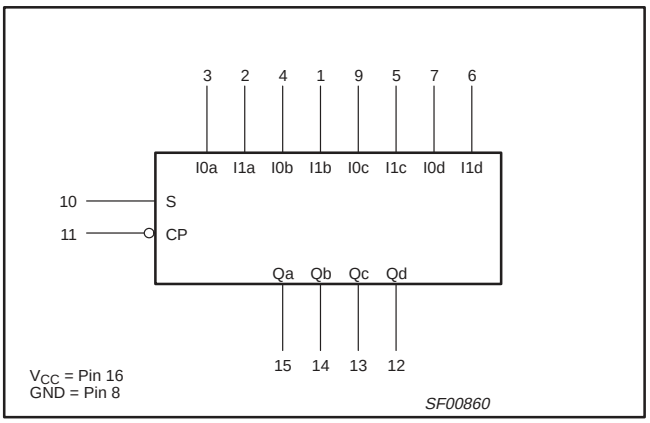
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F298N	SOT38-4
16-pin plastic SO	N74F298D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

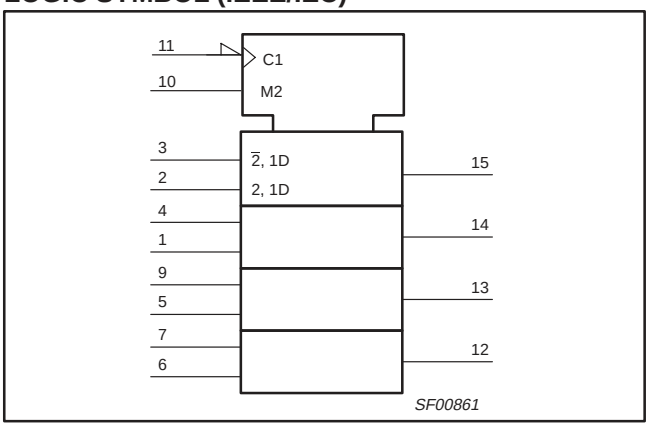
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a, I0b, I0c, I0d	Data inputs	1.0/1.0	20µA/0.6mA
I1a, I1b, I1c, I1d	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock input (active falling edge)	1.0/1.0	20µA/0.6mA
Qa, Qb, Qc, Qd	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

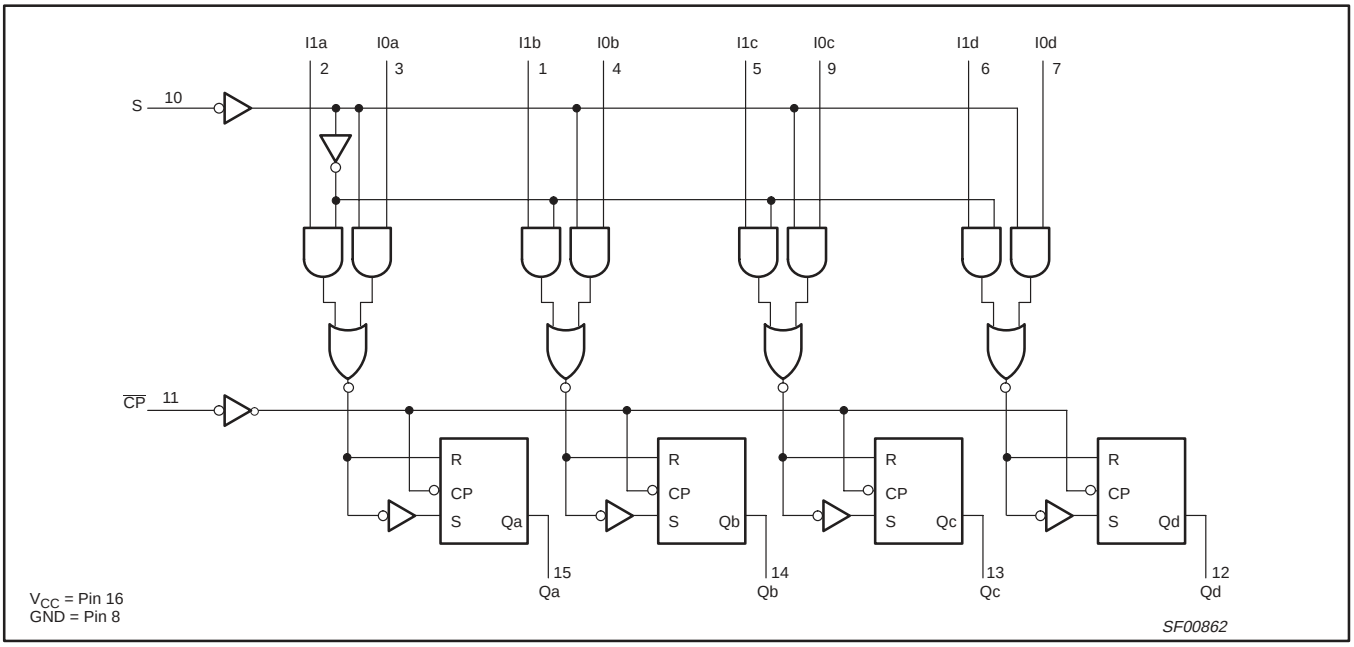
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	OPERATING MODE
$\overline{CP}$	S	I0n	I1n	Qn	
↓	l	l	X	L	Load source “0”
↓	l	h	X	H	
↓	h	X	l	L	Load source “1”
↓	h	X	h	H	

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low clock transition
X = Don’t care
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]		LIMITS			UNIT
					MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} =– MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[NO TAG]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				32	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform NO TAG	110	115		105		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ tp Qn	Waveform NO TAG	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

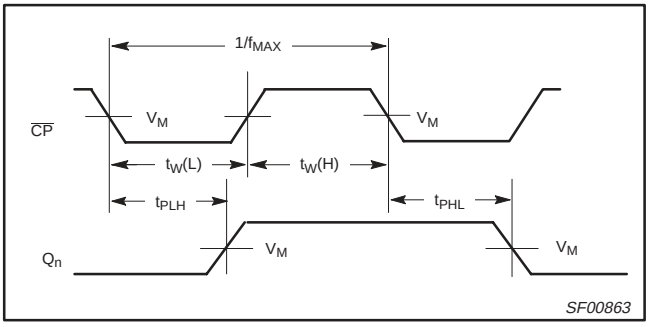
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low I0n, I1n to $\overline{CP}$	Waveform NO TAG	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low I0n, I1n to $\overline{CP}$	Waveform NO TAG	1.0 1.0			1.0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low S to $\overline{CP}$	Waveform NO TAG	6.0 5.0			7.0 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low S to $\overline{CP}$	Waveform NO TAG	0 0			0 0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width, High or Low	Waveform NO TAG	5.0 5.0			5.0 7.0		ns

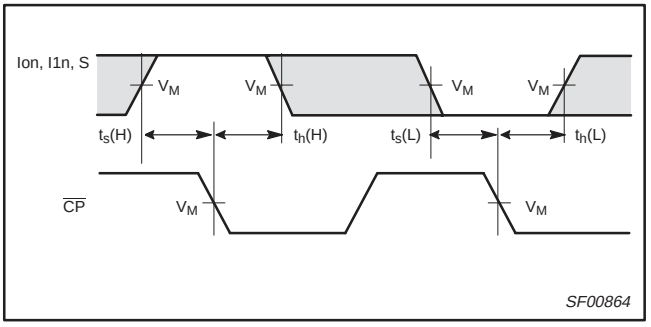
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

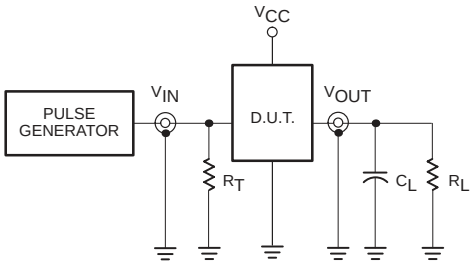


Waveform 1. Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

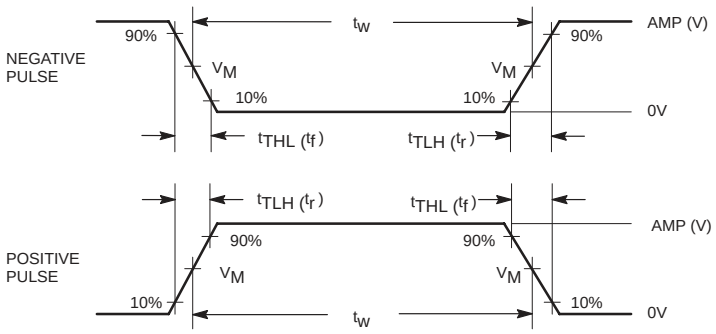


Waveform 2. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

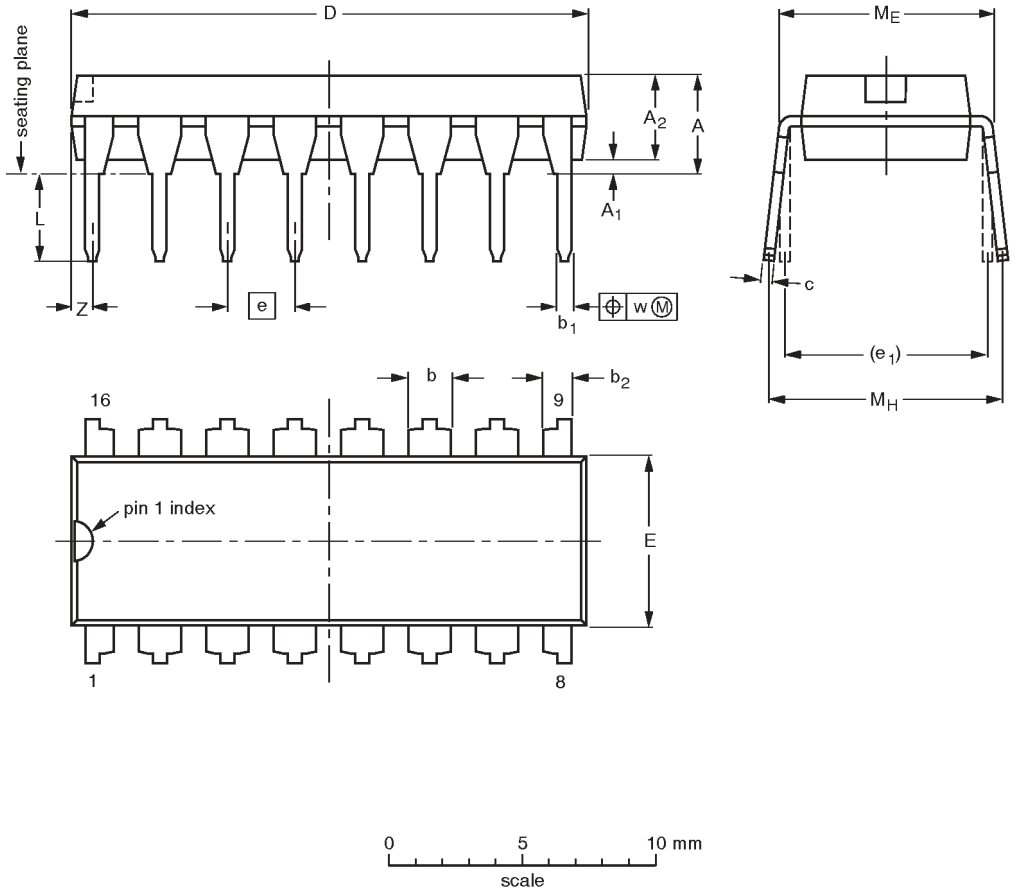
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

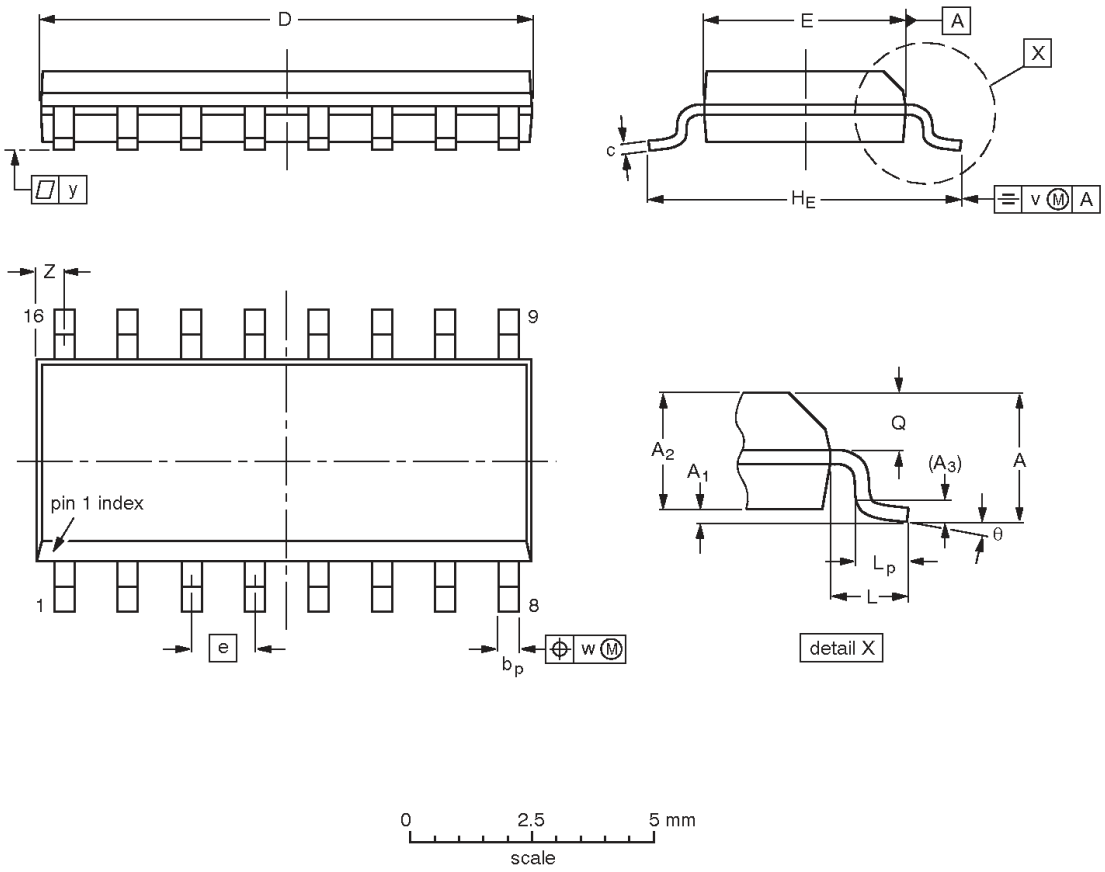
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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