To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

DATA SHEET

RENESAS

MOS FIELD EFFECT TRANSISTOR
μPA2792AGR

SWITCHING
N- AND P-CHANNEL POWER MOS FET

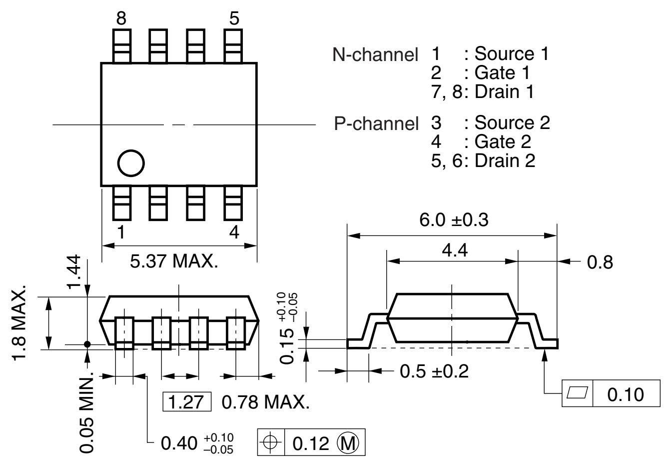
DESCRIPTION

The μPA2792AGR is N- and P-channel MOS Field Effect Transistors designed for Motor Drive application.

FEATURES

- Low on-state resistance
  - N-channel $R_{DS(on)1}$ = 12.5 mΩ MAX. (V_{GS} = 10 V, I_D = 5 A)
  - $R_{DS(on)2}$ = 21 mΩ MAX. (V_{GS} = 4.5 V, I_D = 5 A)
  - P-channel $R_{DS(on)1}$ = 18 mΩ MAX. (V_{GS} = –10 V, I_D = –5 A)
  - $R_{DS(on)2}$ = 26 mΩ MAX. (V_{GS} = –4.5 V, I_D = –5 A)
- Low input capacitance
  - N-channel C_{iss} = 2200 pF TYP.
  - P-channel C_{iss} = 2200 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



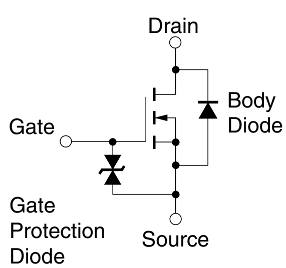
ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2792AGR-E1-AT Note	Pure Sn	Tape 2500 p/reel	Power SOP8
μPA2792AGR-E2-AT Note			

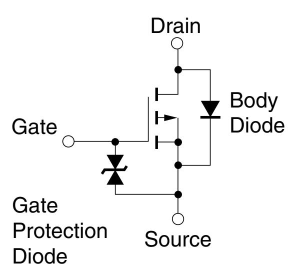
Note Pb-free (This product does not contain Pb in external electrode and other parts.)

EQUIVALENT CIRCUITS

N-channel



P-channel



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C. All terminals are connected.)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	∓20	V
Drain Current (DC)	$I_{D(DC)}$	±10	∓10	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±40	∓40	A
Total Power Dissipation (1 unit) Note2	P_{T1}	1.7		W
Total Power Dissipation (2 units) Note2	P_{T2}	2.0		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	–55 to +150		°C
Single Avalanche Current Note3	I_{AS}	10	–10	A
Single Avalanche Energy Note3	E_{AS}	10		mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 2000 mm^2 x 1.6 mm

3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 → 0 V

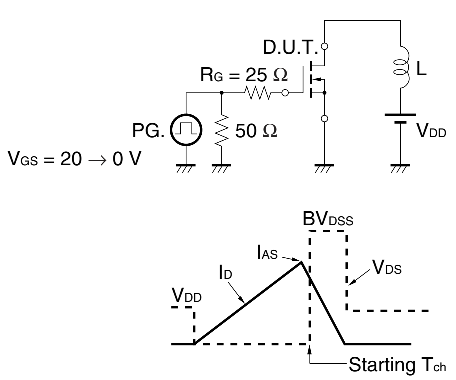
ELECTRICAL CHARACTERISTICS (T_A = 25°C. All terminals are connected.)

N-channel

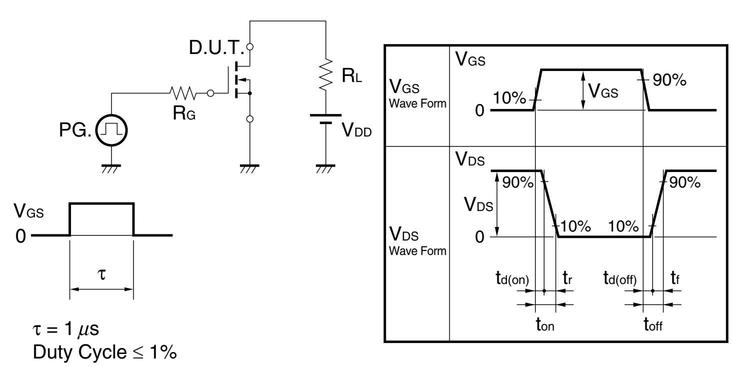
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 5 A	5	10		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 5 A		10	12.5	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 5 A		14.5	21	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,		2200		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		380		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		250		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 5 A,		9.6		ns
Rise Time	t_r	V_{GS} = 10 V,		21		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		52		ns
Fall Time	t_f			12		ns
Total Gate Charge	Q_G	I_D = 10 A,		42		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 24 V,		6.2		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		13		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 10 A, V_{GS} = 0 V		0.83	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 10 A, V_{GS} = 0 V,		30		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		22		nC

Note Pulsed

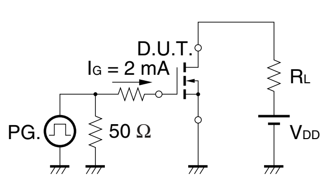
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

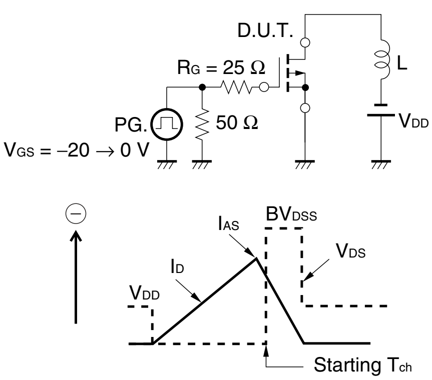


P-channel

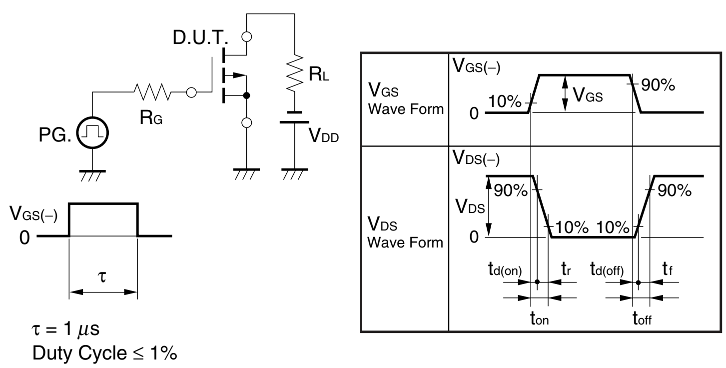
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.7	–2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = –10 V, I_D = –5 A	6	12.9		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –5 A		14	18	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –5 A		17.5	26	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V,		2200		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		510		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		410		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –5 A,		12		ns
Rise Time	t_r	V_{GS} = –10 V,		19		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		130		ns
Fall Time	t_f			36		ns
Total Gate Charge	Q_G	I_D = –10 A,		47		nC
Gate to Source Charge	Q_{GS}	V_{DD} = –24 V,		5.2		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		15		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 10 A, V_{GS} = 0 V		0.87	1.5	V
Reverse Recovery Time	t_{rr}	I_F = –10 A, V_{GS} = 0 V,		57		ns
Reverse Recovery Charge	Q_{rr}	di/dt = –50 A/μs		41		nC

Note Pulsed

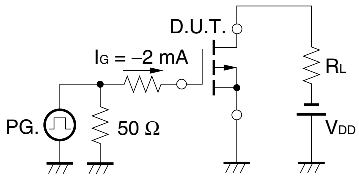
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



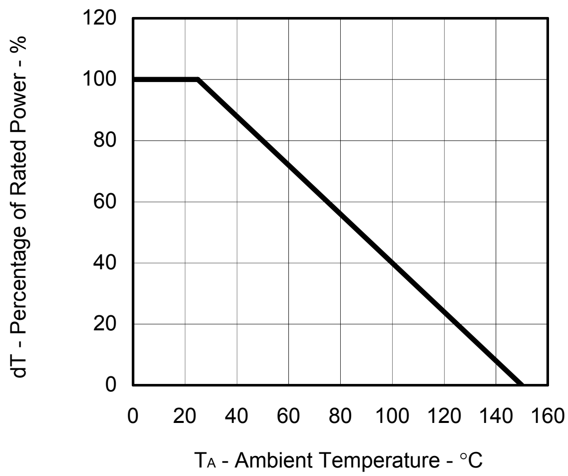
TEST CIRCUIT 3 GATE CHARGE



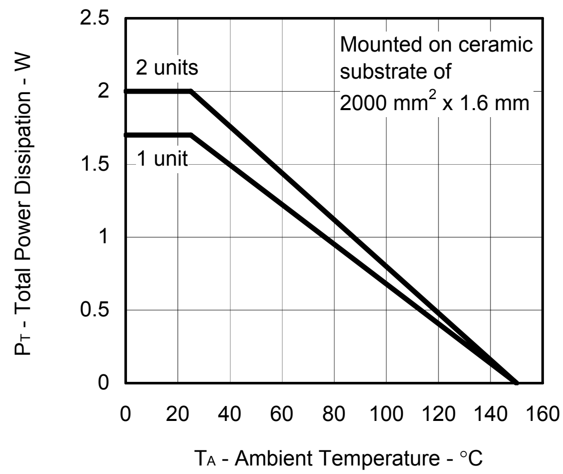
TYPICAL CHARACTERISTICS (T_A = 25°C)

(1) N-channel

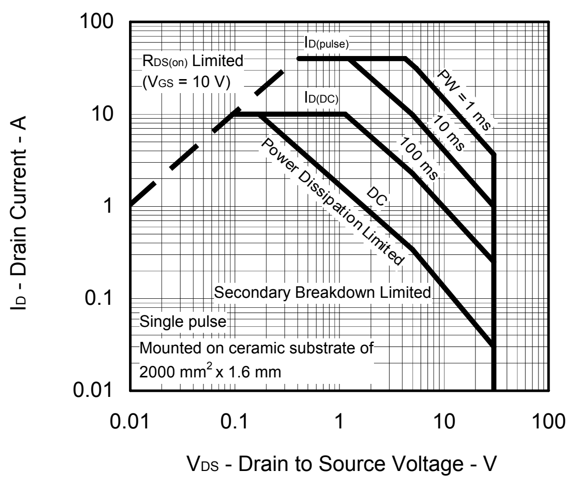
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



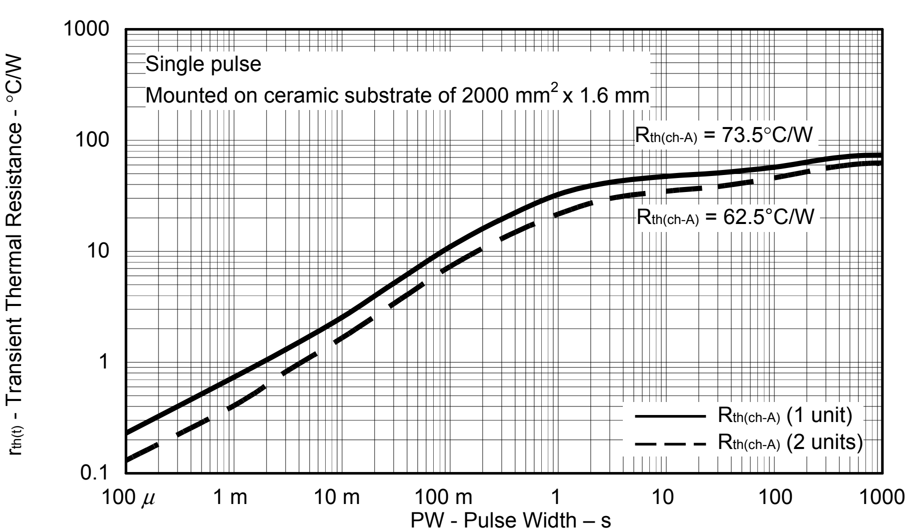
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



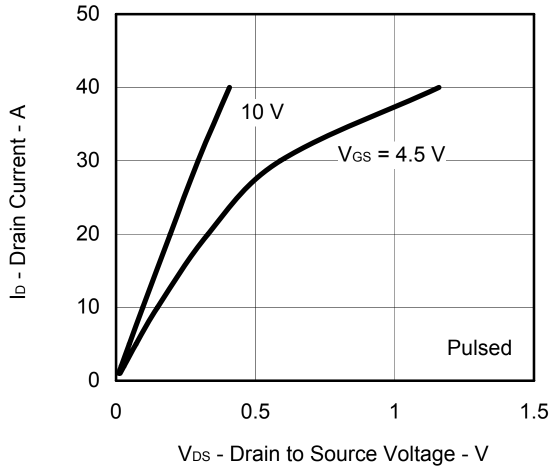
FORWARD BIAS SAFE OPERATING AREA



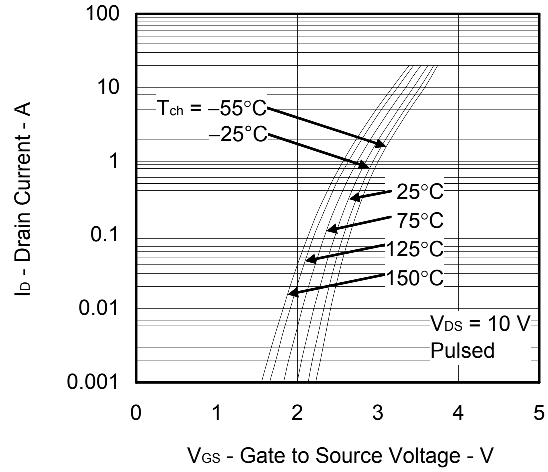
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



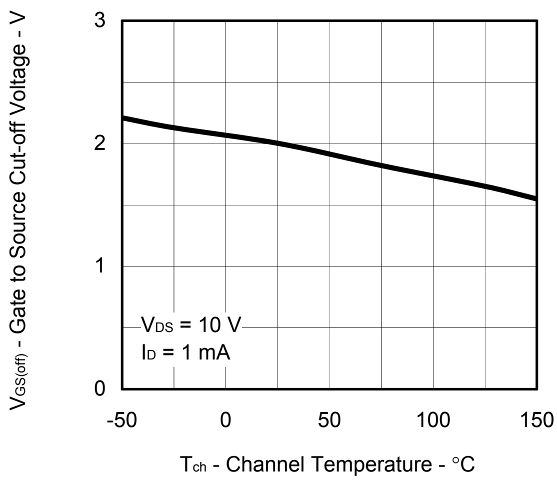
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



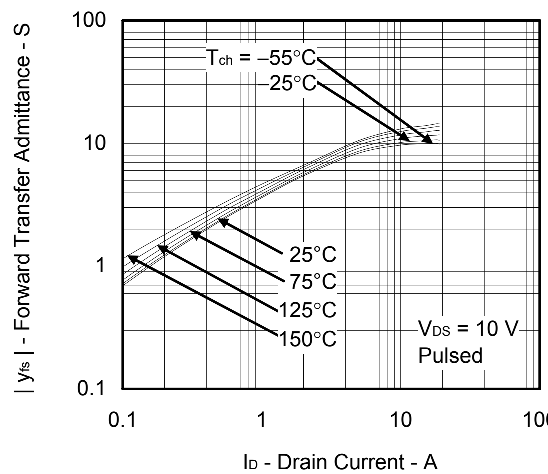
FORWARD TRANSFER CHARACTERISTICS



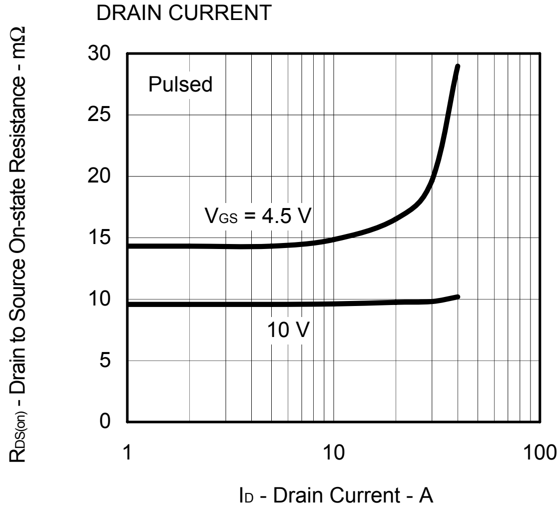
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



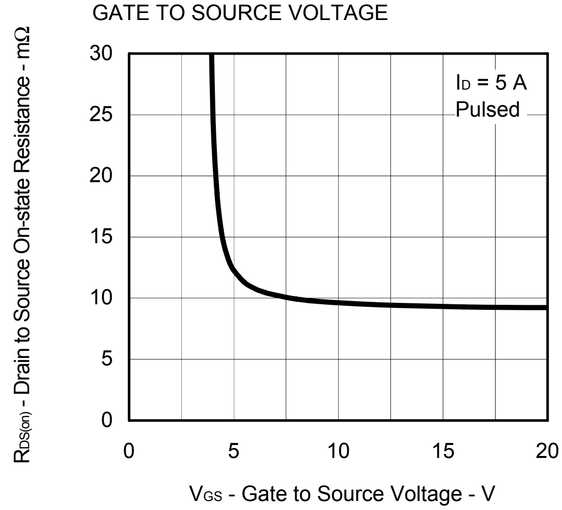
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



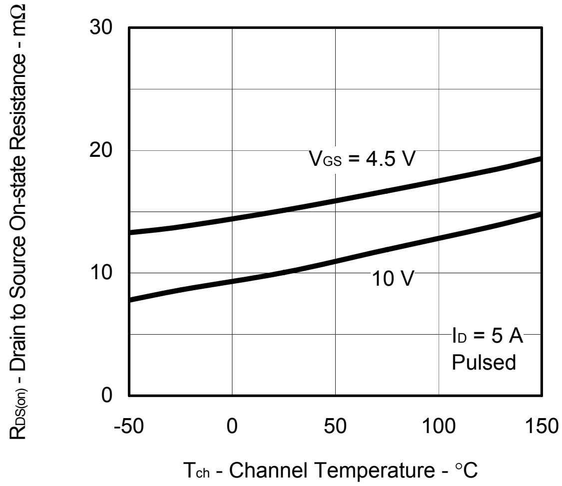
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



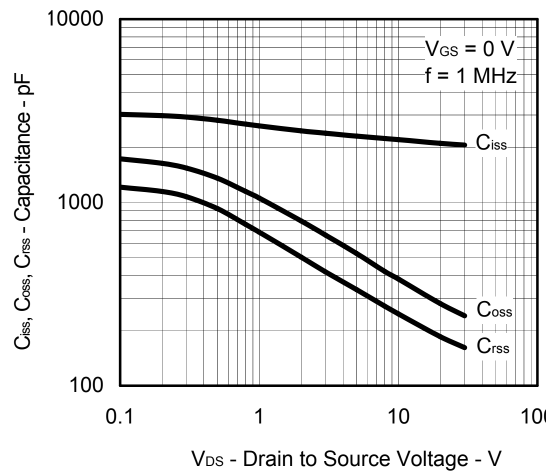
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



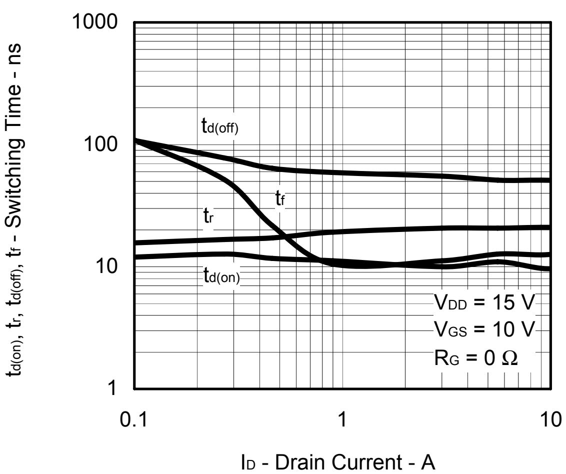
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



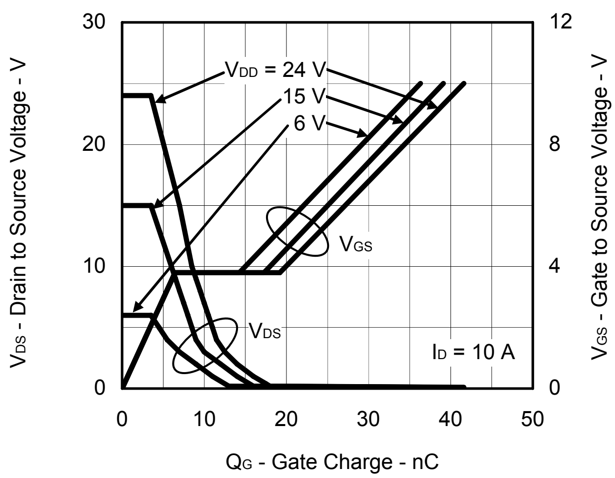
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



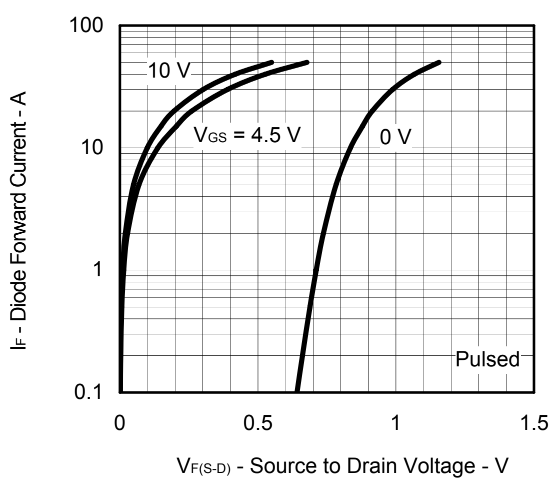
SWITCHING CHARACTERISTICS



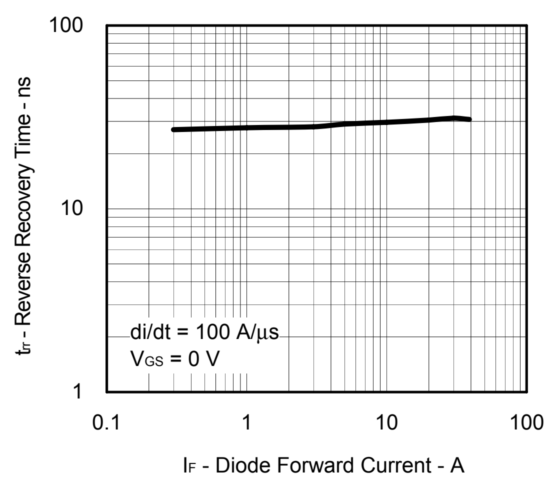
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



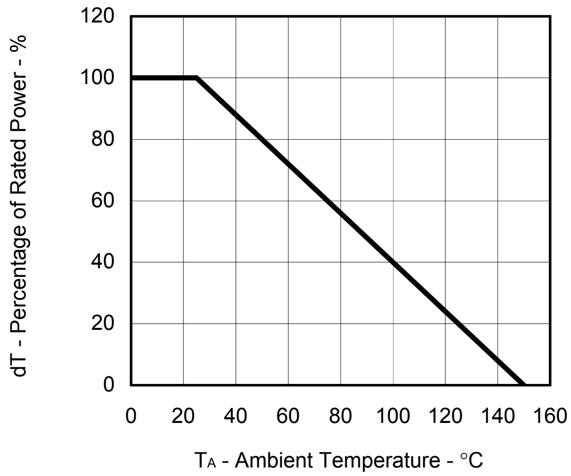
SOURCE TO DRAIN DIODE FORWARD VOLTAGE

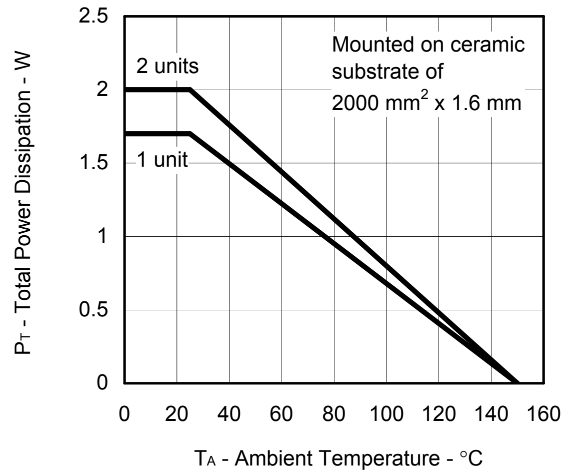


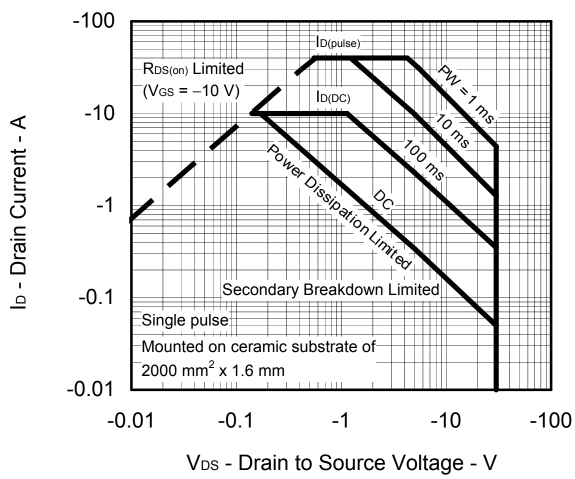
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

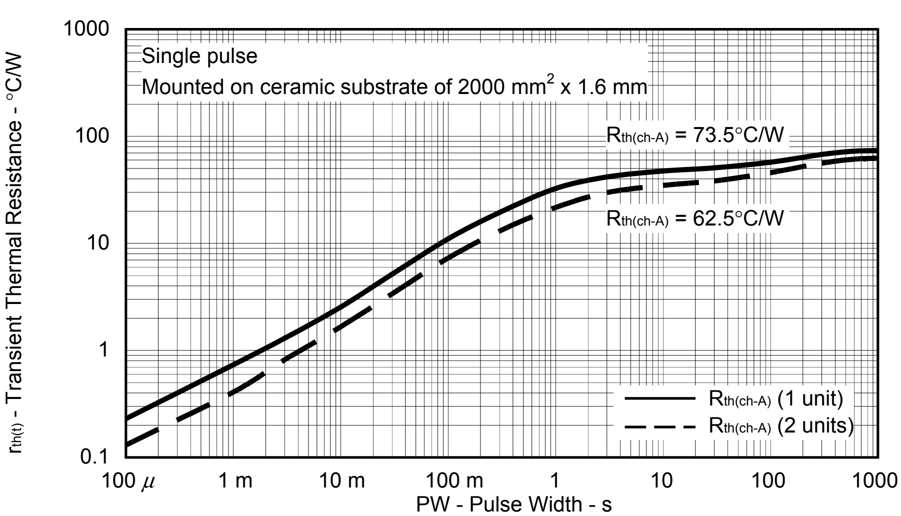


(2) P-channel

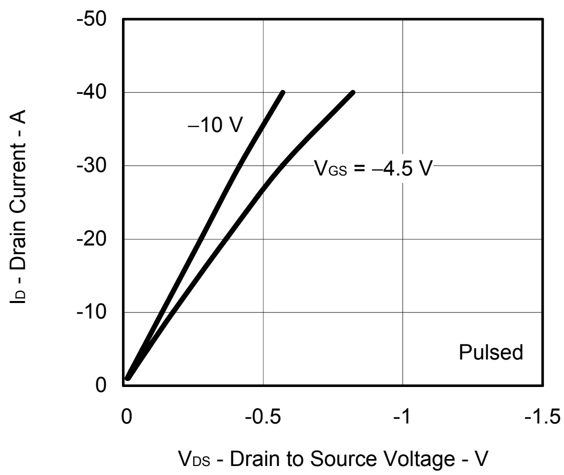

DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA
dT - Percentage of Rated Power - %
TA - Ambient Temperature - °C
0
20
40
60
80
100
120
140
160


TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE
PT - Total Power Dissipation - W
TA - Ambient Temperature - °C
2 units
1 unit
Mounted on ceramic
substrate of
2000 mm2 x 1.6 mm

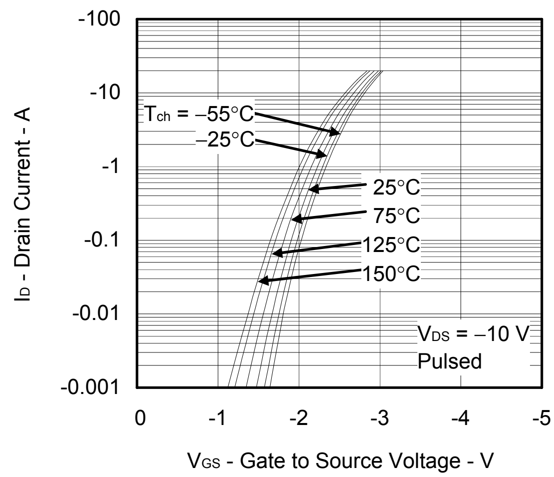

FORWARD BIAS SAFE OPERATING AREA
ID - Drain Current - A
VDS - Drain to Source Voltage - V
RDS(on) Limited
(VGS = –10 V)
ID(pulse)
ID(DC)
PW = 1 ms
10 ms
100 ms
DC
Power Dissipation Limited
Secondary Breakdown Limited
Single pulse
Mounted on ceramic substrate of
2000 mm2 x 1.6 mm


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
rth(t) - Transient Thermal Resistance - °C/W
PW - Pulse Width - s
Single pulse
Mounted on ceramic substrate of 2000 mm2 x 1.6 mm
Rth(ch-A) = 73.5°C/W
Rth(ch-A) = 62.5°C/W
Rth(ch-A) (1 unit)
Rth(ch-A) (2 units)

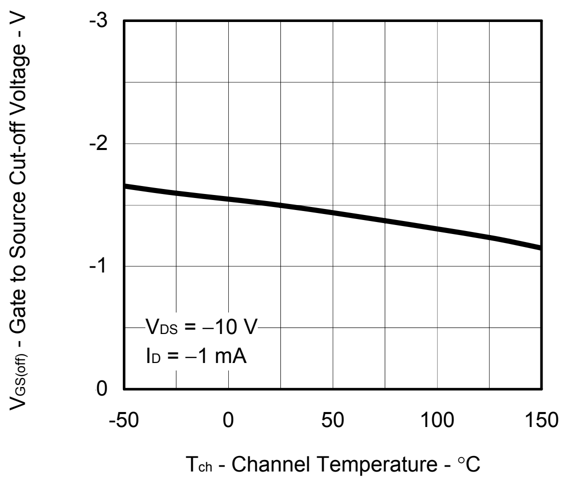
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



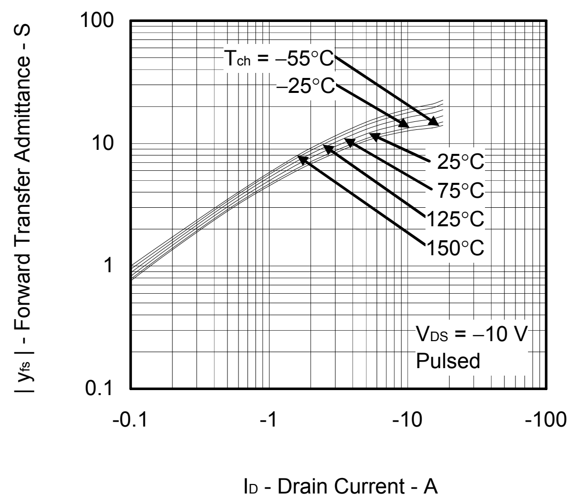
FORWARD TRANSFER CHARACTERISTICS



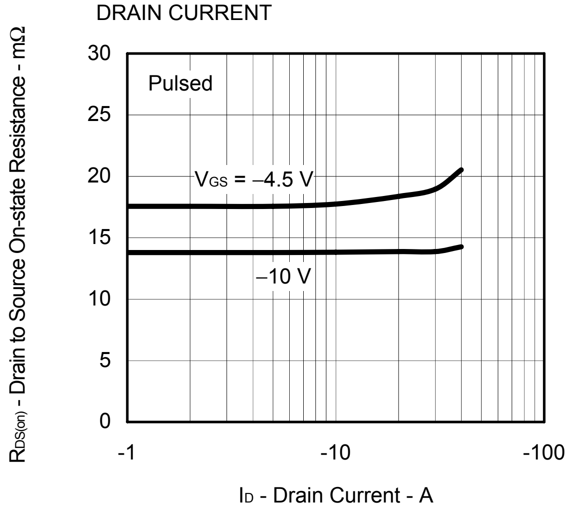
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



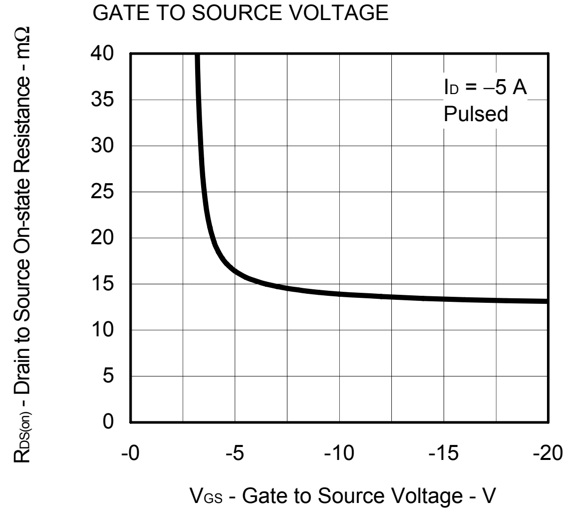
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



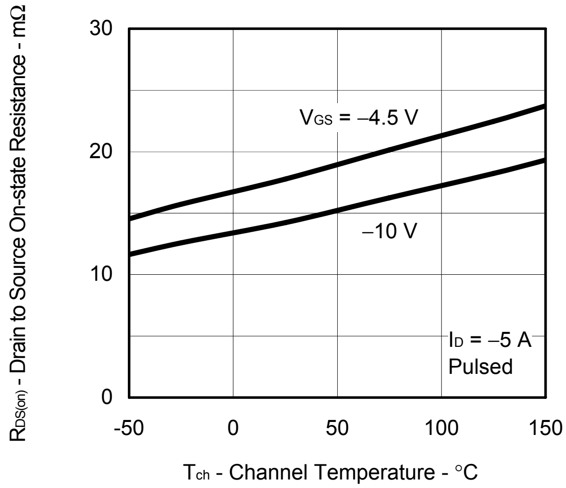
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



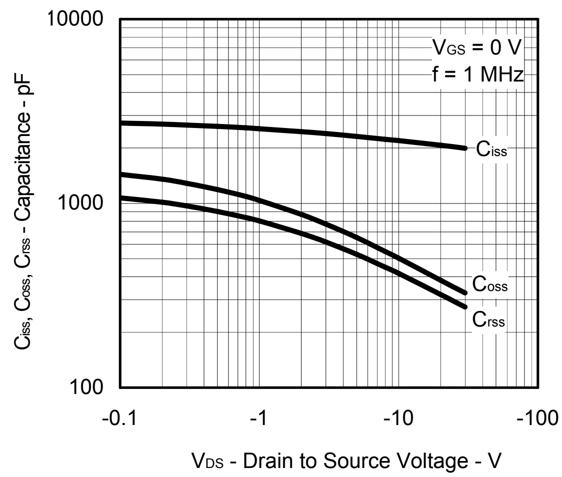
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



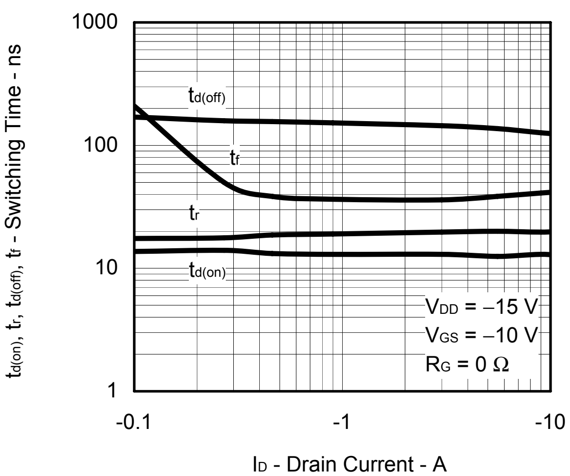
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



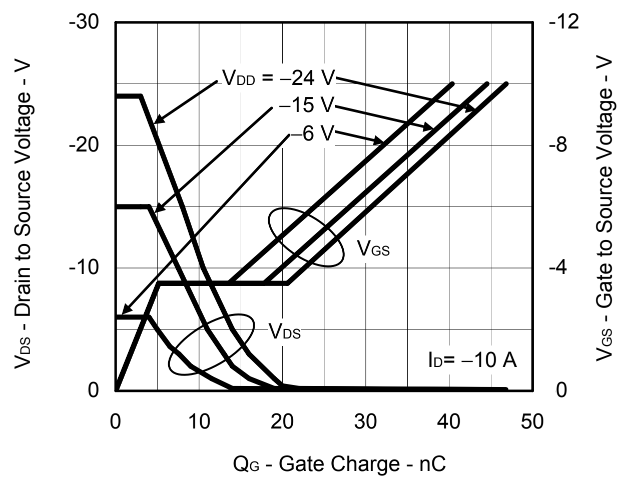
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



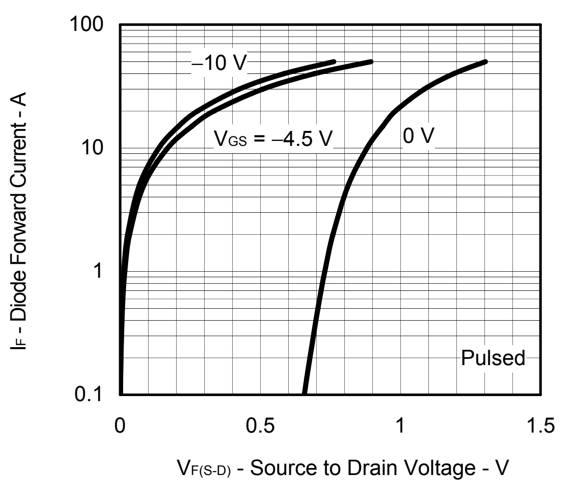
SWITCHING CHARACTERISTICS



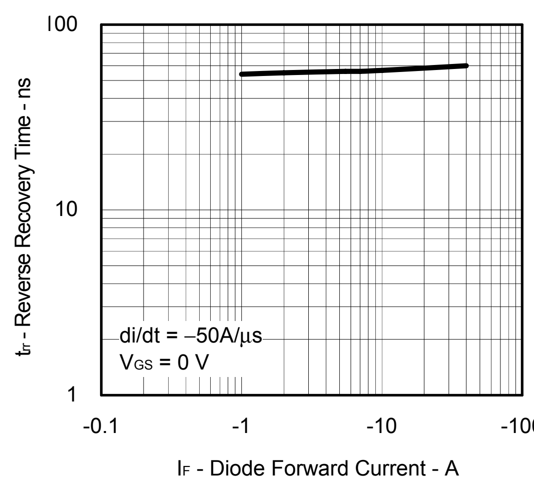
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

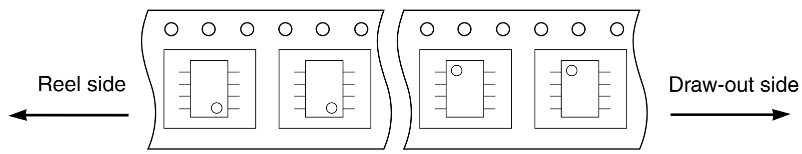


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

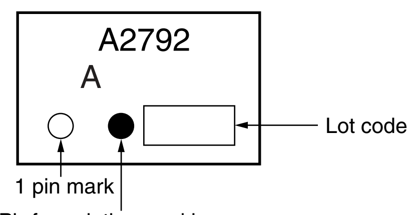


TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The μPA2792AGR should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).