3A, 36V, Synchronous Step-Down Converter

General Description

The RT2875A/B is a high efficiency, current-mode synchronous DC-DC step-down converter that can deliver up to 3A output current over a wide input voltage range from 4.5V to 36V. The device integrates 95mΩ high-side and 70mΩ low-side MOSFETs to achieve high conversion efficiency. The current-mode control architecture supports fast transient response and simple external compensation. A cycle-by-cycle current limit function provides protection against shorted output and an external soft-start eliminates input current surge during start-up. The RT2875A/B provides complete protection functions such as input under-voltage lockout, output under-voltage protection, over-current protection and thermal shutdown.

The RT2875A/B is available in the thermal enhanced TSSOP-14 (Exposed Pad) package.

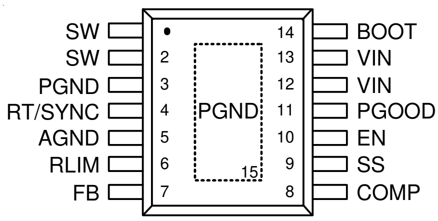
Features

- **3A Output Current**
- **Internal N-MOSFETs**
- **Current Mode Control**
- **Adjustable Switching Frequency : 300kHz to 2.1MHz**
- **Adjustable Current Limit : 1.5A to 6A**
- **Synchronous to External Clock : 300kHz to 2.1MHz**
- **Adjustable Output Voltage from 0.6V to 24V**
- **High Efficiency Up to 95%**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Current Limit**
- **Input Under-Voltage Lockout**
- **Output Under-Voltage Protection**
- **Thermal Shutdown**
- **AEC-Q100 Grade 2 Certification**
- **RoHS Compliant and Halogen Free**

Applications

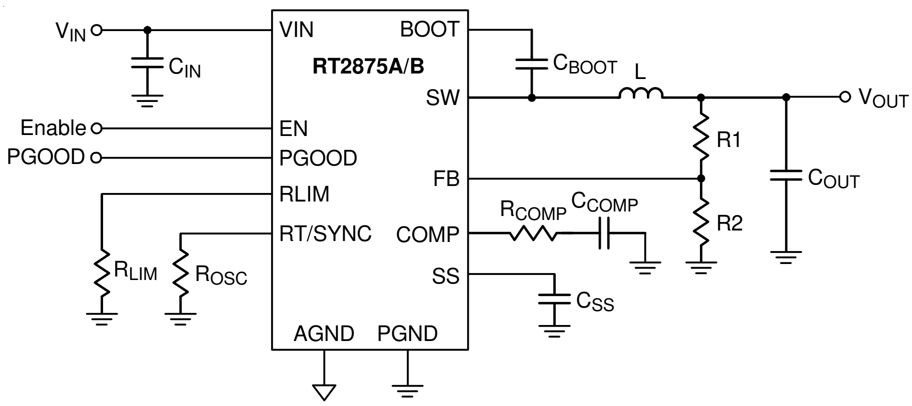
- Point of Load Regulator in Distributed Power Systems
- Digital Set Top Boxes
- Broadband Communications
- Vehicle Electronics

Pin Configuration



TSSOP-14 (Exposed Pad)

Simplified Application Circuit



Ordering Information

RT2875A/B□□□

- Label Part Number
  - (Z0W) : Sbucon = LGS & Exposed Pad-Option 2
  - (Y0W) : Sbucon = LGS & Exposed Pad-Option 2
  - (Y1W) : Subcon = GTK & Exposed Pad-Option 3
- Package Type
  - CP : TSSOP-14 (Exposed Pad)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- AQ : Latched UVP
- BQ : Hiccup Mode UVP

Marking Information

RT2875AQGCP

RT2875AQ
GCPYMDNN

RT2875AQGCP : Product Number

YMDNN : Date Code

RT2875BQGCP

RT2875BQ
GCPYMDNN

RT2875BQGCP : Product Number

YMDNN : Date Code

Note :

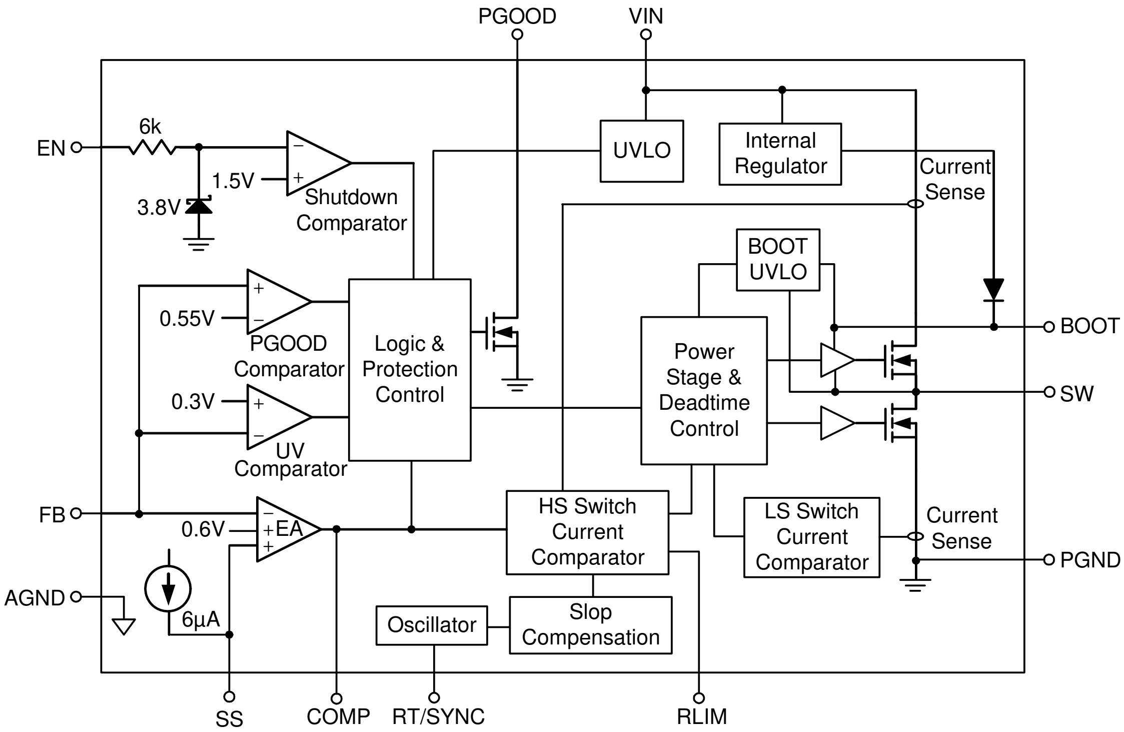
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	SW	Switch node. Connect to external L-C filter.
3, 15 (Exposed Pad)	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
4	RT/SYNC	Oscillator resistor and external frequency synchronization input. Must connect a resistor from this pin to GND to set the switching frequency. If SYNC clock is requested, connect an external clock to change the switching frequency.
5	AGND	Analog ground.
6	RLIM	Current limit setting. Connect a resistor from this pin to GND to set the current limit value.
7	FB	Feedback voltage input. The pin is used to set the output voltage of the converter to regulate to the desired via a resistive divider. Feedback reference = 0.6V.
8	COMP	Compensation node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
9	SS	Soft-start time setting. Connect a capacitor from SS to GND to set the soft-start period.
10	EN	Enable control input. High = Enable.
11	PGOOD	Power good indicator output.
12, 13	VIN	Power input. Support 4.5V to 36V input voltage. Must bypass with a suitable large ceramic capacitor at this pin.
14	BOOT	Bootstrap supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between the BOOT and SW pins.

Functional Block Diagram



Operation

The RT2875A/B is current-mode synchronous step-down converter. In normal operation, the high-side N-MOSFET is turned on when the S-R latch is set by the oscillator and is turned off when the current comparator resets the S-R latch. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal (V_{FB}) with the internal 0.6V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, and then the error amplifier's output voltage rises to allow higher inductor current to match the load current.

Switching Frequency

The switching frequency can be set by using extra resister RT or external clock. Switching frequency range is from 300kHz to 2.1MHz.

Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for high-side gate driver.

Enable

The converter is turned on when the EN pin is higher than 1.6V. When the EN pin is lower than 0.4V, the converter will enter shutdown mode and reduce the supply current lower than 10μA.

Soft-Start (SS)

In order to prevent the converter output voltage from overshooting during the startup period, the soft-start function is necessary. The soft-start time is adjustable by an external capacitor.

BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high-side MOSFET at any condition. The BOOT UVLO usually actives at extremely high conversion ratio or the higher V_{OUT} application operates at very light load. With such conditions, the low-side MOSFET may not have sufficient turn-on time to charge the BOOT capacitor. The device monitors BOOT pin capacitor voltage and force to turn on the low-side MOSFET when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_L}$ (typically, 2.4V). Meanwhile, the minimum off time is extended to 380ns (typically) hence prolong the BOOT capacitor charging time. The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.7V).

UV Comparator

If the feedback voltage is lower than 0.3V, the UV Comparator will go high to turn off the high-side MOSFET. The output under voltage protection is designed to operate in Hiccup mode. When the UV condition is removed, the converter will resume switching.

Current Setting

The current limit of high side MOSFET is adjustable by an external resistor connected to the RLIM pin. The current limit range is from 1.5A to 6A.

Thermal Shutdown

The over-temperature protection function will shut down the switching operation when the junction temperature exceeds 180°C. Once the junction temperature cools down by approximately 15°C, the converter will automatically resume switching.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- −0.3V to 40V
- Switch Voltage, SW ---------- −0.3V to (V_{IN} + 0.3V)
- BOOT to SW ---------- −0.3V to 6V
- Power Good Voltage, PGOOD ---------- −0.3V to 40V
- Other Pins ---------- −0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSSOP-14 (Exposed Pad) ---------- 4.464W
- Package Thermal Resistance (Note 2)
  TSSOP-14 (Exposed Pad), θ_{JA} ---------- 28°C/W
  TSSOP-14 (Exposed Pad), θ_{JC} ---------- 4.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- −65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 36V
- Junction Temperature Range ---------- −40°C to 150°C
- Ambient Temperature Range ---------- −40°C to 105°C

Electrical Characteristics

(V_{IN} = 12V, T_A = −40°C to 105°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current			V_{EN} = 0V	--	--	10	μA
Switching quiescent current with no load at DCDC output			V_{EN} = 2V, V_{FB} = 0.64V, R_{LIM} = 91k, R_{OSC} = 169k	--	--	1.3	mA
Feedback Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 36V	0.588	0.6	0.612	V
Error Amplifier Trans-conductance		G_{EA}	ΔIC = ±10μA	--	950	--	μA/V
Switch On-Resistance	High-Side	$R_{DS(ON)1}$		--	95	--	mΩ
	Low-Side	$R_{DS(ON)2}$		--	70	--	
High-Side Switch Leakage Current			V_{EN} = 0V, V_{SW} = 0V	--	1	--	μA
Current Limit Setting Rage			(Note 5)	1.5	--	6	A
High-Side Switch Current Limit 1		H_{OC1}	R_{LIM} = 100kΩ	1.79	2.1	2.41	A
High-Side Switch Current Limit 2		H_{OC2}	R_{LIM} = 47kΩ	3.52	4	4.48	A
High-Side Switch Current Limit 3		H_{OC3}	R_{LIM} = 33kΩ	4.84	5.5	6.16	A
Low-Side Switch Current Limit			From drain to source	--	2	--	A
COMP to Current Sense Transconductance		G_{CS}		--	5.2	--	A/V
Switching Frequency Range			Include Sync mode and RT mode set point	300	--	2100	kHz

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency1		f_{OSC1}	R_t = 169kΩ	275	305	335	kHz
Switching Frequency2		f_{OSC2}	R_t = 51kΩ	0.83	0.98	1.13	MHz
Switching Frequency3		f_{OSC3}	R_t = 23kΩ	1.89	2.1	2.31	MHz
Short Circuit Oscillation Frequency			V_{FB} = 0V, R_{OSC} = 100kΩ, V_{IN} = 12V	--	31.25	--	kHz
Minimum SYNC Pulse width				--	20	--	ns
SYNC Input Voltage	High-Level			--	--	2	V
	Low- Level			0.8	--	--	
Minimum On-Time		t_{ON}		--	100	--	ns
EN Input Voltage	Logic-High	V_{IH}		1.4	1.5	1.6	V
	Hysteresis		EN hysteresis voltage	--	0.2	--	
Input Under-Voltage Lockout Threshold		V_{UVLO}	VIN rising	--	4.1	--	V
		ΔV_{UVLO}	Hysteresis	--	300	--	mV
Power Good Threshold			Rising	--	90	--	%
			Falling	--	85	--	
Power Good Output High Leakage Current			V_{FB} = V_{REF}, V_{PGOOD} = 5.5V	--	30	--	nA
Power Good Output Low			I_{PGOOD} = 0.4mA	--	--	0.3	V
Soft-Start Charge Current		I_{SS}		--	6	--	μA
SW Discharge Resistance				--	80	--	Ω
Thermal Shutdown		T_{SD}		160	180	200	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	15	--	°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

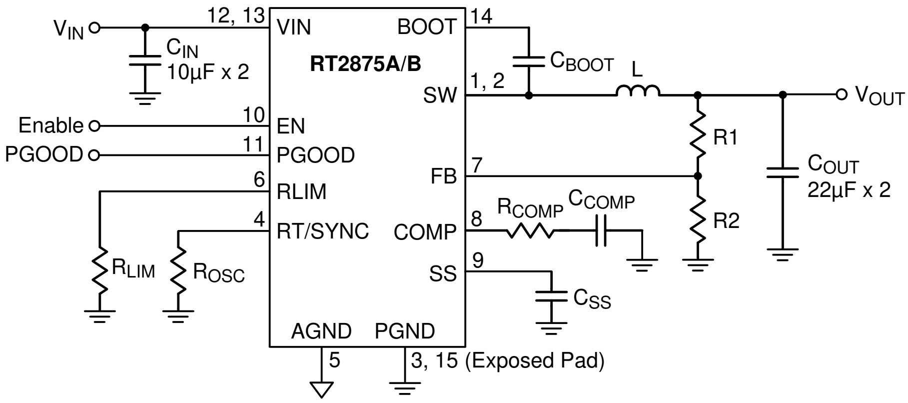
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Typical Application Circuit

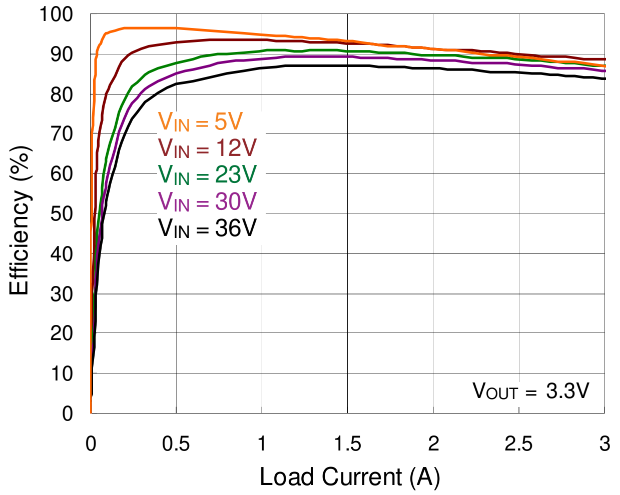


For 500kHz Only

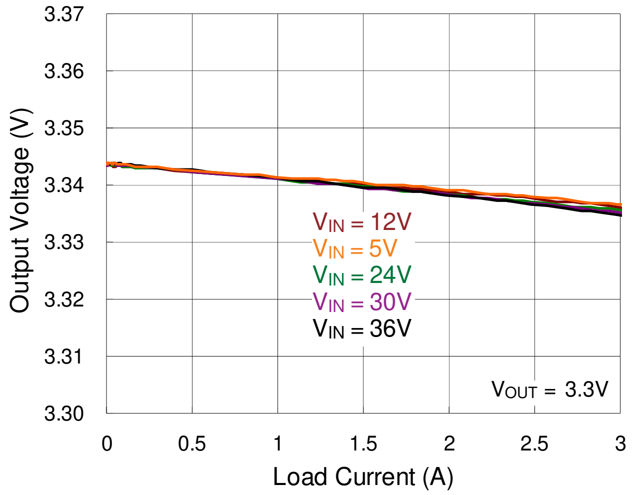
V_{OUT}	R1 (kΩ)	R2 (kΩ)	R_{OSC} (kΩ)	R_{COMP} (kΩ)	C_{COMP} (nF)	L (μH)
12	102	5.36	100	32	3.9	10
8	102	8.25	100	20	3.3	8.2
5	110	15	100	15	3.3	6.8
3.3	115	25.5	100	10	3.3	4.7
2.5	25.5	8.06	100	7.5	3.3	3.6
1.2	10	10	100	4.3	3.9	2.2

Typical Operating Characteristics

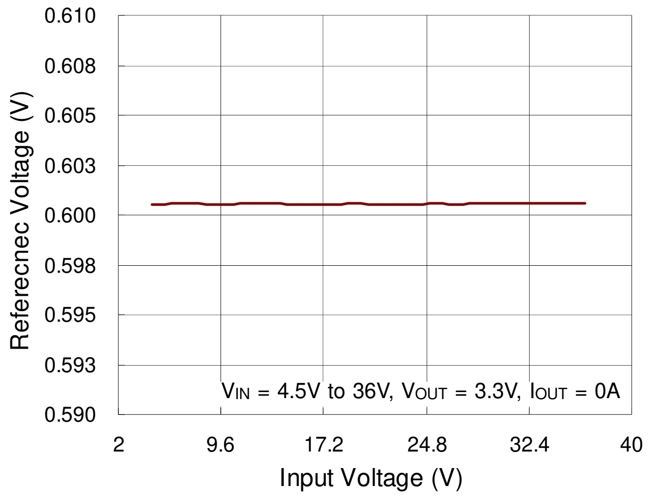
Efficiency vs. Load Current



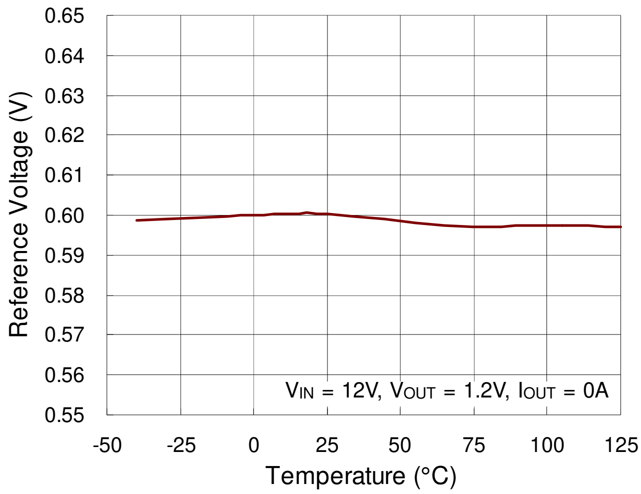
Output Voltage vs. Load Current



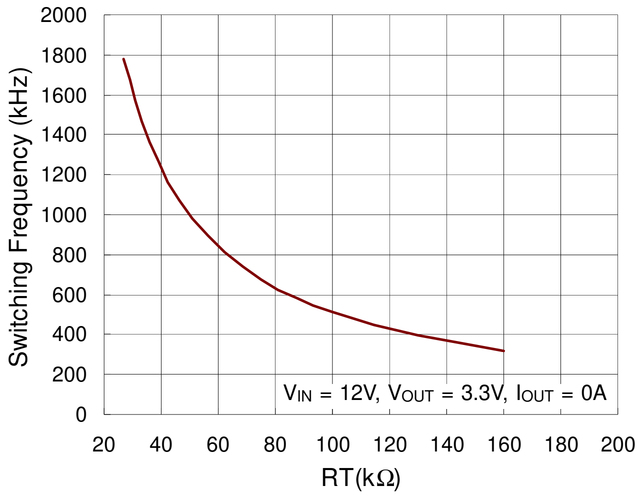
Referecnec Voltage vs. Input Voltage



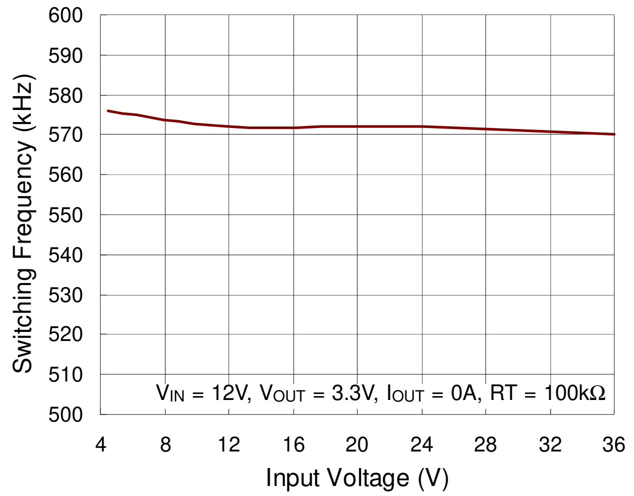
Reference Voltage vs. Temperature

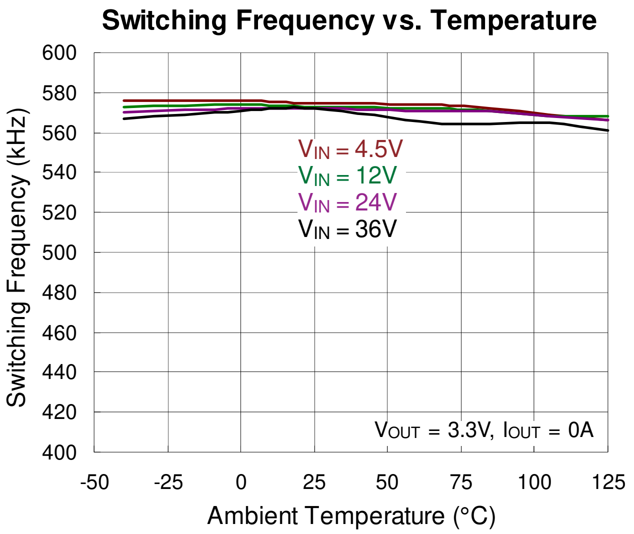


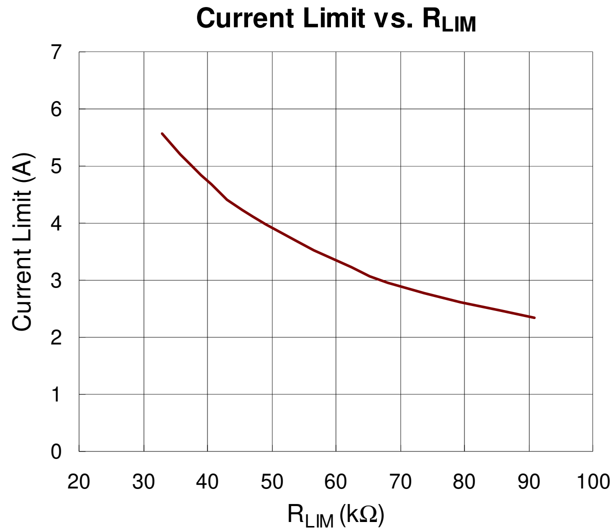
Switching Frequency vs. RT

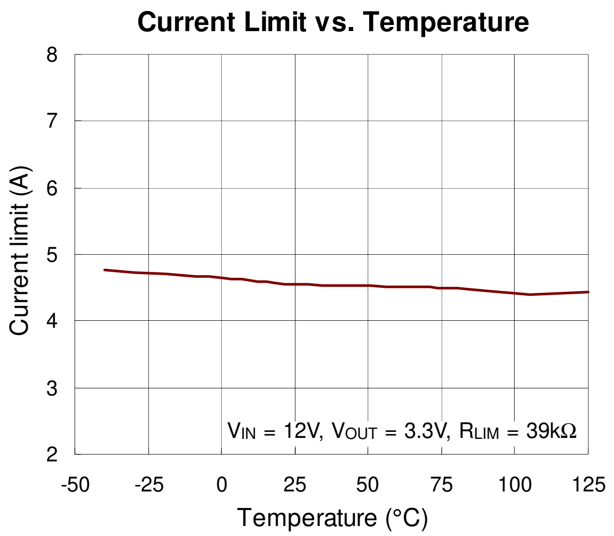


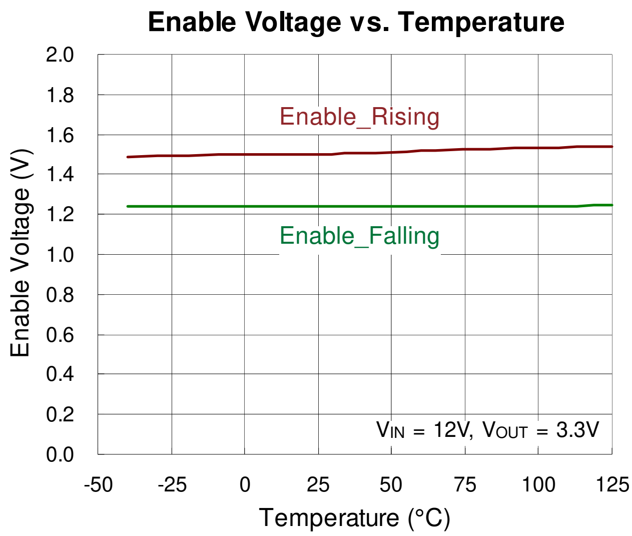
Switching Frequency vs. Input Voltage

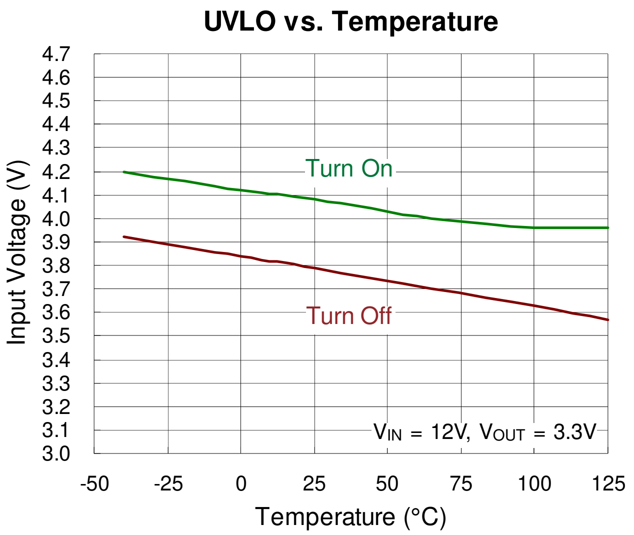


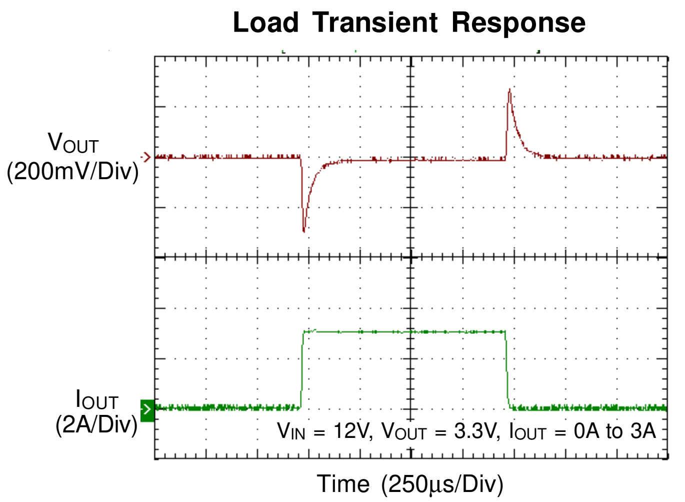

Switching Frequency vs. Temperature
Switching Frequency (kHz)
Ambient Temperature (°C)
VIN = 4.5V
VIN = 12V
VIN = 24V
VIN = 36V
VOUT = 3.3V, IOUT = 0A


Current Limit vs. RLIM
Current Limit (A)
RLIM (kΩ)

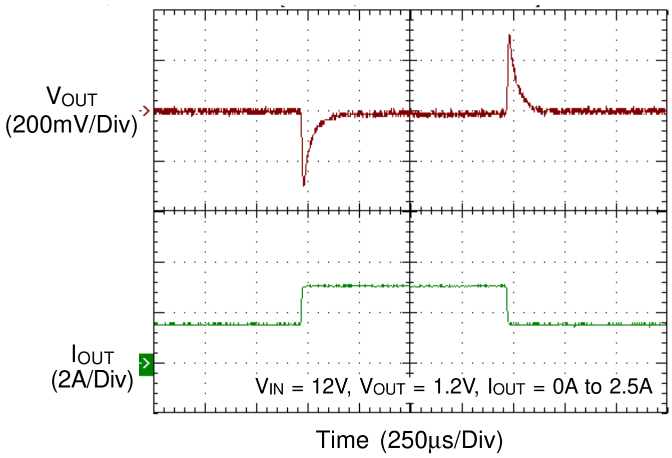

Current Limit vs. Temperature
Current limit (A)
Temperature (°C)
VIN = 12V, VOUT = 3.3V, RLIM = 39kΩ


Enable Voltage vs. Temperature
Enable Voltage (V)
Temperature (°C)
Enable_Rising
Enable_Falling
VIN = 12V, VOUT = 3.3V

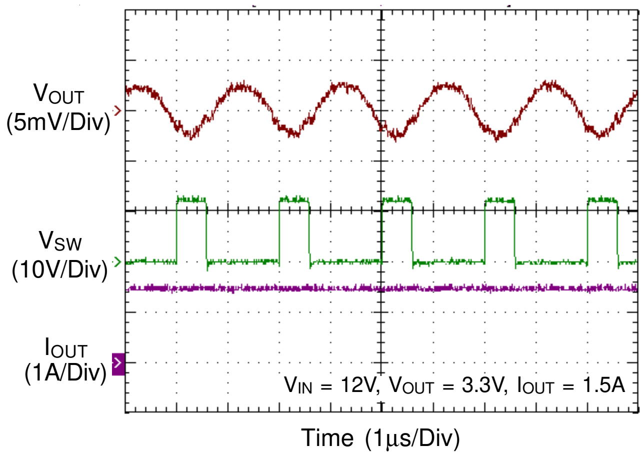

UVLO vs. Temperature
Input Voltage (V)
Temperature (°C)
Turn On
Turn Off
VIN = 12V, VOUT = 3.3V


Load Transient Response
VOUT (200mV/Div)
IOUT (2A/Div)
VIN = 12V, VOUT = 3.3V, IOUT = 0A to 3A
Time (250μs/Div)

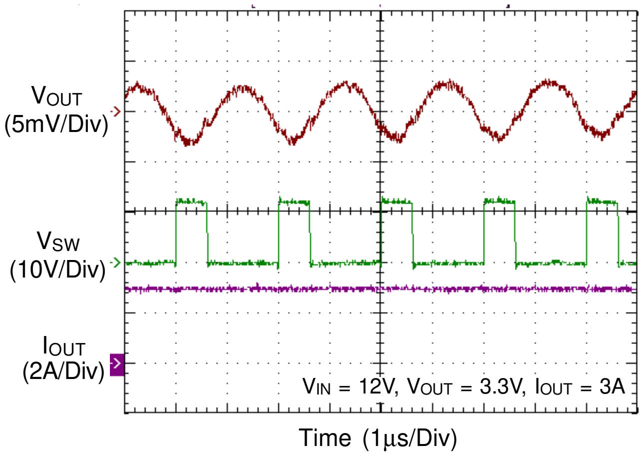
Load Transient Response



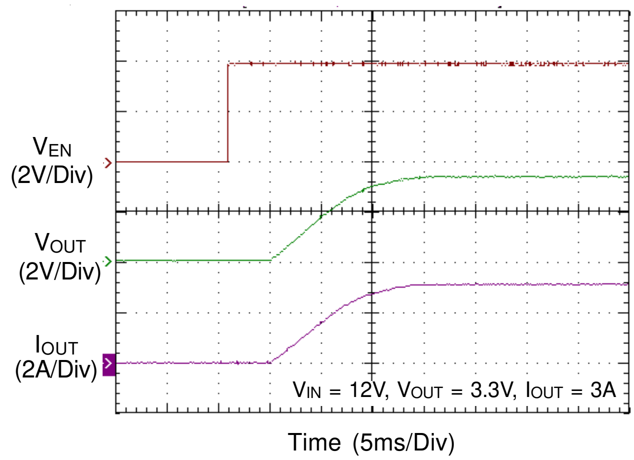
Switching



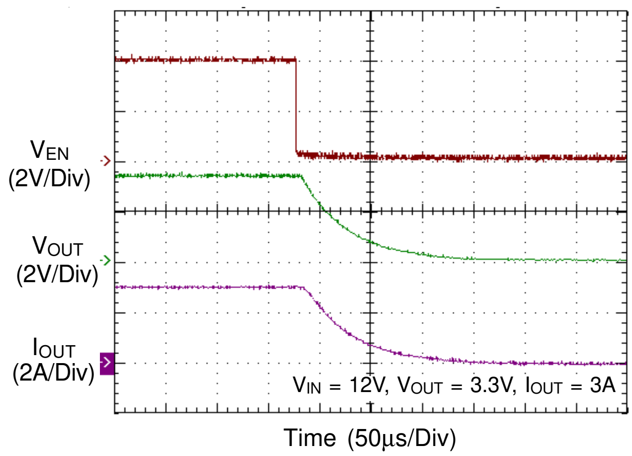
Switching



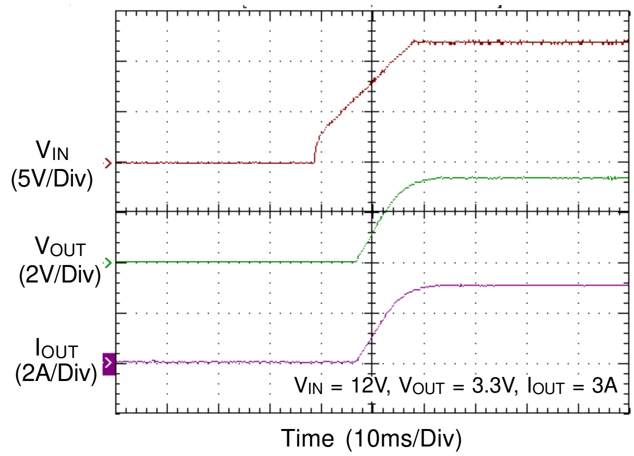
Power On from EN



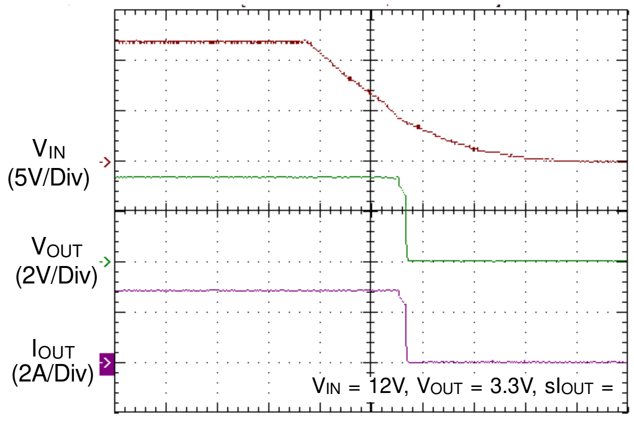
Power Off from EN



Power On from VIN



Power Off from VIN



Application Information

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

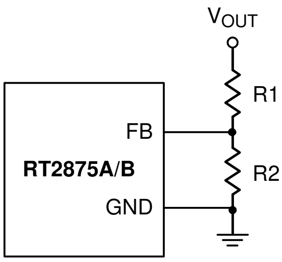


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the reference voltage (0.6V typ.).

Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between BOOT pin and SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage which is built in an internal regulator each time the low-side MOSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications a 0.1µF, 0603 ceramic capacitor with X7R is recommended and the capacitor should have a 6.3 V or higher voltage rating.

External Bootstrap Diode

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side MOSFET and improve efficiency when the input voltage is below 5.5V, switching frequency is higher than 1MHz or duty ratio is higher than 65%. Keeps $V_{BOOT-SW}$ always higher than 3V to prevent BOOT UVLO function executed. The recommended application circuit is shown in Figure 2. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54.

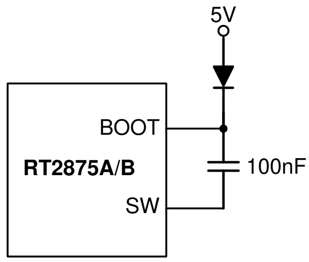


Figure 2. External Bootstrap Diode

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT2875A/B quiescent current drops to lower than 10µA. Driving the EN pin high (>1.6V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 3).

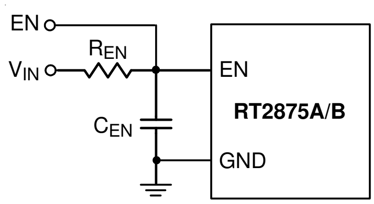


Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 4. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

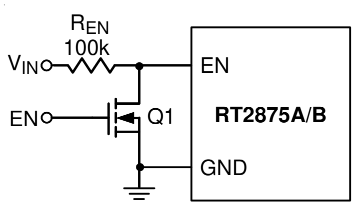


Figure 4. Digital Enable Control Circuit

Under-Voltage Protection

Hiccup Mode

The RT2875B provides Hiccup Mode Under-Voltage Protection (UVP). When the V_{FB} voltage drops below 0.3V, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT2875B will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

Latch Mode

For the RT2875A it provides Latch-Off Mode Under Voltage Protection (UVP). When the V_{FB} voltage drops below 0.3V, UVP will be triggered and the RT2875A will shut down in Latch-Off Mode. In shutdown condition, the RT2875A can be reset by EN pin or power input VIN.

Hiccup Mode

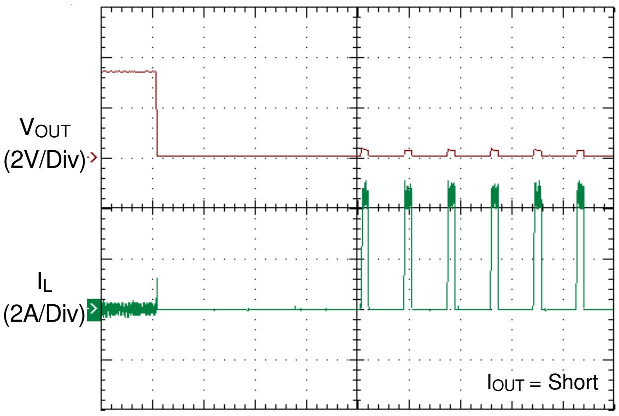


Figure 5. Hiccup Mode Under Voltage Protection

Over-Temperature Protection

The RT2875A/B features an Over-Temperature Protection (OTP) circuitry to prevent from overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 180°C. Once the junction temperature cools down by approximately 15°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 150°C.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

C_{IN} and C_{OUT} Selection

The input capacitance, $C_{IN,}$ is needed to filter the trapezoidal current at the Source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 10μF low ESR ceramic capacitors are suggested. For the suggested capacitor, please refer to Table 3 for more details.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Switching Frequency Setting

The switching frequency can be set by using extra resister RT or external clock. Switching frequency range is from 300kHz to 2.1MHz. Through extra resister RT connect to RT/SYNC pin to setting the switching frequency F_S, below offer approximate formula equation :

Setting Frequency = F_S (kHz)

$x = [F_S - 31.379] / 47691$

R_{OSC} (kΩ) = (1 / x)

The RT2875A/B can be synchronized with an external clock ranging from 300kHz to 2.1MHz applied to the RT/SYNC pin. The external clock duty cycle must be from 10% to 90%. The RT/SYNC pin is at logic-high level (>2V). If the EN pin is pulled to low-level for 10μs above, the IC will shut down.

Current Setting

The current limit of high side MOSFET is adjustable by an external resistor connected to the RLIM pin. The current limit range is from 1.5A to 6A. When the inductor current reaches the current limit threshold, the COMP voltage will be clamped to limit the inductor current. Inductor current ripple current also should be considered into current limit setting. Current limit minimum value should be set as below :

Current limit minimum = (I_O(max) + 1 / 2 inductor current ripple) x 1.2

Through extra resister RLIM connect to RLIM pin to setting the current limit value below offer approximate formula equation :

I_{SET} = current limit value (A)

$y = (I_{SET} - 0.4206) / 167.79$

R_{LIM} (kΩ) = (1 / y)

Soft-Start

The RT2875A/B provides soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. The soft-start timing can be programmed by the external capacitor C_{SS} between SS and GND. An internal current source I_{SS} (6μA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during softstart interval. The typical soft start time is calculated as follows :

Soft-Start time $t_{SS} = C_{SS}$ x 0.6 / 6μA

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 150°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSSOP-14 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (150°C − 25°C) / (28°C/W) = 4.464W for TSSOP-14 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

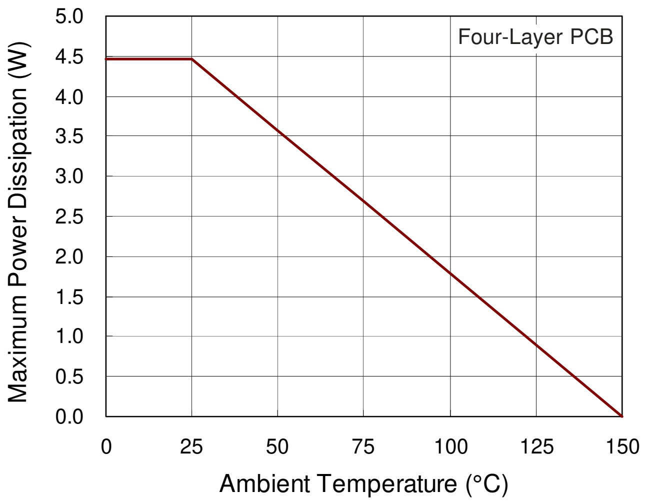
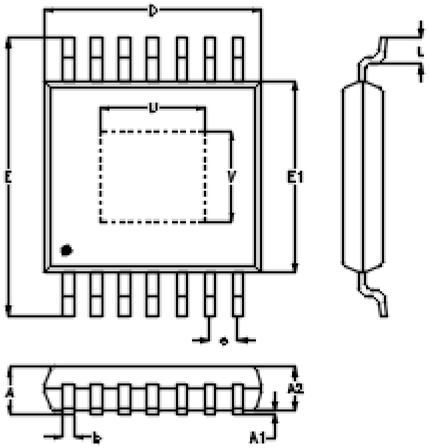


Figure 6. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		1.000	1.200	0.039	0.047
A1		0.000	0.150	0.000	0.006
A2		0.800	1.050	0.031	0.041
b		0.190	0.300	0.007	0.012
D		4.900	5.100	0.193	0.201
e		0.650		0.026	
E		6.300	6.500	0.248	0.256
E1		4.300	4.500	0.169	0.177
L		0.450	0.750	0.018	0.030
U	Option1	1.900	2.900	0.075	0.114
	Option2	2.350	2.850	0.093	0.112
	Option3	2.640	3.100	0.104	0.122
V	Option1	1.600	2.600	0.063	0.102
	Option2	2.250	2.750	0.089	0.108
	Option3	2.550	3.000	0.100	0.118

14-Lead TSSOP (Exposed Pad) Plastic Package

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