NEW PRODUCT

Description

The PAM8124 is a 15W efficient, Class-D audio power amplifier for driving stereo speakers in a single-ended configuration; or a mono speaker in a bridge-tied-load configuration. The PAM8124 can drive stereo speakers (SE) as low as 4Ω. Due to the low power dissipation and high efficiency, up to 95%, the device can be used without any external heat sink when playing music.

The gain of the amplifier is controlled by 2 gain selectable pins, offering 20dB, 26dB, 32dB, and 36dB gain selections.

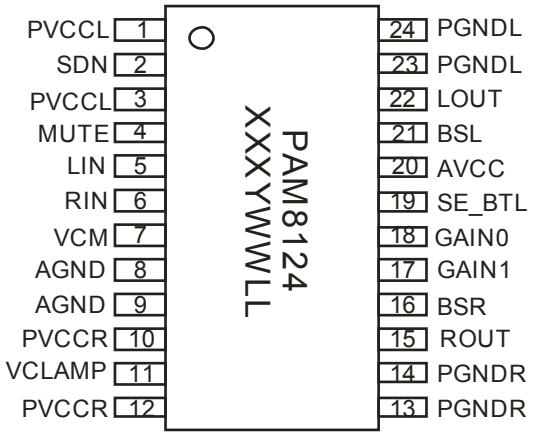
The PAM8124 is available in a TSSOP-24-EP package.

Features

- 30W/Ch into 8Ω BTL Load from 22V Supply
- 15W/Ch into 4Ω SE Load from 22V Supply
- 10W/Ch into 8Ω SE Load from 24V Supply
- Operate from 10V to 26V
- Single-Ended Analog Inputs
- Supports Multiple Output Configurations:
  - 2-Ch Single-Ended (SE, Half-Bridge)
  - 1-Ch Bridge-Tied Load (BTL, Full-Bridge)
- Four Selectable Fixed-gain Settings
- No Pop Noise for Start-up and Shut-down Sequences
- Internal Oscillator (No External Components Required)
- High Efficient Class-D Operation Eliminates Need for Heat Sinks
- Thermal and Short-Circuit Protection with Auto Recovery
- Space-Saving Surface-Mount TSSOP-24EP Package
- Pb-Free Package

Pin Assignments

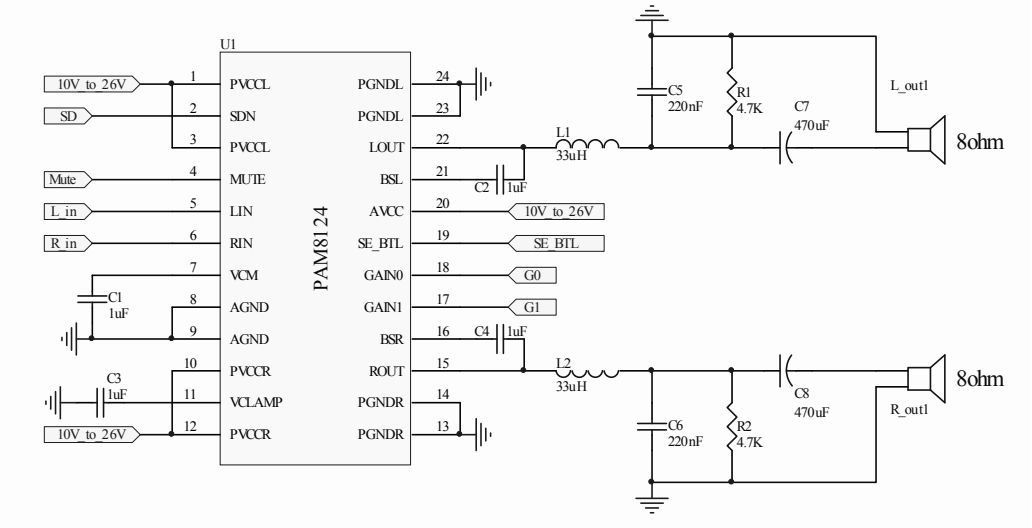
TSSOP-24-EP



Applications

- Televisions
- Home Sound Systems
- Active Speakers

Typical Applications Circuit



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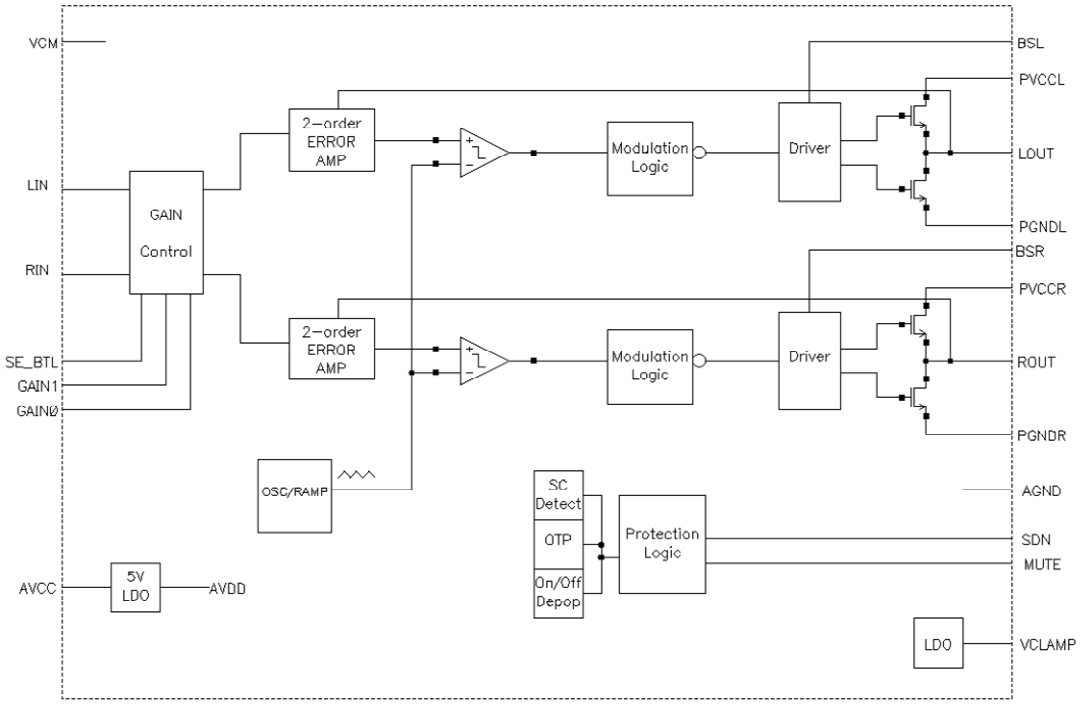
Pin Descriptions

Pin	Name	I/O/P	Function
1, 3	PVCCL	P	Power supply for left channel H-bridge, not connected to PVCCR or AVCC
2	SDN	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to AVCC
4	MUTE	I	A logic high on this pin disables the outputs. A low on this pin enables the outputs. TTL logic levels with compliance to AVCC
5	LIN	I	Audio input for left channel
6	RIN	I	Audio input for right channel
7	VCM	O	Reference for analog cells
8, 9	AGND	P	Analog ground for digital/analog cells in core
10, 12	PVCCR	P	Power supply for right channel H-bridge, not connected to PVCCL or AVCC
11	VCLAMP	P	Internally generated voltage supply for bootstrap. Not to be used as a supply or connected to any component other than the decoupling capacitor.
13, 14	PGNDR	P	Power ground for right channel H-bridge
15	ROUT	O	Class-D H-bridge output for right channel
16	BSR	I/O	Bootstrap I /O for right channel H-bridge
17	GAIN1	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
18	GAIN0	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
19	SE_BTL	I	A logic low on this pin enables one single-ended input in BTL configuration. A logic high on this pin enables two inputs in SE/BTL configuration. TTL logic levels with compliance to AVCC
20	AVCC	P	High-voltage analog power supply
21	BSL	I/O	Bootstrap I /O for left channel H-bridge
22	LOUT	O	Class-D H-bridge output for left channel
23, 24	PGNDL	P	Power ground for left channel H-bridge

Functional Block Diagram



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Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage (VCC)	28	V
Logic Input Voltage (SDN, MUTE, GAIN0, GAIN1, SE_BTL)	-0.3 to V_{CC} +0.3	V
Analog Input Voltage (LIN, RIN)	-0.3 to +5.5	V
Storage Temperature	-65 to +150	°C
Maximum Junction Temperature	150	°C
Junction to ambient thermal resistance	40	°C/W

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	10	26	V
T_A	Operating Ambient Temperature Range	-40	+85	°C
T_J	Junction Temperature Range	-40	+125	°C

Electrical Characteristics (@T_A = +25°C, V_{CC} = 24V, Gain = 20dB, R_L = 8Ω unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
|VOS|	Class-D output offset voltage(measured differently)	V_i = 0V, A_V = 36dB		20	100	mV
$I_{CC(q)}$	Quiescent supply current	SDN = 2.5V, MUTE = 0V, No Load		25	40	mA
$I_{CC(MUTE)}$	Quiescent supply current in mute mode	MUTE = 2.5V, No load		25	40	mA
$I_{CC(SDN)}$	Quiescent current in shutdown mode	SDN = 0.8V, No load		30	60	μA
$R_{DS(ON)}$	Drain-source on-state resistance	I_O = 0.5A		150		mΩ
G	Gain	GAIN1 = 0.8V, GAIN0 = 0.8V	18	20	22	dB
		GAIN1 = 0.8V, GAIN0 = 2.5V	24	26	28	
		GAIN1 = 2.5V, GAIN0 = 0.8V	30	32	34	
		GAIN1 = 2.5V, GAIN0 = 2.5V	34	36	38	
	Mute Attenuation	Vi = 1Vrms		-60		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVpp, f = 1kHz,gain = 20dB		-52		dB
P_O	Output Power at 1% THD+N	R_L = 4Ω, f = 1kHz		14		W
		R_L = 8Ω, f = 1kHz		8		
	Output Power at 10% THD+N	R_L = 4Ω, f = 1kHz		18		
		R_L = 8Ω, f = 1kHz		10		
THD+N	Total harmonic distortion + noise	R_L =4Ω, f = 1kHz, Po = 10W		0.15		%
		R_L = 8Ω, f = 1kHz, Po = 5W		0.08		
Vn	Output integrated noise floor	20Hz to 22kHz, A-weighted, Gain = 20dB		200		μV
Cs	Crosstalk	P_O = 1W, f = 1kHz, Gain = 20dB		-70		dB
SNR	Signal-to-noise ratio	THD+N<1%, f = 1kHz, Gain = 20dB		92		dB
OTP	Thermal trip point			160		°C
OTH	Thermal hysteresis			60		°C
fosc	Oscillator frequency	SE_BTL = 2.5V	250	300	350	kHz
		SE_BTL = 0.8V		360		

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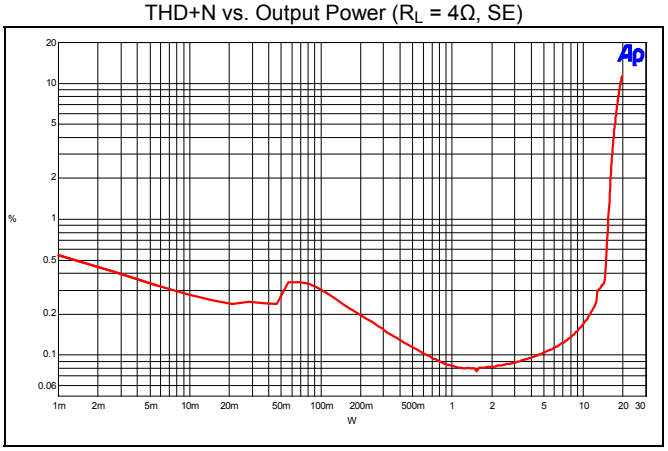
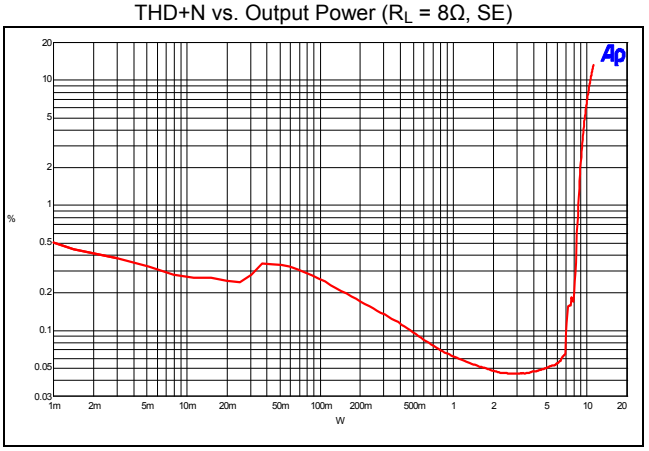
Performance Characteristics (@T_A = +25°C, V_{CC} = 24V, f = 1kHz, Gain = 20dB unless otherwise specified.)

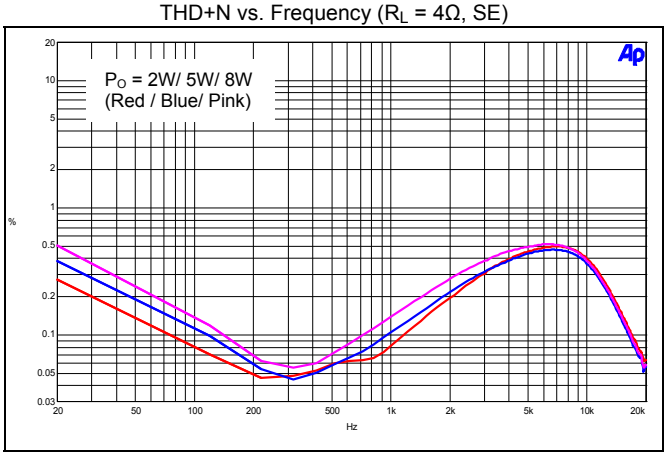
THD+N vs. Output Power (R_L = 4Ω, SE)



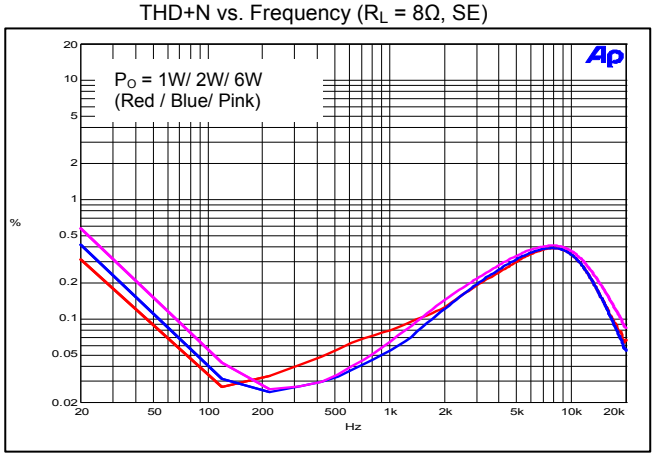
THD+N vs. Output Power (R_L = 8Ω, SE)



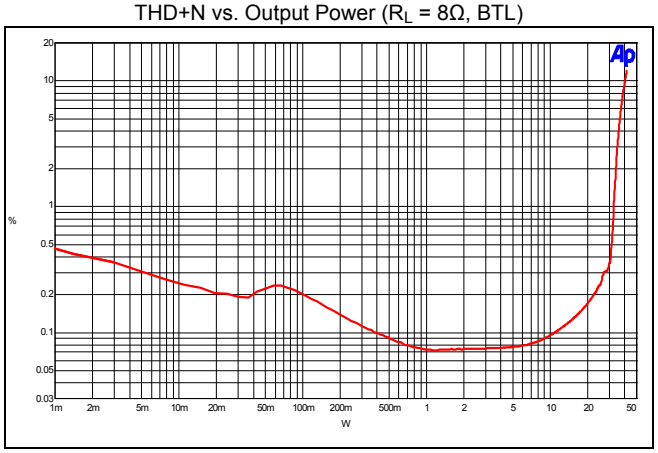
THD+N vs. Frequency (R_L = 4Ω, SE)



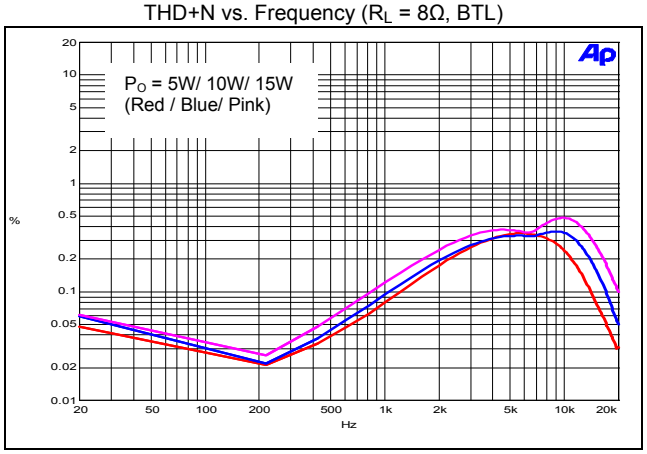
THD+N vs. Frequency (R_L = 8Ω, SE)



THD+N vs. Output Power (R_L = 8Ω, BTL)



THD+N vs. Frequency (R_L = 8Ω, BTL)



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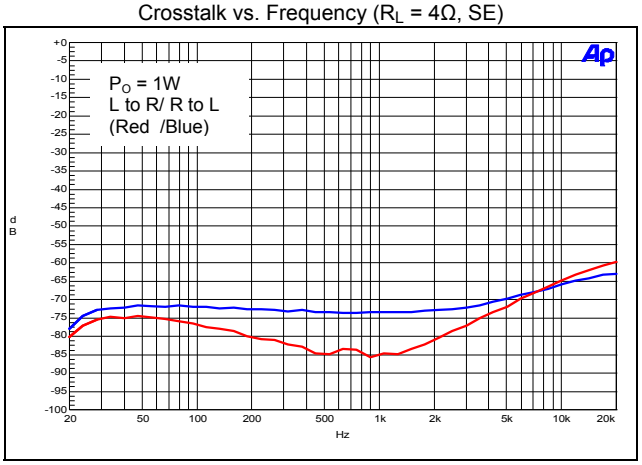
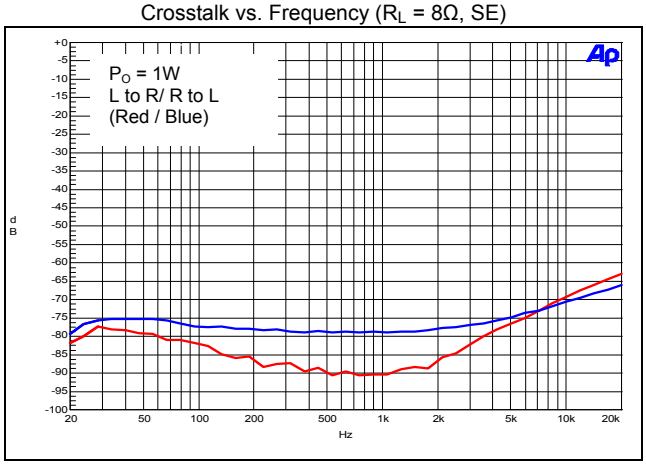
Performance Characteristics (@T_A = +25°C, V_{CC} = 24V, f = 1kHz, Gain = 20dB unless otherwise specified.)

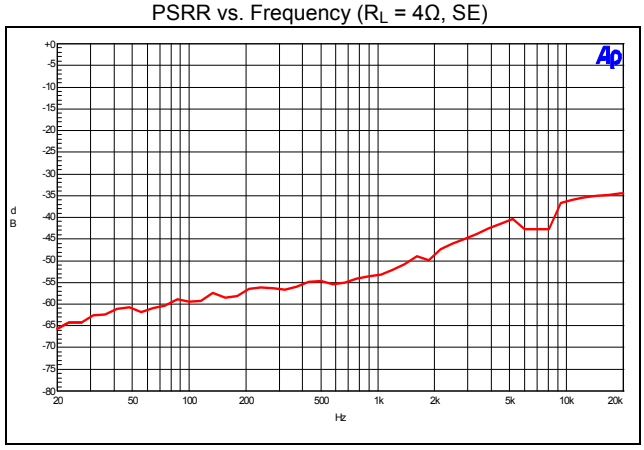
Crosstalk vs. Frequency (R_L = 4Ω, SE)



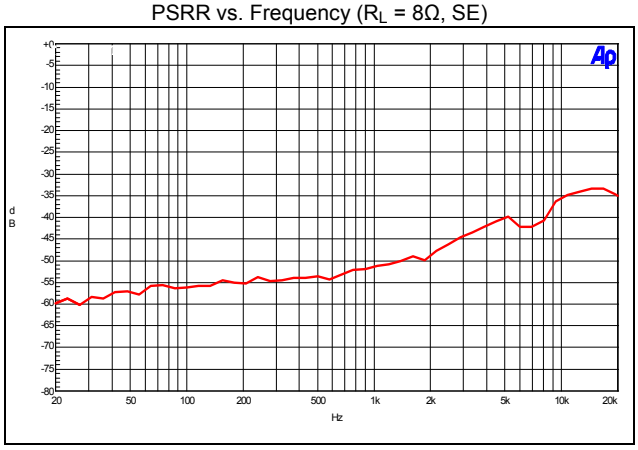
Crosstalk vs. Frequency (R_L = 8Ω, SE)



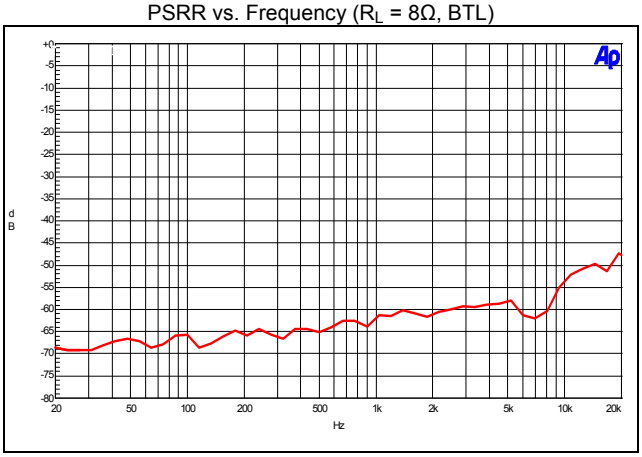
PSRR vs. Frequency (R_L = 4Ω, SE)



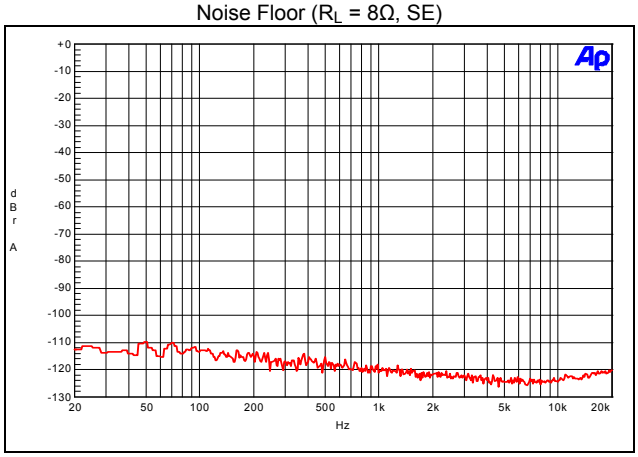
PSRR vs. Frequency (R_L = 8Ω, SE)



PSRR vs. Frequency (R_L = 8Ω, BTL)



Noise Floor (R_L = 8Ω, SE)



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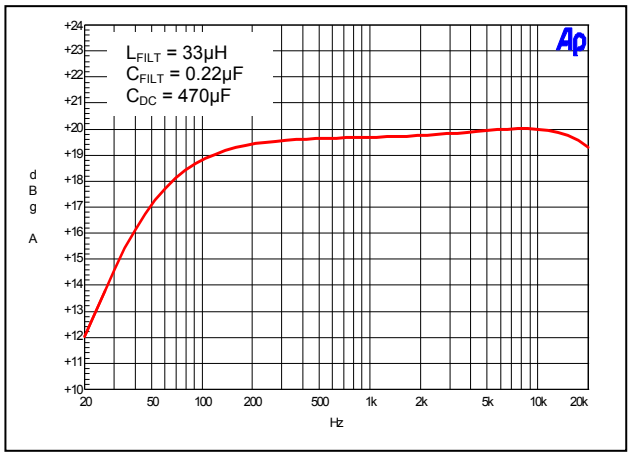
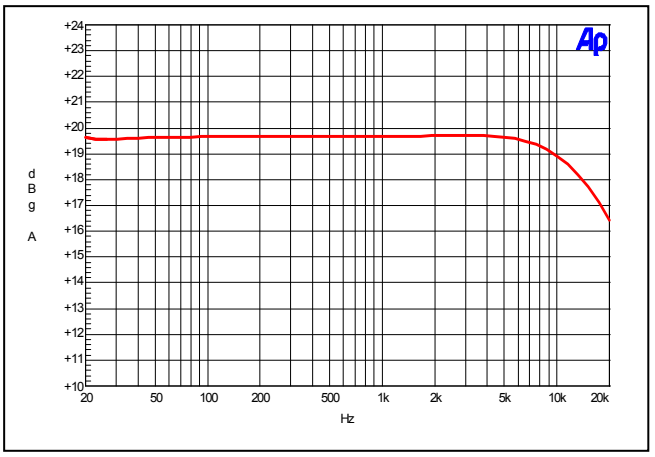
Performance Characteristics (@T_A = +25°C, V_{CC} = 24V, f = 1kHz, Gain = 20dB unless otherwise specified.)

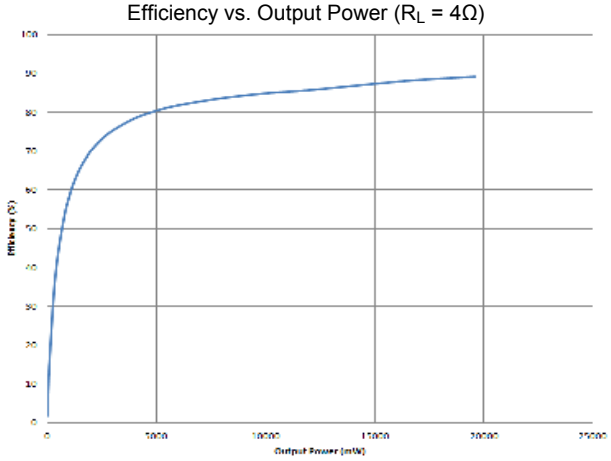
Frequency Response (R_L = 8Ω, SE)



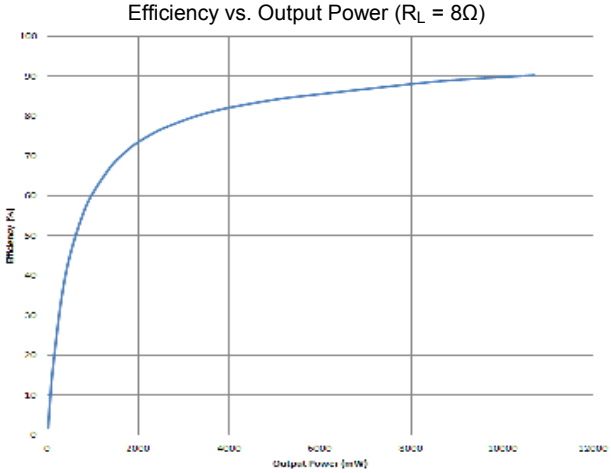
Frequency Response (R_L = 8Ω, BTL)



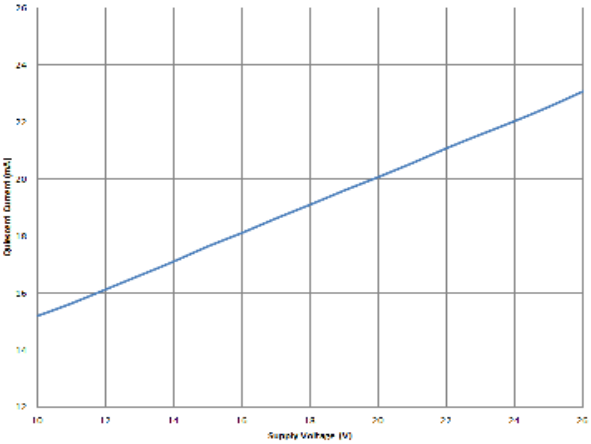
Efficiency vs. Output Power (R_L = 4Ω)



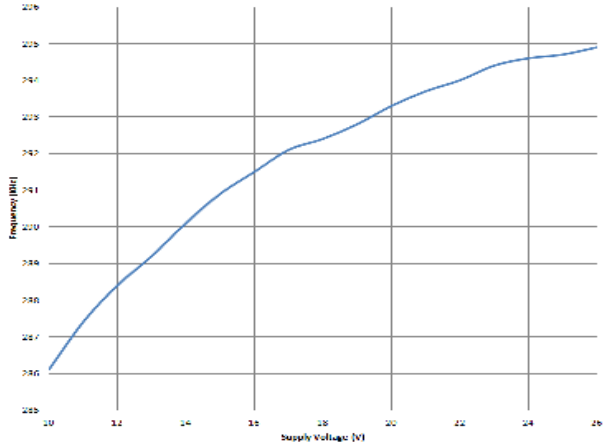
Efficiency vs. Output Power (R_L = 8Ω)



Quiescent Current vs. Supply Voltage



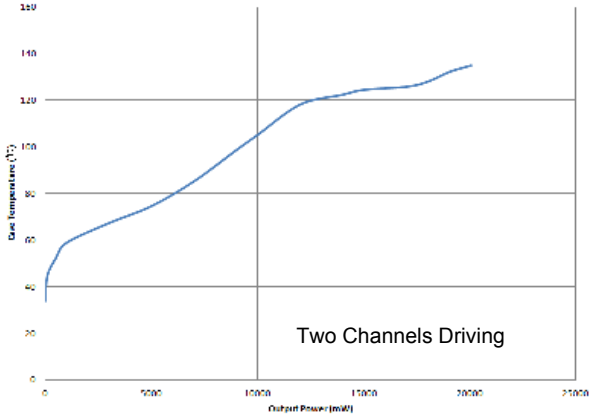
OSC Frequency vs. Supply Voltage



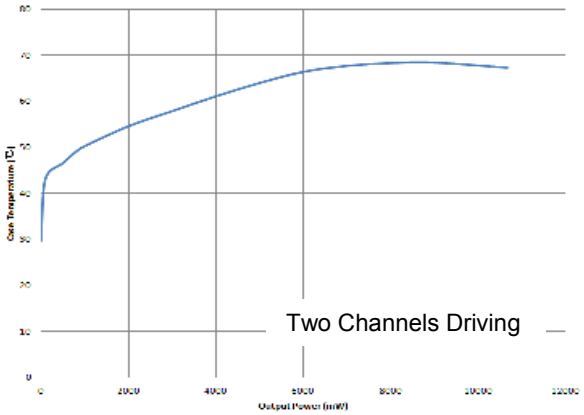
NEW PRODUCT

Performance Characteristics (@T_A = +25°C, V_{CC} = 24V, f = 1kHz, Gain = 20dB unless otherwise specified.)

Case Temperature vs. Output Power (R_L = 4Ω)



Case Temperature vs. Output Power (R_L = 8Ω)



Application Information

Input Capacitors (Ci)

In the typical application, an input capacitor Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$f_C = \frac{1}{(2\pi RiCi)}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 40kΩ and the specification calls for a flat bass response are down to 20Hz. Equation is reconfigured as followed:

$$Ci = \frac{1}{(2\pi Rif_c)}$$

When input resistance variation is considered Ci is 200nF, so one would likely choose a value of 220nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice.

Gain Setting Control

The gain of the PAM8124 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in following table are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

Table 1: Gain Setting

Gain1	Gain0	Amplifier Gain (dB), Typical	Input Impedance (kΩ), Typical (Ri)
0	0	20	40
0	1	26	20
1	0	30	10
1	1	36	6.67

NEW PRODUCT

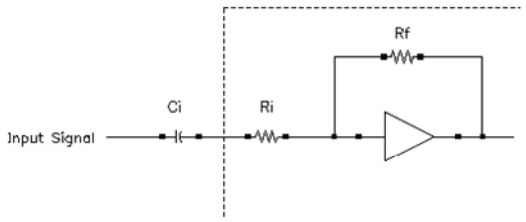
Application Information (cont.)

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value (6.67kΩ ±20%) to the largest value (40kΩ ±20%). As a result, if a single capacitor is used in the input high-pass filter, the –3dB cutoff frequency may change when changing gain steps.

The –3dB frequency can be calculated using the following Equation. Use the Ri values given in Table 1.

$$fc = \frac{1}{(2\pi RiCi)}$$



Single-Ended Output Capacitor

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls off with decreasing frequency at a rate of 20dB/decade. The cutoff frequency is determined by:

$$f_{coh} = \frac{1}{2\pi R_L C_{SE}}$$

Table 2 shows some common component values and the associated cutoff frequencies:

Table 2: Common Filter Responses

R_L-Speaker Impedance (Ω)	CSE-DC Blocking Capacitor (μF)		
	fc = 60Hz (-3dB)	fc = 40Hz (-3dB)	fc = 20Hz (-3dB)
4	680	1000	2200
6	470	680	1500
8	330	470	1000

Output Filter and Frequency Response

For the best frequency response, a flat pass band output filter (second-order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the LOUT and ROUT pins. There are several possible configurations, depending on the speaker impedance and whether the output configuration is single-ended (SE) or bridge-tied load (BTL). Table 3 lists the recommended values for the filter components. It is important to use a high-quality capacitor in this application. A rating of at least X7R is required.

Table 3: Recommended Filter Output Components

Output Configuration	Speaker Impedance(Ω)	Filter Inductor(μH)	Filter Capacitor(nF)
Single Ended (SE)	4	22	680
	8	33	220
Bridge Tied Load (BTL)	8	22	680

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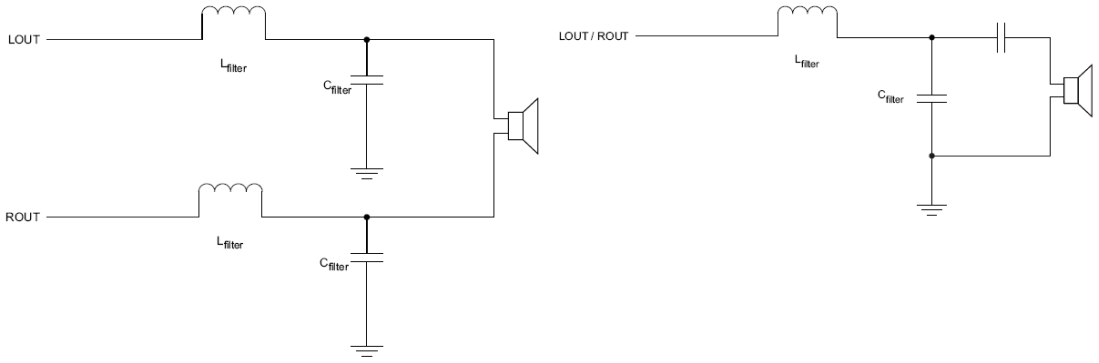
Application Information (cont.)



BTL Filter Configuration **SE Filter Configuration**

Power and Heat Dissipation

Choose speakers that are able to stand large output power from the PAM8124. Otherwise, speaker may suffer damage.

Heat dissipation is very important when the device works in full power operation. Two factors affect the heat dissipation, the efficiency of the device that determines the dissipation power, and the thermal resistance of the package that determines the heat dissipation capability.

Generally, class-D amplifiers are high efficiency and need no heat sink. Operating at higher powers a heat sink still may not be necessary if the PCB is carefully designed to achieve good thermal dissipation.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

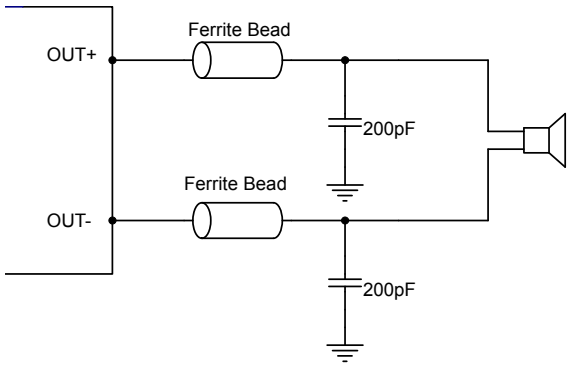


Figure 1. Ferrite Bead Filter to Reduce EMI

Dual-Side PCB

To achieve good heat dissipation, the PCB's copper plate should be thicker than 35um and the copper plate on both sides of the PCB should be utilized for heat sink. The thermal pad on the bottom of the device should be soldered to the plate of the PCB, and via holes, usually 9 to 16, should be drilled in the PCB area under the device and deposited copper on the vias should be thick enough so that the heat can be dissipated to the other side of the plate. There should be no insulation mask on the other side of the copper plate. It is better to drill more vias on the PCB around the device if possible.

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Application Information (cont.)

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8124. A logic high on this pin causes the outputs to run at a constant 50% duty cycle. A logic low on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs.

Shutdown Operation

The PAM8124 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The SDN input terminal should be pulling high during normal operation when the amplifier is in use. Pulling SDN low causes the outputs to mute and the amplifier to enter a low-current state. SDN should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

For the best start-up pop performance, the amplifier should be set in mute mode prior to restarting the amplifier.

Internal Bias Generator Capacitor Selection

The internal bias generator (VCM) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the VCM terminal is critical for achieving the best device performance. During startup or recovery from shutdown state the VCM capacitor determines the rate at which the amplifier starts up. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the class-D output switching-on other than that of the startup time. However, at least a 0.47μF capacitor is recommended for the VCM capacitor.

Another function of the VCM capacitor is to bypass high frequency noise on the internal bias generator.

Power Supply Decoupling, CS

The PAM8124 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor of 0.1μF is typically recommended, placed as close as possible to the device's PVCC lead. To filter lower-frequency noises a large aluminium electrolytic capacitor of 470μF or greater is recommended, placed near the audio power amplifier. The 10μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSL and BSR Capacitors

The half H-bridge output stages use NMOS transistors therefore requiring bootstrap capacitors for the high side of each output to turn on correctly. A ceramic capacitor 220nF or more rated for over 25V must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from LOUT to BSL and another 220nF capacitor from ROUT to BSR. It is recommended to use 1μF BST capacitor to replace 220nF for lower than 100Hz applications.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator is used to clamp the gate voltage. A 1μF capacitor must be connected from VCLAMP to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with VCC and may not be used to power any other circuitry.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-Circuit Protection

The PAM8124 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts (BTL mode), output-to-GND shorts, or output-to-VCC shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is not a latched fault. If the short was removed, the normal operation is restored.

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Application Information (cont.)

Thermal Protection

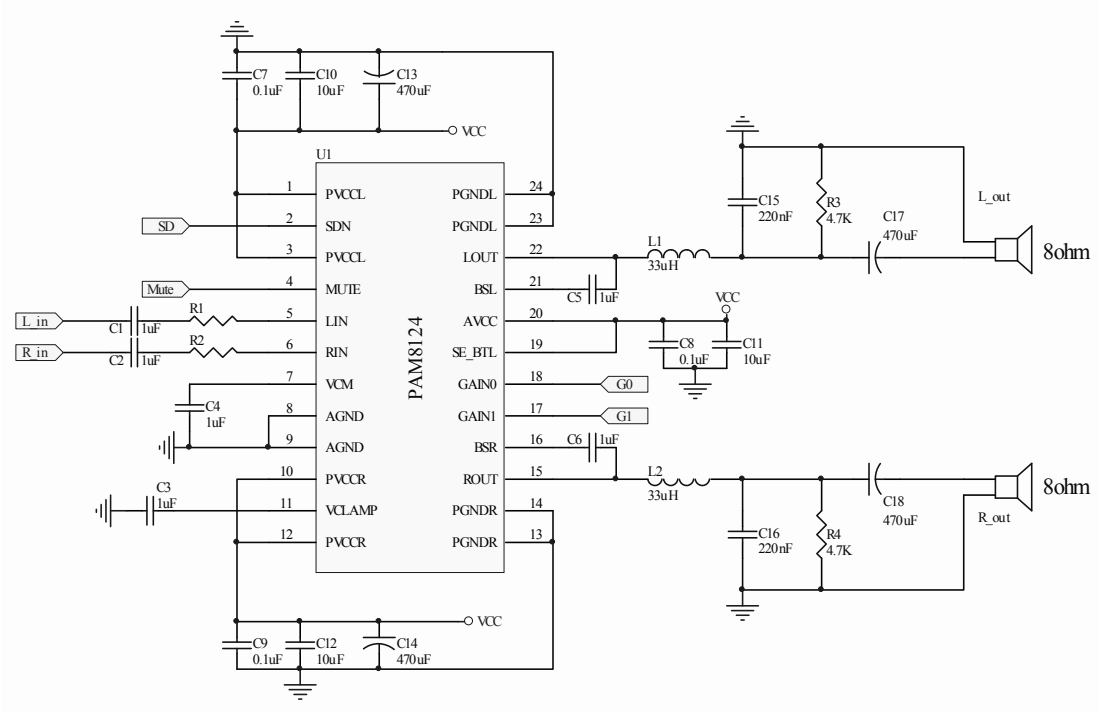
Thermal protection on the PAM8124 prevents damage to the device when the internal die temperature exceeds 160°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault, the thermal fault is cleared once the temperature of the die is reduced by 60°C. The device begins normal operation at this point without external system intervention.

Over Voltage Protection and Under Voltage Lock-out (OVP and UVLO)

An over voltage protection (OVP) circuit is integrated in PAM8124, when the supply voltage is over 28V the OVP is active and then the output stage is disabled. The PAM8124 will auto recovery when the supply voltage is lower than the OVP threshold.

The PAM8124 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 9V or below, the PAM8124 goes into a state of shutdown. When the supply voltage is higher than UVLO threshold normal operation is resumed.

Typical Applications Circuits



Schematic for Single-Ended (SE) Configuration (8Ω Speaker)

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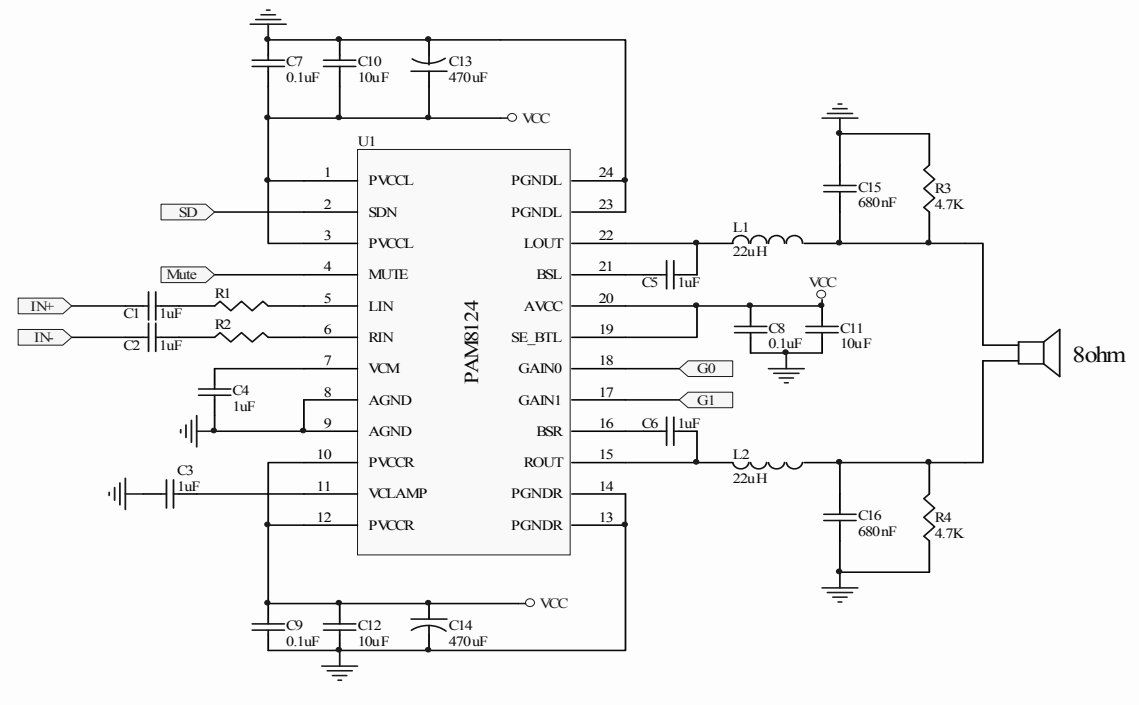
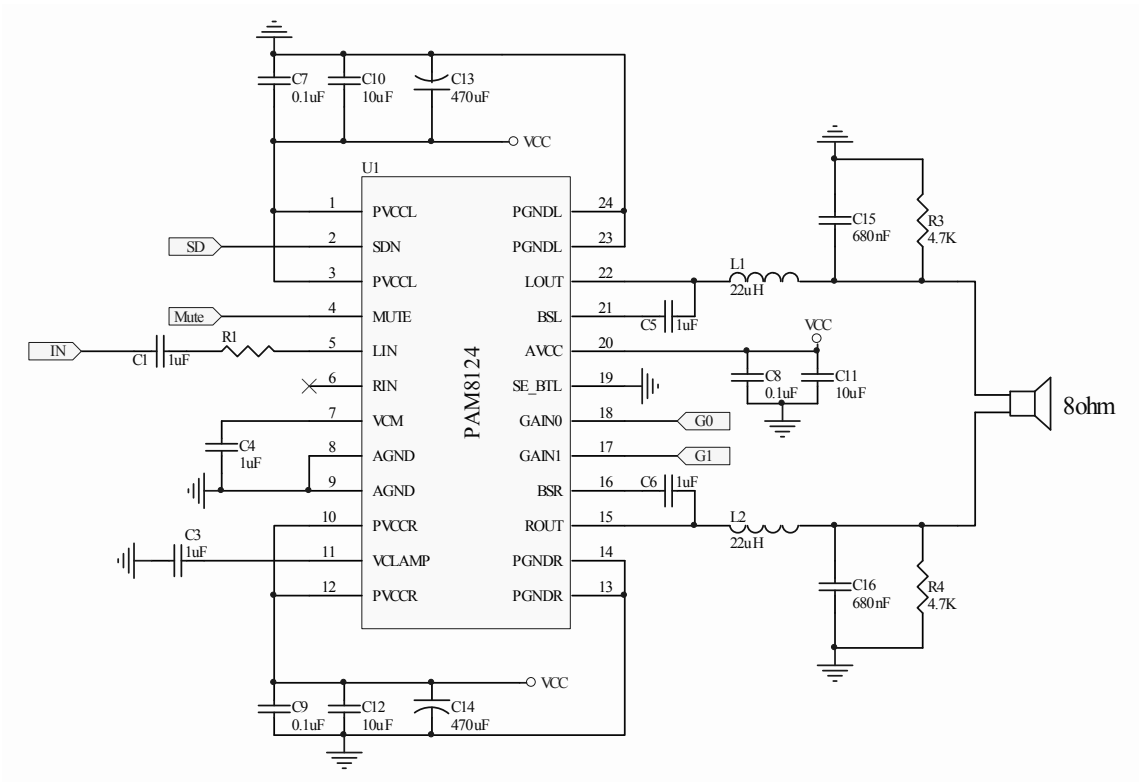
Application Information (cont.)

Typical Applications Circuits (cont.)



Schematic for Bridge-Tied-Load (BTL) Configuration with Differential Input (8Ω Speaker)



Schematic for Bridge-Tied-Load (BTL) Configuration with Single-Ended Input (8Ω Speaker)

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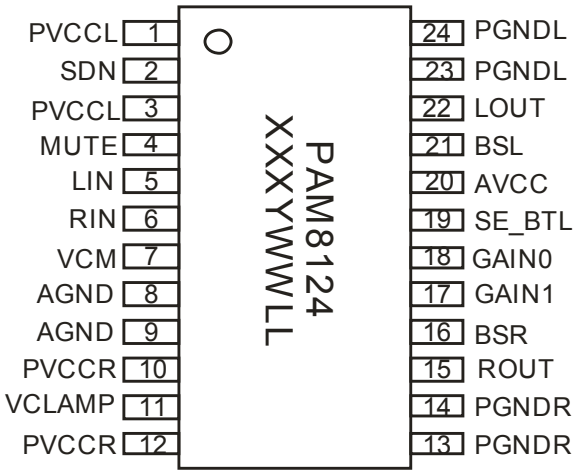
Ordering Information

PAM8124 X X X

Package Type	Package Configuration	Shipping Package
R: TSSOP	H: 24 Pin	R: Tape & Real

Part Number	Package	Standard Package
PAM8124RHR	TSSOP-24-EP	3000 Units/Tape&Reel

Marking Information



PAM8124: Product Code

X: Internal Code

Y: Year

W: Week

LL: Internal Code

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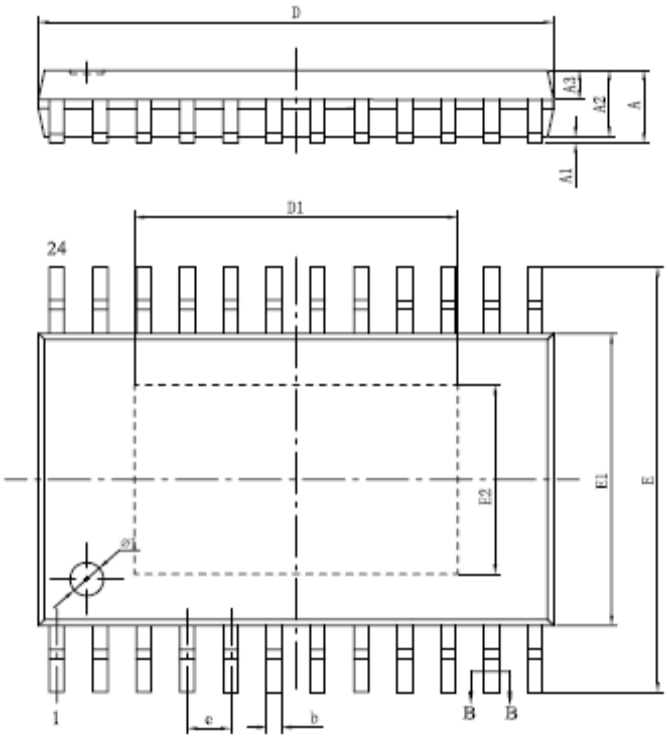
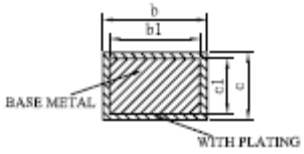
Package Outline Dimensions (All dimensions in mm.)

Package: TSSOP-24-EP





SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	7.70	7.80	7.90
D1	4.73	4.83	4.93
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.75	2.85	2.95
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
S	0.20	—	—
Ø1	Ø0.8X0.05-0.10DP		
θ	0	—	8°
L/F载体尺寸 (mil)	122*190		

NEW PRODUCT

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