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THS6032 Low-Power ADSL Central-Office Line Driver Evaluation Module

User's Guide

Preface

Related Documentation From Texas Instruments

■ ***THS6032 LOW-POWER ADSL CENTRAL-OFFICE LINE DRIVER*** (TI Literature Number SLOS233). This is the data sheet for the THS6032 amplifier integrated circuit used on the EVM

■ ***THS4001 HIGH-SPEED LOW-POWER OPERATIONAL AMPLIFIER*** (TI Literature Number SLOS206) This is the data sheet for the THS4001 amplifier integrated circuit used on the EVM.

■ ***PowerPAD™ Thermally Enhanced Package*** (TI Literature Number SLMA002) This is the technical brief for the special PowerPAD™ package in which the THS6032 amplifier IC is supplied.

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Contents

Figures

Chapter 1

General Information

This chapter details the Texas Instruments (TI™) THS6032 low-power ADSL central-office line driver evaluation module (EVM), SLOP134. It includes a list of EVM features, a brief description of the module illustrated with a pictorial and schematic diagrams, EVM specifications, details on configuring, connecting, and using the EVM, and a discussion on high-speed amplifier and PowerPAD™ package design considerations.

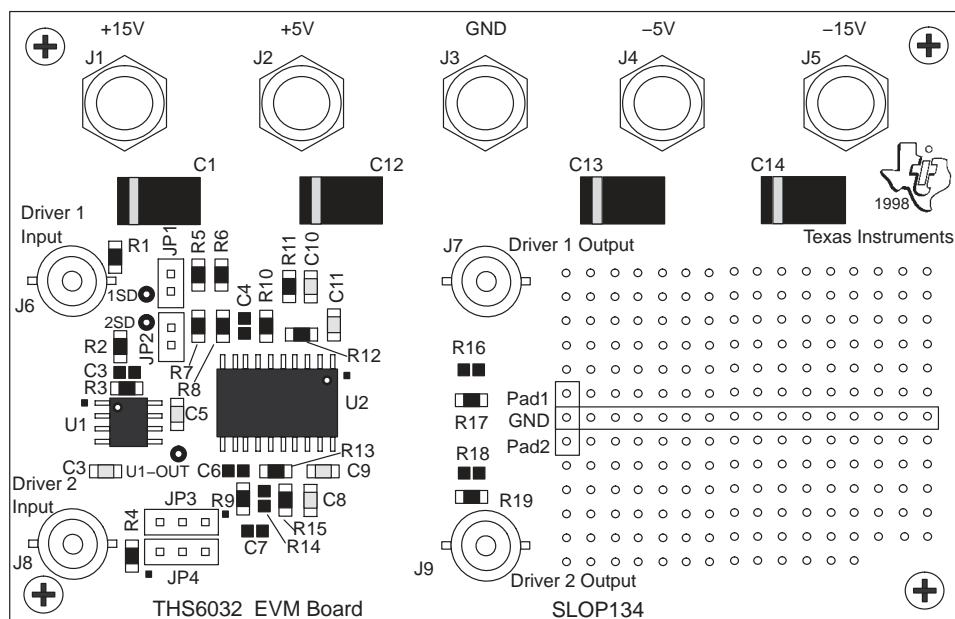**Topic**   **Page**

1.1 Features

THS6032 low-power ADSL central-office line driver EVM features include:

- A Complete Central Office Side ADSL Differential Line Driver

- Multiple Input Configurations Set Via On Board Jumpers

- Includes Test Points and Jumpers for Easy Control of Shutdown Functions

- A THS4001 High-Speed Amplifier as an Inverter

- Standard BNC Connectors Inputs and Outputs

- High-Efficiency Class-G Amplifier Topology

- Nominal 50-Ω Impedance Inputs

- Pad Area On Board For User Component Placement and Testing

- Good Example of PowerPAD™ Package and High-Speed Amplifier Design and Layout

1.2 Description

The TI THS6032 low-power ADSL central-office line driver evaluation module (EVM) is a complete central office side ADSL high-speed driver circuit. It consists of the TI THS6032 low-power ADSL central-office line driver IC, a TI THS4001 high-speed, low-power operational amplifier IC, and a number of passive parts, all mounted on a multilayer circuit board (Figure 1–1). The EVM uses standard BNC connectors for inputs and outputs and also includes a pad area for user component connection and testing. It is completely assembled, fully tested, and ready to use — just connect it to power, a signal source, and a load (if desired).

Figure 1−1. THS6032 Evaluation Module

Input power is applied to the EVM through banana jacks J1 through J5. Because of the special class-G architecture of the THS6032, two supplies are required to achieve a highly-efficient line driver. The schematic for the EVM appears in Figure 1–2.

Figure 1–2. THS6032 Evaluation Module Schematic

The THS6032 EVM is equipped with a separate BNC connector for the driver 1 input and the driver 2 input. Each input is terminated with a 50-Ω resistor to provide correct line impedance matching (Figure 1–2). Using a source with a 50-Ω output impedance will create a voltage divider at the EVM inputs. Thus, accurate knowledge of the source output characteristics is required to determine proper input signal amplitudes.

Driver outputs are routed through central office side ADSL-standard 12.4-Ω resistors to provide correct transmission line impedance matching when run through a 1:2 transformer with a 100-Ω termination. These resistors also allow separate receivers to view a differential input signal from the transmission line.

All of the amplifiers on the EVM (THS6032 and THS4001) follow the classic operational amplifier gain equations:

$$\text{Inverting Gain} = \frac{-R_F}{R_G} \tag{1}$$

$$\text{Noninverting Gain} = 1 + \frac{R_F}{R_G} \tag{2}$$

The gain of the amplifiers can be easily changed to support different applications by changing resistor ratios. Any of the components on the EVM board can be replaced with different values. Also, component pads have been placed in convenient locations on the PCB (shown as components with the value X in the schematic) to allow numerous modifications to the basic EVM configuration. However, care must be taken, because the surface-mount solder pads on the board are somewhat fragile and will not survive a large number of soldering/desoldering operations.

The THS6032 IC is a current-feedback amplifier (CFB), and, because of this, extra care must be taken to ensure that a feedback resistor is always included in the design. In addition, there must never be a capacitor directly in the feedback path between the noninverting input and the amplifier output. Disregarding this guideline will likely result in a part that oscillates. The THS4001 IC amplifier used on the EVM, however, is a classic voltage-feedback amplifier (VFB) and has no restrictions on resistors or capacitors in the feedback path. But, to maximize bandwidth, high value resistors and capacitors should be used with discretion.

The shutdown feature of the THS6032 IC is implemented on this EVM and each amplifier on the IC has a separate shutdown control input. A *LOW* shutdown signal allows normal THS6032 operation and a *HIGH* (5-V) signal places the corresponding amplifier into a low-power mode. Onboard jumpers JP1 and JP2 provide manual shutdown control (install shunts to shut down amplifier) and test points 1SD and 2SD allow external shutdown control with standard TTL-level signals (with jumper shunts removed). See Figure 1–3.

*Figure 1−3. THS6032 Evaluation Module Shutdown Control*
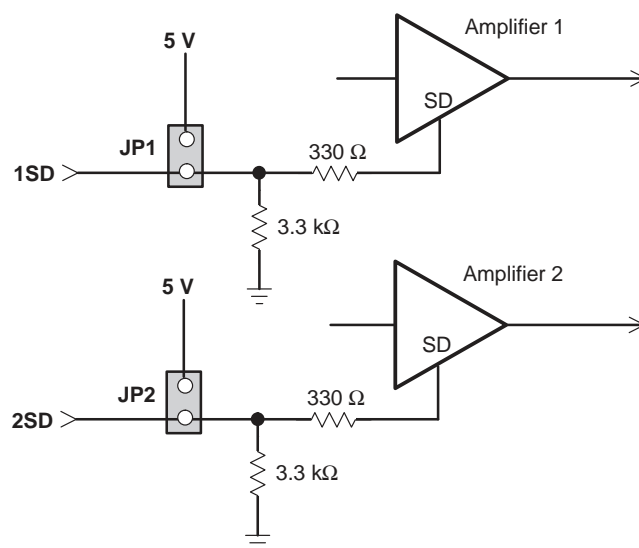
Note that unlike most amplifiers, the THS6032 amplifiers go into a low-output impedance state while in shutdown mode to properly terminate the communication lines. Without this proper line termination, the receiver amplifiers (not included on this EVM) are not able to sense the incoming signals on the communication lines. Thus, the system is able to receive signals while the line drivers are shut down and conserving power.

Finally, the EVM circuit board is a good example of proper board layout for high-speed amplifier and PowerPAD™ designs. It can be used as a guide for user application layouts.

1.3 Input Configuration

The THS6032 EVM inputs can be configured in several different ways to provide a wide variety of circuits to support different applications (Figure 1−4). Each of the two jumpers on the EVM is a three-pin header that is used as a SPDT switch by placing a shunt across two pins to select either of two possible signal routes.

Figure 1−4. THS6032 Evaluation Module Block Diagram
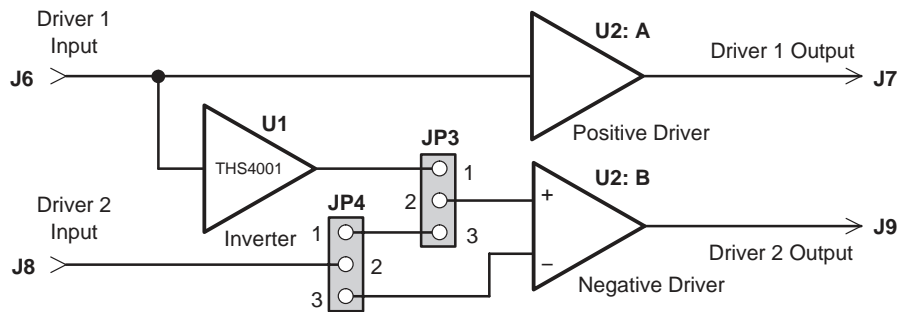
❑ Jumper JP3:

■ 1−2 — connects the noninverting input of driver 2 (U2: B) to the THS4001 inverting amplifier (U1) output

■ 2−3 — connects the noninverting input of driver 2 (U2: B) to the input connector (J4) when jumper JP4 is set appropriately

❑ Jumper JP4:

■ 1−2 — connects the driver 2 input connector (J8) to the noninverting input of driver 2 (U2:B) when jumper JP3 is set appropriately

■ 2−3 — connects the driver 2 input connector (J8) to the inverting input of driver 2 (U2:B) when jumper JP3 is set appropriately

For example, to use a single-ended input, jumper JP3 should be set to 1−2 and the input signal applied to input connector J6. The output of the THS6032 drivers is a differential signal due to the inverter (U1) and JP3 being set to 1−2. For a differential source, JP3 should be set to 2−3, JP4 should be set to 1−2 and the differential input signal applied between input connectors J6 and J8.

If JP4 is in the 2−3 position, components C7 and R14 must be installed, R9 must be removed, and a 0-Ω resistor must be installed in the C6 position for proper operation.

1.4 THS6032 EVM Specifications

Supply voltage range, $\pm V_{CC}$ (J1, J5) .... $\pm$ 5 V to $\pm$ 15 V

$\pm V_{CC}$ (J2, J4) Class G operation .... $\pm$ 3 V to $\pm$ 15 V

$\pm V_{CC}$ (J2, J4) Class AB operation[†] .... Gnd

Supply current, I_{CC} .... 26 mA

Input voltage, V_I .... $\pm V_{CC}$, max

Output drive, THS6032 drivers, I_O .... 500 mA, typ each

Continuous total power dissipation at TA = 25°C (THS6032), ... 5.8 W, max

[†] Even though the THS6032 amplifier IC incorporates a class G output stage, normal class AB operation can be accomplished by connecting J2 and J4 to the GND terminal (J3).

For complete THS6032 amplifier IC specifications, parameter measurement information, and additional application information, see the THS6032 data sheet, TI Literature Number SLOS233.

1.5 Using The THS6032 EVM

The THS6032 EVM operates from two split power supplies with voltages of ± 5 V to ± 15 V. As shipped, the output of driver 1 is equal to a noninverting gain of 10 when using the single-ended input mode. The output of driver 2 is equal to an inverting gain of 10 under the same conditions. An oscilloscope is typically used to view and analyze the EVM output signals.

1) Ensure that all power supplies are set to *OFF* before making power supply connections to the THS6032 EVM.

2) Connect appropriate split power supplies to the banana jacks on the module marked *+15 V* (J1), *+5 V* (J2), *–5 V* (J4), and *–15 V* (J5).

3) Connect the power supply grounds to the module banana jack marked *GND* (J3).

4) Connect an oscilloscope probe to U2, pin2. This is the driver 1 amplifier output. Connecting directly to the **DRIVER 1 OUTPUT** BNC connector (J7) with a 50-Ω nominal impedance cable and probe is not recommended. The source impedance of driver 1 is only 12.4 Ω; such a connection could cause reflections to occur at high frequencies and is not a true measurement of the amplifier performance.

5) Set jumper J3 to the 1–2 position.

6) Set jumper J4 to the 1–2 position.

7) Remove the jumper on JP1.

8) Remove the jumper on JP2.

9) Set the power supplies to *ON*

10) Connect a signal input to the **DRIVER 1 INPUT** BNC (J6).

Each input connector on this EVM is terminated with a 50-Ω resistor to ground. With a 50-Ω source impedance, the voltage seen by the THS6032 amplifier IC on the EVM will be 1/2 the source signal voltage applied to the EVM input connector.

11) Verify the output signal on the oscilloscope. With a high-impedance scope probe, the output signal should be twice the source amplitude. When connected to J9 (driver 2 output), the signal should be 180° phase shifted from the driver 1 output (J7).

1.6 THS6032 EVM Performance

Figure 1–5 shows the typical single-ended frequency response of the THS6032 EVM drivers when single-endedly loaded. This data was collected using a single-ended input (J6 and J8, respectively) with a 25-Ω single-ended load connected between the driver outputs and ground, as shown in the test circuit of Figure 1–6.

Typical bandwidth is approximately 65 MHz for both drivers. The difference between the output signals of driver 1 and driver 2 is primarily due to the difference in the high-frequency characteristics of the source traces. Component values can be changed to cause the two responses to track more closely, but since ADSL signals are limited to 2 MHz and below, the high-frequency imbalance can usually be ignored.

Figure 1–5. THS6032 EVM Driver Frequency Response With Single-Ended Input and Output
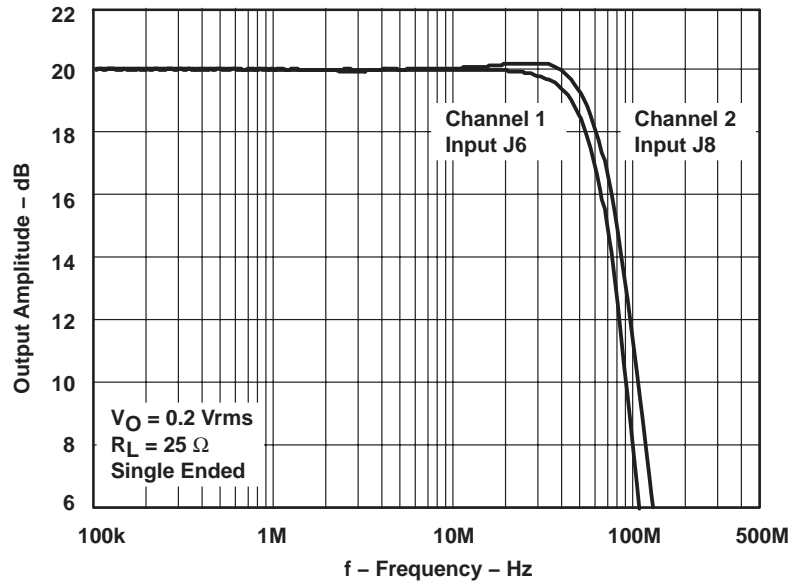
Figure 1–6. THS6032 EVM Driver Single-Ended Frequency Response Test Circuit
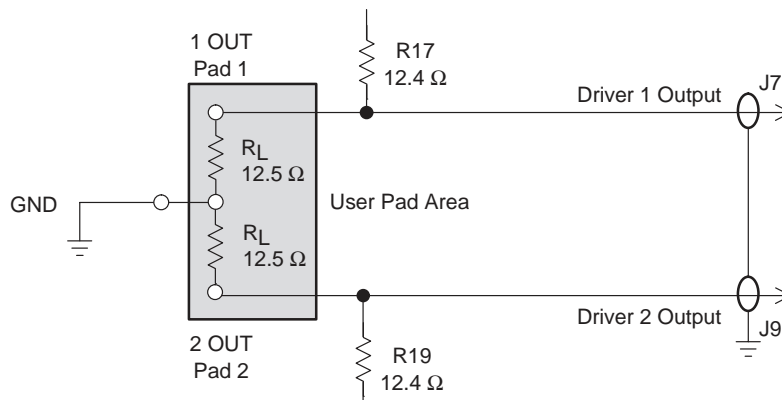
Figure 1–7 shows the typical single-ended frequency response when the channel 2 input signal is routed through inverting amplifier U1. The inverting amplifier is a THS4001 device and adds its own frequency characteristics to the source signal. Jumpers JP3 and JP4, along with the additional input trace lengths of Channel 2 (which will always have parasitic effects), also affect the frequency characteristics of the source signal before it reaches the input of the THS6032 amplifier IC. In most cases, these changes to the high-frequency characteristics can be minimized with an optimal layout. But since the EVM was designed to provide exceptional channel 2 input signal flexibility, some high-frequency characteristic tradeoffs were unavoidable. The user can adjust component values to improve the response somewhat, but since ADSL signals are typically limited to 2 MHz and below, such adjustments may not be very productive.

Figure 1–7. THS6032 EVM Channel 2 Driver Frequency Response With Single-Ended Input and Output

General Information
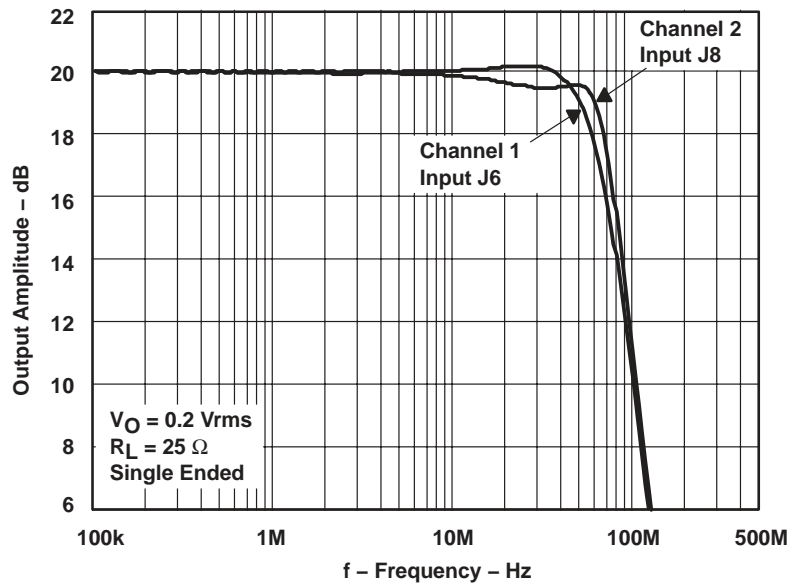
1–8 shows the typical differential frequency response of the THS6032 drivers when loaded differentially with a 50-Ω load as shown in Figure 1–9. This data was collected using a single-ended input (J6) and inverting amplifier U1 to create a differential signal source.

The advantage of using the current feedback amplifier design is evident in the frequency response graph. A bandwidth of 55 MHz with a gain of 10 provides reduced distortion for the *low* frequency ADSL signals. Changing the gains of each amplifier yields similar bandwidths and makes system design much easier to control.

Figure 1−8. THS6032 EVM Driver Frequency Response With Differential Input and Output
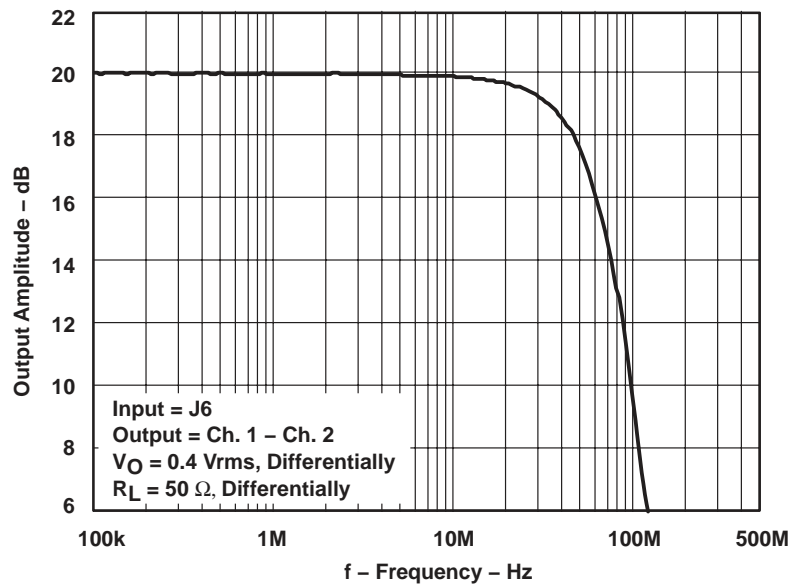
Figure 1−9. THS6032 EVM Driver Differential Frequency Response Test Circuit
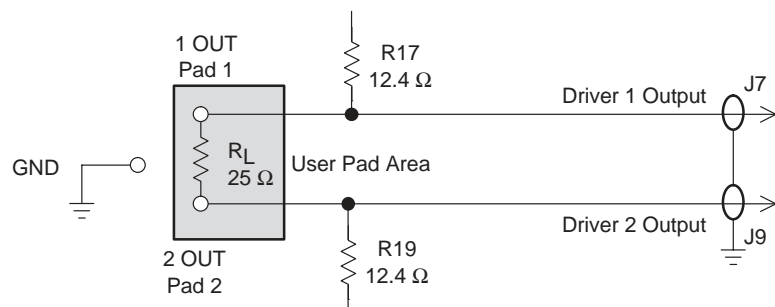
1.7   General High-Speed Amplifier Design Considerations

The THS6032 EVM layout has been designed and optimized for use with high-speed signals and can be used as an example when designing THS6032 applications. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregard of these basic design considerations could result in less than optimum performance of the THS6032 low-power ADSL central-office line driver IC.

Surface-mount components were selected because of the extremely low lead inductance associated with this technology. Also, because surface-mount components are physically small, the layout can be very compact. This helps minimize both stray inductance and capacitance.

Tantalum power supply bypass capacitors (C1, C12, C13, and C14) at the power input pads help supply currents for rapid, large signal changes at the amplifier output. The 0.1 µF power supply bypass capacitors (C3, C5, and C8 through C11) are placed as close as possible to the IC power input pins in order to keep the PCB trace inductance to a minimum. This improves high-frequency bypassing and reduces harmonic distortion.

A proper ground plane should always be used with high-speed circuit design. This provides low-inductive ground connections for return current paths. Special attention is needed for the inverting input pins. Stray capacitance at these pins can seriously degrade the performance of the amplifiers. In addition, ground plane coupling into these pins can cause noise to appear at the outputs of the amplifiers. This is especially important for the inverting pin while the amplifier is operating in the noninverting mode. Because the voltage at this pin swings directly with the noninverting input voltage, any stray capacitance would allow currents to flow into the ground plane, causing possible gain error and/or oscillation. Capacitance variations at the amplifier IC input pin of less than 1 pF can significantly affect the response of the amplifier.

In general, it is always best to keep signal lines as short and as straight as possible. Sharp 90° corners should generally be avoided; round corners or a series of 45° bends should be used, instead. Stripline techniques should also be incorporated when signal lines are greater than 3 inches in length. These traces should be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Such signal lines should also be properly terminated with an appropriate resistor.

Finally, proper termination of all inputs and outputs should be incorporated into the layout. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier IC. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in amplifier phase-margin and improves the amplifier stability for improved performance such as reduced peaking and settling times.

1.8   General PowerPAD™ Design Considerations

The THS6032 IC is mounted in a special package incorporating a thermal pad that transfers heat from the IC die directly to the PCB. The PowerPAD™ package is constructed using a downset leadframe. The die is mounted on the leadframe but is electrically isolated from it. The bottom surface of the lead frame is exposed as a metal thermal pad on the underside of the package and makes physical contact with the PCB. Because this thermal pad is in direct physical contact with both the die and the PCB, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad mounting point on the PCB.

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach as used on the THS6032 EVM, which is built on a multilayer PCB with an internal ground plane.

1)   Prepare the PCB with a top side etch pattern as shown in Figure 1−10. There should be etch for the leads as well as etch for the thermal pad.

Figure 1−10. PowerPAD™ PCB Etch and Via Pattern – Minimum Requirements

Thermal pad area (0.19 x 0.21) with 18 vias
(Via diameter = 13 mils)
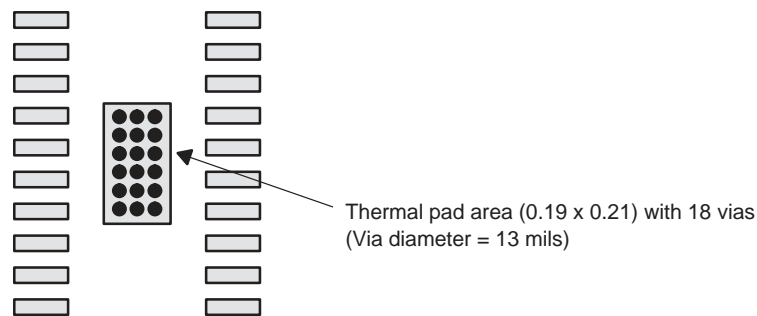
2)   Place 18 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.

3)   Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This will help dissipate the heat generated from the THS6032. These additional vias may be larger than the 13 mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered, therefore, wicking is generally not a problem.

4)   Connect all holes to the internal ground plane.

5)   When connecting these holes to the ground plane, **DO NOT** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6032 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.

6) The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its 18 holes. The bottom-side solder mask should cover the 18 holes of the thermal pad area. This eliminates the solder from being pulled away from the thermal pad area during the reflow process.

7) Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.

8) With these preparatory steps in place, the THS6032 is simply placed in position and run through the solder reflow operation as any standard surface mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS6032 in its PowerPAD™ package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 21.5°C/W. For a given θ_{JA}, the maximum power dissipation, shown in Figure 1–11, is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6032 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
        θ_{JC} = Thermal coefficient from junction to case (0.37°C/W)
        θ_{CA} = Thermal coefficient from case to ambient air

Figure 1–11. Maximum Power Dissipation vs Free-Air Temperature

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE
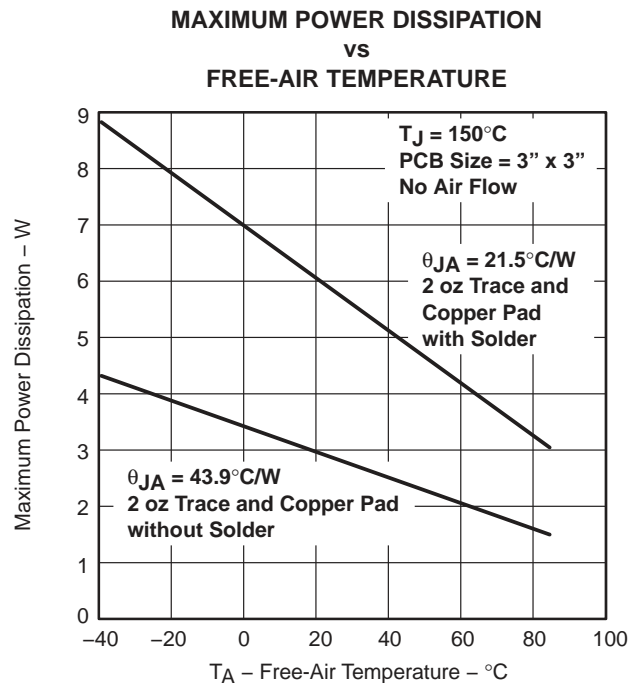
Even though the THS6032 EVM PCB is larger than the one in the example above, the results should correlate very well because the traces and the vias of the EVM PCB interrupt the thermal continuity of the ground plane. The THS6032 EVM is a good example of proper thermal management when using PowerPAD™-mounted devices.

Correct PCB layout and manufacturing techniques are critical for achieving adequate transfer of heat away from the PowerPAD IC package. More details on proper board layout can be found in the *THS6032 Low-Power ADSL Central-Office Line Driver* data sheet (SLOS233). For more general information on the PowerPAD package and its thermal characteristics, see the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package* (SLMA002).

Reference

This chapter includes a parts list and PCB layout illustrations for the THS6032 EVM.

2.1 THS6032 Low-Power ADSL Central-Office Line Driver EVM Parts List

Table 2–1. THS6032 EVM Parts List

Reference	Description	Size	Quantity	Manufacturer/Distributor Part Number
C1, C12, C13, C14	CAPACITOR, 6.8 µF, 35 V, 20%, TANTALUM, SM		4	(SPRAGUE) 293D685X9035D2T
C3, C5, C8, C9, C10, C11	CAPACITOR, 0.1 µF, CERAMIC, 10%, SM	0805	6	(MuRata) GRM40-X7R104K25
J6, J7, J8, J9	JACK, BNC, PC-MOUNT (AMPHONEL)		4	(MOUSER) 523-31-5329
J1,J2,J3, J4, J5	JACK, BANANA RECEPTANCE, FOR 0.25″ DIA. HOLE		5	
JP1,JP2	HEADER, 2 PIN, 0.1″ CTRS., 0.025″ SQ. PINS		2	
JP3,JP4	HEADER, 3 PIN, 0.1″ CTRS., 0.025″ SQ. PINS		2	
P1 – P4	SHORTING JUMPERS, 0.1″ CTRS, FOR 0.025″ SQ. PINS		4	
R9, R10	RESISTOR, 49.9 Ω, 1/10W, 1% SM	0805	2	
R1, R4	RESISTOR, 49.9 Ω, 1/8W, 1% SM	1206	2	
R11, R15	RESISTOR, 75 Ω, 1/10W, 1% SM	0805	2	
R7, R8	RESISTOR, 330 Ω, 1/10W, 5% SM	0805	2	
R12, R13	RESISTOR, 681 Ω, 1/10W, 1% SM	0805	2	
R5, R6	RESISTOR, 3.3 kΩ, 1/10W, 5% SM	0805	2	
R2, R3	RESISTOR, 1 kΩ, 1/10W, 1% SM	0805	2	
R17, R19	RESISTOR, 12.4 Ω, 1/8W, 1% SM	1206	2	
U2	IC, THS6032CDWP		1	(TI) THS6032CDWP
U1	IC, OP AMP, THS4001CD	SOIC-8	1	(TI) THS4001CD
R16, R18	RESISTOR, X OHMS, 1/8W, 1%, SM†	1206	2	
R14	RESISTOR, X OHMS, 1/10W, 1%, SM†	0805	1	
C2, C4, C6, C7	CAPACITOR, X µF, 10% CERAMIC†	0805	4	
1SD, 2SD, U1–Out	TEST POINT (RED)		3	(FARNELL) 240–345
	4-40 TREAD HEX STANDOFF, 0.625″ LENGTH, 0.250 O.D.		4	(MOUSER) 534-1804
	4-40 TREAD HEX STANDOFF SCREWS		4	
PCB1	PCB, THS6032 EVM SLOP134		1	

† The values of these components are to be determined by the user in accordance with the application requirements.

2.2 THS6032 EVM Board Layouts

Board layout examples of the THS6032 EVM PCB are shown in the following illustrations. They are not to scale and appear here only as a reference.

Figure 2−1. THS6032 EVM Top Assembly
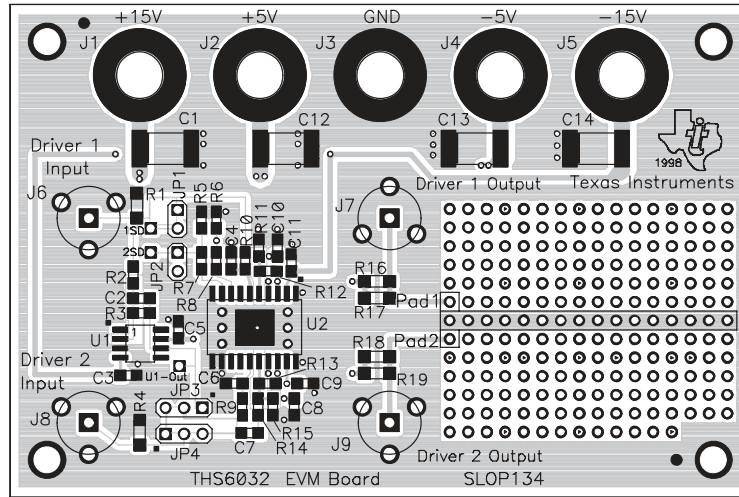
Figure 2−2. THS6032 EVM PC Board: Layer 1 — Top Side Layer
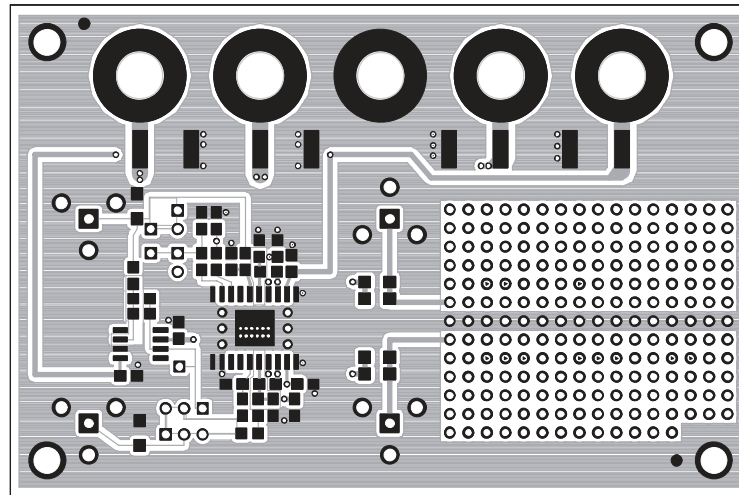
Figure 2−3. THS6032 EVM PC Board: Layer 2 — Back Side Ground Plane Layer

IMPORTANT NOTICE