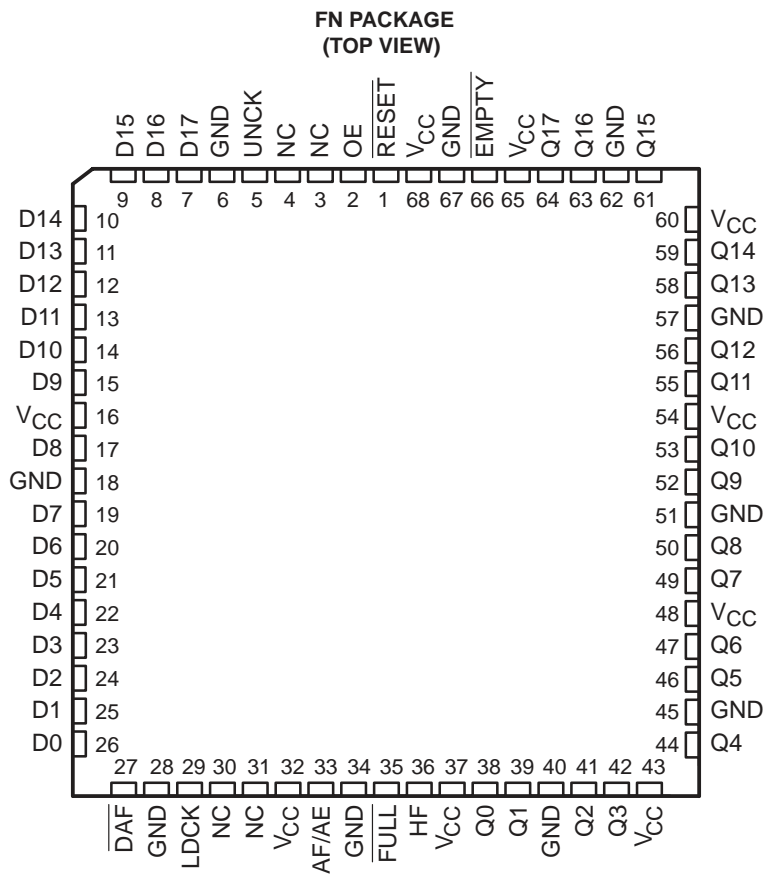


# SN74ACT7802

## 1024 × 18 STROBED FIRST-IN, FIRST-OUT MEMORY

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- Member of the Texas Instruments Widebus™ Family
- Low-Power Advanced CMOS Technology
- Load and Unload Clocks Can Be Asynchronous or Coincident
- 1024 Words × 18 Bits
- Programmable Almost-Full/Almost-Empty Flag
- Empty, Full, and Half-Full Flags
- Fast Access Times of 30 ns With a 50-pF Load
- Fall-Through Time Is 20 ns Typical
- Data Rates up to 40 MHz
- High-Output Drive for Direct Bus Interface
- 3-State Outputs
- Package Options Include 68-Pin (FN) and 80-Pin Thin Quad Flat (PN) Packages



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



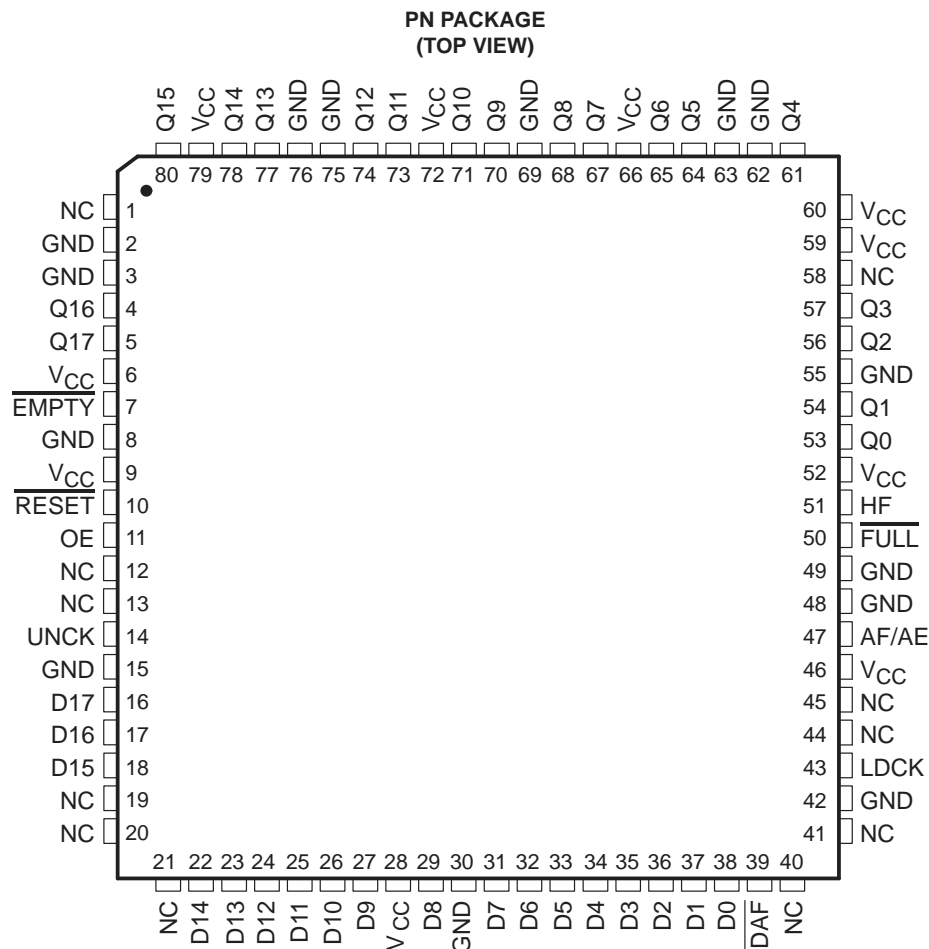
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### description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7802 is a 1024-word by 18-bit FIFO for high-speed applications. It processes data in a bit-parallel format at rates up to 40 MHz and access times of 30 ns.

Data is written into the FIFO memory on a low-to-high transition on the load-clock (LDCK) input and is read out on a low-to-high transition on the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, LDCK has no effect on the data in the memory; when the memory is empty, UNCK has no effect.

A low level on the reset ( $\overline{\text{RESET}}$ ) input resets the FIFO internal clock stack pointers and sets full ( $\overline{\text{FULL}}$ ) high, almost full/almost empty (AF/AE) high, half full (HF) low, and empty ( $\overline{\text{EMPTY}}$ ) low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The Q outputs are noninverting and are in the high-impedance state when the output-enable (OE) input is low.

When writing to the FIFO after a reset pulse or when the FIFO is empty, the first active transition on LDCK drives  $\overline{\text{EMPTY}}$  high and causes the first word written to the FIFO to appear on the Q outputs. An active transition on UNCK is not required to read the first word written to the FIFO. Each subsequent read from the FIFO requires an active transition on UNCK.

The SN74ACT7802 can be cascaded in the word-width direction but not in the word-depth direction.

The SN74ACT7802 is characterized for operation from 0°C to 70°C.



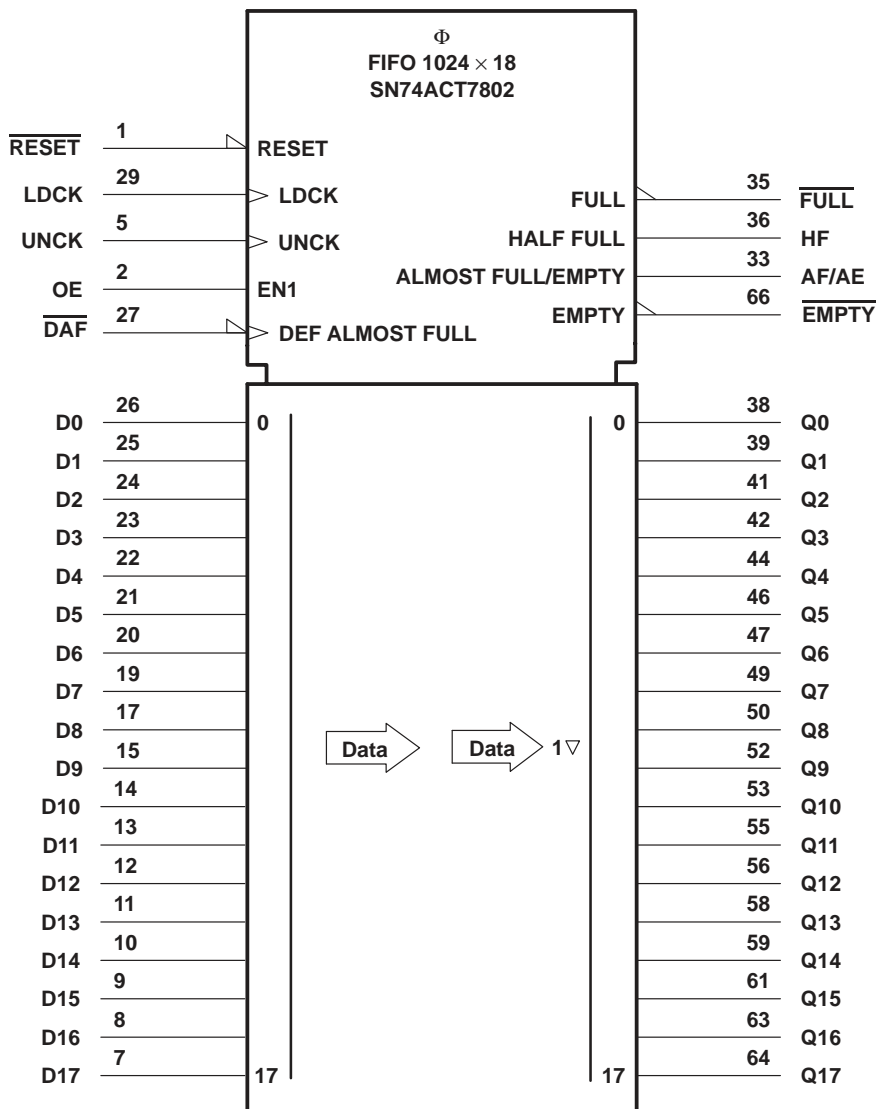
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logic symbol†



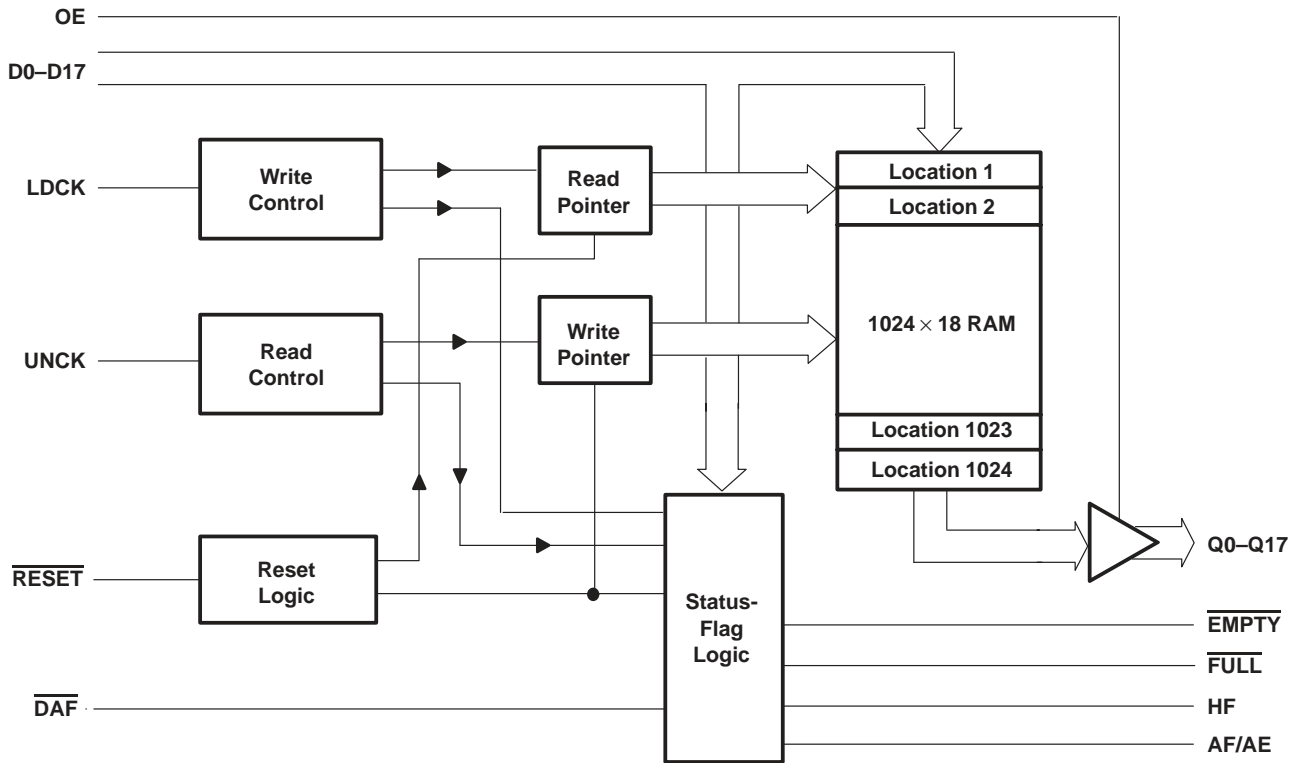
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the FN package.

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## 1024 × 18 STROBED FIRST-IN, FIRST-OUT MEMORY

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### functional block diagram



### Terminal Functions

TERMINAL NAME	NO.†	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AE, or the default value of 256 can be used for the almost-empty almost-full offset (X). AF/AE is high when memory contains X or fewer words or (1024 – X) or more words. AF/AE is high after reset.
$\overline{\text{DAF}}$	27	I	Define almost-full flag. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the AF/AE offset value (X). With DAF held low, a low pulse on RESET defines AF/AE using X.
D0–D17	7–15, 17, 19–26	I	18-bit data input port
$\overline{\text{EMPTY}}$	66	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	35	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	36	O	Half-full flag. HF is high when the FIFO memory contains 512 or more words. HF is low after reset.
LDCK	29	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
OE	2	I	Output enable. When OE is low, the data outputs are in the high-impedance state.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	18-bit data-output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	5	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

† Terminal numbers listed are for the FN package.



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### offset value values for AF/AE

The FIFO memory status is monitored by the  $\overline{\text{FULL}}$ ,  $\overline{\text{EMPTY}}$ , HF, and AF/AE flags. The  $\overline{\text{FULL}}$  output is low when the memory is full; the  $\overline{\text{EMPTY}}$  output is low when the memory is empty. The HF output is high when the memory contains 512 or more words and low when it contains fewer than 512 words. The level of the AF/AE flag is determined by both the number of words in the FIFO and a user-definable offset X. AF/AE is high when the FIFO is almost full or almost empty, i.e., when it contains X or fewer words or  $(1024 - X)$  or more words. The AF/AE offset value is either user-defined or the default value of 256; it is programmed during each reset cycle as follows:

#### user-defined X:

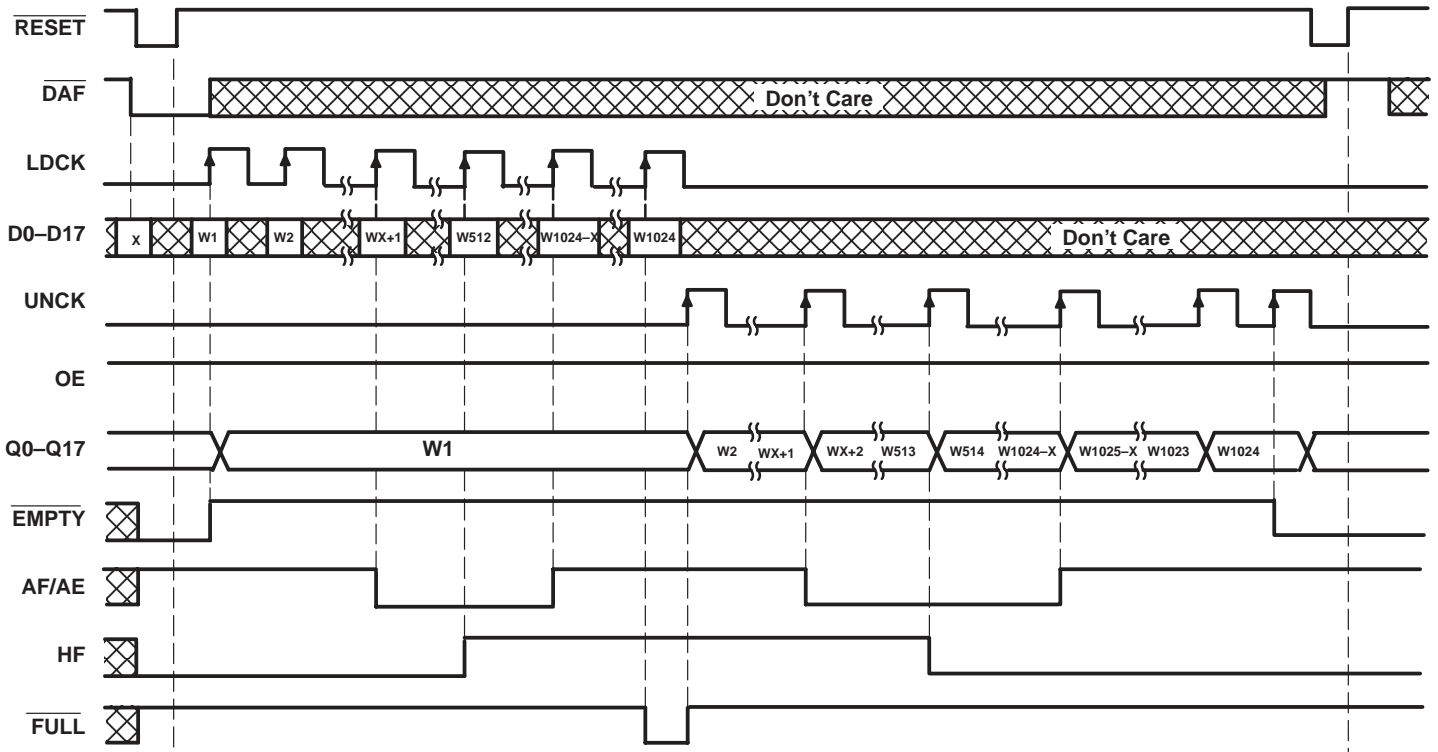
Take  $\overline{\text{DAF}}$  from high to low.

If  $\overline{\text{RESET}}$  is not already low, take  $\overline{\text{RESET}}$  low.

With  $\overline{\text{DAF}}$  held low, take  $\overline{\text{RESET}}$  high. This defines the AF/AE flag using X.

#### default X:

To redefine the AF/AE flag using the default value of  $X = 256$ , hold  $\overline{\text{DAF}}$  high during the reset cycle.



Define the AF/AE Offset Value (X)  
 Using the Data on D0 – D8

Define the AF/AE Offset Value (X)  
 Using the Default Value of 256

Figure 1. Write, Read, and Flag Timing Reference

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ .....	–0.5 V to 7 V
Voltage range applied to a disabled 3-state output .....	–0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): FN package .....	39°C/W
PN package .....	62°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions

		'ACT7802-25		'ACT7802-40		'ACT7802-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8		0.8	V
$I_{OH}$	High-level output current		–8		–8		–8	mA
$I_{OL}$	Low-level output current		16		16		16	mA
$T_A$	Operating free-air temperature	0	70	0	70	0	70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
$V_{OH}$	$V_{CC} = 4.5$ V,	$I_{OH} = -8$ mA	2.4			V
$V_{OL}$	$V_{CC} = 4.5$ V,	$I_{OL} = 16$ mA			0.5	V
$I_I$	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or 0			±5	μA
$I_{OZ}$	$V_{CC} = 5.5$ V,	$V_O = V_{CC}$ or 0			±5	μA
$I_{CC}^{\S}$	$V_I = V_{CC} - 0.2$ V or 0				400	μA
$\Delta I_{CC}^{\S}$	$V_{CC} = 5.5$ V,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			1	mA
$C_i$	$V_I = 0$ ,	$f = 1$ MHz		4		pF
$C_o$	$V_O = 0$ ,	$f = 1$ MHz		8		pF

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§  $I_{CC}$  tested with outputs open



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### timing requirements over recommended operating conditions (see Figures 1 and 2)

		'ACT7802-25		'ACT7802-40		'ACT7802-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	40		25		16.7		MHz
$t_w$	Pulse duration	LDCK high or low	10	14	20	ns		
		UNCK high or low	10	14	20			
		$\overline{\text{DAF}}$ high	10	10	10			
		$\overline{\text{RESET}}$ low	20	25	25			
$t_{\text{su}}$	Setup time	D0–D7 before LDCK $\uparrow$	4	5	5	ns		
		$\overline{\text{RESET}}$ inactive (high) before LDCK $\uparrow$	5	5	5			
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}\downarrow$	5	5	5			
		Define AF/AE: $\overline{\text{DAF}}\downarrow$ before $\overline{\text{RESET}}\uparrow$	7	7	7			
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}\uparrow$	5	5	5			
$t_h$	Hold time	D0–D7 after LDCK $\uparrow$	1	2	2	ns		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}\downarrow$	0	0	0			
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}\uparrow$	0	0	0			
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}\uparrow$	0	0	0			

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7802-25			'ACT7802-40		'ACT7802-60		UNIT
			MIN	TYP $\dagger$	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$	LDCK or UNCK		40			25		16.7		MHz
$t_{\text{pd}}$	LDCK $\uparrow$	Any Q	8	20	30	8	35	8	45	ns
	UNCK $\uparrow$		12		30	12	35	12	45	
$t_{\text{pd}}^\ddagger$	UNCK $\uparrow$	Any Q	21							ns
$t_{\text{PLH}}$	LDCK $\uparrow$	$\overline{\text{EMPTY}}$	4		18	4	20	4	22	ns
$t_{\text{PHL}}$	UNCK $\uparrow$	$\overline{\text{EMPTY}}$	2		18	2	20	2	22	ns
	$\overline{\text{RESET}}\downarrow$		2		18	2	20	2	22	
	LDCK $\uparrow$	$\overline{\text{FULL}}$	4		18	4	20	4	22	
$t_{\text{PLH}}$	UNCK $\uparrow$	$\overline{\text{FULL}}$	4		17	4	19	4	21	ns
	$\overline{\text{RESET}}\downarrow$		2		17	2	19	2	21	
$t_{\text{pd}}$	LDCK $\uparrow$	AF/AE	2		20	2	22	2	24	ns
	UNCK $\uparrow$		2		20	2	22	2	24	
$t_{\text{PLH}}$	$\overline{\text{RESET}}\downarrow$	AF/AE	2		17	2	19	2	21	ns
	LDCK $\uparrow$	HF	2		18	2	20	2	22	
$t_{\text{PHL}}$	UNCK $\uparrow$	HF	2		18	2	20	2	22	ns
	$\overline{\text{RESET}}\downarrow$		2		17	2	19	2	21	
$t_{\text{en}}$	OE	Any Q	2		12	2	14	2	16	ns
$t_{\text{dis}}$	OE	Any Q	2		14	2	16	2	18	ns

$\dagger$  All typical values are at  $V_{\text{CC}} = 5$  V,  $T_A = 25^\circ\text{C}$ .

$\ddagger$  This parameter is measured with  $C_L = 30$  pF (see Figure 3).

### operating characteristics, $V_{\text{CC}} = 5$ V, $T_A = 25^\circ\text{C}$

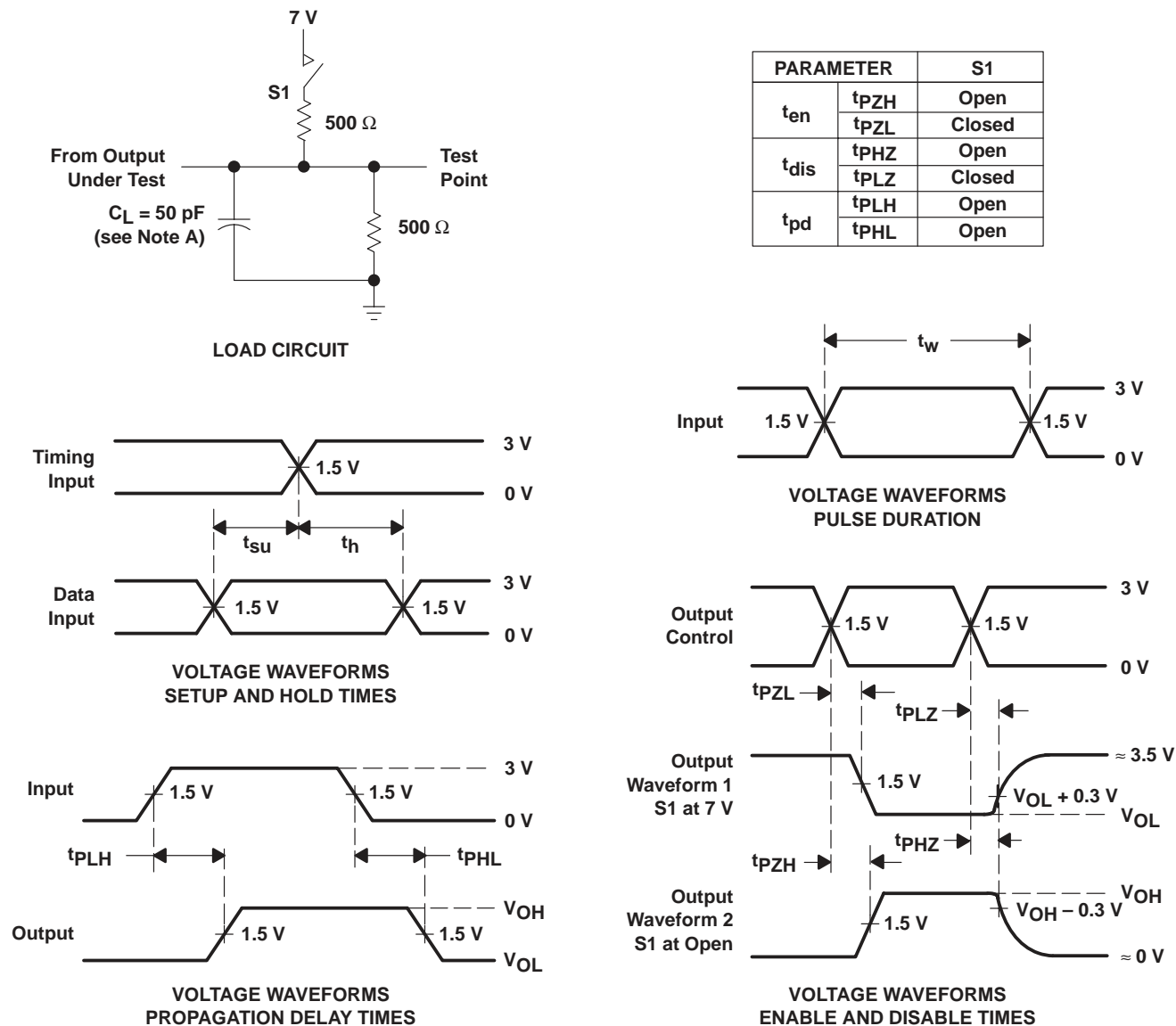
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance per channel $C_L = 50$ pF, $f = 5$ MHz	65	pF



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PARAMETER MEASUREMENT INFORMATION



NOTE A: CL includes probe and jig capacitance.

Figure 2. Load Circuit and Voltage Waveforms

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### TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME  
VS  
LOAD CAPACITANCE

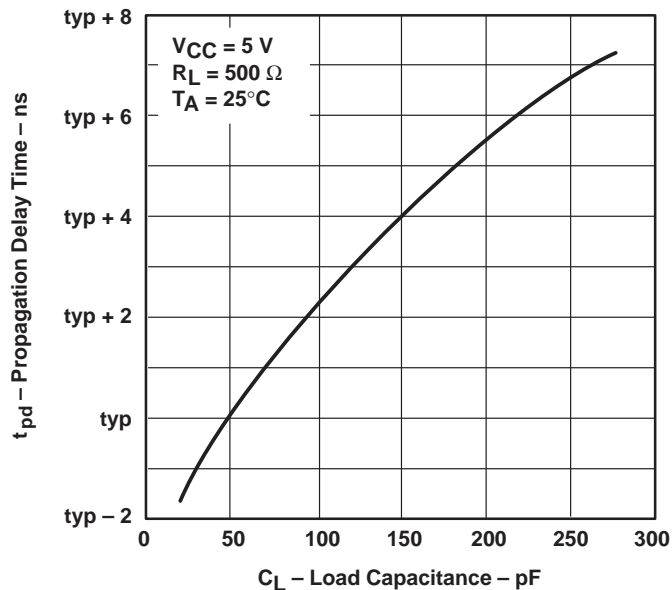


Figure 3

POWER DISSIPATION CAPACITANCE  
VS  
SUPPLY VOLTAGE

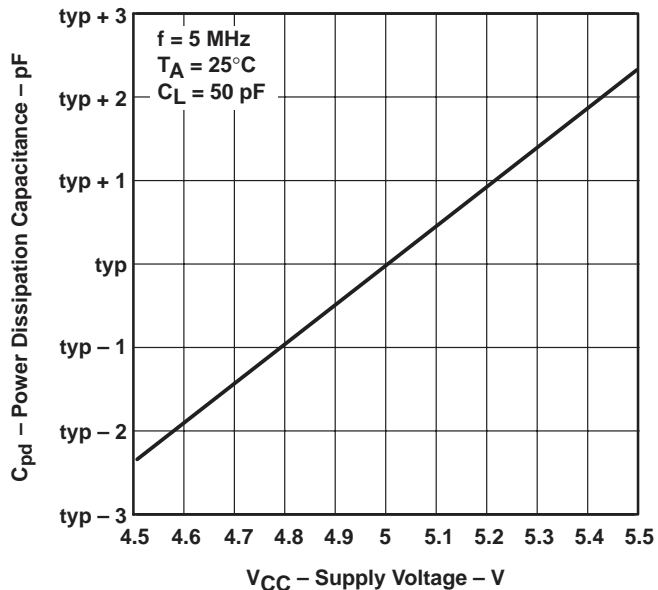
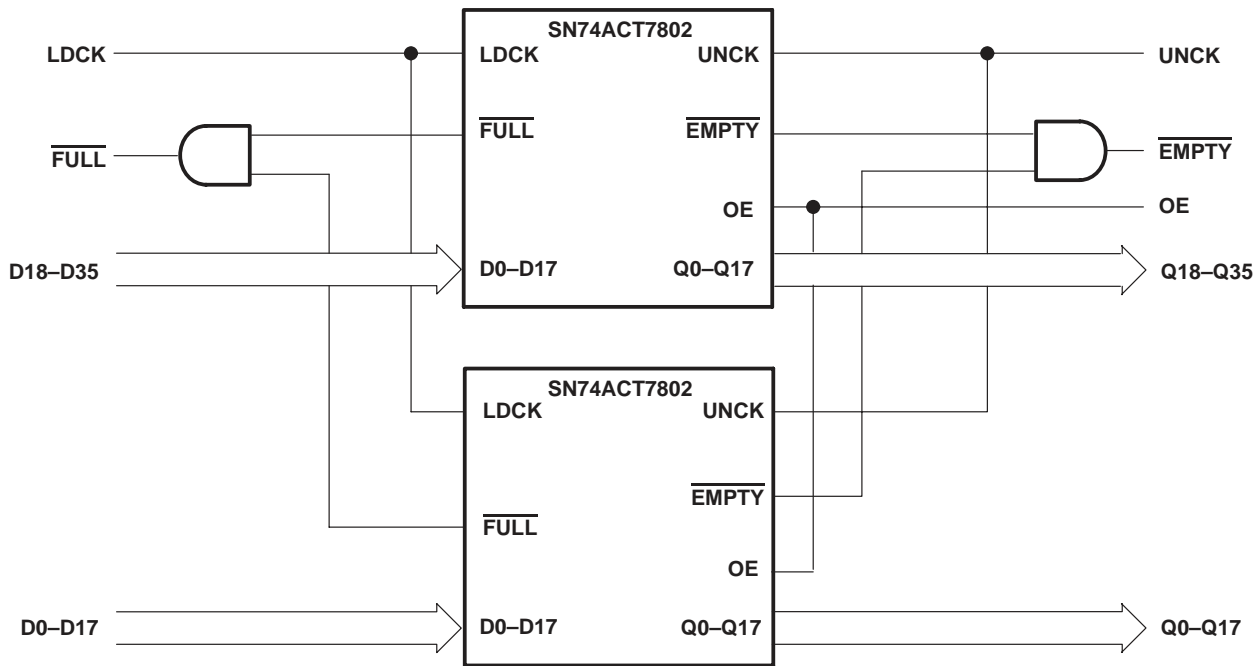


Figure 4

**APPLICATION INFORMATION**



**Figure 5. Word-Width Expansion: 1024 × 36 Bit**

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