10A, 24V, 600kHz Step-Down Converter with Synchronous Gate Driver

General Description

The RT7259 is a synchronous step-down DC/DC converter with an integrated high side internal power MOSFET and a gate driver for a low side external power MOSFET. It can deliver up to 10A output current from a 4.5V to 24V input supply. The RT7259's current mode architecture allows the transient response to be optimized over a wider input voltage and load range. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT7259 is synchronizable to an external clock with frequency ranging from 300kHz to 1.5MHz.

The RT7259 is available in WDFN-14L 4x3 package.

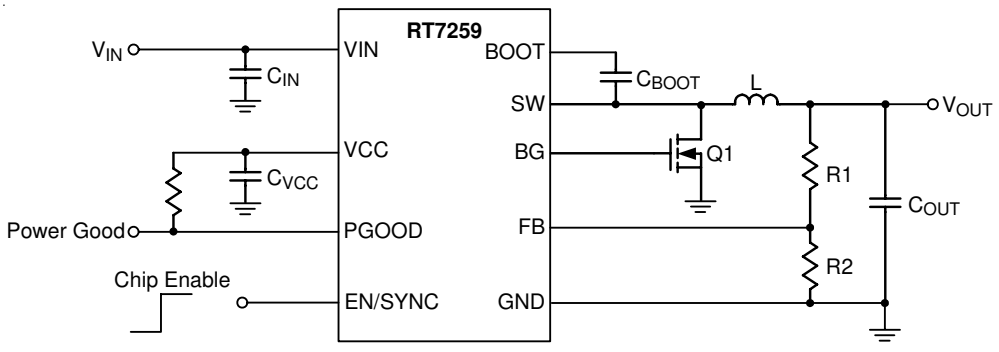
Applications

- Point of Load Regulator in Distributed Power System
- Digital Set top Boxes
- Personal Digital Recorders
- Broadband Communications
- Flat Panel TVs and Monitors

Features

- **4.5V to 24V Input Voltage Range**
- **10A Output Current**
- **45mΩ Internal High Side N-MOSFET**
- **Current Mode Control**
- **600kHz Switching Frequency**
- **Adjustable Output from 0.808V to 15V**
- **Up to 95% Efficiency**
- **Internal Compensation**
- **Stable with Ceramic Capacitors**
- **Synchronous External Clock : 300kHz to 1.5MHz**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection**
- **Power Good Indicator**
- **Thermal Shutdown Protection**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



Ordering Information

RT7259□□

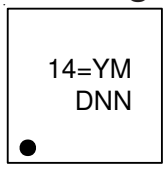
- Package Type
  QW : WDFN-14L 4x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

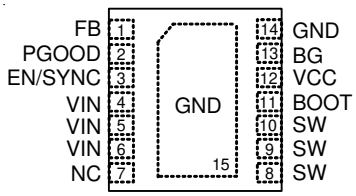


14= : Product Code

YMDNN : Date Code

Pin Configurations

(TOP VIEW)

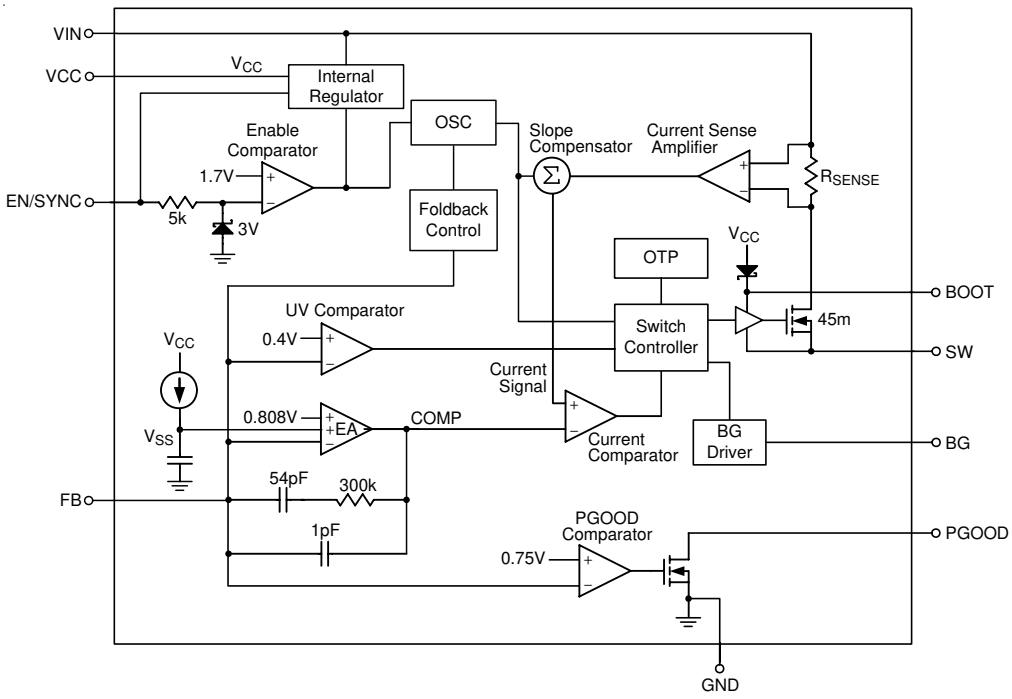


WDFN-14L 4x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Feedback Input. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an external resistive divider. The feedback reference voltage is 0.808V typically.
2	PGOOD	Power Good Indicator with Open Drain. A 100kΩ pull-high resistor is needed. The output of this pin is pulled to low when the FB is lower than 0.75V; otherwise it is high impedance.
3	EN/SYNC	Enable or External Frequency Synchronization Input. A logic-high (2V < EN < 5.5V) enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 3μA. For external frequency synchronization operation, the available frequency range is from 300kHz to 1.5MHz.
4, 5, 6	VIN	Power Input. The available input voltage range is from 4.5V to 24V. A 22μF or larger input capacitor is needed to reduce voltage spikes at the input.
7	NC	No Internal Connection.
8, 9, 10	SW	Switching Node. Output of the internal high side MOSFET. Connect this pin to external low side N-MOSFET, inductor and bootstrap capacitor.
11	BOOT	Bootstrap for High side Gate Driver. Connect a 1μF ceramic capacitor between the BOOT pin and SW pin.
12	VCC	BG Driver Bias Supply. Decouple with a 1μF X5R/X7R ceramic capacitor between the VCC pin and GND.
13	BG	Gate Driver Output. Connect this pin to the gate of the external low side N-MOSFET.
14, 15 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.

Function Block Diagram



Operation

The RT7259 is a synchronous high voltage Buck Converter that can support the input voltage range from 4.5V to 24V and the output current can be up to 10A. The RT7259 uses a constant frequency, current mode architecture. In normal operation, the high side N-MOSFET is turned on when the Switch Controller is set by the oscillator (OSC) and is turned off when the current comparator resets the Switch Controller. While the N-MOSFET is turned off, the external low side N-MOSFET is turned on by BG Driver with 5V driving voltage from Internal Regulator (V_{CC}) until next cycle begins.

High side MOSFET peak current is measured by internal R_{SENSE}. The Current Signal is where Slope Compensator works together with sensing voltage of R_{SENSE}. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.808V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the COMP voltage then rises to allow higher inductor current to match the load current.

UV Comparator : If the feedback voltage (V_{FB}) is lower than threshold voltage 0.4V, the UV Comparator's output will go high and the Switch Controller will turn off the high side MOSFET. The output under voltage protection is designed to operate in Hiccup mode.

Oscillator (OSC) : The internal oscillator runs at nominal frequency 600kHz and can be synchronized by an external clock in the range between 300kHz and 1.5MHz from EN/SYNC pin.

PGOOD Comparator : When the feedback voltage (V_{FB}) is higher than threshold voltage 0.75V, the PGOOD open drain output will be high impedance.

Enable Comparator : Internal 5kΩ resistor and Zener diode are used to clamp the input signal to 3V. A 1.7V reference voltage is for EN logic-high threshold voltage. The EN pin can be connected to VIN through a 100kΩ resistor for automatic startup.

Foldback Control : When V_{FB} is lower than 0.7V, the oscillation frequency will be proportional to the feedback voltage.

Soft-Start (SS) : An internal current source charges an internal capacitor to build the soft-start ramp voltage (V_{SS}). The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 2ms.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 26V
- Switching Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
  SW (AC) < 20ns ---------- –5V to 30V
- BOOT to SW ---------- –0.3V to 6V
- All Other Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-14L 4x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  WDFN-14L 4x3, θ_{JA} ---------- 60°C/W
  WDFN-14L 4x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 4.5V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current			V_{EN} = 0V	--	1	--	μA
Supply Current			V_{EN} = 3V, V_{FB} = 1V	--	0.9	--	mA
Reference Voltage		V_{REF}	4.5V ≤ V_{IN} ≤ 24V	0.796	0.808	0.82	V
Feedback Current		I_{FB}	V_{FB} = 0.8V	--	10	--	nA
High Side Switch On Resistance		$R_{DS(ON)}$		--	45	--	mΩ
High Side Switch Current Limit			BOOT – SW = 4.8V	--	16	--	A
Oscillation Frequency		f_{OSC1}		--	600	--	kHz
Short Circuit Oscillation Frequency		f_{OSC2}	V_{FB} = 0V	--	190	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.6V	--	90	--	%
Minimum On-Time		t_{ON}	V_{FB} = 1V	--	100	--	ns
Input Under Voltage Lockout Threshold		V_{UVLO}		4	4.2	4.4	V
Input Under Voltage Lockout Threshold Hysteresis		ΔV_{UVLO}		--	400	--	mV
EN Threshold Voltage	Logic-High	V_{IH}		2	--	5.5	V
	Logic-Low	V_{IL}		--	--	0.4	
Sync Frequency Range		f_{Sync}		0.3	--	1.5	MHz
EN Turn-Off Delay		t_{OFF}		--	10	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pull Low Current		V_{EN} = 2V	--	1	--	μA
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Power Good Threshold Rising			--	0.75	--	V
Power Good Threshold Hysteresis			--	40	--	mV
Power Good Pin Level		PGOOD Sink 10mA	--	--	0.125	V
BG Driver Bias Supply Voltage	V_{CC}		4.5	5	--	V
Gate Driver Sink Impedance	R_{Sink}		--	0.9	--	Ω
Gate Driver Source Impedance	R_{Source}		--	3.3	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

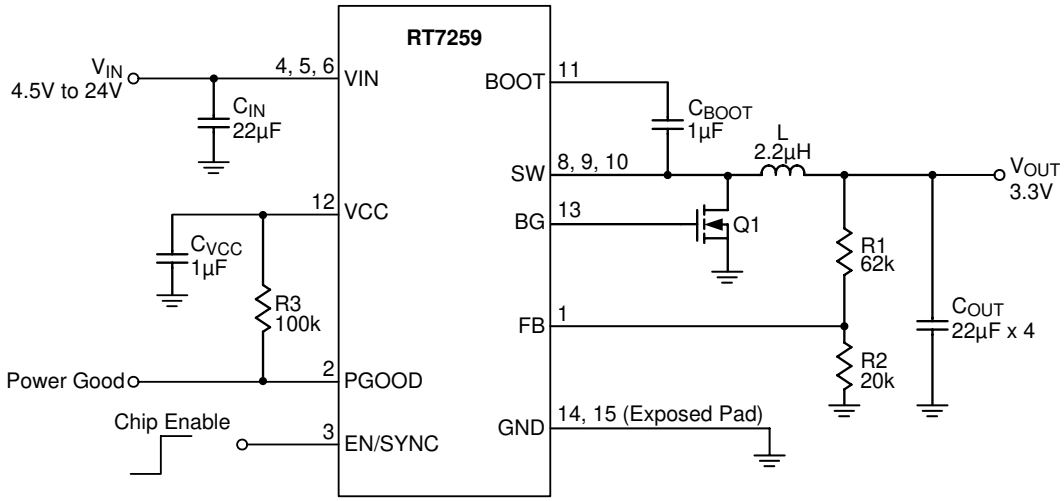
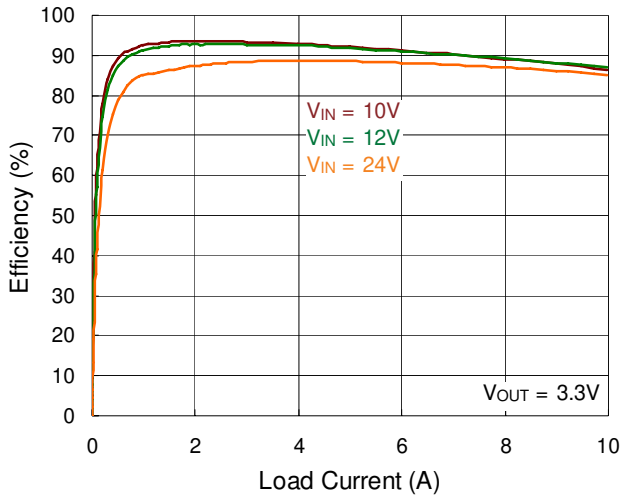


Table 1. Recommended Component Selection

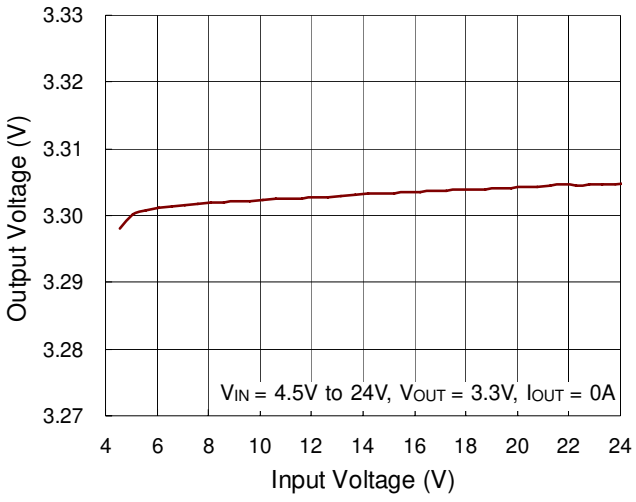
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
1.2	62	127	1.5	22µF x 4
1.8	70	57	1.5	22µF x 4
2.5	69	33	2.2	22µF x 4
3.3	62	20	2.2	22µF x 4
5	93	18	2.8	22µF x 4
8	120	13.5	3.6	22µF x 4

Typical Operating Characteristics

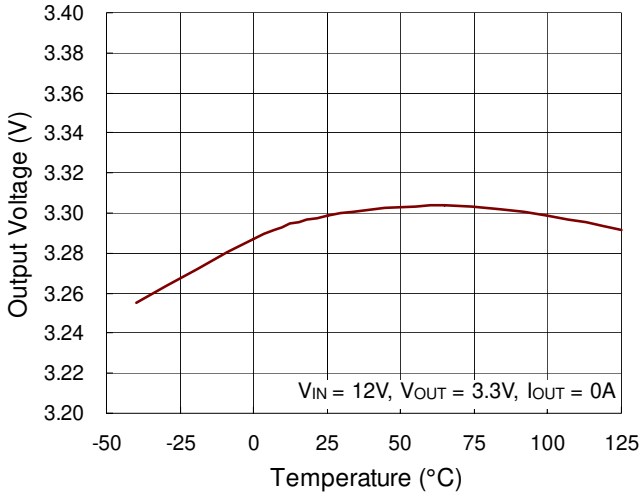
Efficiency vs. Load Current



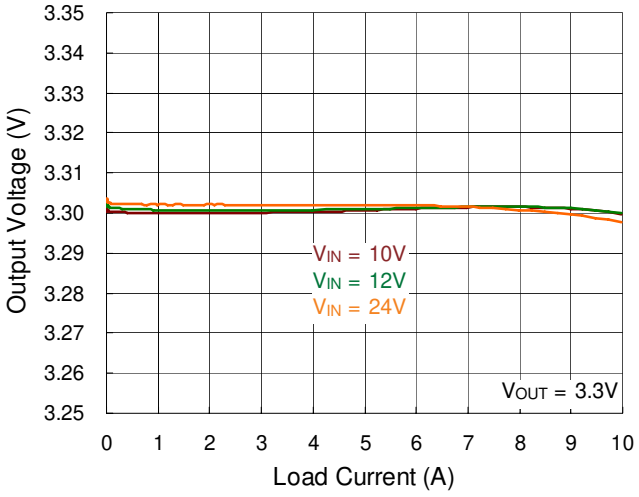
Output Voltage vs. Input Voltage



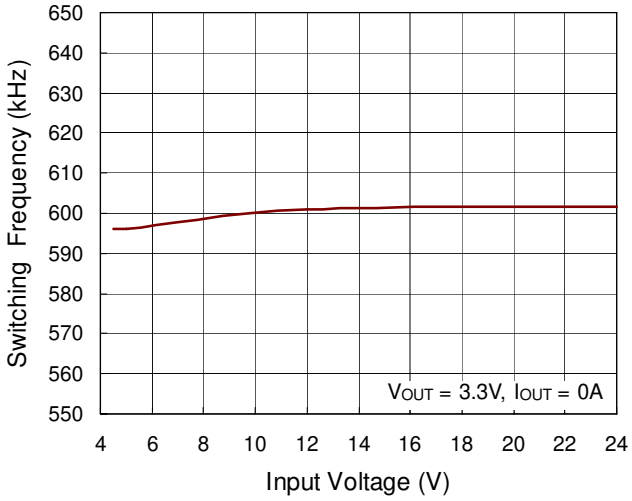
Output Voltage vs. Temperature



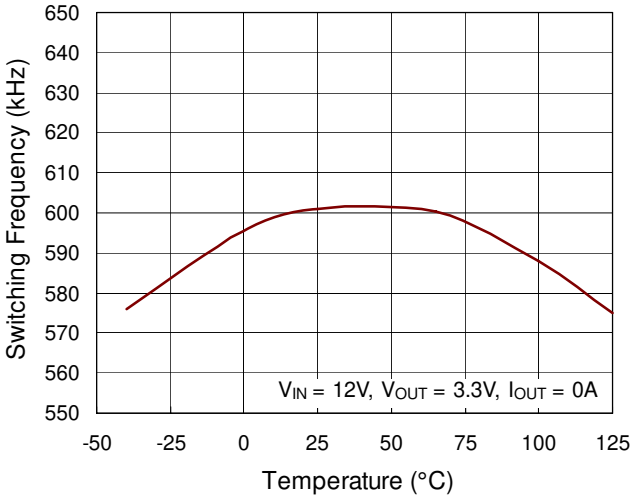
Output Voltage vs. Load Current



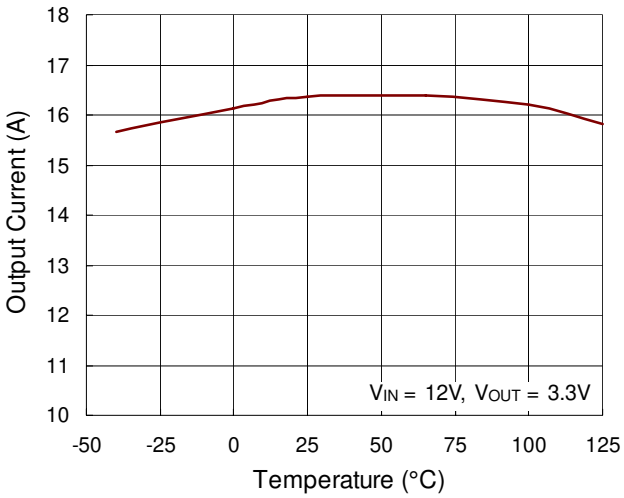
Switching Frequency vs. Input Voltage



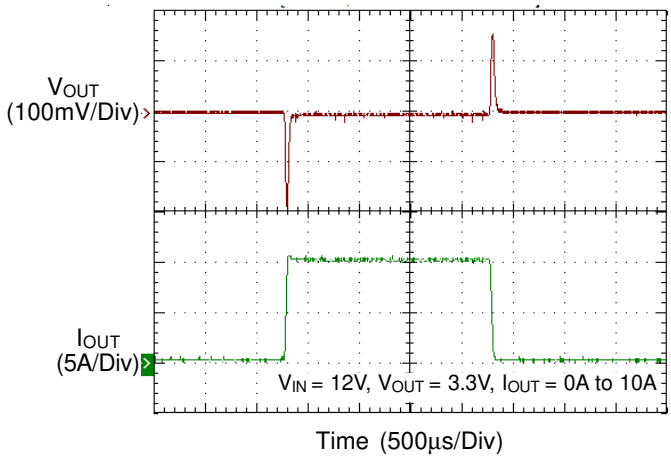
Switching Frequency vs. Temperature



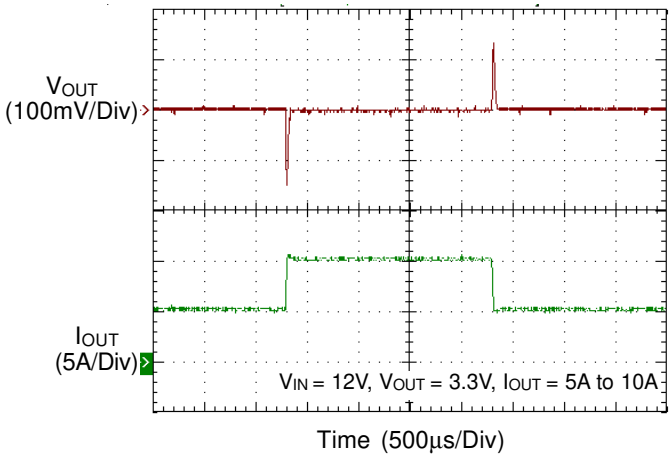
Current Limit vs. Temperature



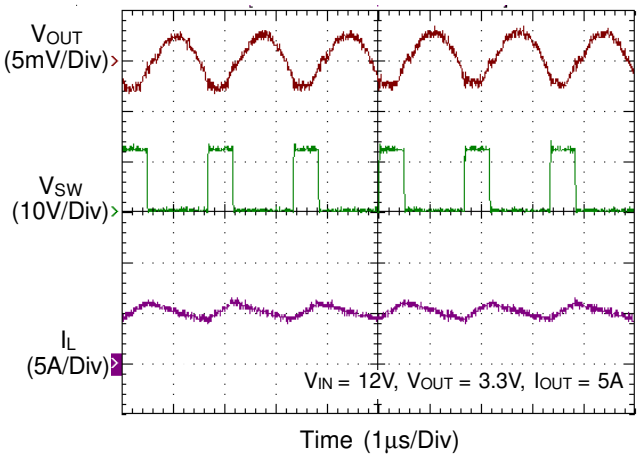
Load Transient Response



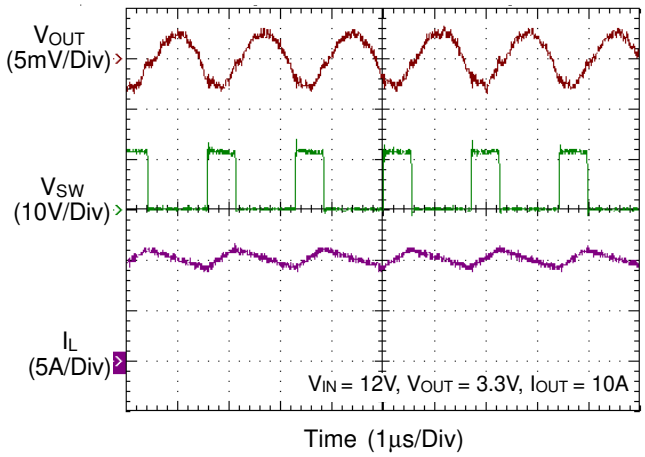
Load Transient Response



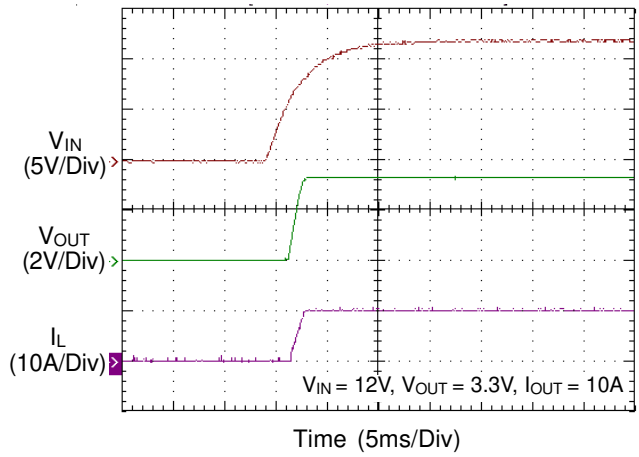
Output Ripple Voltage



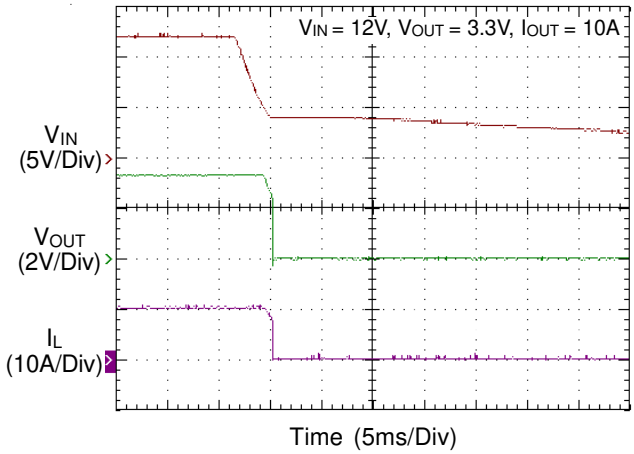
Output Ripple Voltage



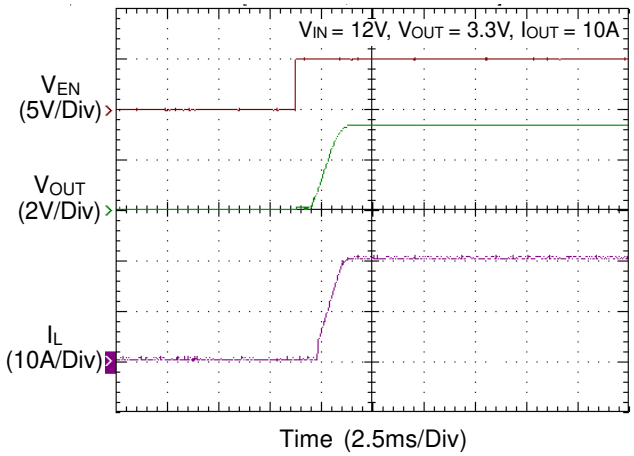
Power On from VIN



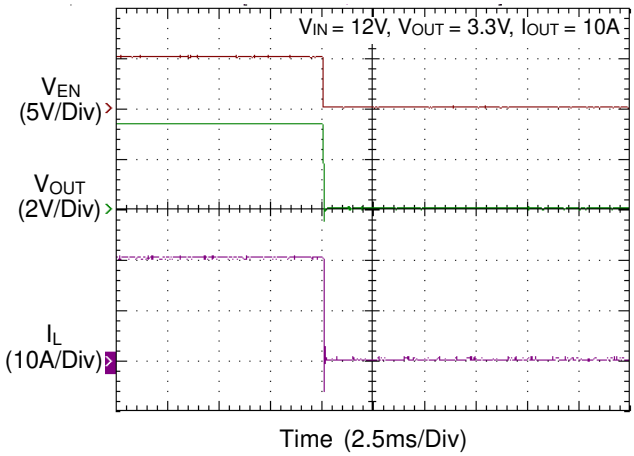
Power Off from VIN



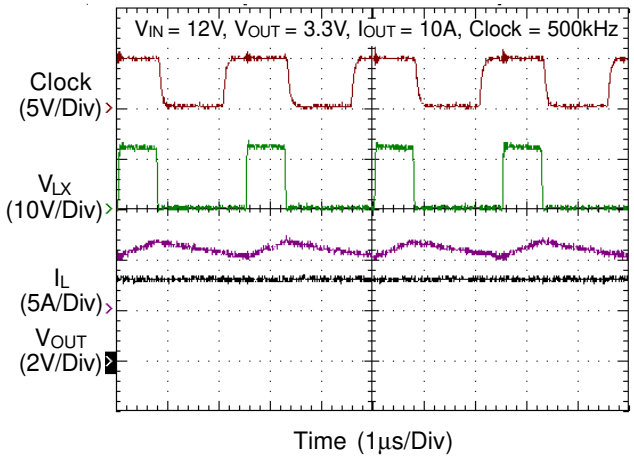
Power On from EN



Power Off from EN



External SYNC



Application Information

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

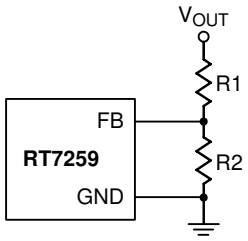


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the feedback voltage (0.808V typ.).

External Bootstrap Diode

Connect a 1μF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7259. Note that the external boot voltage must be lower than 5.5V.

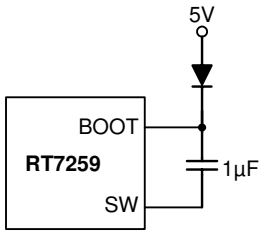


Figure 2. External Bootstrap Diode

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT7259 quiescent current drops to lower than 3μA. Driving the EN pin high (2V < EN < 5.5V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 3).

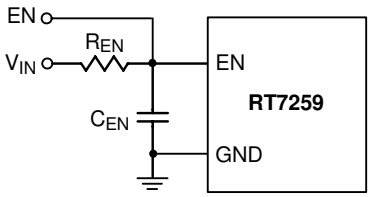


Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin, as shown in Figure 4. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} pin and the EN pin. MOSFET Q2 will be under logic control to pull down the EN pin.

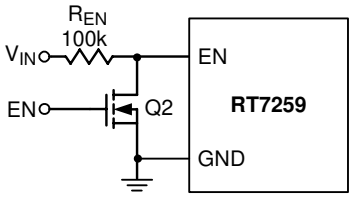


Figure 4. Digital Enable Control Circuit

The chip starts to operate when V_{IN} rises to 4.2V (UVLO threshold). During the V_{IN} rising period, if an 8V output voltage is set, V_{IN} is lower than the V_{OUT} target value and it may cause the chip to shut down. To prevent this situation, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust enable threshold, as shown in Figure 5. For example, the setting V_{OUT} is 8V and V_{IN} is from 0V to 12V, when V_{IN} is higher than 10V, the chip is triggered to enable the converter. Assume R_{EN1} = 50kΩ. Then,

$$R_{EN2} = \frac{(R_{EN1} \times V_{EN\_T})}{(V_{IN\_S} - V_{EN\_T})}$$

where V_{EN_T} is the enable comparator's logic-high reference threshold voltage (1.7V) and V_{IN_S} is the target turn on input voltage (10V in this example). According to the equation, the suggested resistor R_{EN2} is 10.2kΩ.

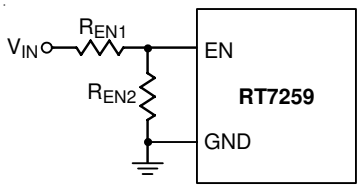


Figure 5. Resistor Divider for Lockout Threshold Setting

Soft-Start

The RT7259 provides soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. An internal current source charges an internal capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 2ms.

Operating Frequency and Synchronization

The internal oscillator runs at 600kHz (typ.) when the EN/SYNC pin is at logic-high level (>2V). If the EN pin is pulled to low-level for 10μs above, the IC will shut down. The RT7259 can be synchronized with an external clock ranging from 300kHz to 1.5MHz applied to the EN/SYNC pin. The external clock duty cycle must be from 10% to 90%.

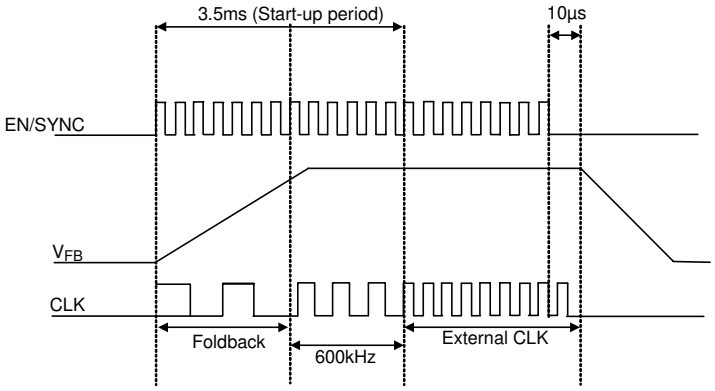


Figure 6. Startup Sequence Using External Sync Clock

Figure 6 shows the synchronization operation in startup period. When the EN/SYNC is triggered by an external clock, the RT7259 enters soft-start phase and the output voltage starts to rise. When V_{FB} is lower than 0.7V, the oscillation frequency will be proportional to the feedback voltage. With higher V_{FB}, the switching frequency is relatively higher. After startup period about 3.5ms, the IC operates with the same frequency as the external clock.

Over Temperature Protection

The RT7259 features an Over Temperature Protection (OTP) circuitry to prevent from overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

Under Voltage Protection

For the RT7259, it provides Hiccup Mode Under Voltage Protection (UVP). When the V_{FB} voltage drops below 0.4V, the UVP function will be triggered to shut down switching operation. If the UV condition remains for a period, the RT7259 will retry every 2ms. When the UV condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

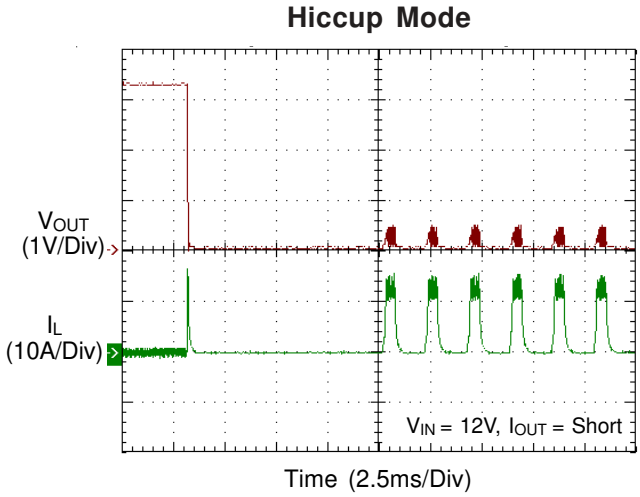


Figure 7. Hiccup Mode Under Voltage Protection

Duty Cycle Limitation

The RT7259 has a maximum duty cycle 90%. The minimum input voltage is determined by the maximum duty cycle and its minimum operating voltage 4.5V. The voltage drops of high side MOSFET and low side MOSFET also must be considered for the minimum input voltage.

The minimum duty cycle can be calculated by the following equation :

Duty Cycle(min) = f_{SW} x t_{ON}(min)

where fsw is the switching frequency, t_{ON} (min) is the minimum switch on time (100ns). This equation shows that the minimum duty cycle increases when the switching frequency is increased. Therefore, slower switching frequency is necessary to achieve high V_{IN}/V_{OUT} ratio application.

External N-MOSFET Selection

The RT7259 is designed to operate using an external low side N-MOSFET. Important parameters for the power MOSFETs are the breakdown voltage (BV_{DSS}), threshold voltage (V_{GS_TH}), on-resistance ($R_{DS(ON)}$), total gate charge (Qg) and maximum current ($I_{D(MAX)}$). The gate driver voltage is from internal regulator (5V, V_{CC}). Therefore logic level N-MOSFET must be used in the RT7259 application. The total gate charge (Qg) must be less than 50nC, lower Qg characteristics results in lower power losses. Drain-source on-resistance ($R_{DS(ON)}$) should be as small as possible, less than 30mΩ is desirable. Lower $R_{DS(ON)}$ results in higher efficiency.

Table 2. External N-MOSFET Selection

Part No.	Manufacture
Si7114	Vishay
A04474	ALPHA & OMEGA
FDS6670AS	Fairchild
IRF7821	International Rectifier

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can reduce voltage. For the highest efficiency operation, however, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (cause a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 3 for the inductor selection reference.

Table 3. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
Zenithtek	ZPWM	10 x 10 x 4
		6 x 6 x 3
WE	74477	10 x 10 x 4
TAIYOYUDEN	NR8040	8 x 10 x 4

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

Table 4. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C_{IN}	MURATA	GRM31CR61E106K	10	1206
C_{IN}	TDK	C3225X5R1E106K	10	1206
C_{IN}	TAIYO YUDEN	TMK316BJ106ML	10	1206
C_{OUT}	MURATA	GRM31CR60J476M	47	1206
C_{OUT}	TDK	C3225X5R0J476M	47	1210
C_{OUT}	MURATA	GRM32ER71C226M	22	1210
C_{OUT}	TDK	C3225X5R1C22M	22	1210

For the input capacitor, two 10μF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to Table 4 for more details.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. This ringing can couple to the output and be mistaken. A sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step load change. When a step load occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} x ESR also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT7259, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-14L 4x3 package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board.

The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for WDFN-14L 4x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT7259 package, the derating curves in Figure 8 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

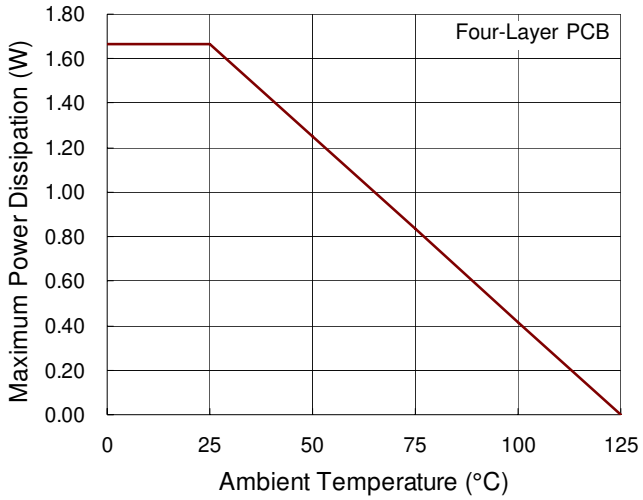


Figure 8. Derating Curves for RT7259 Package

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT7259.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT7259.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 9 for reference.

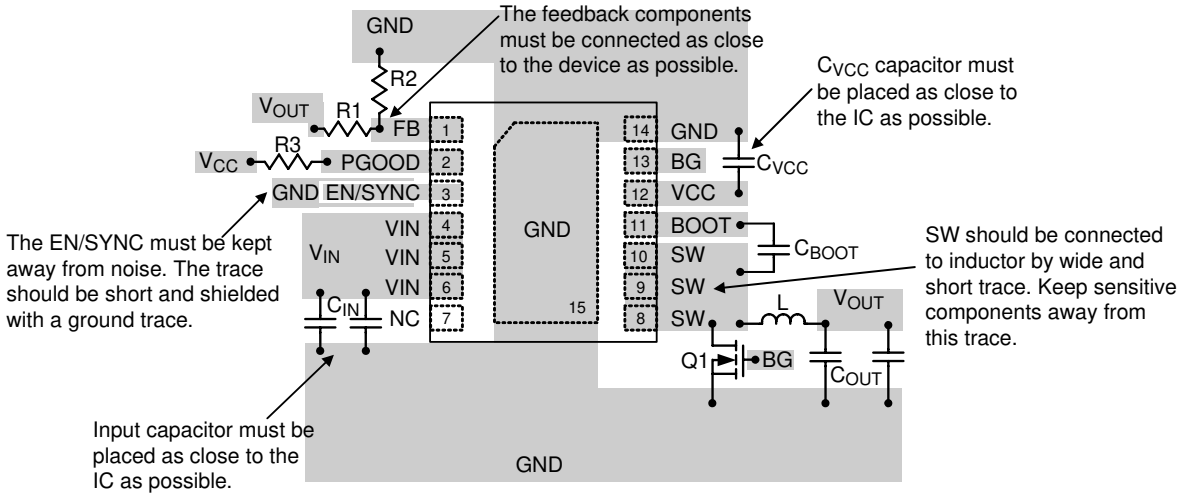
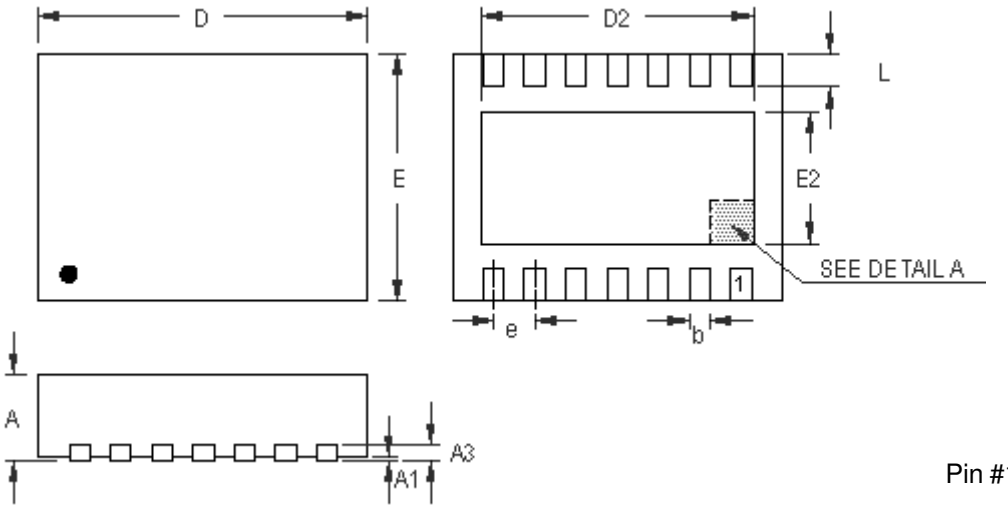
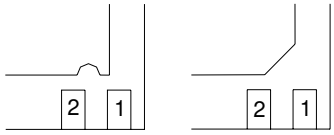


Figure 9. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	3.250	3.350	0.128	0.132
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 14L DFN 4x3 Package

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