

## FEATURES

- 9-bit latch
- Extended 100E VEE range of -4.2V to -5.5V
- Parity detection/generation
- 800ps max. D to Output
- Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with Motorola MC10E/100E175
- Available in 28-pin PLCC package

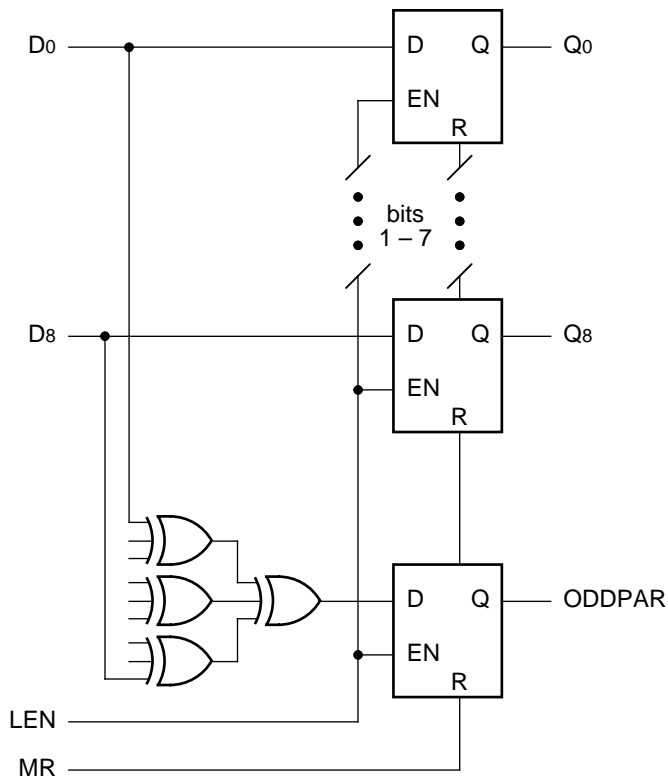
## DESCRIPTION

The SY10/100E175 are 9-bit latches. They also feature a tenth latched output (ODDPAR) which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

The E175 can also be used to generate byte parity by using D8 as the parity-type select (L = even parity, H = odd parity) and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

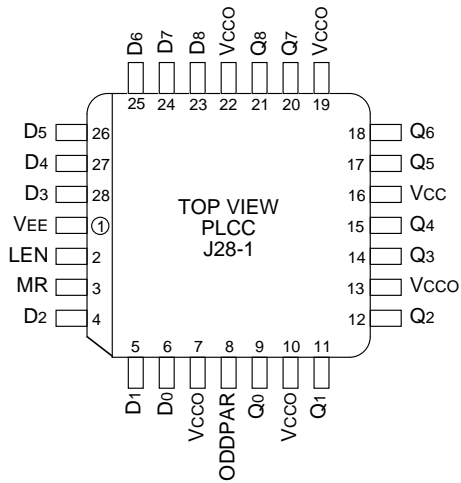
## BLOCK DIAGRAM



## PIN NAMES

Pin	Function
D0 – D8	Data Inputs
LEN	Latch Enable
MR	Master Reset
Q0 – Q8	Data Outputs
ODDPAR	Parity Output
Vcco	Vcc to Output

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E175JC	J28-1	Commercial	SY10E175JC	Sn-Pb
SY10E175JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E175JC	Sn-Pb
SY100E175JC	J28-1	Commercial	SY100E175JC	Sn-Pb
SY100E175JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E175JC	Sn-Pb
SY10E175JZ <sup>(3)</sup>	J28-1	Commercial	SY10E175JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E175JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E175JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E175JZ <sup>(3)</sup>	J28-1	Commercial	SY100E175JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E175JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E175JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**TRUTH TABLE**

D	LEN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of D <sub>n</sub> HIGH
L	L	L	L	H if odd no. of D <sub>n</sub> HIGH
X	H	L	Q <sub>0</sub>	Q <sub>0</sub>
X	X	H	L	L

**DC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—	
I <sub>EE</sub>	Power Supply Current	—	110	132	—	110	132	—	110	132	mA	—	
		10E	—	110	132	—	110	132	—	110			132
		100E	—	110	132	—	110	132	—	127			152

**AC ELECTRICAL CHARACTERISTICS**

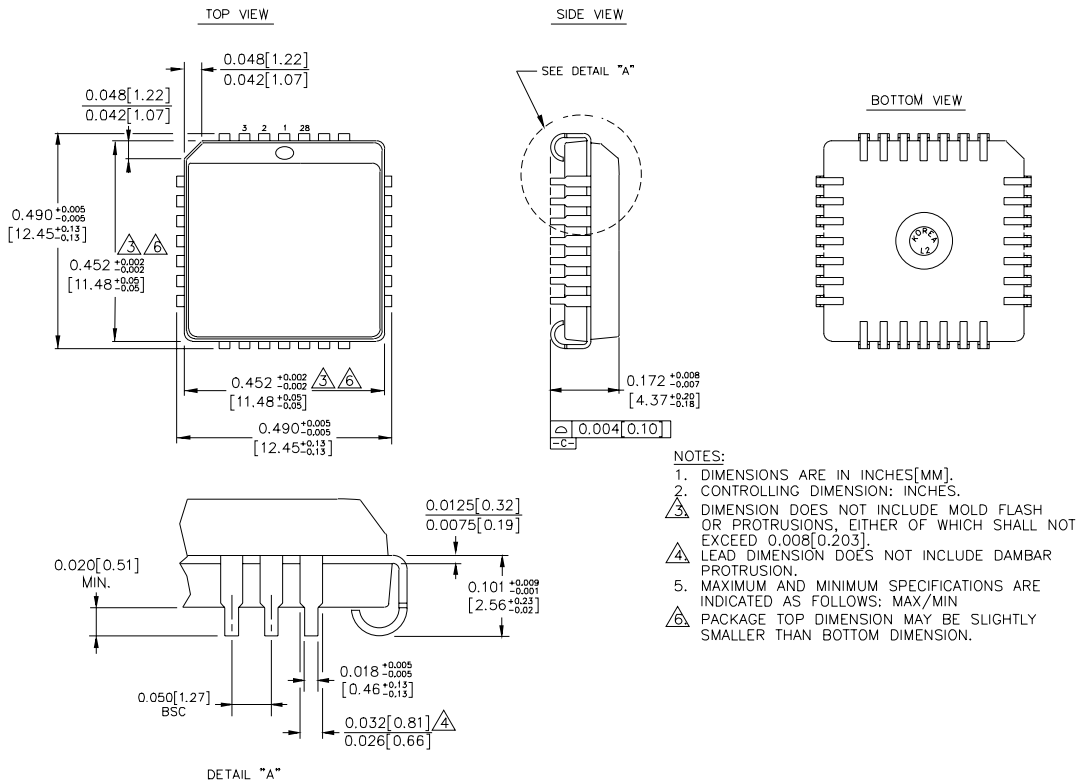
VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>PD</sub>	Propagation Delay to Output										ps	—
	D to Q	450	600	800	450	600	800	450	600	800		
	D to ODDPAR	850	1150	1450	850	1150	1450	850	1150	1450		
	LEN to Q	525	700	900	525	700	900	525	700	900		
	LEN to ODDPAR	525	700	900	525	700	900	525	700	900		
	MR to Q (t <sub>PHL</sub> )	525	700	900	525	700	900	525	700	900		
t <sub>S</sub>	Set-up Time										ps	—
	D (Q)	275	100	—	275	—	—	275	—	—		
t <sub>H</sub>	D (ODDPAR)	900	700	—	900	—	—	900	—	—	ps	—
	Hold Time											
t <sub>H</sub>	D (Q)	175	-100	—	175	—	—	175	—	—	ps	—
	D (ODDPAR)	-300	-700	—	-300	—	—	-300	—	—		
t <sub>RR</sub>	Reset Recovery Time	850	600	—	850	600	—	850	600	—	ps	—
t <sub>skew</sub>	Within-Device Skew										ps	1
	LEN, MR	—	75	—	—	75	—	—	75	—		
	D to Q	—	75	—	—	75	—	—	75	—		
t <sub>r</sub>	D to ODDPAR	—	200	—	—	200	—	—	200	—	ps	—
	Rise/Fall Times	300	500	800	300	500	800	300	500	800		
t <sub>f</sub>	20–80%											

**Note:**

1. Within-device skew is defined as identical transitions on similar paths through a device.

**28-PIN PLCC (J28-1)**



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