



12-Bit DACs with 32-Channel Sample-and-Hold Outputs

General Description

The MAX5331/MAX5332/MAX5333 are 12-bit digital-to-analog converters (DACs) with 32 sample-and-hold (SHA) outputs for applications where a high number of programmable voltages are required. These devices include a clock oscillator and a sequencer that updates the DAC with codes from an internal SRAM. No external components are required to set offset and gain.

The MAX5331/MAX5332/MAX5333 feature a -4.5V to +9.2V output voltage range. Other features include a 3.2mV/step resolution, with output linearity error, typically 0.03% of full-scale range (FSR). The 100kHz refresh rate updates each SHA every 320 μ s, resulting in negligible output droop. Remote ground sensing allows the outputs to be referenced to the local ground of a separate device.

These devices are controlled through a 20MHz SPI™/QSPI™/MICROWIRE™-compatible 3-wire serial interface. Immediate update mode allows any channel's output to be updated within 20 μ s. Burst mode allows multiple values to be loaded into memory in a single, high-speed data burst. All channels are updated within 330 μ s of data being loaded.

Each device features an output clamp and output resistors for filtering. The MAX5331 features a 50 Ω output impedance and is capable of driving up to 250pF of output capacitance. The MAX5332 features a 500 Ω output impedance and is capable of driving up to 10nF of output capacitance. The MAX5333 features a 1k Ω output impedance and is capable of driving up to 10nF of output capacitance.

The MAX5331/MAX5332/MAX5333 are available in 12mm x 12mm, 64-pin TQFP and 10mm x 10mm, 68-pin thin QFN packages.

Applications

MEMS Mirror Servo Control
Industrial Process Control
Automatic Test Equipment
Instrumentation

Features

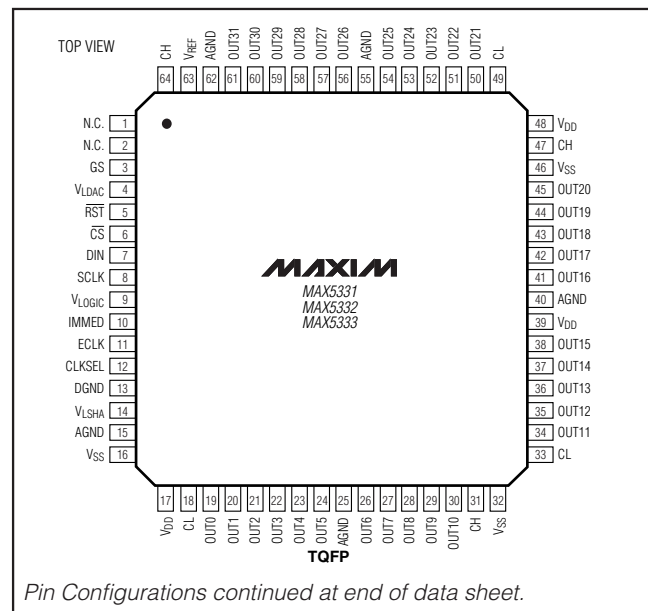
- ◆ Integrated 12-Bit DAC and 32-Channel SHA with SRAM and Sequencer
- ◆ 32 Voltage Outputs
- ◆ 0.03% FSR (typ) Output Linearity
- ◆ 3.2mV Output Resolution
- ◆ Flexible Output Voltage Range
- ◆ Remote Ground Sensing
- ◆ Fast Sequential Loading: 1.3 μ s per Register
- ◆ Burst- and Immediate-Mode Addressing
- ◆ No External Components Required for Setting Gain and Offset
- ◆ Integrated Output Clamp Diodes
- ◆ Three Output-Impedance Options
MAX5331 (50 Ω), MAX5332 (500 Ω), and
MAX5333 (1k Ω)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5331UCB	0°C to +85°C	64 TQFP
MAX5331UTK*	0°C to +85°C	68 Thin QFN
MAX5332UCB	0°C to +85°C	64 TQFP
MAX5332UTK*	0°C to +85°C	68 Thin QFN
MAX5333UCB	0°C to +85°C	64 TQFP
MAX5333UTK*	0°C to +85°C	68 Thin QFN

*Future product—contact factory for availability.

Pin Configurations



Pin Configurations continued at end of data sheet.

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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX5331/MAX5332/MAX5333

12-Bit DACs with 32-Channel Sample-and-Hold Outputs

ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND	-0.3V to +12.2V
V _{SS} to AGND	-6.0V to +0.3V
V _{DD} to V _{SS}	+15V
V _{LDAC} , V _{LOGIC} , V _{LSHA} to AGND or DGND	-0.3V to +6V
REF to AGND	-0.3V to +6V
GS to AGND	V _{SS} to V _{DD}
CL and CH to AGND	V _{SS} to V _{DD}
Logic Inputs to DGND	-0.3V to +6V
DGND to AGND	-0.3V to +2V
Maximum Current into OUT _n	±10mA

Maximum Current Into Logic Inputs	±20mA
Continuous Power Dissipation (T _A = +70°C)	
64-Pin TQFP (derate 13.3mW/°C above +70°C)	1066mW
68-Pin Thin QFN (derate 28.6mW/°C above +70°C)	2285mW
Operating Temperature Range	0°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10V, V_{SS} = -4V, V_{LOGIC} = V_{LDAC} = V_{LSHA} = +5V, V_{REF} = +2.5V, AGND = DGND = V_{GS} = 0, R_L ≥ 10MΩ, C_L = 50pF, CLKSEL = +5V, f_{ECLK} = 400kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		12			Bits
Output Range	V _{OUT_n}	(Note 1)	V _{SS} + 0.75		V _{DD} - 2.4	V
Offset Voltage		Code = 4F3 hex		±15	±200	mV
Offset Voltage Tempco				±50		μV/°C
Gain Error		(Note 2)			±1	%
Gain Tempco				±5		ppm/°C
Integral Linearity Error	INL	V _{OUT_n} = -3.25V to +7.6V		0.03	0.1	%FSR
Differential Linearity Error	DNL	V _{OUT_n} = -3.25V to +7.6V, monotonicity guaranteed to 12 bits		±0.5	±1	LSB
Maximum Output Drive Current	I _{OUT}	Sinking and sourcing	±2			mA
DC Output Impedance	R _{OUT}	MAX5331	35	50	65	Ω
		MAX5332	350	500	650	
		MAX5333	700	1000	1300	
Maximum Capacitive Load		MAX5331		250		pF
		MAX5332		10		nF
		MAX5333		10		
DC Crosstalk		Internal oscillator enabled (Note 3)		-90		dB
Power-Supply Rejection Ratio	PSRR	Internal oscillator enabled		-80		dB

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MAX5331/MAX5332/MAX5333

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10V, V_{SS} = -4V, V_{LOGIC} = V_{LDAC} = V_{LSHA} = +5V, V_{REF} = +2.5V, AGND = DGND = V_{GS} = 0, R_L ≥ 10MΩ, C_L = 50pF, CLKSEL = +5V, f_{ECLK} = 400kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Sample-and-Hold Settling		(Note 4)			0.08	%
SCLK Feedthrough				0.5		nV•s
f _{SEQ} Feedthrough				0.5		nV•s
Hold Step				0.25	1	mV
Droop Rate		V _{OUT_} = 0 (Note 5)		1	300	μV/ms
Output Noise				250		μVRMS
REFERENCE INPUT						
Input Resistance			7			kΩ
Reference Input Voltage	V _{REF}			2.5		V
GROUND-SENSE INPUT						
Input Voltage Range	V _{GS}		-0.5		+0.5	V
Input Bias Current	I _{GS}	-0.5V ≤ V _{GS} ≤ 0.5V	-60		0	μA
GS Gain		(Note 6)	0.998	1	1.002	V/V
DIGITAL-INTERFACE DC CHARACTERISTICS						
Input High Voltage	V _{IH}		2.0			V
Input Low Voltage	V _{IL}				0.8	V
Input Current					±1	μA
TIMING CHARACTERISTICS (Figure 2)						
Sequencer Clock Frequency	f _{SEQ}	Internal oscillator	80	100	120	kHz
External Clock Frequency	f _{ECLK}	(Note 7)			480	kHz
SCLK Frequency	f _{SCLK}				20	MHz
SCLK Pulse-Width High	t _{CH}		15			ns
SCLK Pulse-Width Low	t _{CL}		15			ns
$\overline{\text{CS}}$ -Low to SCLK-High Setup Time	t _{CSS0}		15			ns
$\overline{\text{CS}}$ -High to SCLK-High Setup Time	t _{CSS1}		15			ns
SCLK-High to $\overline{\text{CS}}$ -Low Hold Time	t _{CSH0}		10			ns

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +10V$, $V_{SS} = -4V$, $V_{LOGIC} = V_{LDAC} = V_{LSHA} = +5V$, $V_{REF} = +2.5V$, $AGND = DGND = V_{GS} = 0$, $R_L \geq 10M\Omega$, $C_L = 50pF$, $CLKSEL = +5V$, $f_{ECLK} = 400kHz$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK-High to \overline{CS} -High Hold Time	t_{CSH1}		0			ns
DIN to SCLK High Setup Time	t_{DS}		15			ns
DIN to SCLK High Hold Time	t_{DH}		0			ns
\overline{RST} -to- \overline{CS} Low		(Note 8)			500	μs
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 9)	8.55	10	11.60	V
Negative Supply Voltage	V_{SS}	(Note 9)	-5.25	-4	-2.75	V
Supply Difference		$V_{DD} - V_{SS}$ (Note 9)			14.5	V
Logic Supply Voltage	V_{LOGIC} , V_{LDAC} , V_{LSHA}		4.75	5	5.25	V
Positive Supply Current	I_{DD}			32	42	mA
Negative Supply Current	I_{SS}		-40	-32		mA
Logic Supply Current	I_{LOGIC}	(Note 10)		1	1.5	mA
		$f_{SCLK} = 20MHz$ (Note 11)		2	3	

Note 1: The nominal zero-scale voltage (code = 0) is $-4.0535V$. The nominal full-scale voltage (code = FFF hex) is $+9.0503V$. The output voltage is limited by the output range specification, restricting the usable range of DAC codes. The nominal zero-scale voltage can be achieved when $V_{SS} < -4.9V$, and the nominal full-scale voltage can be achieved when $V_{DD} > +11.5V$.

Note 2: Gain is calculated from measurements:

for voltages $V_{DD} = 10V$ and $V_{SS} = -4V$ at codes C00 hex and 4F3 hex
 for voltages $V_{DD} = 11.6V$ and $V_{SS} = -2.9V$ at codes FFF hex and 253 hex
 for voltages $V_{DD} = 9.25V$ and $V_{SS} = -5.25V$ at codes D4F hex and 0 hex
 for voltages $V_{DD} = 8.55V$ and $V_{SS} = -2.75V$ at codes C75 hex and 282 hex

Note 3: Steady-state change in any output with an 8V change in an adjacent output.

Note 4: Settling during the first update for an 8V step. The output will settle to within the linearity specification on subsequent updates. Tested with an external sequencer clock frequency of 480kHz.

Note 5: External clock mode with the external clock not toggling.

Note 6: The output voltage is the sum of the DAC output and the voltage at GS. GS gain is measured at 4F3 hex.

Note 7: The sequencer runs at $f_{SEQ} = f_{ECLK} / 4$. Maximum speed is limited by settling of the DAC and SHAs. Minimum speed is limited by acceptable droop and update time after a burst-mode update.

Note 8: V_{DD} rise to \overline{CS} low = 500 μs maximum.

Note 9: Guaranteed by gain-error test.

Note 10: The serial interface is inactive. $V_{IH} = V_{LOGIC}$, $V_{IL} = 0$.

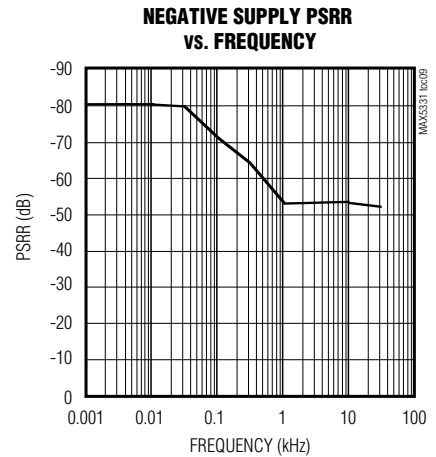
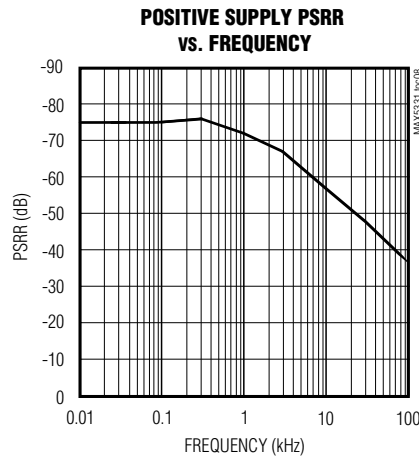
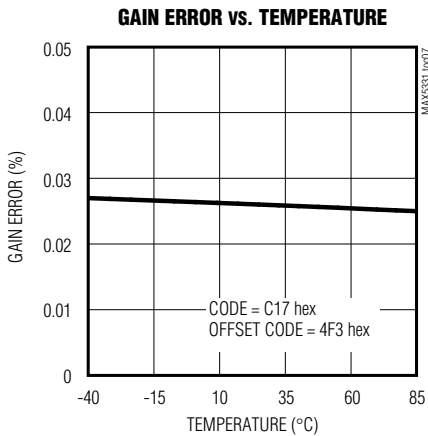
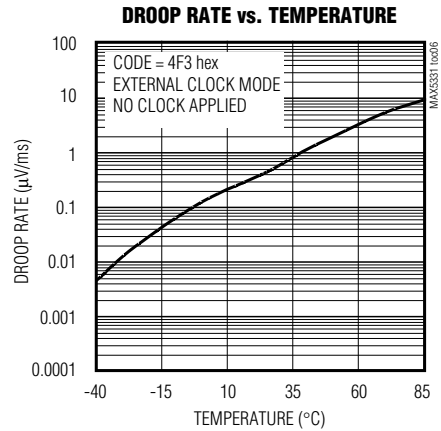
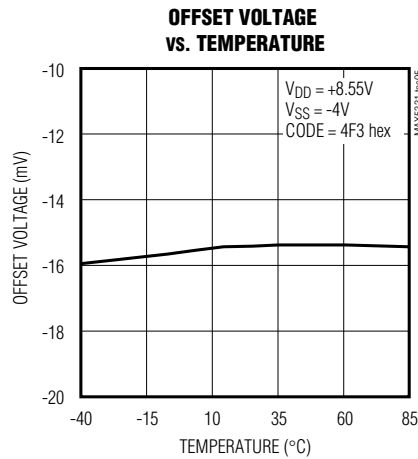
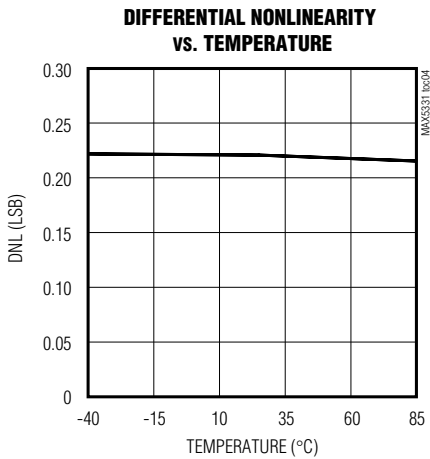
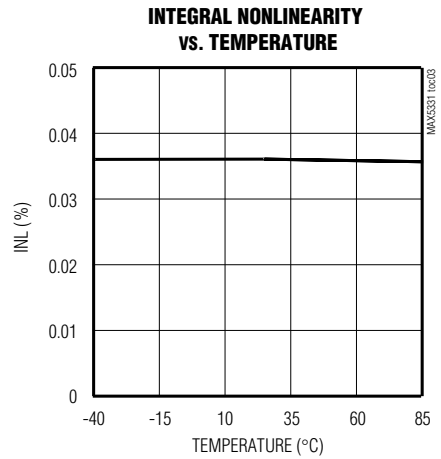
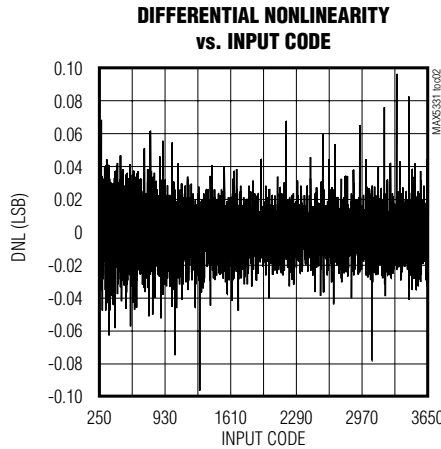
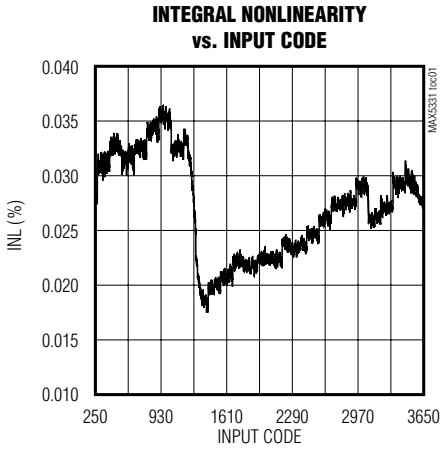
Note 11: The serial interface is active. $V_{IH} = V_{LOGIC}$, $V_{IL} = 0$.

12-Bit DACs with 32-Channel Sample-and-Hold Outputs

Typical Operating Characteristics

($V_{DD} = +10V$, $V_{SS} = -4V$, $V_{REF} = +2.5V$, $V_{GS} = 0$, $T_A = +25^\circ C$, unless otherwise noted.)

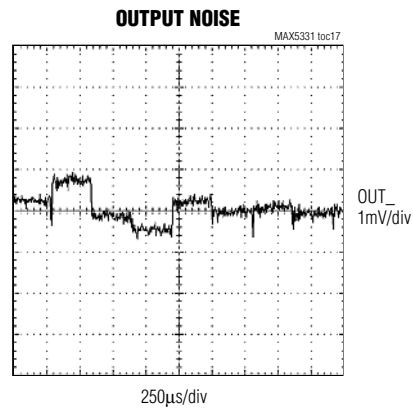
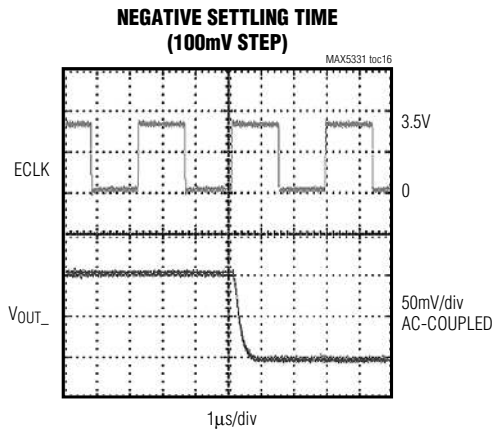
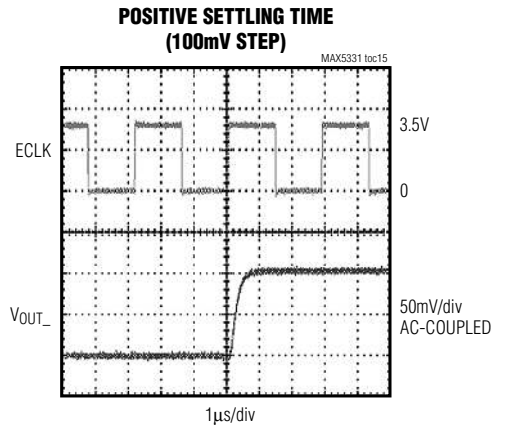
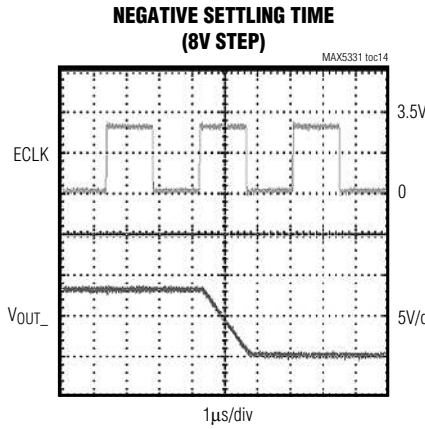
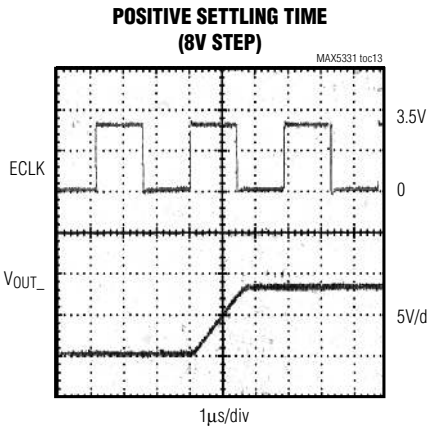
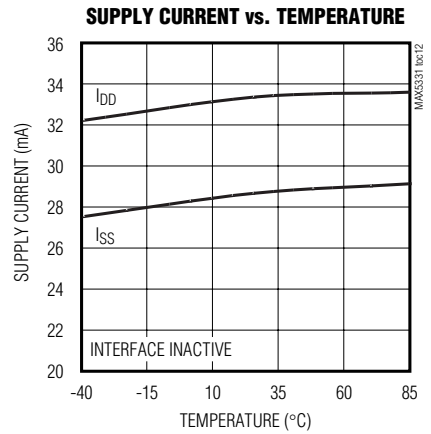
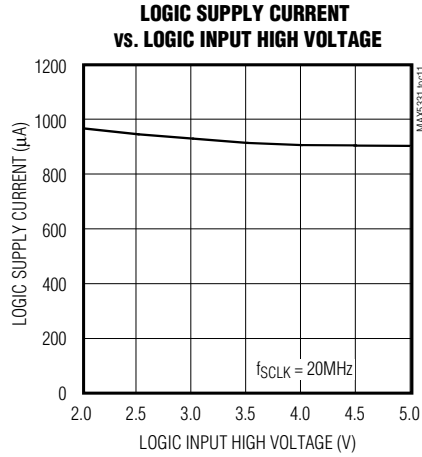
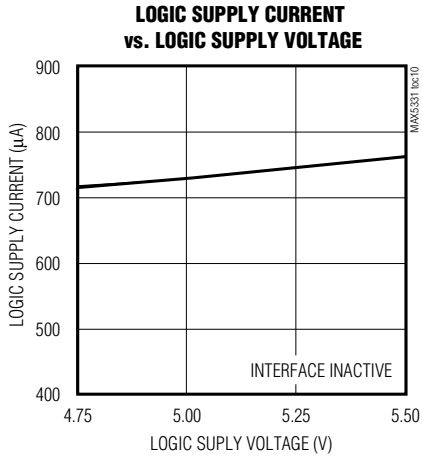
MAX5331/MAX5332/MAX5333



12-Bit DACs with 32-Channel Sample-and-Hold Outputs

Typical Operating Characteristics (continued)

($V_{DD} = +10V$, $V_{SS} = -4V$, $V_{REF} = +2.5V$, $V_{GS} = 0$, $T_A = +25^\circ C$, unless otherwise noted.)



12-Bit DACs with 32-Channel Sample-and-Hold Outputs

Pin Description

PIN		NAME	FUNCTION
TQFP	THIN QFN		
1, 2	1, 2, 17, 34, 51, 68	N.C.	No Connection. Not internally connected.
3	3	GS	Ground-Sensing Input
4	4	V _L DAC	+5V DAC Power Supply
5	5	$\overline{\text{RST}}$	Reset Input
6	6	$\overline{\text{CS}}$	Chip-Select Input
7	7	DIN	Serial-Data Input
8	8	SCLK	Serial-Clock Input
9	9	V _{LOGIC}	+5V Logic Power Supply
10	10	IMMED	Immediate-Update Mode
11	11	ECLK	External Sequencer Clock Input
12	12	CLKSEL	Clock-Select Input
13	13	DGND	Digital Ground
14	14	V _L SHA	+5V Sample-and-Hold Power Supply
15, 25, 40, 55, 62	15, 26, 42, 58, 65	AGND	Analog Ground
16, 32, 46	16, 33, 48	V _{SS}	Negative Power Supply
17, 39, 48	18, 41, 50	V _{DD}	Positive Power Supply
18, 33, 49	19, 35, 52	CL	Output Clamp Low Voltage
19	20	OUT0	Output 0
20	21	OUT1	Output 1
21	22	OUT2	Output 2
22	23	OUT3	Output 3
23	24	OUT4	Output 4
24	25	OUT5	Output 5
26	27	OUT6	Output 6
27	28	OUT7	Output 7
28	29	OUT8	Output 8
29	30	OUT9	Output 9
30	31	OUT10	Output 10
31, 47, 64	32, 49, 67	CH	Output Clamp High Voltage
34	36	OUT11	Output 11
35	37	OUT12	Output 12
36	38	OUT13	Output 13
37	39	OUT14	Output 14
38	40	OUT15	Output 15
41	43	OUT16	Output 16
42	44	OUT17	Output 17

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12-Bit DACs with 32-Channel Sample-and-Hold Outputs

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	THIN QFN		
43	45	OUT18	Output 18
44	46	OUT19	Output 19
45	47	OUT20	Output 20
50	53	OUT21	Output 21
51	54	OUT22	Output 22
52	55	OUT23	Output 23
53	56	OUT24	Output 24
54	57	OUT25	Output 25
56	59	OUT26	Output 26
57	60	OUT27	Output 27
58	61	OUT28	Output 28
59	62	OUT29	Output 29
60	63	OUT30	Output 30
61	64	OUT31	Output 31
63	66	VREF	Reference Voltage Input

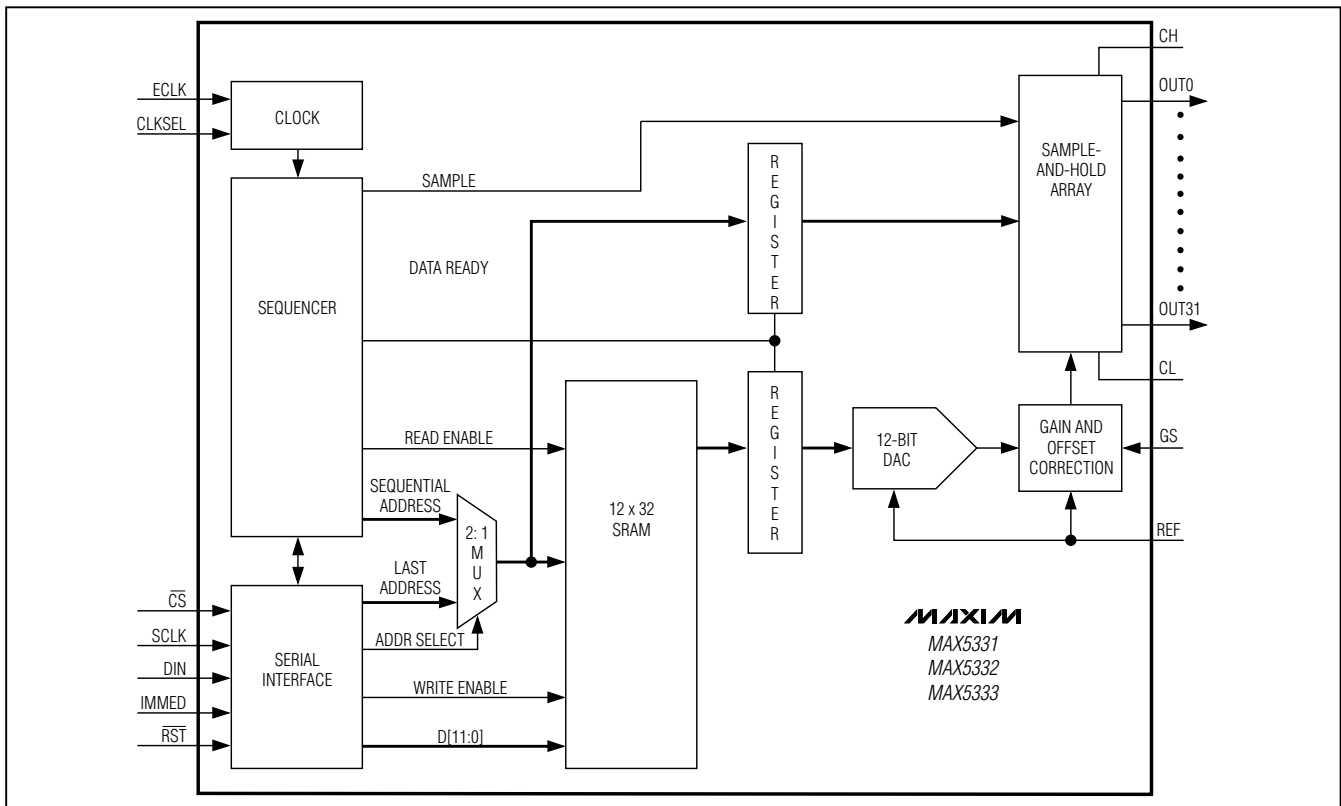


Figure 1. Functional Diagram

12-Bit DACs with 32-Channel Sample-and-Hold Outputs

MAX5331/MAX5332/MAX5333

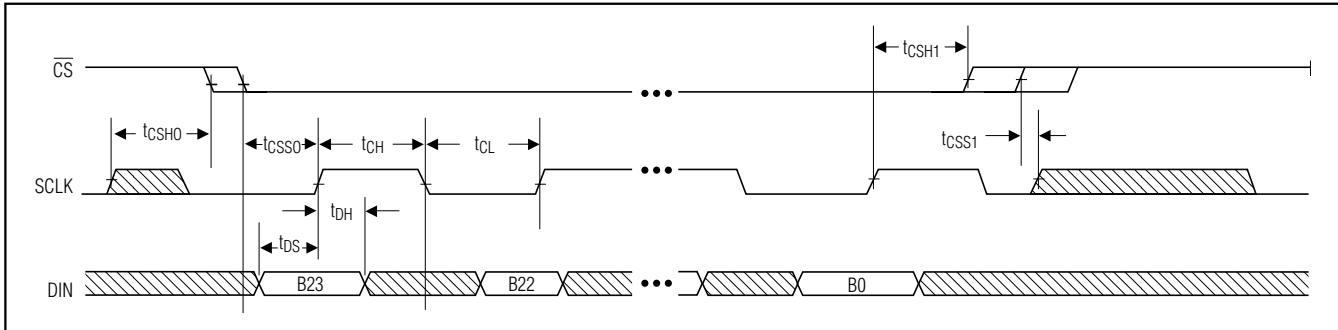


Figure 2. Serial-Interface Timing Diagram

Detailed Description

Sample-and-Hold Amplifiers

The MAX5331/MAX5332/MAX5333 contain 32 buffered SHA circuits with internal hold capacitors. Internal hold capacitors minimize leakage current, dielectric absorption, feedthrough, and required board space. The MAX5331/MAX5332/MAX5333 provide a very low 1 μ V/ms droop rate.

Output

The MAX5331/MAX5332/MAX5333 include output buffers on each channel. The devices contain output resistors in series with the buffer output (Figure 3) for ease of output filtering and capacitive load driving stability.

Output loads increase the analog supply current (I_{DD} and I_{SS}). Excessively loading the outputs drastically increases power dissipation. Do not exceed the maximum power dissipation specified in the *Absolute Maximum Ratings*.

The maximum output voltage range depends on the analog supply voltages available and the output clamp voltages (see the *Output Clamp* section):

$$(V_{SS} + 0.75V) \leq V_{OUT_} \leq (V_{DD} - 2.4V)$$

The devices have a fixed theoretical output range determined by the reference voltage, gain, and mid-scale offset. The output voltage for a given input code is calculated as follows:

$$V_{OUT_} = \left(\frac{\text{code}}{4096} \right) \times V_{REF} \times 5.2428 - (1.6214 \times V_{REF}) + V_{GS}$$

where code is the decimal value of the DAC input code, V_{REF} is the reference voltage, and V_{GS} is the voltage at the ground-sense input. With a 2.5V reference, the nominal end points are -4.0535V and +9.0503V (Table 1). Note that these are “virtual” internal end-point voltages and cannot be reached with all

Table 1. Code Table

DAC INPUT CODE		NOMINAL OUTPUT VOLTAGE (V)	$V_{REF} = +2.5V$
MSB	LSB		
1111	1111 1111	9.0503	Full-scale output.
1100	0111 0101	6.15	Maximum output with $V_{DD} = 8.55V$.
1000	0000 0000	2.5	Midscale output.
0100	1111 0011	0	$V_{OUT_} = 0$. All outputs default to this code after power-up.
0010	1000 0010	-2.0	Minimum output with $V_{SS} = -2.75V$.
0000	0000 0000	-4.0535	Zero-scale output.

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combinations of negative and positive power-supply voltages. The nominal, usable DAC end-point codes for the selected power supplies can be calculated as:

$$\text{Lower end-point code} = 2048 - ((2.5V - (V_{SS} + 0.75V) / 3.2mV) \text{ (result} \geq 0))$$

$$\text{Upper end-point code} = 2048 + ((V_{DD} - 2.4 - 2.5V) / 3.2mV) \text{ (result} \leq 4095)$$

The resistive voltage-divider formed by the output resistor (R_O) and the load impedance (R_L), scales the output voltage. Determine $V_{OUT_}$ as follows:

$$\text{Scaling factor} = \frac{R_L}{R_L + R_O}$$

$$V_{OUT_} = V_{CHOLD} \times \text{scaling factor}$$

Ground Sense

The MAX5331/MAX5332/MAX5333 include a ground-sense input (GS), which allows the output voltages to be referenced to a remote ground. The voltage at GS is added to the output voltage with unity gain. Note that the resulting output voltage must be within the valid output voltage range set by the power supplies.

Output Clamp

The MAX5331/MAX5332/MAX5333 clamp the output between two externally applied voltages. Internal diodes at each channel restrict the output voltage to:

$$(V_{CH} + 0.7V) \geq V_{OUT_} \geq (V_{CL} - 0.7V)$$

The clamping diodes allow the MAX5331/MAX5332/MAX5333 to drive devices with restricted input ranges. The diodes also allow the outputs to be clamped during power-up or fault conditions. To disable output clamping, connect CH to V_{DD} and CL to V_{SS} , setting the clamping voltages beyond the maximum output voltage range.

Serial Interface

The MAX5331/MAX5332/MAX5333 are controlled by an SPI-/QSPI-/MICROWIRE-compatible 3-wire interface. Serial data is clocked into the 24-bit shift register in an MSB-first format, with the 12-bit DAC data and S3–S0 (all zeros) preceding the 5-bit SRAM address, 2-bit control, and a fill zero (Figure 4). The input word is framed by \overline{CS} . The first rising edge of SCLK after \overline{CS} goes low clocks in the MSB of the input word.

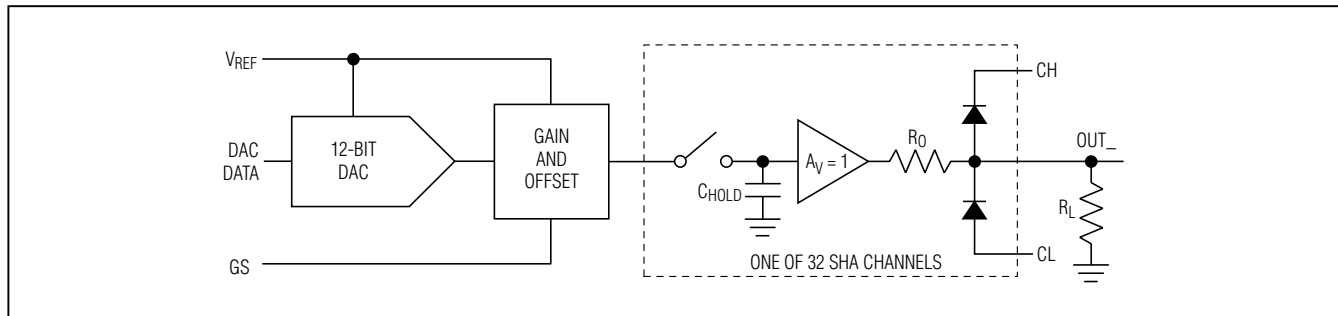


Figure 3. Analog Block Diagram

DATA												ADDRESS					CONTROL						
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0	A4	A3	A2	A1	A0	C1	C0	0
												0	0	0	0						0		
MSB																						LSB	

Figure 4. Input-Word Sequence

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Table 2. Channel/Output Selection

A4	A3	A2	A1	A0	OUTPUT
0	0	0	0	0	OUT0 selected
0	0	0	0	1	OUT1 selected
0	0	0	1	0	OUT2 selected
0	0	0	1	1	OUT3 selected
0	0	1	0	0	OUT4 selected
0	0	1	0	1	OUT5 selected
0	0	1	1	0	OUT6 selected
0	0	1	1	1	OUT7 selected
0	1	0	0	0	OUT8 selected
0	1	0	0	1	OUT9 selected
0	1	0	1	0	OUT10 selected
0	1	0	1	1	OUT11 selected
0	1	1	0	0	OUT12 selected
0	1	1	0	1	OUT13 selected
0	1	1	1	0	OUT14 selected
0	1	1	1	1	OUT15 selected
1	0	0	0	0	OUT16 selected
1	0	0	0	1	OUT17 selected
1	0	0	1	0	OUT18 selected
1	0	0	1	1	OUT19 selected
1	0	1	0	0	OUT20 selected
1	0	1	0	1	OUT21 selected
1	0	1	1	0	OUT22 selected
1	0	1	1	1	OUT23 selected
1	1	0	0	0	OUT24 selected
1	1	0	0	1	OUT25 selected
1	1	0	1	0	OUT26 selected
1	1	0	1	1	OUT27 selected
1	1	1	0	0	OUT28 selected
1	1	1	0	1	OUT29 selected
1	1	1	1	0	OUT30 selected
1	1	1	1	1	OUT31 selected

When each serial word is complete, the value is stored in the SRAM at the address indicated and the control bits are saved. Note that data may be corrupted if CS is not held low for an integer multiple of 24 bits.

All the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. Their switching threshold is compatible with TTL and most CMOS logic levels.

Serial-Input Data Format and Control Codes

The 24-bit serial-input format, shown in Figure 4, comprises 16 bits (D12–D0 and S3–S0 = 0), 5 address bits (A4–A0), 2 control bits (C1, C0), and a fill zero. The address code selects the output channel as shown in Table 2. The control code configures the device as follows:

- 1) If C1 = 1, immediate-update mode is selected. If C1 = 0, burst mode is selected.
- 2) If C0 = 0, the internal sequencer clock is selected. If C0 = 1, the external sequencer clock is selected. This must be repeated with each data word to maintain external input.

12-Bit DACs with 32-Channel Sample-and-Hold Outputs

The operating modes can also be selected externally through CLKSEL and IMMED. If the control bit in the serial word and the external signal conflict, the signal that is a logic 1 is dominant.

Modes of Operation

The MAX5331/MAX5332/MAX5333 feature three modes of operation:

- Sequence mode
- Immediate-update mode
- Burst mode

Table 3. Update Mode

UPDATE MODE	UPDATE TIME
Immediate-Update Mode	$2/f_{SEQ}$
Burst Mode	$33/f_{SEQ}$

Sequence Mode

Sequence mode is the default operating mode. The internal sequencer continuously scrolls through the SRAM, updating each of the 32 SHAs. At each SRAM address location, the stored 12-bit DAC code is loaded to the DAC. Once settled, the DAC output is acquired by the corresponding SHA. Using the internal sequencer clock, the process typically takes 320 μ s to update all 32 SHAs (10 μ s per channel). Using an external sequencer clock, the update process takes 128 clock cycles (four clock cycles per channel).

Immediate-Update Mode

Immediate-update mode is used to change the contents of a single SRAM location, and update the corresponding SHA output. In immediate-update mode, the

selected output is updated before the sequencer resumes operation. Select immediate-update mode by driving either IMMED or C1 high.

The sequencer is interrupted when \overline{CS} is taken low. The input word is then stored in the proper SRAM address. The DAC conversion and SHA sample in progress are completely transparent to the serial bus activity. The SRAM location of the addressed channel is then modified with the new data. The DAC and SHA are updated with the new voltage. The sequencer then resumes scrolling at the interrupted SRAM address.

This operation can take up to two cycles of the 10 μ s sequencer clock. Up to one cycle is needed to allow the sequencer to complete the operation in progress before it is freed to update the new channel. An additional cycle is required to read the new data from memory, update the DAC, and strobe the sample-and-hold. The sequencer resumes scrolling from the location at which it was interrupted. Normal sequencing is suppressed while loading data, thus preventing other channels from being refreshed. Under conditions of extremely frequent immediate updates (i.e., 1000 successive updates), this can result in unacceptable droop.

Figure 5 shows an example of an immediate-update operation. In this example, data for channel 20 is loaded, while channel 7 is being refreshed. The sequencer operation is interrupted, and no other channels are refreshed as long as \overline{CS} is held low. Once \overline{CS} returns high, and the remainder of an f_{SEQ} period (if any) has expired, channel 20 is updated to the new data. Once channel 20 has been updated, the sequencer resumes normal operation at the interrupted channel 7.

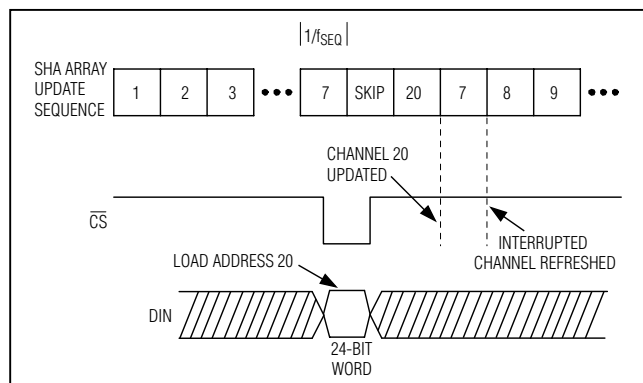


Figure 5. Immediate-Update-Mode Timing Example

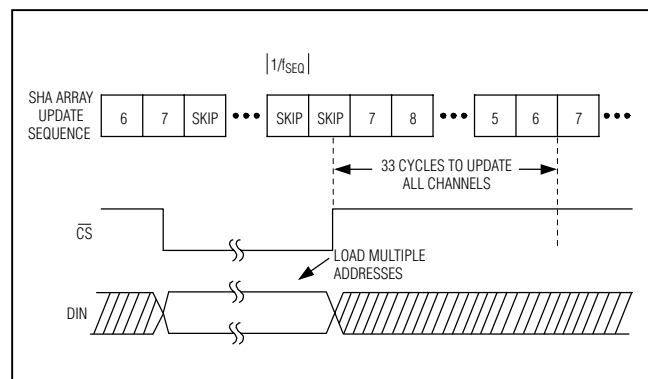


Figure 6. Burst-Mode Timing Example

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Burst Mode

Burst mode allows multiple SRAM locations to be loaded at high speed. During burst mode, the output voltages are not updated until the data burst is complete and control returns to the sequencer. Select burst mode by driving both IMMED and C1 low.

The sequencer is interrupted when \overline{CS} is taken low. All or part of the memory can be loaded while \overline{CS} is low. Each data word is loaded into its specified SRAM address. The DAC conversion and SHA sample in progress are completely transparent to the serial bus activity. When \overline{CS} is taken high, the sequencer resumes scrolling at the interrupted SRAM address. New values are updated when their turn comes up in the sequence.

After burst mode is used, it is recommended that at least one full sequencer loop (320 μ s) is allowed to occur before the serial port is accessed again. This ensures that all outputs are updated before the sequencer is interrupted.

Figure 6 shows an example of a burst-mode operation. As with the immediate-update example, \overline{CS} falls while channel 7 is being refreshed. Data for multiple channels is loaded, and no channels are refreshed as long as \overline{CS} remains low. Once \overline{CS} returns high, sequencing resumes with channel 7 and continues normal refresh operation. Thirty-three fSEQ cycles are required before all channels have been updated.

External Sequencer Clock

An external clock may be used to control the sequencer, altering the output update rate. The sequencer runs at 1/4 the frequency of the supplied clock (ECLK). The external clock option is selected by driving either C0 or CLKSEL high.

When CLKSEL is asserted, the internal clock oscillator is disabled. This feature allows synchronizing the sequencer to other system operations, or shutting down of the sequencer altogether during high-accuracy system measurements. The low 1 μ V/ms droop of these devices ensures that no appreciable degradation of the output voltages occurs, even during extended periods of time when the sequencer is disabled.

Power-On Reset

A power-on reset (POR) circuit sets all channels to 0V (code 4F3 hex) in sequence, requiring 320 μ s. This prevents damage to downstream ICs due to arbitrary reference levels being presented following system power-up. This same function is available by driving \overline{RST} low. During the reset operation, the sequencer is run by the internal clock, regardless of the state of CLKSEL. The reset process cannot be interrupted, serial inputs are ignored until the entire reset process is complete.

Applications Information

Power Supplies and Bypassing

Grounding and power-supply decoupling strongly influence device performance. Digital signals can couple through the reference input, power supplies, and ground connection. Proper grounding and layout can reduce digital feedthrough and crosstalk. At the device level, a 0.1 μ F capacitor is required for the VDD, VSS, and VL₋ inputs. They should be placed as close to the pins as possible. More substantial decoupling at the board level is recommended and is dependent on the number of devices on the board (Figure 7).

The MAX5331/MAX5332/MAX5333 have three separate +5V logic power supplies, VLDAC, VLOGIC, and VLSHA. VLDAC powers the 12-bit DAC. VLSHA powers the control logic of the SHA array. VLOGIC powers the serial interface, sequencer, internal clock, and SRAM. Additional filtering of VLDAC and VLSHA improves the overall performance of the device.

Chip Information

TRANSISTOR COUNT: 16,229
PROCESS: BiCMOS

12-Bit DACs with 32-Channel Sample-and-Hold Outputs

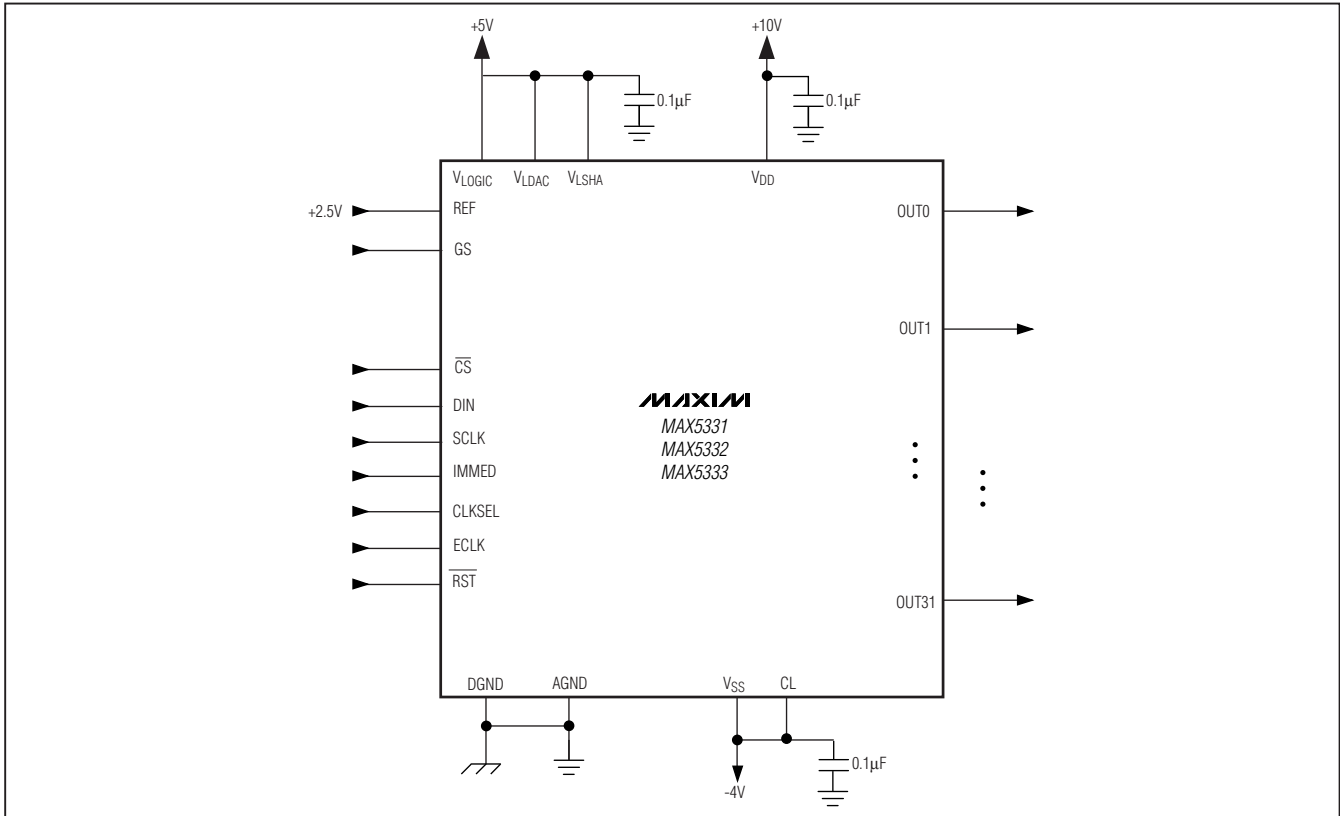
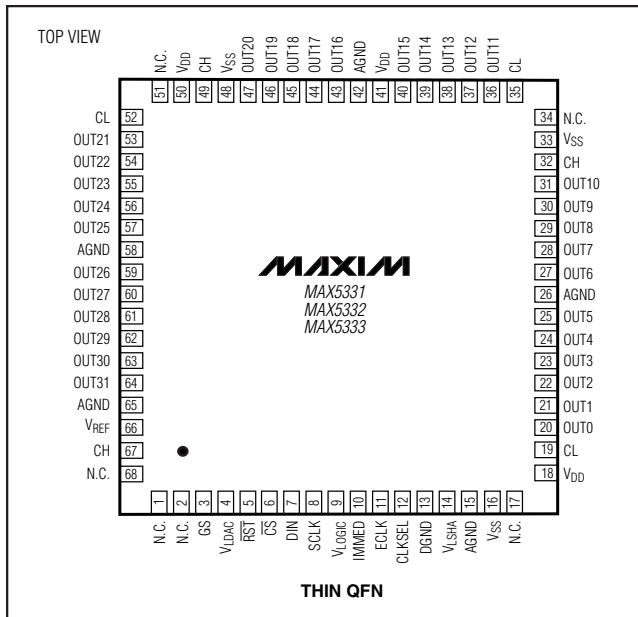


Figure 7. Typical Operating Circuit

Pin Configurations (continued)

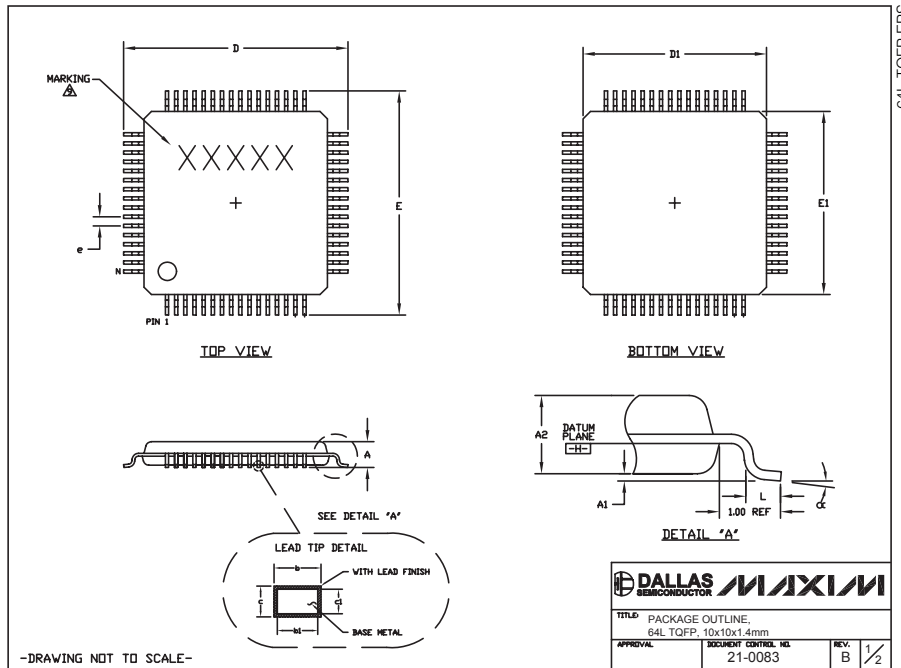


12-Bit DACs with 32-Channel Sample-and-Hold Outputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX5331/MAX5332/MAX5333

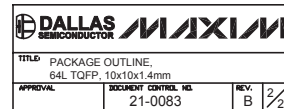


NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE (EED) IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026, VARIATION BCD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

	JEDEC VARIATION	
	BCD	
	64 LEAD	
	MIN.	MAX.
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
D	11.80	12.20
D1	9.80	10.20
E	11.80	12.20
E1	9.80	10.20
e	0.50 BSC.	
L	0.45	0.75
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
CC	0°	7°

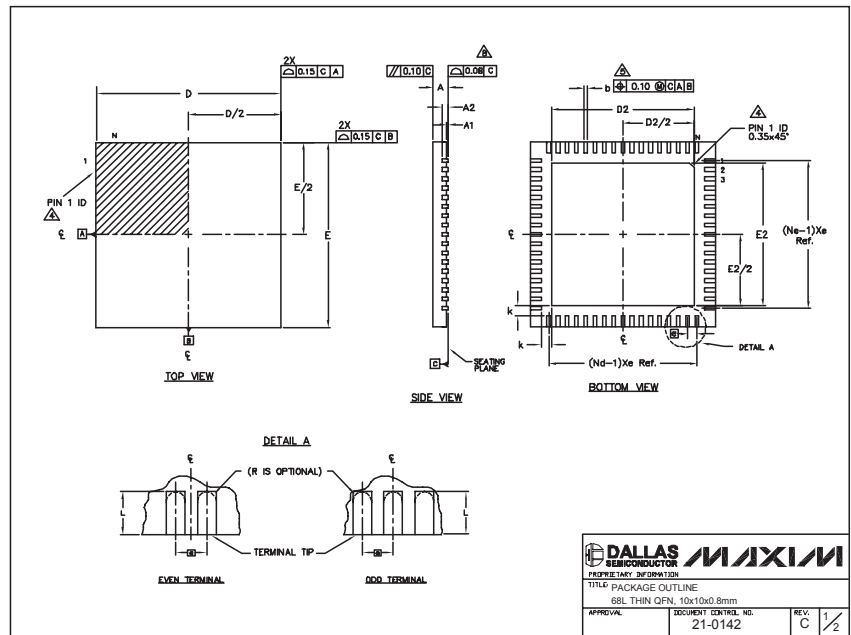
-DRAWING NOT TO SCALE-



12-Bit DACs with 32-Channel Sample-and-Hold Outputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



DALLAS SEMICONDUCTOR **MAXIM**
 PROPRIETARY INFORMATION
 TITLE: PACKAGE OUTLINE
 68L THIN OFN, 10x10x0.8mm
 APPROVAL: _____ DOCUMENT CONTROL NO.: 21-0142 REV: C 1/2

PKG REF.	MIN.	NDM.	MAX.	N	ND	NE
A	0.70	0.75	0.80			
A1	0.00	0.01	0.05			
A2	0.20 REF					
b	0.20	0.25	0.30			
D	9.90	10.00	10.10			
E	9.90	10.00	10.10			
e	0.50 BSC.					
k	0.25	-	-			
L	0.45	0.55	0.65			
N				68		
ND					17	
NE						17
JEDEC	WVND-2					

PKG CODE	D2			E2			DOWN BONDS ALLOWED
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	
T6800-1	7.60	7.70	7.80	7.60	7.70	7.80	NO
T6800-2	7.60	7.70	7.80	7.60	7.70	7.80	YES
T6800-3	7.60	7.70	7.80	7.60	7.70	7.80	NO
T6800-4	7.60	7.70	7.80	7.60	7.70	7.80	YES

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO-220.
- WARPAGE SHALL NOT EXCEED 0.10mm.

DALLAS SEMICONDUCTOR **MAXIM**
 PROPRIETARY INFORMATION
 TITLE: PACKAGE OUTLINE
 68L THIN OFN, 10x10x0.8mm
 APPROVAL: _____ DOCUMENT CONTROL NO.: 21-0142 REV: C 1/2

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