

TPS63710EVM-811 Evaluation Module

The TPS63710EVM-811 facilitates the evaluation of the TPS63710 low noise, 1-A inverting buck converter. The EVM outputs a -1.8-V output voltage at up to 1 A of output current from input voltages between 3.1 V and 14 V. The TPS63710 operates in forced PWM mode with a special low 1/f noise circuit to cleanly supply sensitive analog circuits, such as data converters.

Contents

1	Introduction	1
2	Setup	3
3	TPS63710EVM-811 Test Results	4
4	Board Layout	5
5	Schematic and Bill of Materials	7

List of Figures

1	Loop Response Measurement Modification	2
2	Thermal Performance ($V_{IN} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$)	4
3	Loop Response Measurement ($V_{IN} = 5\text{ V}$, Load = 1 A)	4
4	Top Assembly	5
5	Top Overlay	5
6	Top Layer	6
7	Bottom Layer	6
8	TPS63710EVM-811 Schematic	7

List of Tables

1	Performance Specification Summary	1
2	TPS63710EVM-811 Bill of Materials	7

1 Introduction

The TPS63710 is a synchronous, inverting buck converter. It inverts the supply voltage to a lower (in absolute value), regulated output voltage. The inverting buck topology combined with its low 1/f noise circuitry provides a clean negative voltage for low noise applications.

1.1 Performance Specification

[Table 1](#) provides a summary of the TPS63710EVM-811 performance specifications.

Table 1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input voltage		3.1		14	V
Output voltage setpoint			-1.8		V
Output current	$V_{IN} = 3.1\text{ V}$	0		200	mA
Output current	$V_{IN} \geq 4.5\text{ V}$	0		1	A

1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate additional input and output capacitors. As well, the loop response of the IC can be measured.

1.2.1 Input and Output Capacitors

C4 is provided for an additional input capacitor. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple.

C13 and C14 are provided for additional output capacitors. An additional 22- μ F capacitor may be required in C13 if higher output voltages are used. See the device data sheet for guidelines on the output capacitance required.

1.2.2 Loop Response Measurement

The loop response of the TPS63710EVM-811 can be measured with two simple changes to the circuitry. First, install a 50- Ω resistor across the pads in the middle of the back of the PCB. The pads are spaced to allow installation of an 0603-sized resistor. Second, cut the short section of trace on the top layer between pin 7 and the via. This change is shown in [Figure 1](#). With these changes, an ac signal can be injected into the control loop across the added resistor. The results of this test are shown in [Figure 3](#).

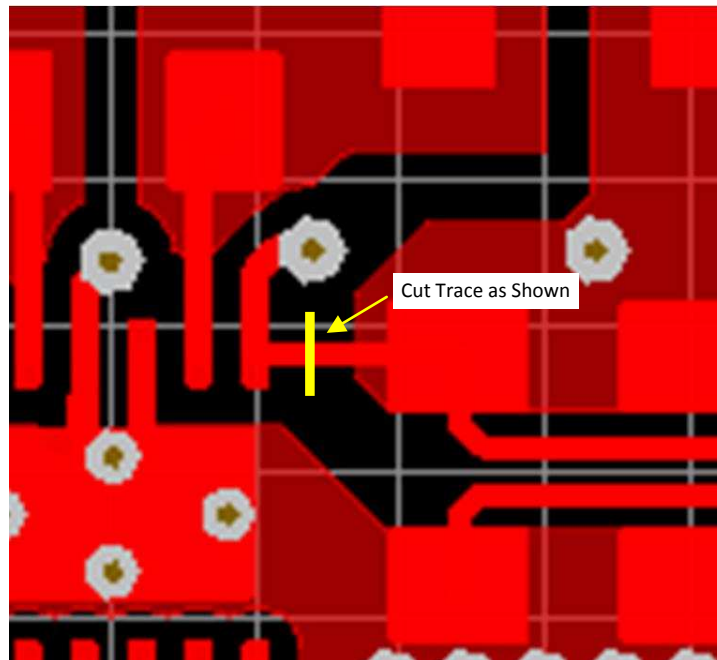


Figure 1. Loop Response Measurement Modification

2 Setup

This section describes how to properly use the TPS63710EVM-811.

2.1 *Input/Output Connector Descriptions*

J1, Pin 1 and 2 – VIN	Positive input connection from the input supply for the EVM.
J1, Pin 3 and 4 – S+/S-	Input voltage sense connections. Measure the input voltage at this point.
J1, Pin 5 and 6 – GND	Input return connection from the input supply for the EVM.
J2, Pin 1 and 2 – VOUT	Negative output voltage connection.
J2, Pin 3 and 4 – S-/S+	Output voltage sense connections. Measure the output voltage at this point.
J2, Pin 5 and 6 – GND	Output return connection.
J3 – PG/GND	The PG output appears on pin 1 of this header with ground on pin 2.
JP1 – EN	EN pin input jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.

2.2 *Setup*

To operate the EVM, set jumper JP1 to the desired position per [Section 2.1](#). Connect the input supply to J1 and connect the load to J2.

3 TPS63710EVM-811 Test Results

The TPS63710EVM-811 was used to take all the data in the TPS63710 data sheet (SLVSD44). See the device data sheet for the performance of this EVM.

Figure 2 shows the thermal performance of the EVM.

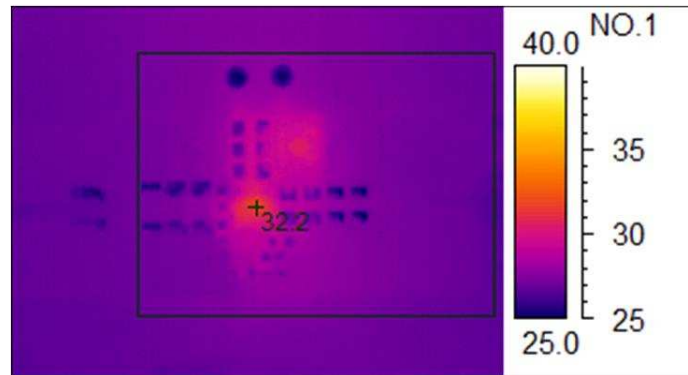


Figure 2. Thermal Performance ($V_{IN} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$)

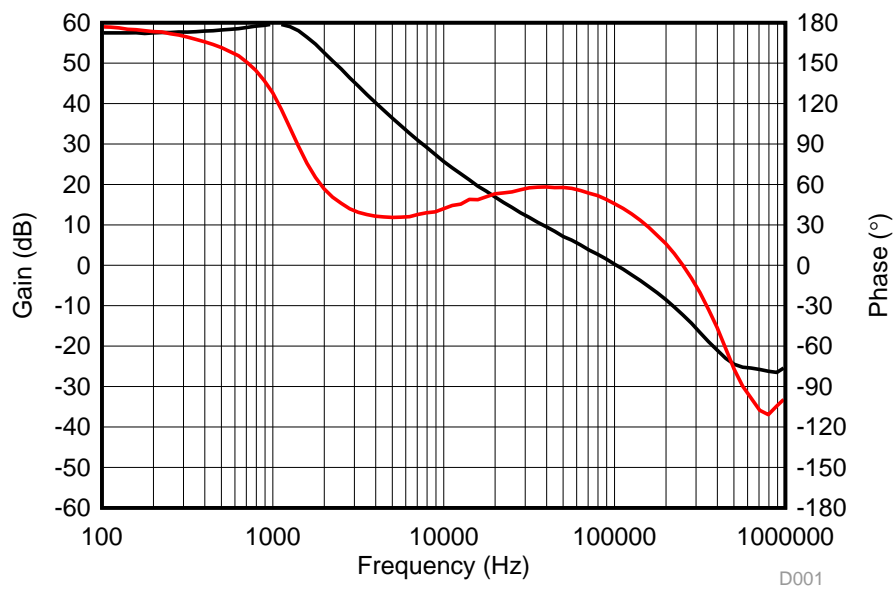


Figure 3. Loop Response Measurement ($V_{IN} = 5\text{ V}$, Load = 1 A)

4 Board Layout

This section provides the TPS63710EVM-811 board layout and illustrations in [Figure 4](#) through [Figure 7](#). The Gerbers are available on the EVM product page: [TPS63710EVM-811](#).

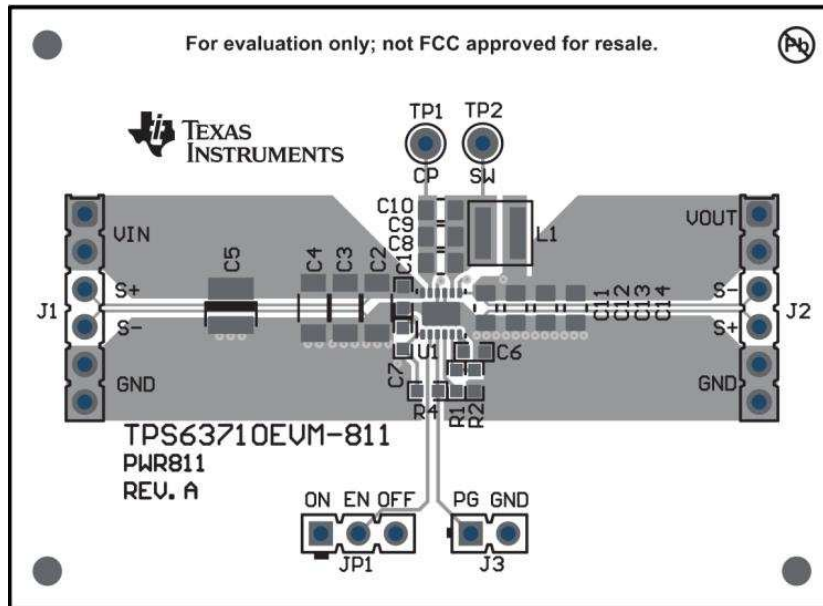


Figure 4. Top Assembly

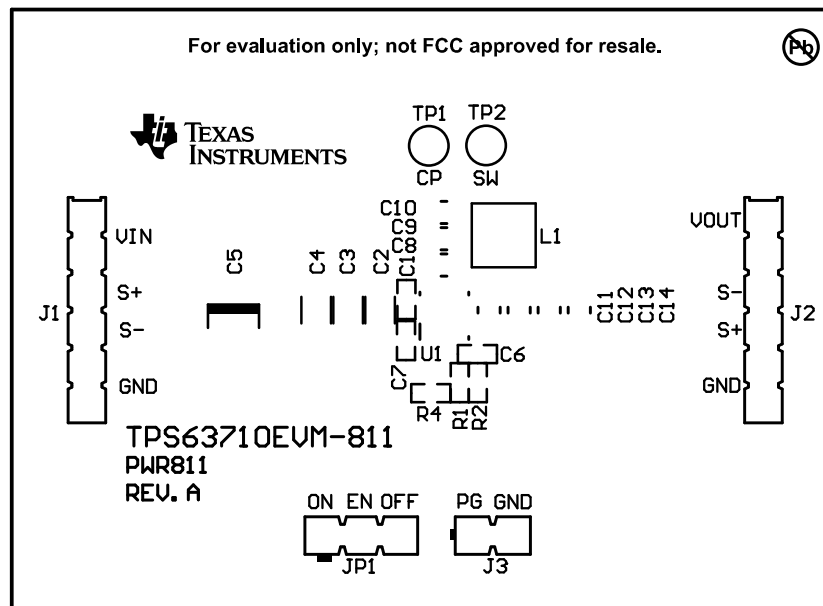


Figure 5. Top Overlay

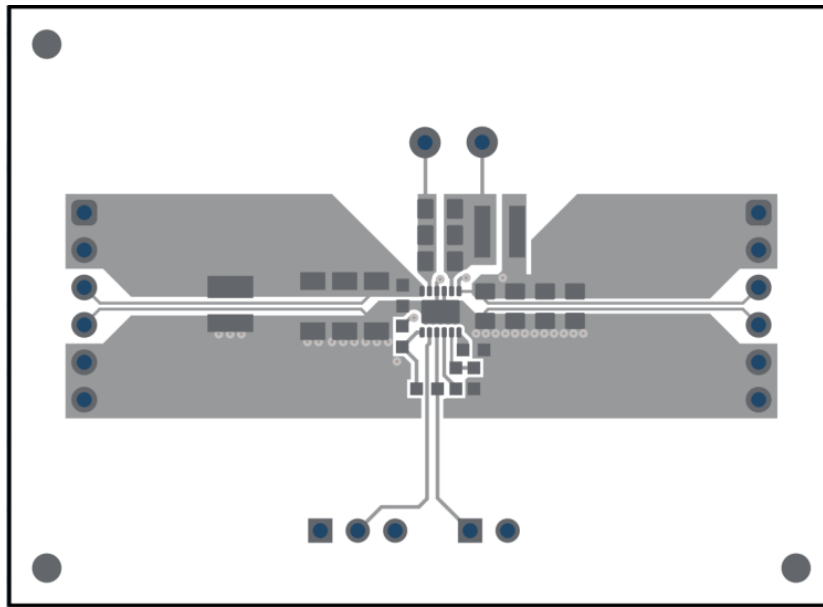


Figure 6. Top Layer

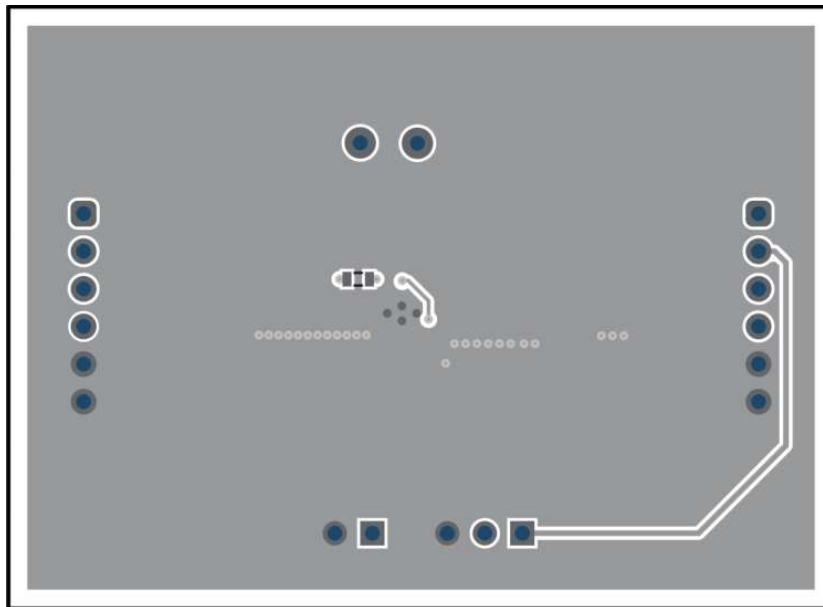


Figure 7. Bottom Layer

5 Schematic and Bill of Materials

This section provides the TPS63710EVM-811 schematic and bill of materials (BOM).

5.1 Schematic

Figure 8 illustrates the EVM schematic.

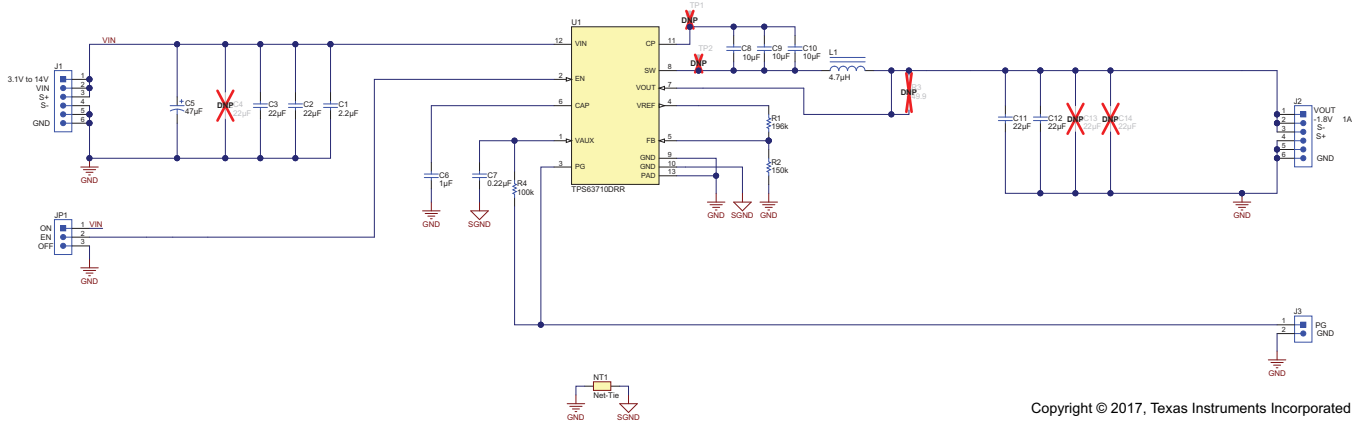


Figure 8. TPS63710EVM-811 Schematic

5.2 Bill of Materials

Table 2 lists the BOM for this EVM.

Table 2. TPS63710EVM-811 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	2.2µF	CAP, CERM, 2.2 µF, 16 V, +/- 10%, X7R	0603	EMK107BB7225KA-T	Taiyo Yuden
C2, C3	2	22µF	CAP, CERM, 22 µF, 16 V, +/- 20%, X7R	1206	EMK316BB7226ML-T	Taiyo Yuden
C5	1	47µF	CAP, TANTALUM, 47 µF, 16 V, +/- 20%, 0.6 ohm	3528	F951C476MBAAQ2	AVX
C6	1	1µF	CAP, CERM, 1 µF, 10 V, +/- 10%, X7R	0603	885012206026	Würth Elektronik
C7	1	0.22µF	CAP, CERM, 0.22 µF, 10 V, +/- 10%, X7R	0603	885012206022	Würth Elektronik
C8, C9, C10	3	10µF	CAP, CERM, 10 µF, 16 V, +/- 20%, X7R	0805	EMK212BB7106MG-T	Taiyo Yuden
C11, C12	2	22µF	CAP, CERM, 22 µF, 10 V, +/- 20%, X7S	0805	C2012X7S1A226M125AC	TDK
L1	1	4.7µH	Inductor, Shielded, 4.7 µH, 2.7 A, 0.05 ohm	4x4x2 mm	XFL4020-472MEB	Coilcraft
R1	1	196k	RES, 196 k, 1%, 0.1 W	0603	Std	Std
R2	1	150k	RES, 150 k, 1%, 0.1 W	0603	Std	Std
R4	1	100k	RES, 100 k, 1%, 0.1 W	0603	Std	Std
U1	1	TPS63710	Synchronous Inverting Buck Converter	3x3 mm	TPS63710DRR	Texas Instruments

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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