DDR3 SDRAM PHY IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02098-1.2

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1. Introduction

1.1. Quick Facts

The Double Data Rate (DDR3) Physical Interface (PHY) IP core is a general purpose IP core that provides connectivity between a DDR3 Memory Controller (MC) and DDR3 memory devices compliant with JESD79-3 specification. This DDR3 PHY IP core provides the industry standard DDR PHY Interface (DFI) bus at the local side to interface with the memory controller. The DFI protocol defines the signals, signal relationships, and timing parameters required to transfer control information and data to and from the DDR3 devices over the DFI bus.

The DDR3 PHY IP core minimizes the effort required to integrate any available DDR3 memory controller with the Lattice FPGA's DDR3 primitives and thereby enables you to implement only the logical portion of the memory controller in the user design. The DDR3 PHY IP core contains all the logic required for memory device initialization, write leveling, read data capture and read data de-skew that are dependent on Lattice FPGA DDR I/O primitives.

This document provides technical information about the DDR3 SDRAM PHY IP Core in Lattice FPGA devices built on the Lattice Nexus™ platform. This information is essential for IP/System developers, verification and software for integration, testing, and validation. In general, design specification from RTL up to IP packaging, IP generation, and integration with Lattice Radiant software is covered in this document.

1.2. Features

- Interfaces to any DDR3 memory controller (MC) through the DDR PHY Interface (DFI) industry specification
- Interfaces to industry standard DDR3 SDRAM components and modules compliant with JESD79-3 specification
- High-performance DDR3 operation up to 533 MHz/1066 Mbps
- Supports memory data path widths of 8, 16, and 32 bits
- Supports on-board memory (up to two chip selects)
- Programmable burst lengths of 8 (fixed), chopped 4 or 8 (on-the-fly), or chopped 4 (fixed)
- Supports automatic DDR3 SDRAM initialization with user mode register programming
- Supports write leveling for each DQS group.
- Supports dynamic On-Die Termination (ODT) controls
- I/O primitives manage read skews (read leveling equivalent)
- Option for controlling memory reset outside the IP core
- 1:1 frequency ratio interface between MC and DFI, 1:2 or 1:4 ratio between DFI and PHY

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals

2. Functional Description

2.1. Block Diagram

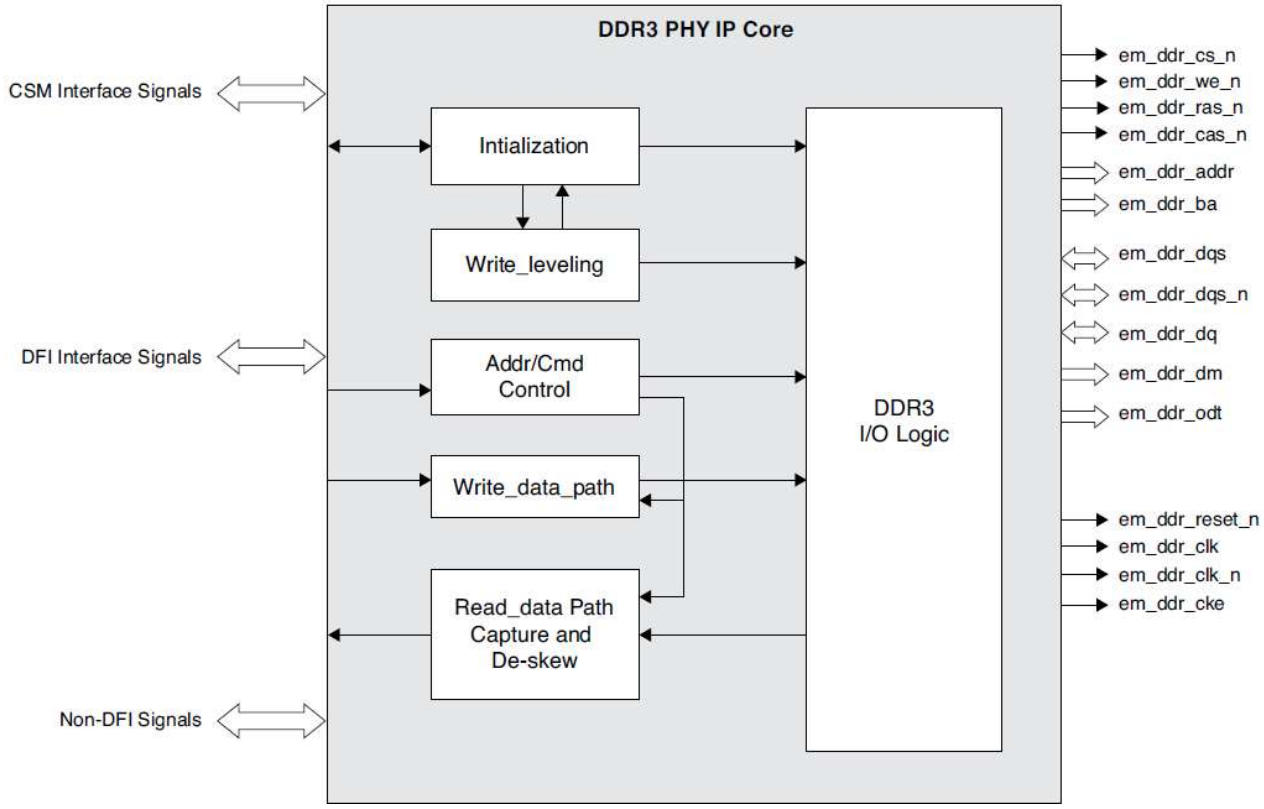

Figure 2.1. DD3 PHY IP Core Block Diagram

2.2. DDR3 PHY IP Components

2.2.1. Clock Synchronization Module (CSM)

The Clock Synchronization Module is included inside the DDR3 PHY IP Core. The CSM logic ensures that the clock domain crossing margin between eclk_i, and sclk_o remains the same for the IDDR and ODDR buses that produce a 2:1 or 4:1 frequency ratio depending on the user setting. The signal csm_ready_o tells you that the sclk_o is stable and can be used for logic application.

The DDR3 PHY IP core works in a 1:1 frequency ratio between the MC and DFI. Inside the DDR3 PHY IP core, the initialization module, write leveling module, address/cmd control module, write data logic and read data capture and de-skew logic operate using sclk_o. These functional modules are implemented as soft logic in the FPGA fabric. This implies that the DFI of the DDR3 PHY IP core follows the 1:1 frequency ratio with the MC.

The DDR3 PHY IP core implements a 1:2 or 1:4 frequency ratio between the functional modules and the DDR I/O primitives. These I/O primitives are the hard logic of the FPGA and they use all the clocks (sclk_o and eclk_i) to implement the selected gearing ratio between the functional block and the PHY memory interface. All transfers from the sclk_o to eclk_i domains and vice-versa happen within the DDR I/O primitives. In a typical case, if the memory controller operates with a 200 MHz system clock (sclk_o) with 1:2 clock frequency ration [4:1 data ratio], the functional modules of the DDR3 PHY IP core also operate with the same 200 MHz sclk_o while the DDR I/O logic of the IP core work primarily with the 400 MHz edge clock (eclk_i).

The combination of this operating clock ratio and the double data rate transfer leads to a user side data bus in the DFI that is four times the width of the memory side data bus. For example, a 32-bit memory side data width requires a 128-bit read data bus and a 128-bit write data bus at the user side interface.

2.2.2. Initialization Module

The Initialization Module performs the DDR3 memory initialization sequence as defined by JEDEC protocol. After power-on or after a normal reset of the DDR3 PHY IP core, memory must be initialized before sending any command to the IP core. It is your responsibility to assert the dfi_init_start_i input to the DDR3 PHY IP core to start the memory initialization sequence. The completion of initialization is indicated by the dfi_init_complete_o output provided by this block.

Since the DDR3 PHY IP core does not use the dfi_data_byte_disable or dfi_freq_ratio DFI signals, the input signal dfi_init_start needs to be asserted by the memory controller to trigger only a memory initialization process. It should be noted that this dfi_init_start_i signal is not used to change the frequency ratio.

2.2.3. Write Leveling

The write leveling block adjusts the DQS-to-CLK relationship for each memory device, using the write level mode of the DDR3 SDRAM when the fly-by wiring is implemented. Write leveling is always done immediately after a memory initialization sequence if write leveling is not disabled through the user interface. When the dfi_init_complete_o signal is asserted after the initialization process it also indicates the completion of write leveling. Along with the assertion of dfi_init_complete_o, the signal wl_err is also asserted if the write leveling process is not successful.

The main purpose of write leveling is to provide better signal integrity by using fly-by topology for the address, command, control and clock signals, and then by de-skewing the DQS signal delays to those signals at the DDR3 DRAM side. Since DDR3 memory modules have adapted fly-by topology, write leveling must be enabled for DIMM based applications. For on-board memory applications, the user interface provides the write leveling function as a user option. When enabled, the PCB for the on-board memory application must be routed using the fly-by topology. Otherwise, write leveling failures may occur due to the lack of guaranteed DQS to CLK edge relationship at the beginning of write level training. Due to this reason, the write leveling option must be disabled if the PCB does not utilize fly-by routing for write leveling.

The write leveling scheme of the DDR3 PHY IP core follows all the steps stipulated in the JEDEC specification. For more details on write leveling, refer to the JEDEC specification JESD79-3.

2.2.4. Read Training

For every read operation, the DDR3 I/O primitives of the device must be initialized at the appropriate time to identify the incoming DQS preamble. Upon proper detection of the preamble, the primitive DQSBUFI extracts a clean DQS signal out of the incoming DQS signal from the memory and generates the DATAVALID output signal that indicates the correct timing window of the valid read data.

The DDR3 PHY IP generates an internal pulse signal, READ[3:0], to the primitive DQSBUFI that is used for the above-mentioned operation. In addition to the READ[3:0] input, another input signal READCLKSEL[2:0] and an output signal, BURSTDET, of the DQSBUFI block are provided to the PHY IP to accomplish the READ signal positioning. Due to the DQS round trip delay that includes PCB routing and I/O pad delays, proper positioning of the READ signal with respect to the incoming preamble is crucial for successful read operations. The DQSBUFI block supports a dynamic READ signal positioning function called read training that enables the PHY IP to position the READ signal within an appropriate timing window by progressively shifting the READ signal and monitoring the positioning result.

This read training is performed as part of the memory initialization process after the write leveling operation is complete. During the read training, the PHY IP generates the READ[3:0] pulse, positions this signal using READCLKSEL[2:0] and monitors the BURSTDET output of DQSBUFI for the result of the current position. The READ signal is set high before the read preamble starts. When the READ pulse is properly positioned, the preamble is detected correctly and the BURSTDET goes high. This guarantees that the generated DATAVALID signal is indicating the correct read valid time window.

The READ signal is generated in the system clock (SCLK) domain and stays asserted for the total burst length of the read operation.

A minimum burst length of four on the memory bus is used in the read training process. The DDR3 PHY IP Core can determine the proper position alignment when there is not a single failure on BURSTDET assertions during the multiple trials. If there is any failure, the IP Core shifts the READ signal position and tries again until it detects no BURSTDET failure.

The PHY IP stores the delay value of the successful position of the READ signal for each DQS group. It uses these delay values during a normal read operation to correctly detect the preamble first, followed by the generation of DATAVALID signal.

2.2.5. Data Logic Path

The Data Path Logic (DPL) block interfaces with the DDR3 I/O modules and is responsible for generating the read data and read data valid signals during read operations. This block implements all the logic needed to ensure that the data write/read to and from the memory is transferred to the local user interface in a deterministic and coherent manner.

2.2.6. Write Data Path

The write data path block interfaces with the DDR3 I/O modules and is responsible for loading the write data along with write data control signals to the DDR3 I/O primitives during write operations. This block implements all the logic needed to ensure that the data write to the memory is transferred from the DFI in a deterministic and coherent manner.

2.2.7. Read Data Path

The read data path block interfaces with the DDR3 I/O modules and is responsible for extracting the read data and read data valid signals during read operations. This block implements all the logic needed to ensure that the data read from the memory is transferred to the DFI in a deterministic and coherent manner. In addition, this block has the logic to deskew the read data delays between different data lanes.

2.2.8. DDR3 I/O Logic

The DDR3 I/O logic block provides the physical interface to the memory device. This block consists mainly of the CrossLink-NX DDR3 I/O primitives supporting compliance to DDR3 electrical and timing requirements. These primitives implement all the interface signals required for memory access and convert the single data rate (SDR) DFI data to double data rate DDR3 data for the write operations. In read mode, they perform the DDR3-to-SDR conversion.

2.3. Signal Descriptions

Table 2.1. DDR3 PHY IP Core Port Descriptions

Pin Name	Direction	Width(Bits)	Description
clk_i	IN	1	Reference clock of the PLL used in the CSM block
CSM Interface Signals			
sclk_o	OUT	1	System Clock used by the PHY IP core. This clock can be used for any interfaced DDR3 memory controller. This is clock generated inside the DDR3 PHY IP Core.
eclk_i	IN	1	Hi-speed clock used by the DDR3 PHY IP
clk_stable_i	IN	1	Signal from the CSM module, which tells that the clock has stabilized
dll_update_o	OUT	1	DQSDLL update request from the IP core to the CSM logic. Remains asserted till update_done_i is set high.
dqsbuf_pause_i	IN	1	Pause signal from CSM to the DDR3 I/O logic
ddr_rst_i	IN	1	Reset signal from CSM to the DDR3 I/O logic
update_done_i	IN	1	Signal to indicate DQSDLL update is completed. dll_update_o is deasserted once this signal is sampled as high.
Non-DFI Interface Signals			
mem_rst_n_i	IN	1	Asynchronous reset signal from the user to reset only the memory device. This signal does not reset the DDR3 PHY IP core's functional modules.
phy_init_act_o	OUT	1	Signal to indicate that the memory initialization process is active.
wl_act_o	OUT	1	Signal to indicate that the memory write leveling process is active.
wl_err_o	OUT	1	Write leveling error Indicates failure in write leveling. The IP core does not work properly if there is a write leveling error. This signal should be checked when the dfi_init_complete_o signal is asserted at the end of the initialization procedure.
rt_err_o	OUT	1	Read Training error Indicates failure in Read Training process. The PHY IP does not work properly if there is a Read Training error. This signal should be checked when dfi_init_complete_o signal is asserted.
csm_ready_o	OUT	1	An active-high output port which tells that sclk_o is already stable.
rst_cntr_ready_o	OUT	1	An active-high output port which tells you that the 200 µs second reset counter has been successfully completed. For users using *Controller Reset to Memory* = disabled, this can serve as an indicator that the memory reset can now be safely deasserted.
DFI Interface Signals			
dfi_rst_n_i	IN	1	Asynchronous reset By default, when asserted, this signal resets the entire IP core and also the DDR3 memory.
dfi_addr_i	IN	ADDR_WIDTH	DFI address bus This signal defines the address information that is intended for the DRAM memory devices for all control commands. The IP core preserves the bit ordering of the dfi_addr_i signals when reflecting this data to the DRAM devices.
dfi_bank_i	IN	3	DFI bank bus This signal defines the bank information that is intended for the DRAM devices for all control commands. The IP core preserves the bit ordering of the dfi_bank signals when reflecting this data to the DRAM devices.

Pin Name	Direction	Width(Bits)	Description
dfi_cas_n_i	IN	1	DFI column address strobe input This signal defines the CAS information that is intended for the DRAM devices for all control commands.
dfi_cke_i	IN	CKE_WIDTH	DFI clock enable input This signal defines the CKE information that is intended for the DRAM devices for all control commands.
dfi_cs_n_i	IN	CS_WIDTH	DFI chip select input This signal defines the chip select information that is intended for the DRAM devices for all control commands.
dfi_odt_i	IN	CS_WIDTH	DFI on-die termination control input This signal defines the ODT information that is intended for the DRAM devices for all control commands.
dfi_ras_n_i	IN	1	DFI row address strobe bus This signal defines the RAS information that is intended for the DRAM devices for all control commands.
dfi_we_n_i	IN	1	DFI write enable input This signal defines the WEN information that is intended for the DRAM devices for all control commands.
dfi_wrdata_i	IN	DATA_WIDTH	Write data bus
dfi_wrdataen_i	IN	1	Write enable input
dfi_byteen_i	IN	BYTE_WIDTH	Write byte-enable input
dfi_rddata_o	OUT	DATA_WIDTH	Read data bus
dfi_rddata_valid_o	OUT	1	Read data valid indicator
dfi_init_complete_o	OUT	1	This output signal is asserted for one clock period after the core completes memory initialization and write leveling. When sampled high, the input signal dfi_init_start_i must be immediately deasserted at the same edge of the sampling clock.
dfi_init_start_i	IN	1	Initialization start request input to the IP core dfi_init_start should be asserted to initiate memory initialization either right after the power-on reset or before sending the first user command to the IP core. Since the DDR3 PHY IP core provides no support for dfi_data_byte_disable or dfi_freq_ratio, this input signal dfi_init_start is provided to the MC only to trigger a memory initialization process.same edge of the sampling clock.
DDR3 SDRAM Memory Interface			
em_ddr_rst_n_o	OUT	1	Asynchronous reset signal from the controller to the memory device. Asserted by the controller for the duration of power on reset or active dfi_rst_n_i or active mem_rst_n_i .
em_ddr_clk_o	OUT	CLKO_WIDTH	Up to 533 MHz memory clock generated by the core. A negative differential pair is automatically generated.
em_ddr_ce_o	OUT	CKE_WIDTH	Memory clock enable generated by the core
em_ddr_addr_o	OUT	DDR_ADDR_WIDTH	Memory address bus – multiplexed row and column address information to the memory
em_ddr_ba_o	OUT	3	Memory bank address
em_ddr_data_io	IN / OUT	DDR_DATA_WIDTH	Memory bi-directional data bus
em_ddr_dm_o	OUT	DDR_BYTE_WIDTH	DDR3 memory write data mask
em_ddr_dqs_io	IN / OUT	DQS_WIDTH	Memory bi-directional data strobe A negative differential pair is automatically generated.
em_ddr_cs_n_o	OUT	DDR_CS_WIDTH	Memory chip select
em_ddr_cas_n_o	OUT	1	Memory column address strobe
em_ddr_ras_n_o	OUT	1	Memory row address strobe

Pin Name	Direction	Width(Bits)	Description
em_ddr_we_n_o	OUT	1	Memory write enable
em_ddr_odt_o	OUT	DDR_CS_WIDTH	Memory on-die termination control

2.4. Attribute Summary

Table 2.2. Attribute Summary for DDR3 SDRAM PHY IP Core

Parameter Name	Values	Default	Description
General Settings			
Device Information			
Memory Selection	*Micron DDR3 1Gb-25E* *Micron DDR3 2Gb-25E* *Micron DDR3 4Gb-25E* *Micron DDR3 1Gb-187E* *Micron DDR3 2Gb-187E* *Micron DDR3 4Gb-187E* *Custom*	*Micron DDR3 1Gb-25E*	Refers to the model of the memory interfaced with the IP. *-25E* memory models are available for frequencies less than or equal to 400 MHz. *-187E* is for 533 MHz.
Fabric Clock (MHz)	[½ Mem Clock, ¼ Mem Clock]	200	Operating output frequency of sclk_o. When using 533 MHz memory clock, only 133.25 MHz (¼ Mem Clock) configuration is allowed.
Mem Clock (MHz)	300/333/400/533	400	Operating frequency of eclk_i
Memory Bit Rate	600/667/800/1066 Mbps	800 Mbps	Displays the target memory bit rate based on the selected frequencies. This value cannot be edited directly, and only used for information.
Gearing Ratio	[4:1],[8:1]	[4:1]	Displays the ratio between the fabric Data Width, and the DDR data width. This value cannot be edited directly, but can be influenced by the ratio of the Fabric Clock and Mem Clock
Memory Configuration			
Memory Type	“On-Board Memory”	“On-Board Memory”	Type of DDR3 memory interfaced with the IP
DDR Bus Size	8/16/24/32	32	This refers to the interface memory bus width (DDR_DATA_WIDTH). For CS_WIDTH = 2 only 8/16 is available.
Clock Width	1/2/4	1	Determines the size of CLKO_WIDTH
CS Width	1/2	1	Determines the number of chips which requires a chip select enable. Available only when DDR Bus Size is less than or equal to 16.
Clock Enable Width	1/2/4	1	Determines the size of CKE_WIDTH
Additional Configuration			
2T Mode	Enabled/Disabled	Disabled	This option allows you to enable or disable the 2T timing for command signals. Available only when CS_WIDTH = 2.
Write Leveling	Enabled/Disabled	Enabled.	This option allows you to enable or disable the write leveling operation of the DDR3 PHY IP core.
Controller Reset to Memory	Enabled/Disabled	Enabled	When this option is enabled, the asynchronous reset input signal, dfi_rst_n_i , to the DDR3 PHY IP core resets both the core and the memory devices. Otherwise, the dfi_rst_n_i input of the core resets only the core, not the memory device.

Parameter Name	Values	Default	Description
Read Training Enable	Enabled/Disabled	Enabled	When this option is enabled, the IP automatically performs the necessary read-training to properly time the data when reading from the memory module.
Settings Tab			
Address			
Row Size	12-16	14	This option indicates the default row address size used in the selected memory configuration.
Column Size	10-12	10	This option indicates the default column address size used in the selected memory configuration.
Mode Register 0 Initial Setting			
Burst Length	*Fixed 4*, *On the Fly*, *Fixed 8*	*Fixed 8*	This option sets the Burst Length value in Mode Register 0 during initialization.
CAS Latency	5-8	6	This option sets the CAS Latency value in Mode Register 0 during initialization.
Burst Type	*Sequential*, *Interleave*	*Sequential*	This option sets the Burst Type value in Mode Register 0 during initialization.
Write Recovery	5-12	6	This option sets the Write Recovery value in Mode Register 0 during initialization. It is set in terms of the memory clock.
DLL Control for PD	Slow Exit/Fast Exit	Slow Exit	This option sets the DLL Control for Precharge PD value in Mode Register 0 during initialization.
Mode Register 1 Initial Setting			
ODI Control	*RZQ/6*, *RZQ/7*	*RZQ/6*	This option sets the Output Driver Impedance Control value in Mode Register 1 during initialization.
RTT_Nom (Ω)	*Disabled*, *RZQ/4*, *RZQ/2*, *RZQ/6*, *RZQ/12*, *RZQ/8*	*RZQ/4*	This option sets the nominal termination, Rtt_Nom, value in Mode Register 1 during initialization.
Additive Latency	*AL Disabled*, *CL-1*, *CL-2*	*AL Disabled*	This option sets the Additive Latency, AL, value in Mode Register 1 during initialization.
Mode Register 2 Initial Setting			
CAS Write Latency	5/6	5	This option sets the CAS Write Latency, CWL, value in Mode Register 2 during initialization. This value is tied to 5 when using *Fabric Clock* less than or equal to 400 MHz, and 6 when it is 533 MHz.
RTT_WR	*Off*, *RZQ/4*, *RZQ/2*	*RZQ/4*	This option sets the Dynamic ODT termination, Rtt_WR, value in Mode Register 2 during initialization.
Memory Device Timing TAB			
Command and Address Timing			
Manually Adjust	Enabled/Disabled	Disabled	This option allows you to manually adjust their desired timing parameters when using their own memory device.
TMOD (tCLK)	12-65536	12	Edits the TMOD parameter
TMRD (tCLK)	4-65536	4	Edits the TMRD parameter
Write Leveling and ODT Timing			
TWLMRD (tCLK)	40-65536	40	Edits the TWLMRD parameter
TWLO (ns)	0-9	4	Edits the TWLO parameter

Parameter Name	Values	Default	Description
Refresh, Reset and Power Down Timing			
TXPR (tCLK)	48-65536	48	Edits the TXPR parameter
Calibration Timing			
TZQINIT (tCLK)	512-65536	512	Edits the TZQINIT parameter

2.5. DFI Usage Guide

The DFI specification includes a list of signals required to drive the memory address, command, and control signals to the DFI bus. These signals are intended to be passed to the DRAM devices in a manner that maintains the timing relationship of these signals on the DFI. The DFI is subdivided into the following interface groups:

- Control Interface
- Write Data Interface
- Read Data Interface
- Update Interface (optional)
- Status Interface (optional)
- Training Interface (optional)
- Low Power Control Interface (optional)

The DDR3 PHY IP core provides support for the Control Interface, Write Data Interface and Read Data Interface. The other optional interfaces are not supported.

The Control Interface is a reflection of the DRAM control interface including address, bank, chip select, row strobe, column strobe, write enable, clock enable and ODT control, as applicable for the memory technology. The Write Data Interface and Read Data Interface are used to send valid write data as well as to receive valid read data across the DFI.

IMPORTANT: When considering the amount of delay between enabling the control signals particularly during writing, you must consider the factor between the clocks. A 1:2 clock ratio would always consume more latency ratios compared to a 1:4 clock ratio for the same MR0 register settings, because the clock in the fabric is operating much faster than the DDR memory clock interface. The examples below are intended for a 1:2 configurations.

2.5.1. Initialization Control

DDR3 memory devices must be initialized before the memory controller accesses the devices. The DDR3 PHY IP core starts the memory initialization sequence when the dfi_init_start_i signal is asserted by the memory controller. Once asserted, the dfi_init_start_i signal needs to be held high until the initialization process is completed. The output signal dfi_init_complete_o is asserted high by the core for only one clock cycle period indicating that the core has completed the initialization sequence and is now ready to access the memory. The dfi_init_start_i signal must be deasserted as soon as dfi_init_complete_o is sampled high at the rising edge of sclk_i. If the dfi_init_start_i is left high at the next rising edge of sclk_i, the core sees this as another request for initialization and starts the initialization process again.

Memory initialization is required only once, immediately after the system reset. As part of the initialization process, the core performs write leveling for all the available DQS lanes and stores the write level delay values for each of those lanes. The core ensures a minimum gap of 500 µs between em_ddr_rst_n_o deassertion and the subsequent em_ddr_ce_o assertion. It is your responsibility to ensure minimum reset duration of 200 µs as required by the JEDEC specification.

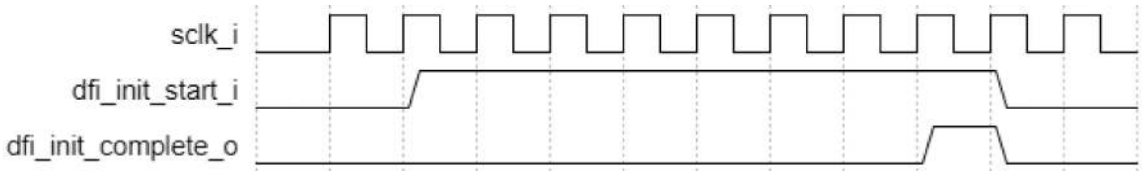

Figure 2.2. Memory Initialization Control Timing

2.5.2. Command and Address

The DFI control signals dfi_addr_i, dfi_bank_i, dfi_cas_n_i, dfi_cke_i, dfi_cs_n_i, dfi_rst_n_i, dfi_odt_i, dfi_ras_n_i and dfi_we_n_i correlate to the DRAM control signals. These control signals are expected to be driven to the memory devices. The timing relationship of the control signals at the DFI bus are maintained at the PHY-DRAM boundary; meaning that all delays are consistent across all signals. The DDR3 PHY IP core supports all the DDR3 memory commands. Refer to the DDR3 SDRAM Command Description and Operation table of the JESD79-3, DDR3 SDRAM Standard for more details about DDR3 memory commands.

Figure 2.3 shows the timing diagram for the Active command and Write/Read command when Additive Latency is selected as 0. The gap between the Active and Write/Read commands is derived from the tRCD value of the memory device. Since the tRCD value is expressed in terms of memory clocks, the corresponding System Clock count at the DFI bus is calculated as (t_{RCD} + 1) / 2. In this calculation, (t_{RC}D + 1) is used to round off the memory clock to sclk_i conversion.

Figure 2.4 shows the timing diagram for the Active command and Write/Read command when Additive latency is selected as 1 or 2. On the memory side, the gap between the Active command and the Write/Read command is 0, 1 or 2 memory clocks more than the tRCD value. This extra delay is due to the combined effect of the 1:2 gearing in the DDR3 PHY IP core and the write/read latency value, odd or even.

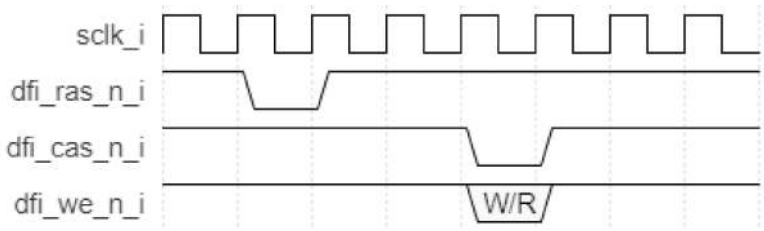

Figure 2.3. Active to Write/Read Command Timing for AL=0

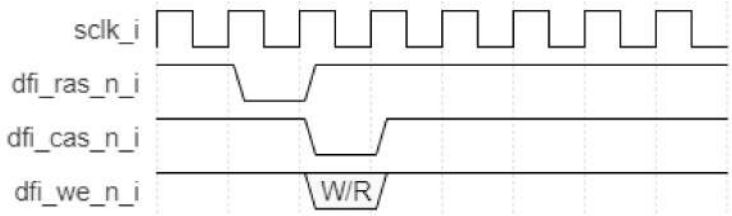

Figure 2.4. Active to Write/Read Command Timing for AL=1 and AL=2

2.5.3. Write Data Interface

The write transaction interface of the DFI includes the write data (dfi_wrdata_i), write byte-enable (dfi_byteen_i), and write data enable (dfi_we_n_i) signals as well as the tphy_wrlat and tphy_wrdata delay timing parameters.

In the DDR3 PHY IP core, the parameter tphy_wrlat has a constant value, which is the write latency in terms of the system clock (sclk_i). The tphy_wrlat is calculated using the equation, tphy_wrlat = (wr_lat +1) / 2 where wr_lat is write latency in terms of memory clock. (wr_lat+1) is used to round off the memory clock to sclk conversion.

The parameter tphy_wrdata is always 0, therefore dfi_wrdata_i is valid from the time dfi_wrdataen_i is asserted.

For a typical write operation, the memory controller asserts the dfi_wrdataen_i signal tphy_wrlat cycles after the assertion of the corresponding write command on the DFI, and for the number of cycles required to complete the write data transfer sent on the DFI control interface. For contiguous write commands, the dfi_wrdataen_i signal is to be asserted tphy_wrlat cycles after the first write command of the stream and is to remain asserted for the entire length of the data stream.

The associated write data (dfi_wrdata_i) and data masking (dfi_byteen_i) are sent along with the assertion of the dfi_wrdataen_i signal on the DFI. The write data timing on the DFI is shown in Figure 2.5 Refer to the evaluation simulation waveform for the DFI bus signal timing for different types of write operations (single, back-to-back, BC4 fixed, BL8 fixed and on-the-fly).

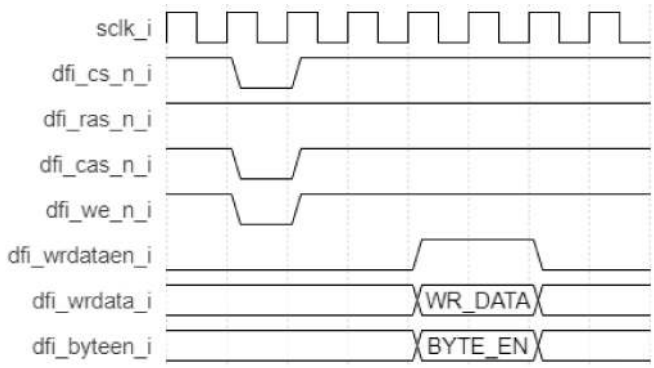

Figure 2.5. DFI Bus Write Timing

2.5.4. Read Data Interface

The read transaction portion of the DFI is defined by the read data enable (dfi_rddata_en), read data (dfi_rddata) bus and the valid (dfi_rddata_valid_o) signals as well as the trddata_en and tphy_rdlat timing parameters.

Since Lattice FPGAs support a preamble detect feature that automatically identifies read data valid timing, the signal dfi_rddata_en is not required for the DDR3 PHY IP core. The timing parameter trddata_en is also not required. The read command is accepted by the core when the dfi command input signal condition indicates a read command.

You can calculate the tphy_rdlat value the memory device's read latency, in terms of sclk_o, is added to this IP core's latency. For a memory read latency (RL) of six memory clocks, the corresponding tphy_rdlat is 12 sclks which is 9 + ((RL+1)/2). In this calculation, (RL+1) is used to round off the memory clock to sclk conversion.

The read data is returned, along with the signal dfi_rddata_valid_o asserted, after tphy_rdlat cycles from the time the read command is asserted. The read data timing on the DFI is shown in Figure 2.6. Refer to the evaluation simulation waveform for the DFI bus signal timing for the different types of read operations (single, back-to-back, BC4 fixed, BL8 fixed and on-the-fly).

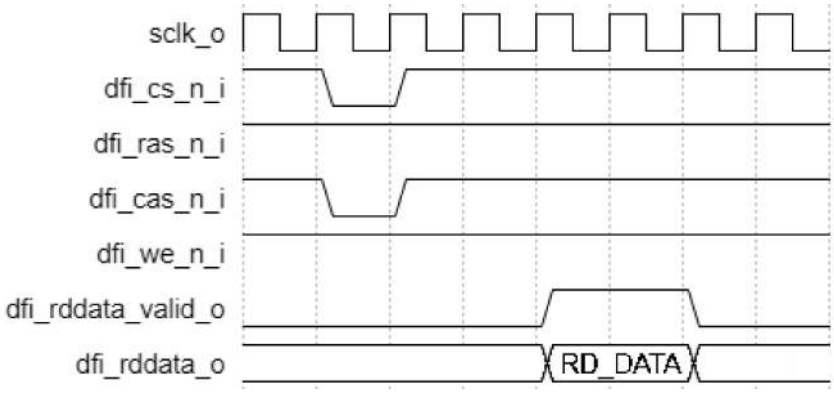

Figure 2.6. DFI Bus Read Timing

2.5.5. Mode Register Programming

The DDR3 SDRAM memory devices are programmed using the mode registers MR0, MR1, MR2, and MR3. The bank address bus (dfi_bank_i) is used to choose one of the mode registers, while the programming data is delivered through the address bus (dfi_addr_i). The memory data bus cannot be used for the mode register programming.

The initialization process uses the mode register initial values selected in the PHY IP user interface. If these mode registers are not re-programmed by the user logic, using the LMR command, they remain in the same configurations as programmed during the initialization process. Table 2.3. shows the list of available parameters and their initial default values from the user interface if they are not changed by the user.

Table 2.3. Initialization Default Values for Mode Register Settings

Type	Register	Value	Description	Local Address	Interface Setting
MR0	Burst Length	2'b00	Fixed 8	addr[1:0]	Yes
	Burst Type	1'b0	Sequential	addr[3]	Yes
	CAS Latency	3'b000	CL = 5	addr[6:4], addr[2]	Yes
	Test Mode	1'b0	Normal	addr[7]	No
	DLL Reset	1'b1	DLL Reset = Yes	addr[8]	No
	WR Recovery	3'b010	6	addr[11:9]	Yes
	DLL Control for precharge PD	1'b1	Fast	addr[12]	Yes
	All others	0	—	addr[DDR_ADDR_WIDTH-1:3]	No
MR1	DLL Enable	1'b0	DLL Enable	addr[0]	No
	ODI Control	2'b00	RZQ/6	addr[5], addr[1]	Yes
	RTT_norm	3'b001	RZQ/4	addr[9], addr[6], addr[2]	Yes
	Additive Latency	2'b00	Disabled	addr[4:3]	Yes
	Write Level Enable	1'b0	Disabled	addr[7]	Yes
	TDQS Enable	1'b0	Disabled	addr[11]	No
	Qoff	1'b0	Enabled	addr[12]	No
	All others	0	—	addr[DDR_ADDR_WIDTH-1:3]	No
MR2	CAS Write Latency	3'b000	5	addr[5:3]	No
	Rtt_WR	2'b01	RZQ/4	addr[10:9]	No
	All others	0	—	—	No
MR3	All	0	—	addr[DDR_ADDR_WIDTH-1:3]	No

LIMITATIONS: When using a clock ratio of 1:4 (gearing 8:1), there are several IP limitations which are NOT present in 1:2 (gearing 4:1) configurations. This is because of the complexities and inherent nature introduced by matching the information from a clock that is ¼ of the memory clock to the double data rate memory interface. These are as follows:

- BC4 is NOT supported, only BL8. When performing BL8 transfers in an 8:1 data ratio, you are expected to provide the full data-width in 1-clock cycle and perform the transaction as though it were a BC4 transaction. There is no need to extend the wr_data_en_i signal compared with the 1:2 (data gearing 4:1).
- When using a 400 MHz or lower memory clock, and the IP is initialized with *Additive Latency = CL-1*, the MRS registers can no longer be overwritten during operation. However, if the *Additive Latency = 0 / CL-2*, you may change the MRS register after the IP has initialized as long as the *Additive Latency* is only toggled between *0 / CL-2*.
- When using a 533 MHz memory clock, the MRS registers can no longer be changed.

3. IP Generation and Evaluation

This chapter provides information on how to generate and synthesize DDR3 SDRAM PHY IP Core using Lattice Radiant software, as well as how to run the simulation. For more information on Lattice Radiant software, refer to Lattice Radiant Software 2.0 User Guide and relevant Lattice tutorials.

3.1. Licensing the IP

An IP core-specific license string is required fully enable the DDR3 SDRAM PHY IP Core in a complete, top-level design. In LIFCL and LFD2NX devices, you can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, and evaluate in the device for a limited time (approximately four hours) without the need of an IP license string. See Hardware Evaluation section for further details. A license string is required to enable timing simulation, and generation of the bitstream file, not limited by the hardware timeout.

3.2. Generation and Synthesis

Lattice Radiant software allows you to generate and customize modules and IPs, and integrate them into the device architecture.

To generate the DDR3 SDRAM PHY IP Core

1. In the **Module/IP Block Wizard** create a new Lattice Radiant software project for the DDR3 SDRAM PHY IP Core.
2. In the dialog box of the **Module/IP Block Wizard** window, configure ADC module according to custom specifications using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.2.

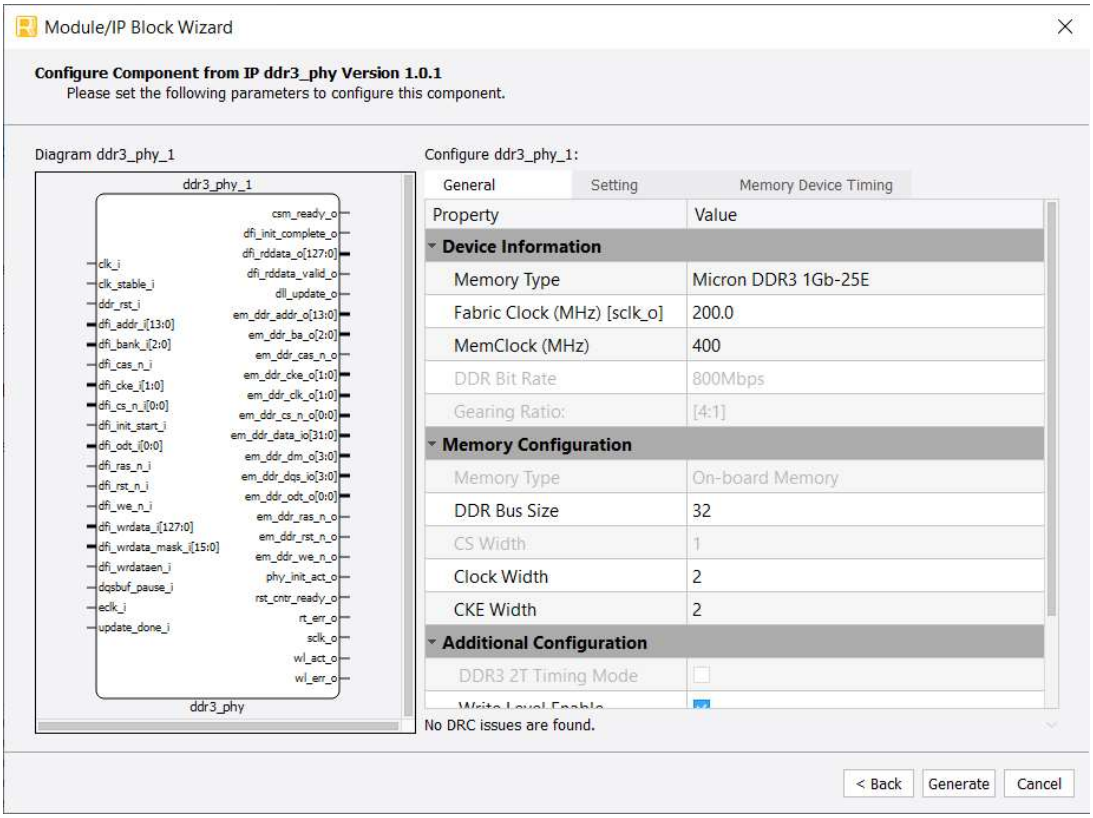

Figure 3.1. Module / IP Block Wizard

3. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 3.2.

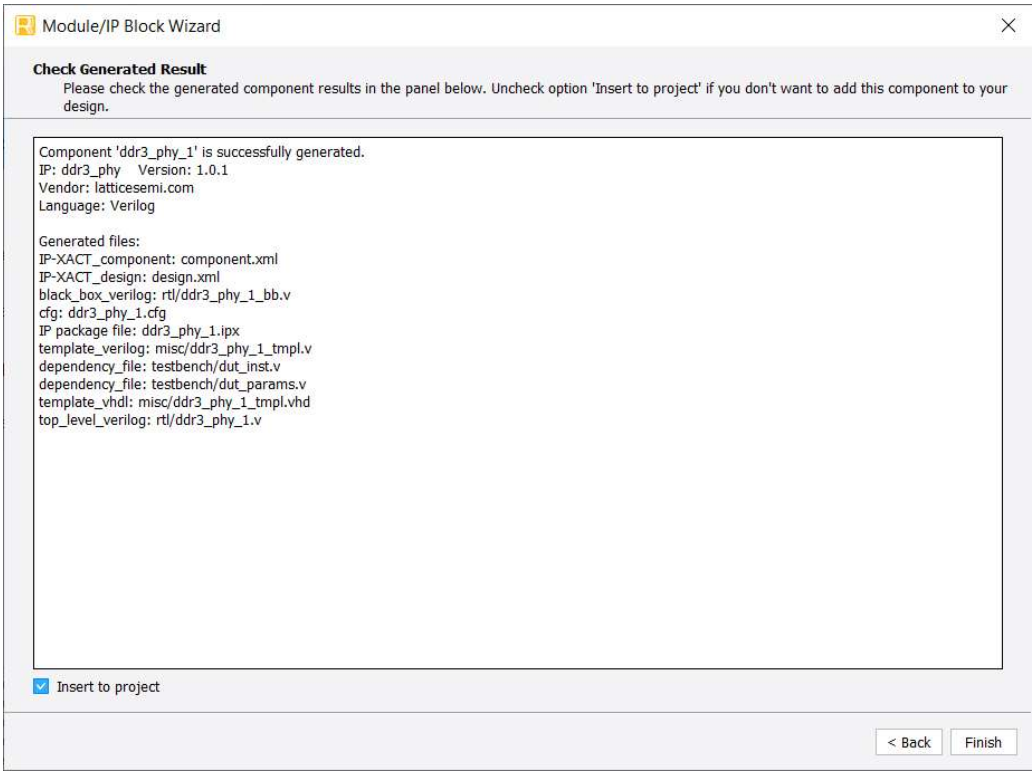

Figure 3.2. Check Generated Result

4. Click **Finish** to generate the Verilog file.
5. Upon generating your desired design, you can synthesize it by clicking **Synthesize Design** located on the top left corner of the screen, as shown in Figure 3.3.

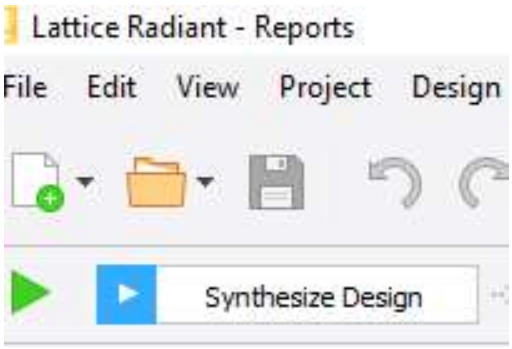

Figure 3.3. Synthesizing Design

3.3. Running Functional Simulation

To run the functional simulation:

1. Add the testbench by right-clicking the implementation name and selecting **Add**.
2. Add the simulation file. Select the testbench file from *<ip_name>\testbench*. The top level RTL is named tb_top.v

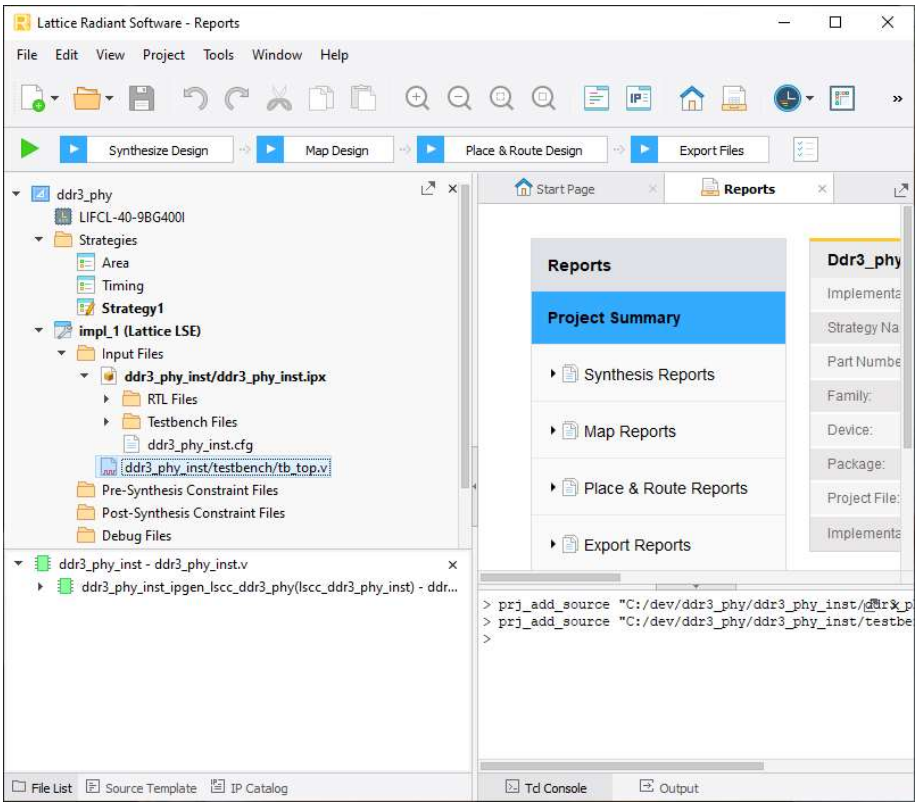

Figure 3.4. Synthesizing Design

3. Once the simulation file is added, simulate the project. Click **Tools > Simulation Wizard** to open the Lattice Radiant software's simulation wizard.
4. Click **Next** once the splash window opens, and begin configuring the testbench.

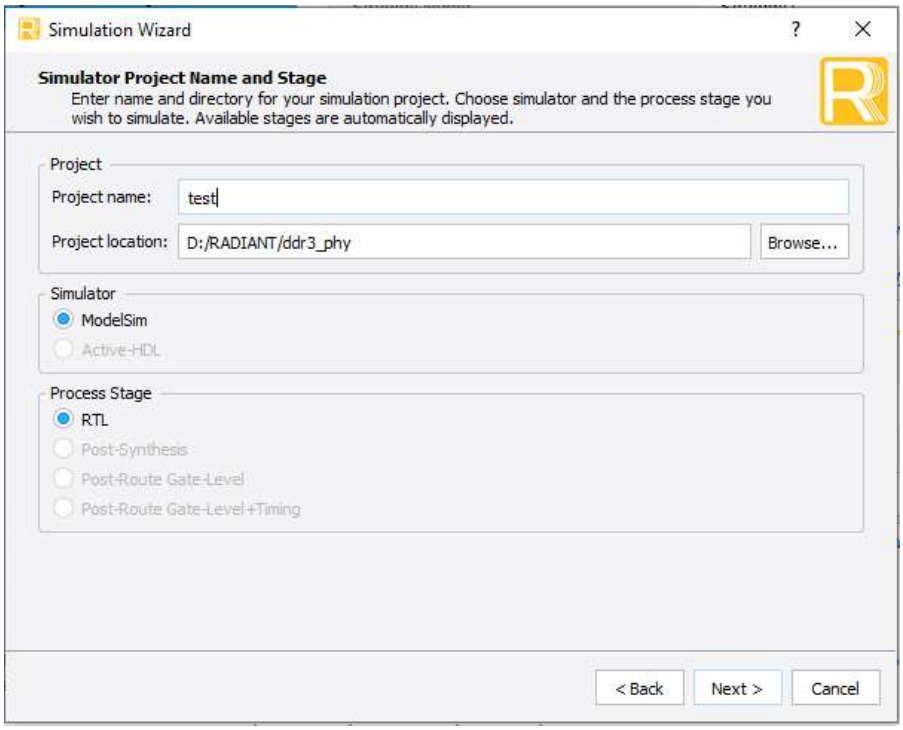

Figure 3.5. Simulation Wizard

5. For this example, name the project as *test* using the Active-HDL simulator and RTL simulation only.
6. Click **Next**. The list of files to be added appears. Make sure that at least two files are added: the generated IP and the top-level testbench.

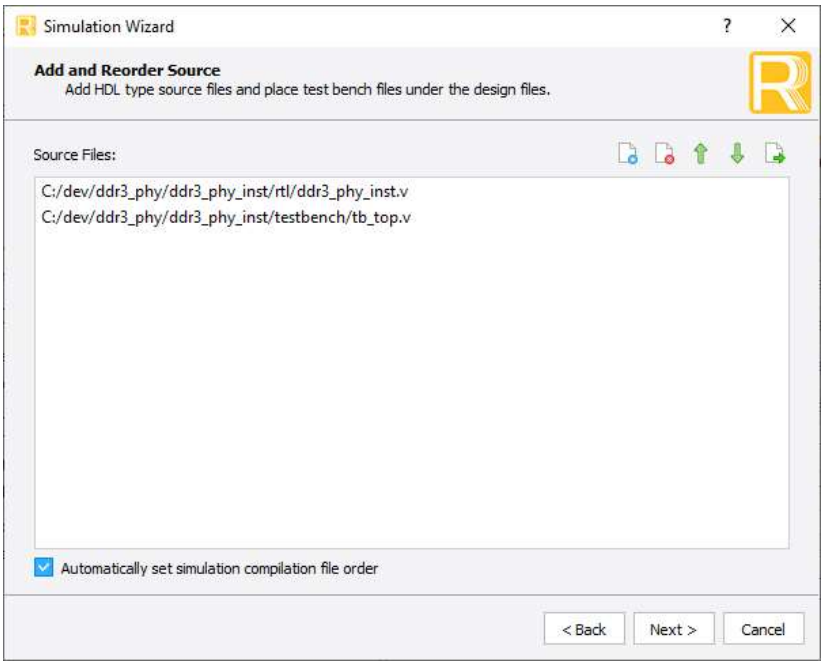

Figure 3.6. File List

7. After clicking **Next**, **Simulation Wizard** parses the included RTL. In this section, make sure that the **Simulation Top Model** is tb_top.

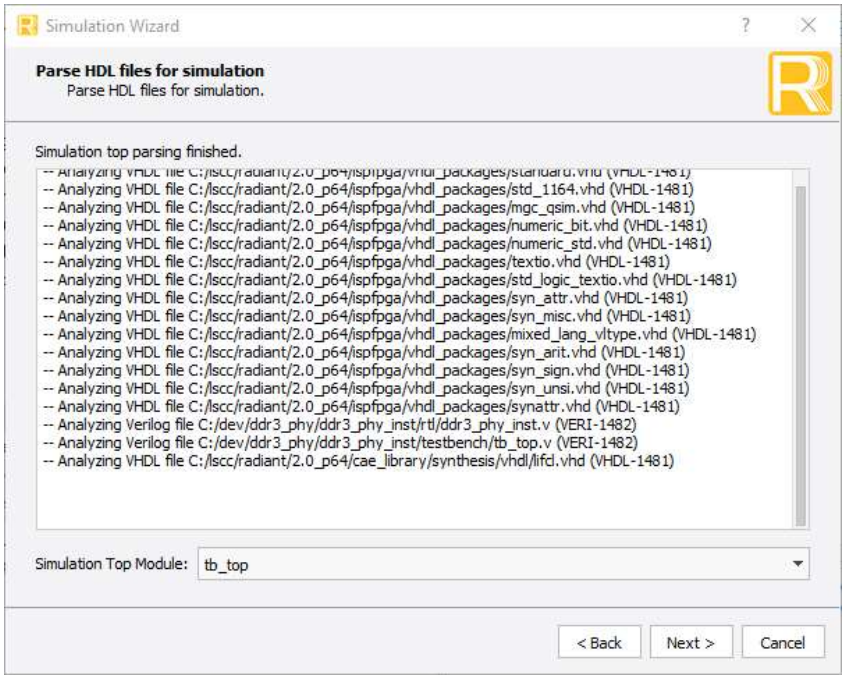

Figure 3.7. Parse HDL Files

8. Once completed, click **Next** and verify that the options **Run simulator**, **Add top-level signals to waveform display**, and **Run simulation** are checked.

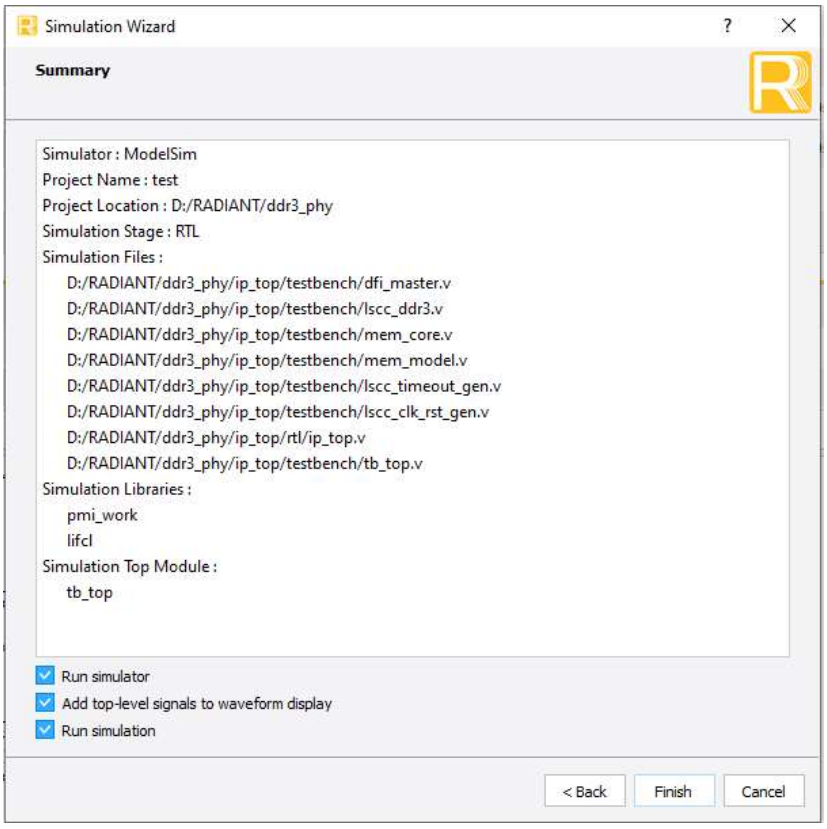

Figure 3.8. Simulation Wizard Summary

9. Click **Finish** to open Active-HDL and run the first 1 µs of the simulation.

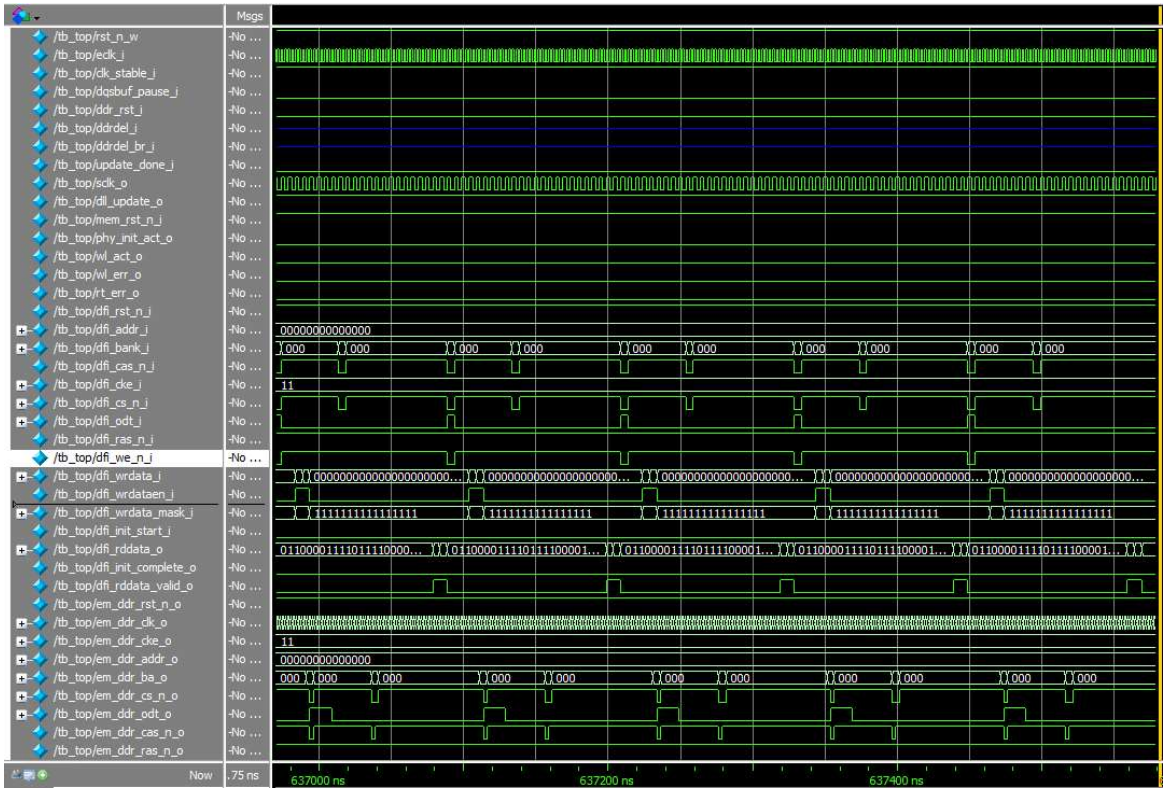

Figure 3.9. Simulation Waveform

3.4. Hardware Evaluation

The DDR3-SDRAM PHY IP Core supports Lattice's IP hardware evaluation capability using Lattice FPGA devices built on the Lattice Nexus platform. This allows you to create versions of the IP core, which operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It can be used to evaluate the core in hardware with user-defined settings and design. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings. The feature is enabled by default.

4. Ordering Part Number

The Ordering Part Number (OPN) for this IP Core are the following:

- DDR3-PHY-CNX-U – DDR3 Physical Interface for CrossLink-NX – Single Design License
- DDR3-PHY-CNX-UT – DDR3 Physical Interface for CrossLink-NX – Site License
- DDR3-PHY-CTNX-U – DDR3 Physical Interface for Certus-NX – Single Design License
- DDR3-PHY-CTNX-UT – DDR3 Physical Interface for Certus-NX – Site License
- DDR3-PHY-CPNX-U – DDR3 Physical Interface for CertusPro-NX – Single Design License
- DDR3-PHY-CPNX-UT – DDR3 Physical Interface for CertusPro-NX – Site License

Appendix A. Resource Utilization

Table A.1. Device and Tool Tested

	Value
Lattice Radiant Software Version	ng2.1 (for Windows)
Device Used	LIFCL-40-9BG400I
Performance Grade	9_High-Performance_1.0V
Synthesis Tool	Synplify Pro (R) Q-2020.03LR, Build 134R, May 8 2020
	Lattice Synthesis Engine (LSE)

Note: Some bits are clipped to accommodate the current configuration with the selected device.

Table A.2. DDR3 PHY Resource Utilization[1]

DDR DATA WIDTH	GEARING	DDR Bit Rate	Synthesis Tool	Register	LUTs	F_{max}
8	X2	800 Mbps	Synplify Pro	654	794	sclk_o = 200 MHz
			LSE	659	1047	sclk_o = 200 MHz
32[2]	X2	800 Mbps	Synplify Pro	1298	1190	sclk_o = 200 MHz
			LSE	1312	1401	sclk_o = 200 MHz
32[2]	X4	800 Mbps	Synplify Pro	1761	1624	sclk_o = 100 MHz
			LSE	1774	1902	sclk_o = 100 MHz
32[2]	X4	1066 Mbps	Synplify Pro	1761	1624	sclk_o = 133.25 MHz
			LSE	1803	1960	sclk_o = 133.25 MHz

Note:

1. Other configurations are set to default. (1066Mbps uses WR = 10 to comply with the JEDEC specification).
2. FIFOs are used on the I/O ports in order to reduce the number of pins required to pass MAP while maintaining the complete set of data-in and data-out ports. A PLL is used to generate the high speed clock (eclk_i) for these configurations. Both the FIFO and PLL resources are not included in this resource utilization report.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

For complete information on JEDEC specifications and documents referred to in this user's guide, visit JEDEC website: http://www.jedec.org.

This IP Core is JESD79-3 compliant, for more information regarding the JEDEC specification, visit JEDEC website: http://www.jedec.org.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, June 2021

Section	Change Summary
Introduction	• Replaced specific product names with Lattice FPGA devices built on the Lattice Nexus platform. • Removed Support for all CrossLink-NX and Certus-NX devices from features list.

IP Generation and Evaluation	• In the Running Functional Simulation section:
	  • Updated and/or renamed Figure 3.5. Simulation Wizard, Figure 3.8. Simulation Wizard Summary, and Figure 3.9. Simulation Waveform.
	  • Removed step 10.
	• Replaced specific devices with *Lattice FPGA devices built on the Lattice Nexus platform* In the Hardware Evaluation section.

Ordering Part Number	Added part numbers.
References	Revised reference to Lattice Radiant Software User Guide and removed link.

Revision 1.1, June 2020

Section	Change Summary
Introduction	Added support for Certus-NX.
Functional Description	• Added support 8:1 gearing and 1:4 frequency ratio in Table 2.2, Clock Synchronization Module (CSM), and Mode Register Programming section. • Added new pins csm_ready_o in DDR3 PHY IP Components section and rst_cntr_ready_o Signal Descriptions section. • Updated Table 2.1 and Table 2.3.
Ordering Part Number	Added this section.
Appendix A. Resource Utilization	Added this section.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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