Rev: 031008

DS33X162 Demo Kit

General Description

The DS33X162 demo kit (DK) is an easy-to-use evaluation board for the DS33X162 Ethernet-over-PDH device. The demo kit contains an option for either T3/E3 or T1/E1 serial links. All serial links are complete with line interface, transformers, and network connections. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC.

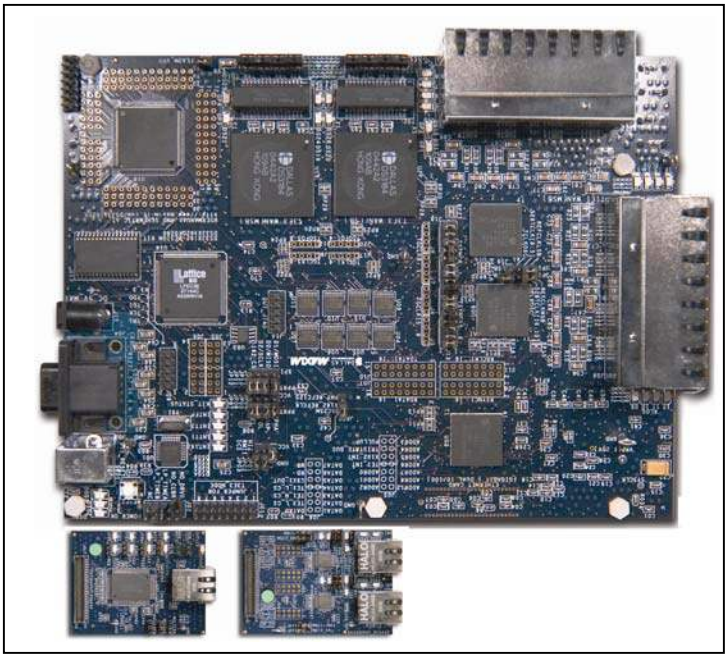
On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

Windows is a registered trademark of Microsoft Corp.

Ordering Information

PART	TYPE
DS33X162DK	Demo card, T3/E3, T1/E1

Demo Kit Board



Features

- **Demonstrates Key Functions of DS33X162 Ethernet Transport Chipset**
- **Includes DS26528 T1/E1 Transceiver, DS3174 T3/E3 Transceiver, Transformers, BNC, and RJ48 Network Connectors and Termination**
- **Includes Ethernet PHY Supporting 10/100 and Gigabit Modes**
- **Provides Support for Hardware and Software Modes**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33X162, DS26528, DS3174, and PHY Registers**
- **All DS33X162 Interface Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal, Ethernet Link, Tx/Rx, and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

Demo Kit Contents

DS33X162DK Main Board
Dual-Port 10/100Mb Ethernet Card
Single-Port 10/100/1000Mb Ethernet Card
5V 2.5A Power Supply
USB Cable, RS232 Cable
T3/E3 BNC-to-2-Pin Adapter
CD-ROM
  ChipView Software and Manual
  DS33X162DK Data Sheet
Configuration Files

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1. System Floorplan

Figure 1-1. DS33X162 System Floorplan

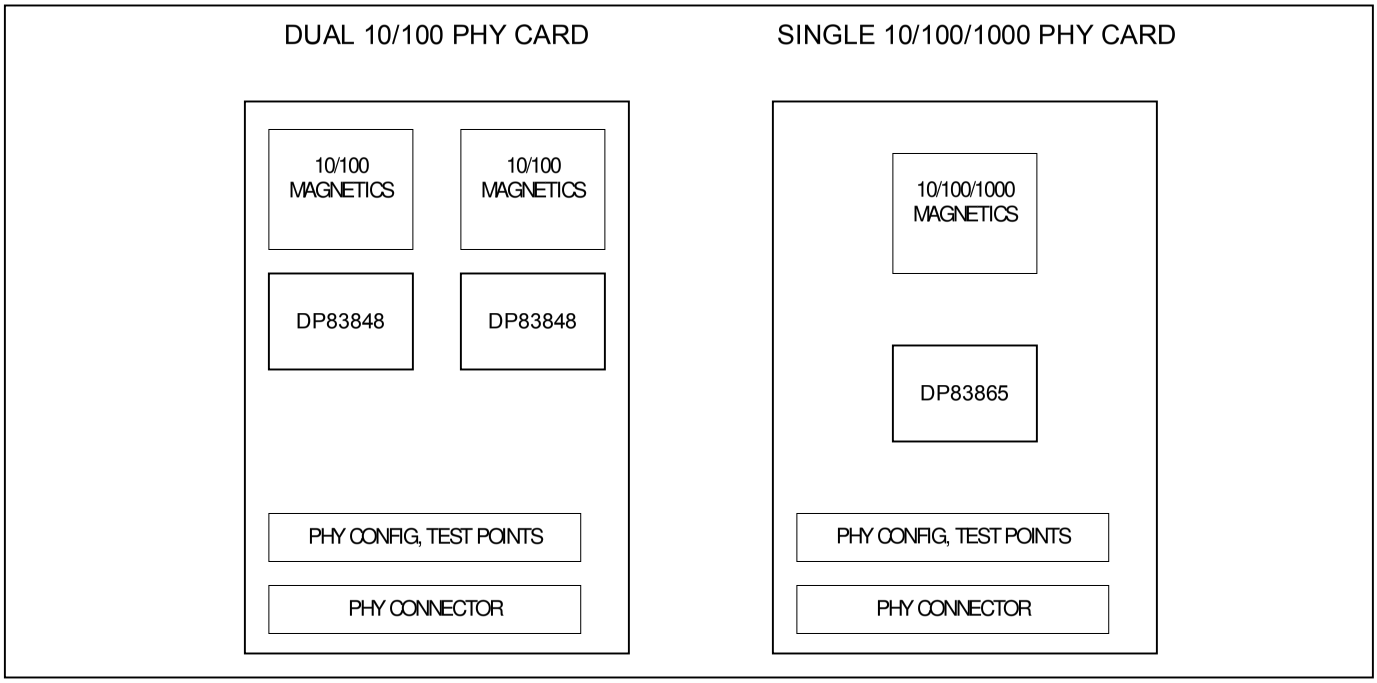
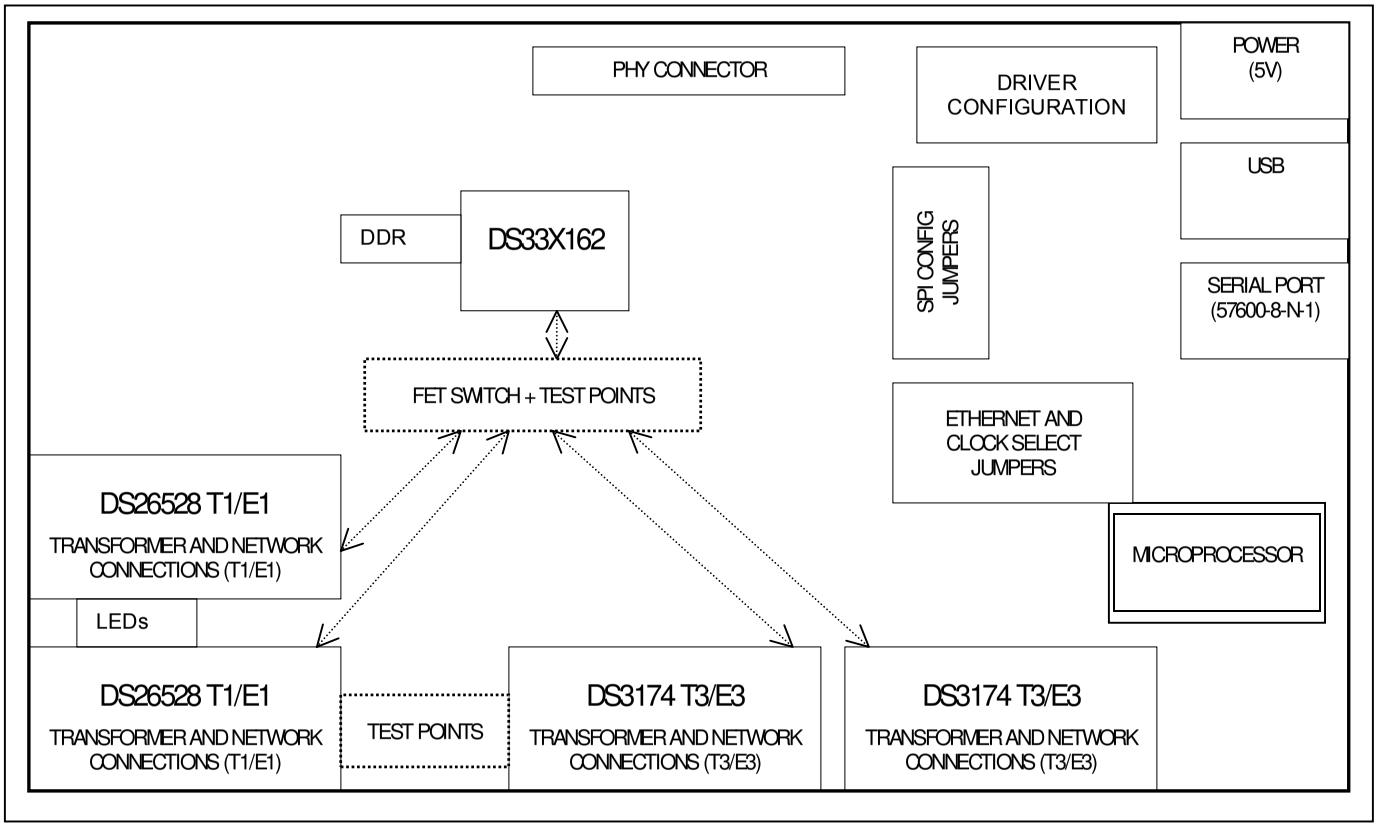


Figure 1-2. DS33X162DK Board Floorplan—Main Board



2. PCB Errata

DS33X162DK02A0 board errata:

- There are no errata associated with the DS33X162DK02A0.

3. File Locations

This demo kit relies upon several supporting files, which are provided on the CD-ROM and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33X162DK.

All locations are given relative to the top directory of the CD-ROM/zip file **DS33X162_cfg_demo_gui**. The DS33X162, DS3174, and DS26528 register definition files and configuration files are listed in Table 3-1.

Table 3-1. File Details

FILE NAME	FILE USAGE
. _DS33X162_GlobalMicroport.def	Top-level definition file to select in ChipView's register mode. This file will autoload the remaining definition files for the DS33X162. (Note that the wan files still need to be loaded (either DS).)
.\DS33X162_Lan.def .\DS33X162_BufferMan.def .\DS33X162_EncapDecap.def .\DS33X162_Vcat.def .\DS33X162_SerialPort.def	DS33X162 dependent files. These are called by the ds33x162_GlobalMicroport.def file listed above.
.\DS33X162_lan_T3wan_ext.mfg	File for manually configuring the DS33X162 to interface with the DS3174.
.\DS33X162_lan_T1wan_ext.mfg	File for manually configuring the DS33X162 to interface with the DS26528.
.\x162_wan1.eset	GUI interface for loading settings when running the Xchip plug-in (launched from the **Tools** menu of the ChipView program).
.\te3_ds3174\DK_ports*\ds3174_evbrd.def Note that there are two folders: **DK_ports_4to1_CS4** and **DK_ports_8to5_CS3**.	Top-level definition file to select the DS3174 T3/E3 transceiver. This file will autoload the remaining definition files for the DS3174.
.\te3_ds3174\ DK_ports*\misc1_p1.def .\te3_ds3174\ DK_ports*\feac_frac_p1.def .\te3_ds3174\ DK_ports*\ttrace_p1.def .\te3_ds3174\ DK_ports*\ds3_p1.def .\te3_ds3174\ DK_ports*\e3751_p1.def .\te3_ds3174\ DK_ports*\e3832_p1.def .\te3_ds3174\ DK_ports*\port1.def	DS3174 dependent files. These are called by the ds3174_evbrd.def file listed above. Files for port 1 are shown; other ports are not listed here.
.\te3_ds3174\ DK_ports_8to5_CS5 \ t3_config_dlb.mfg	DS3174 configuration file for T3 mode.
.\te3_ds3174\ DK_ports_8to5_CS5 \t3_config_AlignedSync_dlb.mfg	DS3174 configuration file for T3 mode. Aligns sync pulses by use of bulk write feature.
.\te3_ds3174\DK_ports_8to5_CS5\ds33x162_no_lb_vcat_ports_5to8_T3.mfg	DS33X162 configuration file for vcat T3 mode.
.\te3_ds3174\DK_ports_4to1_CS4\t3_config_dlb.mfg	DS3174 configuration file for T3 mode.

FILE NAME	FILE USAGE
.\te3_ds3174\DK_ports_4to1_CS4\t3_config_AlignedSync_dlb.mfg	DS3174 configuration file for T3 mode. Aligns sync pulses by use of bulk write feature.
.\te3_ds3174\DK_ports_4to1_CS4\ds33x162_no_lb_vcat_ports_1to4_T3.mfg	DS33X162 configuration file for vcat T3 mode.
.\ds26528\....\DS26528_GLOBAL_T1.def Note that groups of definition files exist for both T1 and E1 modes and also for ports 1 to 8 and ports 9 to 16. This results in a total of four file groups. Only one group is shown here.	Top-level definition file to select the DS26528 T1/E1 transceiver. This file will autoload the remaining definition files for the DS26528.
.\ds26528\...\DS26528_1_LIU_BERT.def .\ds26528\....\DS26528_1_T1.def	DS26528 dependent files. These are called by DS26528_GLOBAL_T1.def file listed above. Files for port 1 are shown; other ports are not listed here.
.\ds26528\ DK_wan_8to1_CS2\T1\DS26528_t1_config.mfg	DS26528 configuration file for T1 mode.
.\ds26528\ DK_wan_8to1_CS2\T1\ds26528…_t1_config_master_bulkWr.mfg	DS26528 configures all 8 ports identically using bulk write mode. Places device in master mode, where TSYNC is an output.
.\ds26528\ DK_wan_8to1_CS2\T1\ds33x162_no_lb_vcat_4ports.mfg	DS33X162 configuration file for vcat mode (ports 1 to 4).
.\ds26528\ DK_wan_8to1_CS2\T1\ds33x162_16ports_vcg.mfg	DS33X162 configuration file for vcat mode (ports 1 to 16).
.\ds26528\ DK_wan_8to1_CS2\disable_framer_lb.mfg .\ds26528\ DK_wan_8to1_CS2\looptime.mfg	DS26528 partial configuration files. These files should be run after a full configuration is made.
*.eset	GUI interface for loading settings when running the Xchip plug-in (launched from the **Tools** menu of the ChipView program).
.\ds26528\ DK_wan_8to1_CS2\E1*.*	Similar files exist for ports 1 to 8 E1 mode.
.\ds26528\ DK_wan_9to16_CS2\[E1 | T1]*.*	Similar files exist for ports 9 to 16 E1 and T1 mode.

4. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the demo kit (DK) software. Text in **bold and underlined** refers to items from the Windows operating system.

4.1 Powering Up the Demo Kit

- Connect the PCB power jack to the wall adapter. A 2.5A supply is recommended.
- Connect the RS232 serial cable or USB cable between the host PC and the demo kit.
- Verify that the jumpers are configured as described in Table 5-1.

4.1.1 General

- Upon power-up the power LEDs (DS01, DS02, DS03 green) will be lit. The DS3174 transceiver LEDs will not be lit. The DS26528 transceiver RLOS + LTC LED will be lit if the device drivers are disabled.
- PHY LINK LED should be lit if an Ethernet cable is connected.

Following are several basic system initializations.

4.2 Basic DS33X162 Initialization

This section covers three basic methods for configuring the DS33X162.

1) Device Driver-Based Configuration. If the pins J02.1+J02.2 are unjumpered, the device driver will auto configure the DS33X162 upon power-up. This enables traffic to pass from the Ethernet port to the serial port. Refer to the device driver documentation for further details. To load the GUI interface for the device drivers, go to the ChipView register mode **Tools** menu and select **Tools→Plugins→DS33XW Device Driver Demo**.
2) Register-Based Configuration—Port 1 T1 Mode
    a) Install jumper J02.1+J02.2 to disable device drivers, and then reset the board. Ensure that J01.1+J01.2 is not installed.
    b) Launch **ChipView.exe** and select **Register View**.
    c) When prompted for a definition file, pick the file named **_DS33X162_GlobalMicroport.def**. Six additional definition files will load.
    d) Go to the **File** menu and select **File→Definition File**. When prompted, select **DK_wan_8to1_CS2\T1\DS26528_GLOBAL_T1.def**.
    e) Go to the **File** menu and select **File→Memory Config File→Load .MFG** file. When prompted, select the file named **DS33X162_lan_T1wan_ext.mfg**.
    f) Go to the **File** menu and select **File→Memory Config File→Load .MFG** file. When prompted, select the file named **DK_wan_8to1_CS2\T1\ds26528_t1_config.mfg**.
3) Register-Based Configuration—Port 1 T3 Mode
    a) Install jumper J02.1+J02.2 to disable device drivers, and then reset the board. Ensure that J01.1+J01.2 is installed.
    b) Launch **ChipView.exe** and select **Register View**.
    c) When prompted for a definition file, pick the file named **_DS33X161_GlobalMicroport.def**. Six additional definition files will load.
    d) Go to the **File** menu and select **File→Definition File**. When prompted select **ds3174_evbrd.def**.
    e) Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **DS33X162_lan_T3wan_ext.mfg**.
    f) Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **DK_ports_4to1_CS4\t3_config_dlb.mfg**.

4.2.1 Additional Configuration for DS33X162

- Using either a patch or crossover cable, connect the Ethernet connector to an ordinary PC or network test equipment. This should cause the link LED to turn on.
- Place a loopback connector at the T1/E1 network side; RLOS and LTC LEDs should go out.
- At this point any packets sent to the DS33X162 are echoed back. Incoming packets (i.e., ping) should cause the **Activity LED** to blink.
- Note that ChipView.exe display settings can be changed using the **Options→Settings** menu.

4.3 Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is *not* the recommended frame source for testing. The ping command goes through the computer's TCPIP stack and sometimes will not be sent out the PC's network connector (i.e., if the PC's ARP cache is out of date). Additionally, ping requires two PCs, as a Windows PC with only one adapter cannot ping itself (a local ping gets sent to "local host" instead of out the connector). However, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be accomplished using CommView. A time-limited demo is available at www.tamos.com/products/commview.
- Wireshark is an excellent (and free) packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters the PC has a different IP address for each adapter. Test equipment allows selection of either adapter. Operating -system-based network traffic is sent out of the default adapter; usually this is the adapter that has recently had connection to a live network.

5. LEDs, Configuration Switches, Jumpers, and Connectors

The DS33X162DK has several configuration switches, oscillators, and jumpers. Table 5-1 provides a description of these signals, given in order of appearance on the PCB, from top to bottom and then left to right (with the board held so that the RS232 and USB connectors are on the right-hand side of the board).

Table 5-1. Main Board PCB Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
YB01 (bottom of PCB)	125MHz Oscillator	—	52	DS33X162 SysClock.
JB01, JB02 (bottom of PCB)	PHY/Ethernet Interface	Card Installed	88	Connector and Test Points for PHY Card Connector. A PHY card (provided) should be installed in this connector.
J01	Mode select for Ports 1 to 8	Not Installed (set for T1/E1 mode)	53	Install jumper to enable T3/E3 mode; remove jumper to set T1/E1 mode. This jumper controls FET switches U04 to UB20. There are a total of 8 jumpers used for controlling ports 1 to 8.
J02	Configuration. All Jumpered. Schematic page 53.	• P1+P2: Jumper to disable drivers (remove to enable drivers). • P3+P4: Jumper to disable interrupt handlers (this jumper is only valid when drivers are enabled). • P5+P6: Jumper to set for SourceTime—WAN ports 1 to 8 TxClock driven by oscillator. Remove to set for LoopTime—WAN TxClock driven by RxClk. (This jumper is only valid when drivers are enabled.) • P7+P8: Jumper to set for SourceTime—WAN ports 9 to 16 TxClock driven by oscillator. Remove to set for LoopTime WAN TxClock driven by RxClock. (This jumper is only valid when drivers are enabled.)		
SW01	System Reset	—	54	System reset.
DS01, DS02, DS03	LED	ON		Power OK LEDs for 1.8V, 2.5V, and 3.3V power supplies. All three LEDs must be lit.
J03	USB	—	58	USB Interface. See folder marked **USBdrivers FT245** for drivers.
J04	RS232 DB9 Connector	—	58	RS232 DB9 Connector. Operates in ASCII mode at 57.6K,8,N,1.
J15	Power Jack	—	54	System Power. Always connected to 5V wall adapter (provided).
JP01	DS33X162 Pin	Jumper P2+3	53	DS33X162 HIZ pin.
JP02	DS33X162 Bias RMII	Jumpered P1+2 (low)		Jumper P1+2 for MII Mode. Jumper P2+3 for RMII Mode. (RMII mode is not available in this demo kit.)
JP03	DS33X162 Bias DCE	Jumpered P1+2 (low)		Jumper P1+2 for DTE Mode. Jumper P2+3 for DCE Mode. (This demo kit does not support DCE mode.)
JP08	PHY Clock In	Jumper P2+3	52	PHY Clock Input. Set for P2+3 in 10/100 mode, driving PHY with 25MHz oscillator. Setting P2+1 drives with DS33X162 RefClk with PHY 125MHz clock (1000Mb mode only).

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
YB02 (Bottom of PCB)	25MHz Oscillator	—	52	25MHz Oscillator. Used for PHY clock in (MII+GMII). Used for DS33X162 RefClk in MII mode.
YB02	PHY RefClk	25MHz	52	PHY Reference Clock. Populated with 25MHz clock in MII mode.
DS04, DS05, DS06	Interrupt LED	—	44	Interrupt LEDs for X162, T3. and T1 Devices.
DS08	Kit Status LED	Off	58	Kit Status LED. Currently not assigned to any software function.
JP07, JP09 to JP12	DS33X162 SPI Test Points	All Jumpered P1+2	43	SPI Test Points for DS33X162. Jumpers are installed to connect the DS33X162 to the processor Data port to the FPGA data pins. Connecting pins 2+3 connects DS33X162 to processor SPI port.
JP05	DS33X162 Bias SPI SWAP	Jumpered P1+2	43	Processor default is to transfer MSB first. Jumper P1+2 to match this setting.
JP04, JP06	DS33X162 Bias SPI CPHA Bias SPI CPOL	Both Jumpered P1+2	43	Processor default is to have normal phase and idle high. See Section 6.3 for further SPI detail.
J05, J06	Test Points	Not used	59	Address Data Bus Test Points. See Section 6.2 regarding control by external processor. Silkscreen for these signals is provided a few inches to the left of the signals.
J09	JTAG	Not Used	60	JTAG connector for programming Lattice FPGA
J16	RJ45 T1E1	User option	63	T1/E1 Connectors for Ports 9 to 16.
DS09 to DS16	RLOS LED	—	69	RLOS LED for DS26528 Ports 9 to 16.
J08	RSYNC Test Points	—	45	Test Points for DS33X162 RSYNC.
J07	RDATA Test Points	—	45	Test Points for DS33X162 RDATA.
J11	RGCLK Test Points	—	45	Test Points for DS33X162 RGCLK.
J10	TDATA Test Points	—	45	Test Points for DS33X162 TDATA.
J14	DS33X162 JTAG	Jumpered P1+3 P7+9	53	JTAG for DS33X162, DS26528, and DS3174. DS33X162 can be isolated from DS26528 and DS3174. Jumpers on P1+3 and P7+9 prevent the devices from entering JTAG mode.
JP13	DS26528 TCLK	Jumpered P1+2	44	DS26528 TCLK Selection for Ports 5 to 8. Jumper pins 1+2 to drive TCLK with RefClk. Jumper pins 2+3 to drive TCLK with TCLK oscillator.
JP14	DS26528 TCLK	Jumpered P1+2	44	DS26528 TCLK Selection for Ports 12 to 16. Jumper pins 1+2 to drive TCLK with RefClk. Jumper pins 2+3 to drive TCLK with TCLK oscillator.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J19	Join DS26528 REFCLKs	Not Jumpered	44	Join reference clocks on DS26528 ports 1 to 8 and ports 9 to 16. This jumper should only be installed when one of the DS26528 devices is in slave mode, and can be a source of bit errors if it is installed with both devices in master mode.
J13	DS26528 TSYNC	Jumpered	76	Jumpered such that all DS26528 ports receive the same TSYNC.
J18	DS26528 TSYNC	Jumpered	68	
J8, J7, J3, J4	DS26528 TGCLK	Not Jumpered	68, 76	Test Points for DS26528 TGCLK.
J17, J9	DS3174 TGCLK	Not Jumpered	81,86	Test Points for DS3174 TGCLK.
J20, J12	DS3174 TSOFO	Not Jumpered	81, 86	Test Points for DS3174 TSOFO.
YB05	Oscillator	—	46	Oscillator for T3/E3 MCLK. Silkscreen and target are provided on topside of PCB.
YB06	Oscillator	—	46	Oscillator for T3/E3 TCLK. Silkscreen and target are provided on top side of PCB.
DS22, DS27, DS29, DS31, DS23, DS28, DS30, DS32	RLOS LED	—	69	RLOS led for DS26528 ports 1-8
J24	RJ45 T1E1	User option	63	T1E1 connectors for ports 9-16
DS17, DS18,DS26, DS20, DS24, DS19, DS25, DS21	LED	User setting (OFF)		DS3174 General-Purpose I/O LED. Not configured by ini files.
J26 to J41	WAN Network Connection	—	80, 85	T3/E3 Jumpers for Network Interface. Used with 2-pin coax adapter (provided).
J42	OnCe	Not used		OnCe debug connector for MMC2107 microcontroller.
J25	Flash VPP	Not used		For programming flash memory.

Table 5-2. Dual-Port PHY Card Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J91, J92	Ethernet Connection	—	109, 111	RJ45 Ethernet Connector. Used in 10/100 modes.
DS65, DS63 DS64, DS66	LED Link	1 of each pair should be lit (when linked)	109, 111	LED to Indicate Link.
DS67,DS68, DS70, DS69	LED Speed	—	109, 111	Lit for 100Mb; off when in 10Mb mode.
DS74, DS72, DS73, DS71	LED Activity	—	109, 111	Blinks when a packet is transmitted or received

		AN_EN	AN1	AN0	FORCED MODE
JP68 JP67 JP69, JP70 JP71, JP72	PHY CONFIG	0	0	0	10BASE-T, Half-Duplex
		0	0	1	10BASE-T, Full-Duplex
		0	1	0	100BASE-T, Half-Duplex
		0	1	1	100BASE-T, Full-Duplex
		1	0	0	10BASE-T, Half-/Full-Duplex
		1	0	1	10BASE SE-Tx, Half-/Full-Duplex
		1	1	0	100BASE-T , Half-Full Duplex
		1	1	1	100BASE-T, Half-Full Duplex

JP73, JP75	RMII	Jumpered P1+2	109, 111	Jumper Pins 1+2 for MII Mode. When in RMII mode, the PHY RefClk must be 50MHz. This clock is sourced from YB02 on the main board.
JP74, JP76	MDIX	Jumpered P2+3	109, 111	Jumper pins 2+3 to enable MDIX.

Table 5-3. Single-Port PHY Card Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J1	Ethernet Connection			RJ45 Ethernet Connector. Used in 10/100 and Gigabit modes.
DS75	LED Duplex	—		LED is on in full-duplex mode.
JP77	Bias PHY Non-IEEE	Jumper P2+3 (high)		Jumper P2+3 to enable IEEE-compliant operation.
JP78	Bias PHY ManMDIX	Jumper P1+2 (high)		Default MDIX setting P1+2 PHY is set to straight mode; P2+3 PHY is in crossover mode.
DS76	LED Activity	—		Flashes for PHY Tx-Rx activity.
DS78+79 DS80+81 DS82+83	LED Link Speed	1 of the 6 should be lit (when linked)		LED to indicate link speed: 1000, 100, or 10Mbps. Only 1 of the 6 LEDs should be lit. See JP15 + JP101 description for setting in GMII mode vs. MII mode.
JP82 + JP81	Bias PHY Speed1 + Speed0	Jumper P1+2 (low) P1+2 (low)		If autonegotiation is enabled, this setting advertises capability for 10/100/1000 speeds. If autonegotiation is disabled, this setting forces 10Mb mode.
		Jumper P2+3 (high) P2+3 (high)		If autonegotiation is enabled, this setting advertises capability for 10/100 speeds. If autonegotiation is disabled, this setting is not legal.
		Jumper P2+3(high) P1+2 (low)		If autonegotiation is enabled, this setting advertises capability for 1000 speeds. If auto negotiation is disabled, this setting forces 1000Mb mode.
Note: When the PHY is in GMII mode, the REFCLK pin on DS33X162 must be driven with 125MHz (JP08_2+1). Additionally, MacClkEn must be enabled (JP82_2+3). In MII mode, RefClk must be driven with 25MHz (JP08_2+1). Here MacClkEn does not matter, but could be disabled to save power and reduce noise.				
JP89	Bias PHY Duplex	Jumper P2+3 (high)		Jumper P2+3 to enable full duplex; jumper P1.2 to force half duplex.
JP86	Bias PHY ANEN	Jumper P2+3 (high)		Jumper P2+3 to enable autonegotiation.
JP79	Bias PHY MultiEn	Jumper P1+2 (high)		PHY Advertisement Setting. P2+3 selects multiple node priority (switch or hub). P1+2 selects single node priority (NIC).
JP80	Bias PHY MdixEn	Jumper P2+3 (low)		P2+3 enables pair swap mode, P1+3 disables pair swap mode
JP82	Bias PHY MacClkEn	Jumper P2+3 (low)		P2+3 PHY clock to MAC output is enabled; P1+2 PHY clock to MAC output is disabled. MAC clock only needs to be enabled in Gigabit mode.
TP17	Test Point			MAC Clock Test Point.

6. Register Access

6.1 Address Map

The external device address space begins at 0x81000000. All offsets given in Table 6-1 are relative to this offset.

Table 6-1. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification .
0X1000 to 0X1FFF	DS33X162	DS33X162 uses CS1.
0X4000 to 0X5FFF	DS26528	DS26528 T1/E1 device, ports 1 to 8. Uses CS_X2.
0X6000 to 0X7FFF	DS26528	DS26528 T1/E1 device, ports 9 to 16. Uses CS_X3.
0X8000 to 0X9FFF	DS3174	DS3174 T3/E3 device ports 1 to 4. Uses CS_X4.
0XA000 to 0XBFFF	DS3174	DS3174 T3/E3 device, ports 5 to 8. Uses CS_X5.

All device registers can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

6.2 Control Through External Processor

The demo kit is intended to be controlled using the on-board microcontroller and a host PC. However, the demo kit has jumper points to allow it to be controlled by an external processor. The DS33X162 can be controlled in SPI mode by attaching to the signals at JP09, JP10, JP11, and JP12. Alternately, the DS33X162 and transceivers (DS26528 and DS3174) can be controlled by jumpering J05.12+14 and then connecting to J05 and J06. Doing so pulls up the tristate_bus signal and places the FPGA in a high-impedance mode (see the Address Map section).

6.3 SPI Mode

The DS33X162 has an option to use both parallel and SPI mode. SPI mode is addressed differently than devices that use a parallel address/data bus. In SPI mode, the DS33X162 does not have an address offset; its base address starts at 0x00.

Table 5-1 details the default bias levels for SPI configuration pins. To change these settings the processor's SPI settings must also change. A special set of definition files must be used when in SPI mode. These are contained in the subfolder **.\DS33X162_spi**. The processor SPI settings can be changed in ChipView's terminal mode using the **SPISG S** function.

6.4 MAC and PHY Registers

The MAC and PHY are accessed indirectly. This process is automated by the indirect register module. To load this module, first select the DS33X162 device driver demo plugin using the **Tools→Plugins** menu. Once the device driver demo loads, select the indirect register module from the **Tools→Indirect register** menu. The first tab of the menu has a selection for the device bus mode. Select **SPI mode** when using the DS33X162.

To test that the indirect register section is working, try to reset the PHY. Select the **PHY** tab, change the **Padd** field to 00001 to select the PHY at MDIO address 1. In the **Data write** field enter 00 00 80 00. Click the **Write PHY** button. At this point the link LED of the PHY should go out (and turn back on within a few seconds).

7. Additional Information/Resources

7.1 DS33X162 Information

For more information about the DS33X162, refer to the DS33X162 data sheet available on our website at www.maxim-ic.com/DS33X162.

7.2 DS33X162DK Information

For more information about the DS33X162DK, including software downloads, refer to the DS33X162DK data sheet available on the our website at www.maxim-ic.com/DS33X162DK.

7.3 Technical Support

For additional technical support, go to www.maxim-ic.com/support.

8. Component List

Table 8-1 shows the component list for the DS33X11 and DS33X162 demo kits and resource cards. This BOM contains the part listing for four boards. These boards are the DS33X11DK, DS33X162DK, DualPhyRC, and GigPhyRC. Each reference designator is only used once. For example, U25 only appears on the DS33X11DK and is not used on any of the other boards. See Table 5-1.

Table 8-1. Component List

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C02, C22, C145, CB19, CB23, CB42, CB95, CB129, CB303, CB319, CB445, CB447, CB452, CB460, CB463	15	D CASE TANT 470uF 6.3V 20%	KEM	T491D477M006AS
Reference designators shown on next row	231	0603 CERAM 4.7uF 6.3V MULTILAYER	UNK	ECJ-1VB0J475M
C03, C08, C11, C14, C15, C16, C17, C21, C24, C29, C33, C45, C49, C51, C52, C91, C92, C96, C97, C115, C119, C120, C122, C123, C129, C137, C138, C141, C142, C146, C149, C151, C153, C158, C258, C263, C265, CB01, CB04, CB06, CB09, CB13, CB16, CB17, CB21, CB24, CB26, CB27, CB28, CB36, CB37, CB41, CB44, CB45, CB46, CB47, CB48, CB58, CB60, CB66, CB67, CB74, CB75, CB76, CB78, CB80, CB84, CB92, CB93, CB98, CB99, CB100, CB104, CB107, CB114, CB115, CB116, CB118, CB123, CB125, CB126, CB137, CB138, CB141, CB144, CB151, CB155, CB158, CB163, CB164, CB166, CB170, CB171, CB172, CB179, CB181, CB183, CB185, CB186, CB188, CB189, CB191, CB192, CB193, CB195, CB197, CB198, CB201, CB204, CB209, CB215, CB218, CB221, CB222, CB227, CB229, CB230, CB231, CB234, CB235, CB239, CB243, CB249, CB251, CB255, CB258, CB263, CB264, CB267, CB270, CB271, CB273, CB276, CB277, CB278, CB284, CB287, CB293, CB294, CB297, CB298, CB302, CB304, CB306, CB307, CB320, CB322, CB327, CB328, CB341, CB343, CB344, CB345, CB347, CB348, CB351, CB352, CB353, CB357, CB358, CB364, CB365, CB366, CB367, CB369, CB370, CB371, CB375, CB376, CB379, CB380, CB388, CB392, CB393, CB395, CB396, CB399, CB400, CB401, CB404, CB405, CB406, CB407, CB408, CB409, CB415, CB416, CB423, CB424, CB425, CB427, CB431, CB436, CB438, CB441, CB442, CB446, CB449, CB453, CB454, CB462, CB467, CB760, CB766, CB768, CB777, CB779, CB789, CB790, CB791, CB792, CB793, CB795, CB798, CB802, CB804, CB805, CB807, CB808, CB810, CB812, CB813, CB815, CB816, CB817, CB818, CB824, CB827, CB856, CB857, CB859				
Reference designators shown on next row	114	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
C04, C05, C06, C07, C09, C10, C18, C20, C32, C37, C40, C41, C42, C50, C57, C70, C89, C98, C104, C113, C114, C118, C125, C133, C134, C136, C148, C150, C261, C266, CB03, CB11, CB14, CB20, CB30, CB34, CB52, CB55, CB61, CB69, CB71, CB73, CB83, CB103, CB109, CB112, CB119, CB120, CB128, CB139, CB150, CB157, CB161, CB167, CB173, CB187, CB194, CB205, CB206, CB207, CB213, CB216, CB217, CB219, CB223, CB224, CB225, CB228, CB240, CB256, CB259, CB261, CB275, CB285, CB295, CB300, CB308, CB332, CB350, CB354, CB359, CB361, CB381, CB385, CB391, CB398, CB402, CB413, CB414, CB419, CB428, CB432, CB435, CB439, CB443, CB444, CB448, CB451, CB466, CB468, CB761, CB765, CB770, CB771, CB772, CB776, CB794, CB803, CB806, CB811, CB819, CB823, CB853, CB855				
C110, C112, CB86, CB87	4	L_0603 CERAM 22pF 25V 5% NPO	AVX	06033A220JAT
C156, C259, CB51, CB762, CB763, CB764, CB767, CB769, CB773, CB774, CB775, CB780, CB782, CB786, CB787, CB788	16	0603 CERAM 0.1uF 16V 10%	Phycomp	06032R104K7B20D
C25, C126, CB10, CB31, CB33, CB88, CB89, CB102, CB145, CB146, CB147, CB315, CB333, CB338, CB363, CB368, CB383, CB417, CB418, CB437	20	L_1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
C28, C31, C132, CB25, CB32, CB35, CB38, CB40, CB43, CB56, CB68, CB81, CB85, CB96, CB105, CB313, CB321, CB324, CB372, CB373, CB384, CB394, CB397, CB410, CB411, CB412, CB422, CB450	28	0603 CERAM .1uF 16V 10%	Panasonic	ECJ-1VB1C104K
C39, C44, C54, C55, C56, C60, C61, C64, C99, C100, C101, C102, C103, C105, C106, C107, C108, C109	18	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C58, C63, C67, C69, C73, C76, C77, C86, C87, CB108, CB153, CB208, CB238, CB252, CB253, CB254	16	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
C59, C62, C65, C66, C68, C71, C72, C75, C78, C79, C80, C81, C82, C83, C84, C85, C116	17	1206 CERAM 560pf 50V 5%	AVXZ	12065A561JAT2A
Reference designators shown on next row (begins with C01)	226	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
C01, C12, C13, C19, C23, C26, C27, C30, C34, C35, C36, C38, C43, C46, C47, C48, C53, C74, C88, C90, C93, C94, C95, C111, C117, C121, C124, C127, C128, C130, C131, C135, C139, C140, C143, C144, C147, C152, C154, C155, C157, C260, C262, C264, CB02, CB05, CB07, CB12, CB18, CB22, CB29, CB39, CB49, CB53, CB57, CB59, CB62, CB63, CB64, CB65, CB70, CB72, CB77, CB79, CB82, CB90, CB91, CB94, CB97, CB101, CB106, CB110, CB111, CB113, CB117, CB121, CB122, CB124, CB130, CB131, CB132, CB133, CB134, CB135, CB136, CB140, CB142, CB148, CB149, CB152, CB154, CB156, CB159, CB160, CB162, CB165, CB168, CB169, CB174, CB175, CB176, CB177, CB178, CB180, CB182, CB184, CB190, CB196, CB199, CB200, CB202, CB203, CB210, CB211, CB212, CB214, CB220, CB226, CB232, CB233, CB236, CB237, CB241, CB242, CB244, CB245, CB246, CB247, CB248, CB250, CB257, CB260, CB262, CB266, CB268, CB269, CB272, CB274, CB280, CB282, CB283, CB286, CB288, CB289, CB296, CB299, CB301, CB305, CB309, CB310, CB311, CB312, CB314, CB316, CB317, CB318, CB323, CB325, CB326, CB329, CB330, CB331, CB334, CB335, CB336, CB337, CB339, CB340, CB342, CB346, CB349, CB355, CB356, CB360, CB362, CB374, CB377, CB378, CB382, CB386, CB387, CB389, CB390, CB403, CB420, CB421, CB426, CB430, CB433, CB434, CB440, CB455, CB456, CB457, CB458, CB459, CB461, CB464, CB465, CB469, CB470, CB757, CB758, CB759, CB778, CB781, CB783, CB784, CB785, CB796, CB797, CB799, CB800, CB801, CB809, CB814, CB820, CB821, CB822, CB825, CB826, CB828, CB829, CB852, CB854, CB858				
CB08, CB15, CB54, CB127, CB143, CB279, CB281, CB290, CB291, CB292	10	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
CB265, CB429	2	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
DB01, DB02, DB03	3	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS02, DS03, DS33, DS34, DS35, DS41, DS42, DS43, DS44, DS45, DS46, DS47, DS48, DS49, DS75, DS76, DS77, DS78, DS79, DS80, DS81, DS82, DS83	24	LED, GREEN, SMD	Panasonic	LN1351C
DS04, DS05, DS06, DS07, DS17, DS18, DS19, DS20, DS21, DS24, DS25, DS26, DS36, DS37, DS38, DS39, DS40	17	L_LED, RED, SMD	Panasonic	LN1251C
DS08, DS50, DS63, DS64, DS65, DS66	6	L_LED, GREEN, SMD	Panasonic	LN1351C
DS09, DS10, DS11, DS12, DS13, DS14, DS15, DS16, DS22, DS23, DS27, DS28, DS29, DS30, DS31, DS32, DS71, DS72, DS73, DS74	20	LED, RED, SMD	Panasonic	LN1251C
DS67, DS68, DS69, DS70	4	LED, AMBER, SMD	Panasonic	LN1451C
H01, H02, H03, H04, H05, H06, H07, H08, H09, H10, H11, H12	12	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	4-40KIT4
J01, J12, J13, J17, J18	5	TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	TSW-108-07-T-D
J02, J50	2	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	NA
J03, J43	2	TYPE B SINGLE RT ANGLE, BLACK	MOL	NA
J04, J51	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J05, J06, J48, J49	4	NON POPULATED HEADER, 14 PIN, DUAL ROW, VERT	Samtec	NOPOP-HDR-TSW-107-14-T-D
J07, J08, J10, J11	4	NOPOP TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	NOPOP-TSW-108-07-T-D

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
J09, J14, J20, J21, J22, J23, J52, J53, J57	9	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J15, J46	2	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	DIGIKEY	CP-002AH-ND
J16, J24	2	CONNECTOR, STACKED OCTAL JACK, 64-PIN, SHIELDED	MOL	SD-44520-001
J19, J25, JB06	3	100 MIL 2 POS JUMPER	NA	NA
J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J44, J45	18	L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	TSW-102-07-T-S
J42, J58	2	100 MIL 2*7 POS JUMPER	NA	NA
J47	1	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J54, J93, J94, J95, J96	5	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPULATE	DNP	DNP
J55	1	HEADER, 14 PIN, DUAL ROW, VERT	Samtec	HDR-TSW-107-14-T-D
J56, J98	2	CONNECTOR, PULSEJACK, 16 PIN	Pulse	JK0654218Z
J91, J92	2	CONNECTOR, FASTJACK SINGLE, 8 PIN FOR NATIONAL PHY	Halo Electronics	HFJ11-2450E
J97, J99	2	SOCKET, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	TFM-125-02-S-D-LC
JB01, JB05	2	PLUG, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	SFM-125-L2-S-D-LC
JB02, JB04	2	TEST POINTS FOR SMD 50 PIN, 2 ROW VERTICAL	NA	NA_NOTPOPULATED
JB03	1	100 MIL 2 POS JUMPER DO NOT POPULATE	NOPOP	NA
Reference designators shown on next row (begins with JP01)	49	100 MIL 3 POS JUMPER	NA	NA
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JP27, JP28, JP29, JP67, JP68, JP69, JP70, JP71, JP72, JP73, JP74, JP75, JP76, JP77, JP78, JP79, JP80, JP81, JP82, JP83, JP84, JP85, JP86				
R01, R02, R42, R43, RB01, RB02, RB04, RB39, RB46, RB47, RB62, RB87, RB88, RB89, RB90, RB91, RB107, RB128, RB231, RB232	20	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
R03, R05, RB09, RB10, RB12, RB14, RB26, RB28, RB96, RB97, RB100, RB113, RB114, RB115, RB116, RB118, RB120, RB122, RB123	19	RES 0603 30 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ300V
R04, RB03, RB05, RB07, RB13, RB18, RB23, RB24, RB25, RB92, RB99, RB101, RB104, RB106, RB121	15	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R06, R07, R39, R41	4	RES 0603 24.3 Ohm 1/16W 1%	Panasonic	ERJ-3EKF24R3V
R08, RB06, RB15, RB17, RB19, RB20, RB21, RB43, RB45	9	L_RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R09, R10, R11, R12, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, RB32, RB33, RB48, RB49, RB50, RB51	32	RES 1206 61.9 Ohm 1/8W 1%	Panasonic	ERJ-8ENF61R9V
R13, RB30, RB31, RB60, RB61, RB109, RB110, RB111, RB127	9	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
R36, R40	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R37, R38	2	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB08, RB41, RB98, RB108	4	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB11, RB95	2	RES 0603 1.5K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ152V
RB119, RB246	2	RES 0603 9.76K Ohm 1/16W 1%	Panasonic	ERJ-3EKF9761V
RB125, RB126, RB129, RB245, RB248, RB249	6	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
RB16, RB22, RB131, RB132	4	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F
RB233, RB234, RB235, RB236, RB239, RB241	6	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
RB237, RB238	2	RES 0603 4.87K Ohm 1/16W 1%	Panasonic	ERJ-3EKF4871V
RB27, RB124, RB130, RB247	4	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
RB29, RB34, RB35, RB36, RB37, RB38	6	RES 0603 51 Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	ERJ-3GEY0R00V
RB40, RB44, RB112, RB240, RB242, RB243, RB244	7	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
RB42, RB117	2	RES 0805 10K Ohm 1/10W 1%	Panasonic	ERJ-6ENF1002V
RB52, RB53, RB54, RB55, RB56, RB57, RB58, RB59, RB63, RB64, RB65, RB66, RB67, RB68, RB69, RB70, RB103, RB105	18	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
RB71, RB72, RB73, RB74, RB75, RB76, RB77, RB78, RB79, RB80, RB81, RB82, RB83, RB84, RB85, RB86, RB93, RB94, RB102	19	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
RP01, RP02, RP03, RP04, RP05, RP06, RP41, RP42, RP43, RP44, RP48, RP49, RPB07, RPB10, RPB109, RPB110	16	4 PACK RESISTOR 24 OHM 2 PCT	KOA	CN1J4TTD240G
RP07, RP08, RP09, RP10, RP12, RP45, RP46, RP47, RP50, RP51, RPB15, RPB19, RPB93, RPB98, RPB107, RPB108, RPB131, RPB132, RPB144, RPB145	20	4 PACK RESISTOR 50 OHM 2 PCT	KOA	CN1J4TTD500G
See next row (begins with RP11)	62	4 PACK RESISTOR 30 OHM 5% QUAD 0402	PANASONIC	EXB-N8V300JX

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
RP11, RP13, RP15, RP16, RP17, RP18, RP19, RP20, RP25, RP26, RP27, RP28, RP29, RP30, RP31, RP32, RP33, RP34, RP35, RP36, RP37, RP38, RP39, RP84, RP85, RP86, RP87, RP88, RP89, RP91, RP92, RP93, RP94, RPB05, RPB08, RPB09, RPB11, RPB13, RPB16, RPB18, RPB21, RPB24, RPB25, RPB30, RPB35, RPB43, RPB44, RPB51, RPB52, RPB58, RPB59, RPB60, RPB61, RPB62, RPB63, RPB64, RPB65, RPB84, RPB87, RPB91, RPB99, RPB143				
RP14, RPB04, RPB06, RPB14, RPB20, RPB22, RPB54, RPB55, RPB56, RPB66, RPB77, RPB79, RPB89, RPB92, RPB94, RPB95, RPB96, RPB97, RPB100, RPB101, RPB103, RPB150	22	4 PACK RESISTOR 10K OHM 5% QUAD 0402	PANASONIC	EXB-N8V103JX
RP21, RP22, RP23, RP24, RPB26, RPB27, RPB28, RPB29, RPB31, RPB32, RPB33, RPB34, RPB36, RPB38, RPB39, RPB40, RPB41, RPB42, RPB45, RPB46, RPB47, RPB49, RPB50, RPB53	24	4 PACK RESISTOR 20 OHM 5% QUAD 0402	PANASONIC	EXB-N8V200JX
RP40, RP90, RPB01, RPB02, RPB03, RPB12, RPB17, RPB37, RPB57, RPB67, RPB68, RPB69, RPB70, RPB71, RPB74, RPB78, RPB80, RPB82, RPB83, RPB85, RPB90, RPB104, RPB149	23	4 PACK RESISTOR 1K OHM 5% QUAD 0402	PANASONIC	EXB-N8V102JX
RPB23, RPB48, RPB72, RPB73, RPB75, RPB76, RPB81, RPB86, RPB102, RPB105, RPB133, RPB135, RPB147	13	4 PACK RESISTOR 330 OHM 5% QUAD 0402	PANASONIC	EXB-N8V331JX
RPB88, RPB106, RPB134, RPB136, RPB137, RPB138, RPB139, RPB140, RPB141, RPB142, RPB146, RPB148	12	4 PACK RESISTOR 2.2K OHM 5% QUAD 0402	PANASONIC	EXB-N8V222JX
SW01	1	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
T01, T02, T03	3	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TB01, TB02, TB03, TB04	4	XFMR, XMIT/RCV, 1 TO 2 AND 1 TO 1, SMT 32 PIN	Pulse	TX1475
TB05	1	XFMR, 1CT_1CT & 1CT_2CT, 12P SMT	Pulse	TX1277
TP01, TPB01, TPB02, TPB07, TPB08, TPB09	6	TEST POINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U01, U19	2	USB UART (USB - 8 bit FIFO), 32 PIN LQFP	FTD	FT245BM
U02	1	ETHERNET EXTENSION DEVICE 16 WAN 2 LAN	DALLAS SEMICONDUCTOR	NA
U03, UB29	2	SPI SERIAL EEPROM 2M 8 PIN SOIC 2.7V to 3.6V	Atmel	AT25F2048N-10SU-2.7
U04, U05, U06, U07, U11, U22, UB12, UB14, UB15, UB17, UB19, UB34	12	IC, OCT BUFFER FET SWITCH 5V 20-PIN TSSOP	Philips	CBT3244APW
U08, U15	2	IC, OCTAL TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS26528N
U09, U10, U12, UB13, UB18, UB20	6	BAD PARTNUM IC, OCT BUFFER FET SWITCH 5V TSOP	Philips	CBT3244APW-T
U13, U23, UB22, UB33	4	CYPRESS SRAM, LAB STOCK	NA	NA
U14, U24	2	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	Lattice	LFEC3E-3T144C

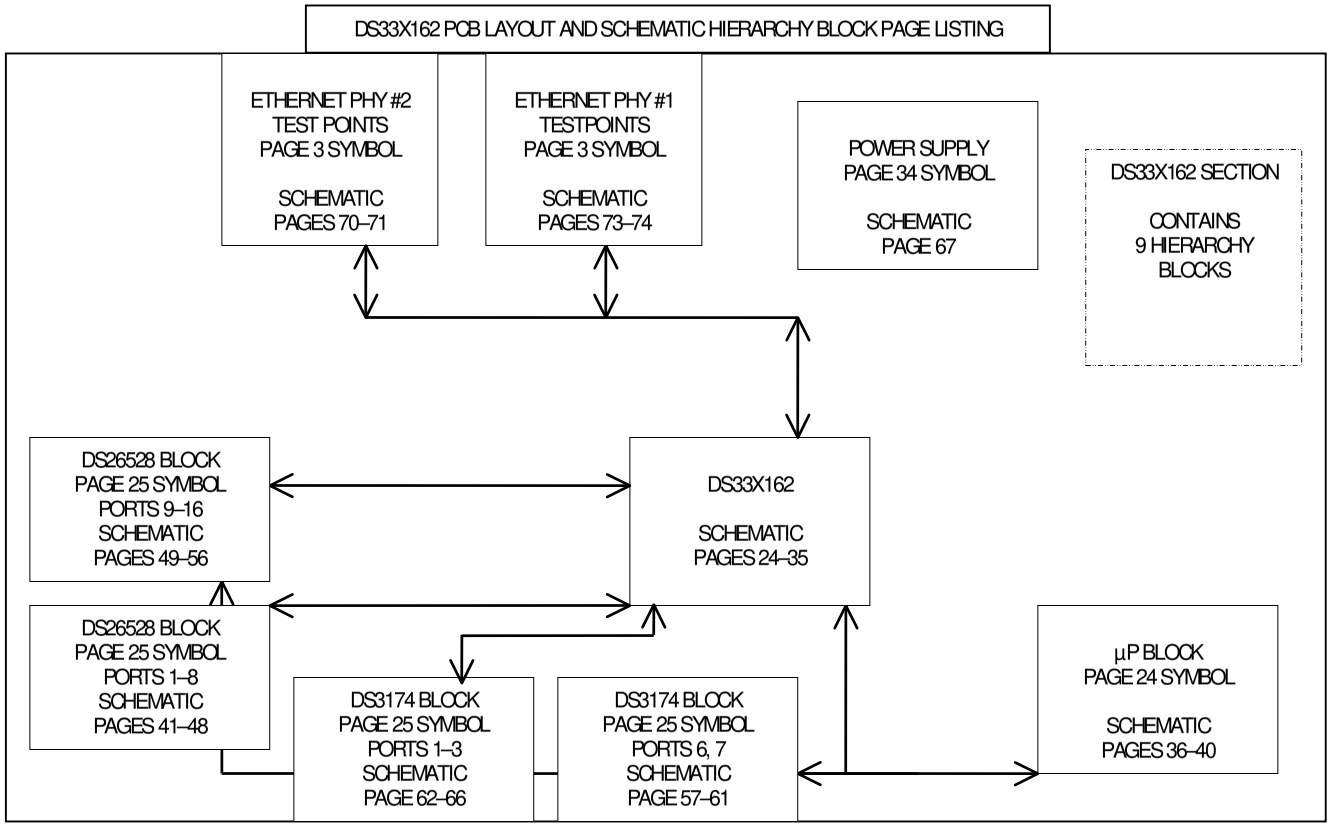
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U16, U17	2	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYs FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U18, U27	2	MMC2107 PROCESSOR	Motorola	MMC2107
U20	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U21	1	IC, SINGLE T1 E1 J1 TRANSCEIVER, 10X10 LQFP, 64-PIN	Dallas Semiconductor	DS26521
U25	1	ETHERNET EXTENSION DEVICE 1 WAN 2 LAN	Dallas Semiconductor	NA
U26, U33	2	GIG PHYTER V, 10/100/1000 ETHERNET PHYSICAL LAYER, 128 PIN QFP	National Semiconductor	DP83865BVH
U31, U32	2	IC, DP83848C PHYTER 10/100 ETHERNET TRANSCEIVER, 48 PIN TQFP	National Semiconductor	DP83848C
UB01, UB28, UB70	3	HIGH SPEED BUFFER	FAIRCHILD	NC7SZ86
UB02, UB36	2	SINK SOURCE DDR TERMINATION REGULATOR	AVNET	LP2995M
UB03, UB35	2	DOUBLE DATA RATE (DDR) SDRAM 2-2-2 TIMING 256MBITX16 TSSOP	MICRON	NA
UB04, UB30	2	IC, LINEAR REG 1.5W, 1.8V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-18
UB05, UB06, UB37, UB38	4	IC, LINEAR REG 1.5W, 2.5V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-25
UB07, UB08, UB09, UB11, UB16, UB23, UB24, UB25, UB26, UB27	10	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB10, UB31	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
UB21, UB32	2	IC, LDO REGULATOR WITH RESET,1.20V OUTPUT 300 MA, 6 PIN SOT23	Maxim	MAX1963EZT120-T
XB01, XB02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, YB07	2	XTAL, LOW PROFILE, 6.00 MHZ	Pletronics	LP49-26-6.00M
YB01, YB03, YB09, YB11	4	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 125.000 MHZ	ECLIPTEK	EC1325HSTS-125.000M+SOCKET
YB02, YB10	2	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ	SaRonix	NTH089AA3-25.000+SOCKET
YB04	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB05	1	OSCILLATOR + Socket, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	SOCKET+NTH039A3-2.0480

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
YB06	1	OSCILLATOR + Socket, CRYSTAL CLOCK, 5V - 1.544 MHZ	SaRonix	SOCKET+NTH039A-1.5440
YB08	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
YB12	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 1.544 MHZ	SaRonix	NTH039A3-1.5440
YB13	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

9. Schematics

The DS33X162DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation follows. The schematic contains nine hierarchal blocks: the microcontroller, DS26528, DS3174, Ethernet PHY, Ethernet Test Points, and Power Supply.

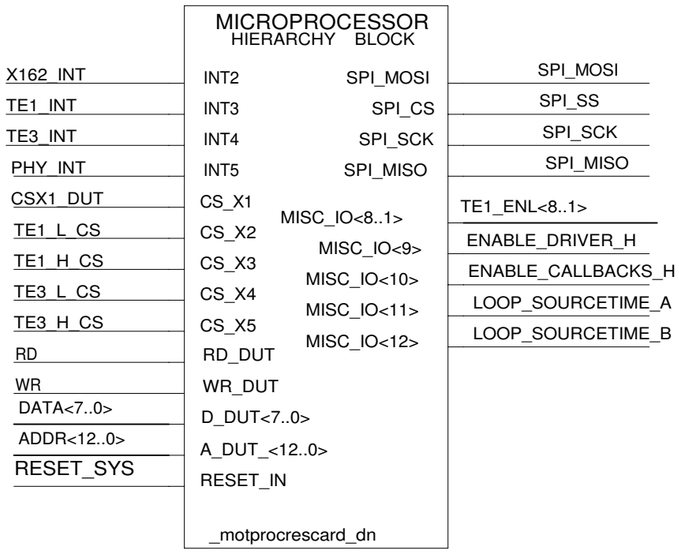
All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

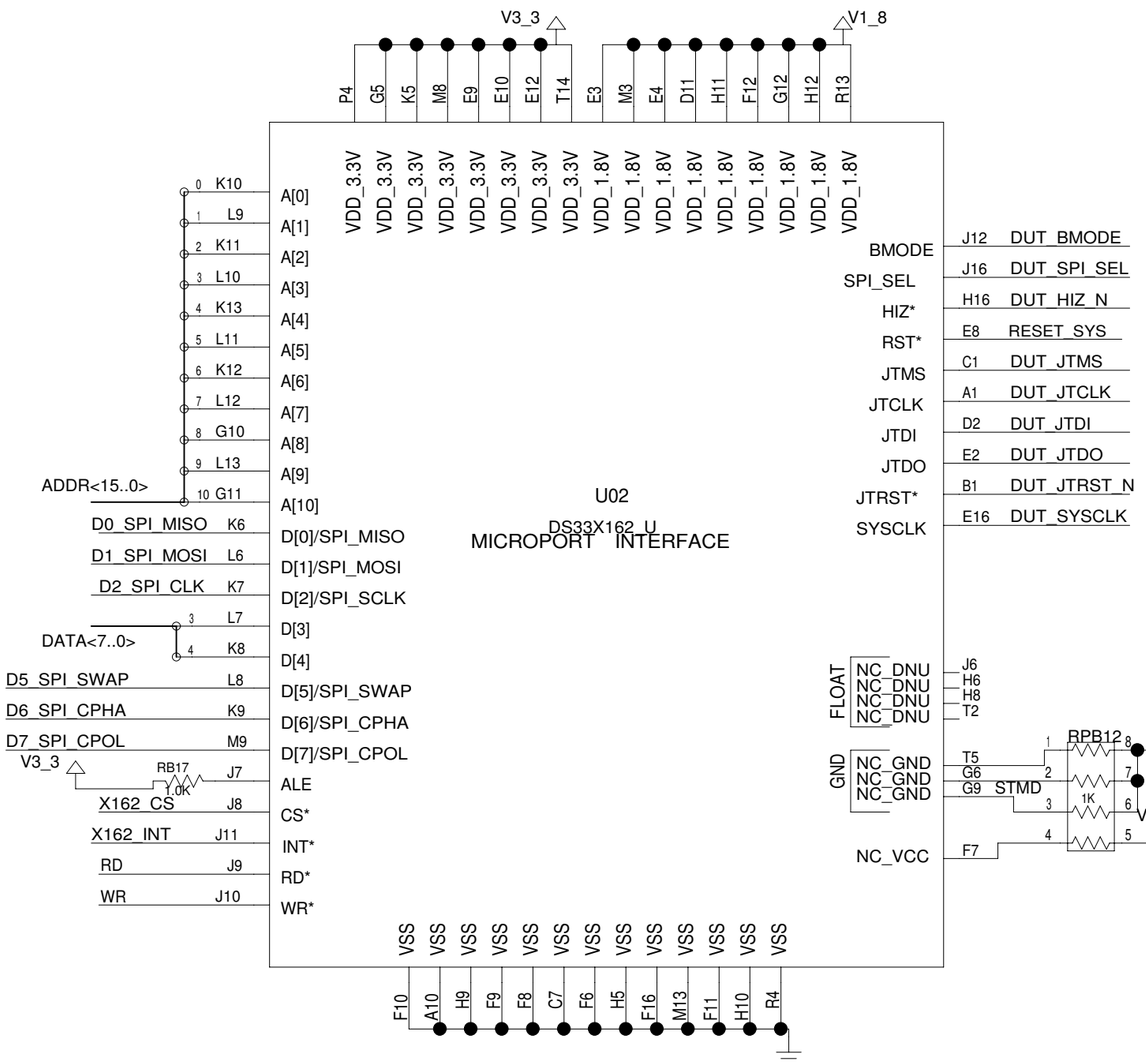


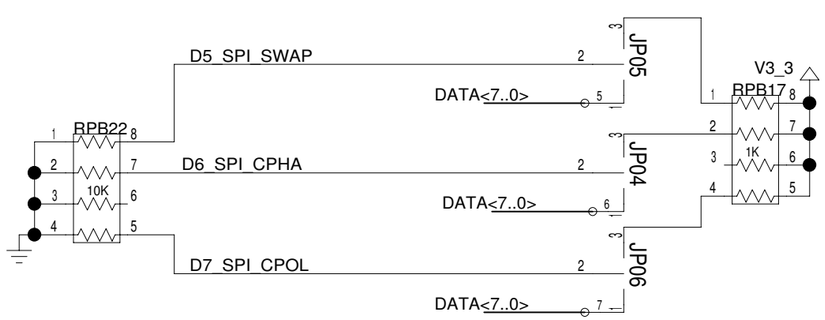
Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

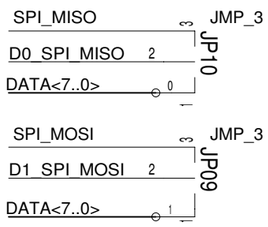
DS33X162DK CONTENTS / INDEX

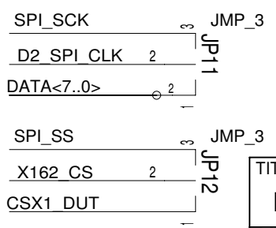
SCHEMATICS FOR GIGABIT AND DUAL PHY CARDS AT
ARE PLACED AT THE END OF THE DS33X162DK SCHEMATIC







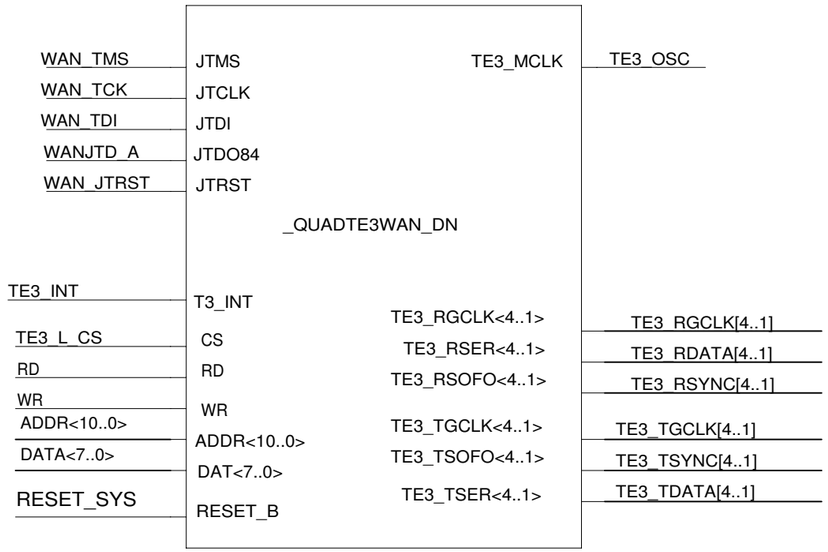


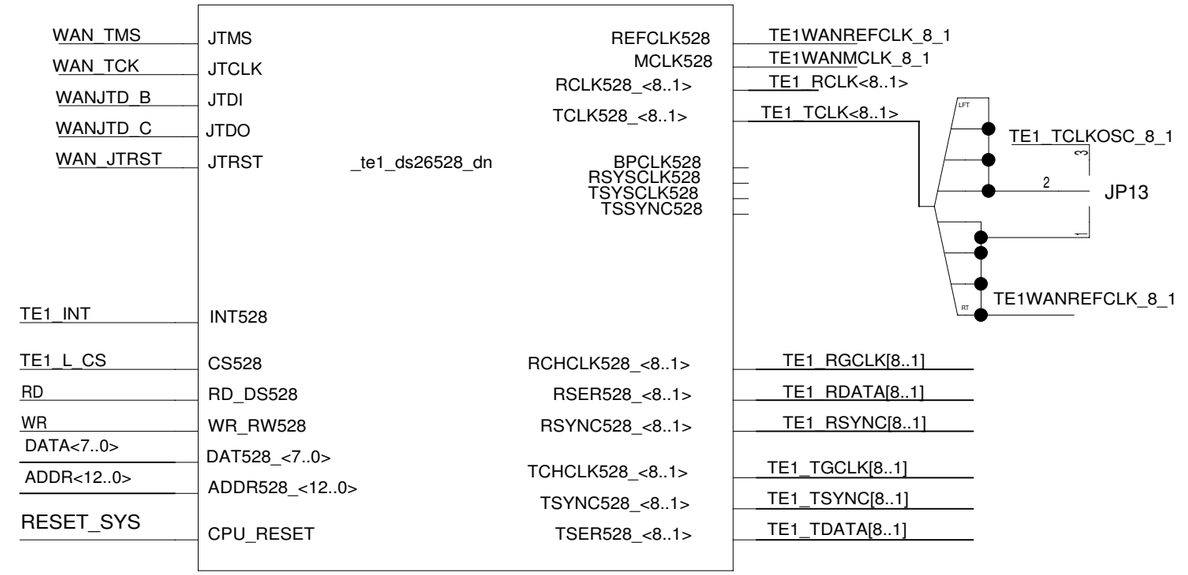


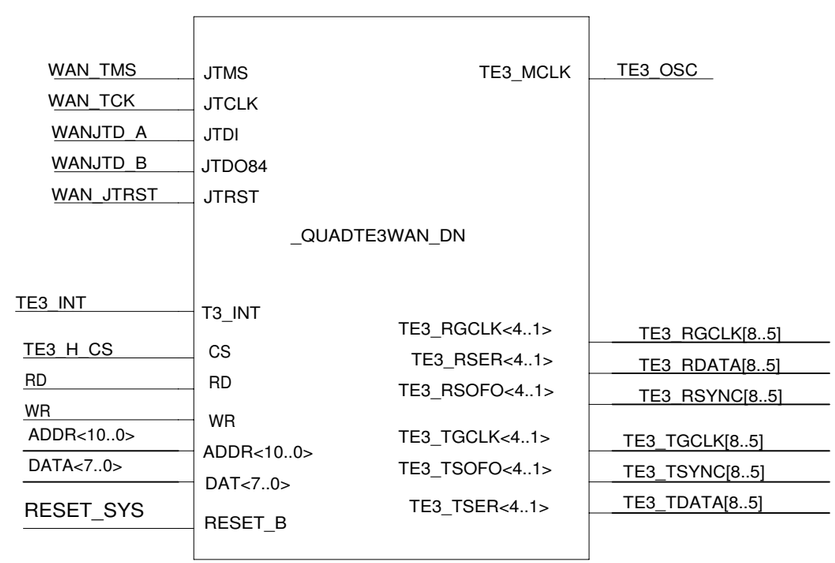
BEGINNING OF DS33X162DK

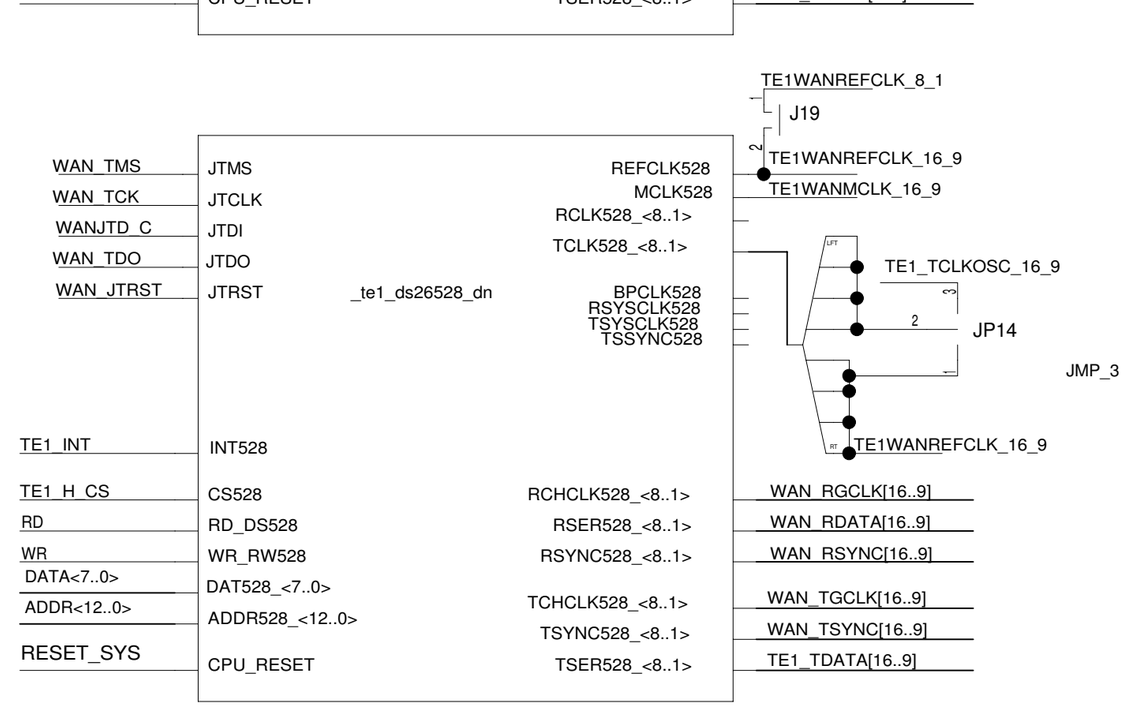
TITLE: DS33X42X82X162EE01A0 MICROPORT. P.24,36-40	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/12(BLOCK) 24/76(TOTAL)

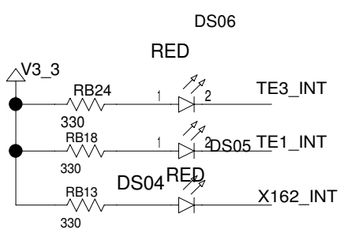
BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\











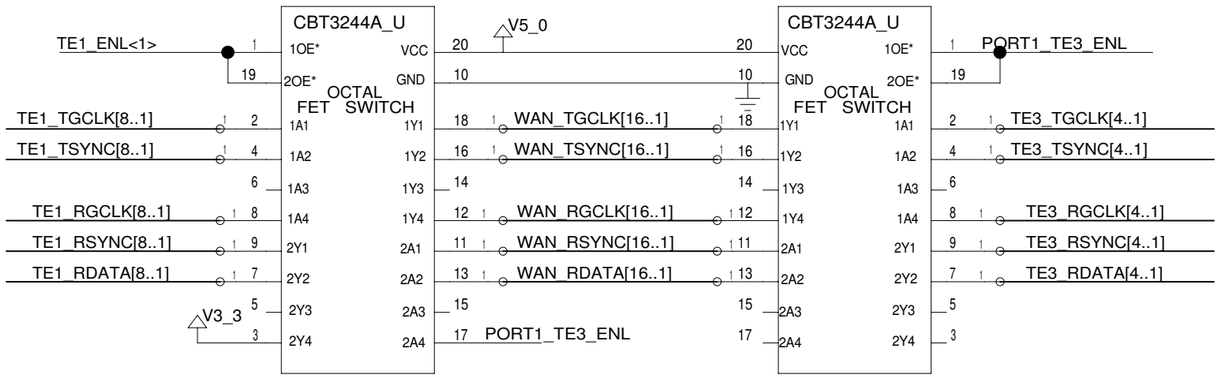
LSB WAN. P.26,41-48(T1),62-66(T3)
MSB WAN. P.25,49-56(T1),57-61(T3)

TITLE: DS33X42X82X162EE01A0 WAN SECTION. P.25-30	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/12(BLOCK) 25/76(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

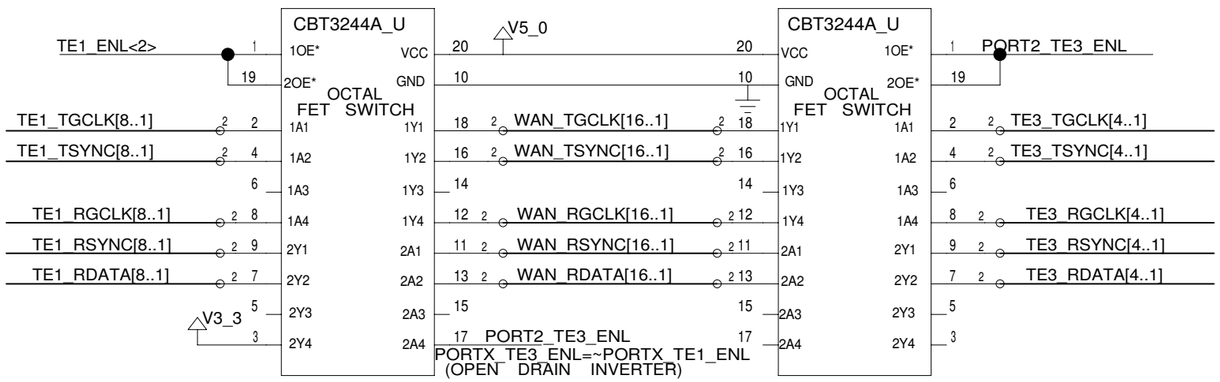
PRINTED Mon May 14 11:04:02 2007

UB15

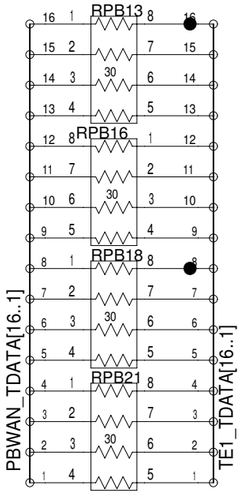


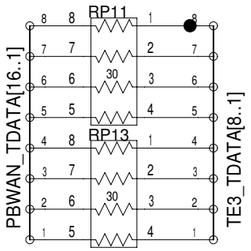
U04

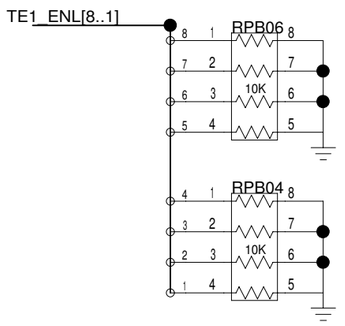
UB14

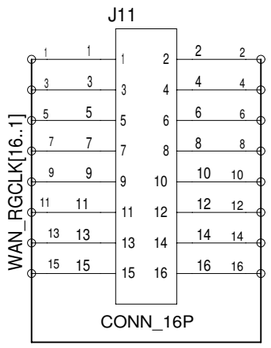


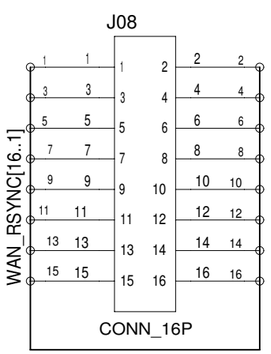
U05

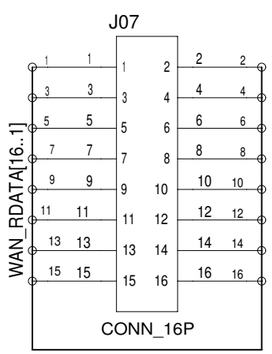


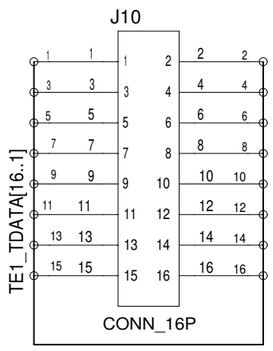






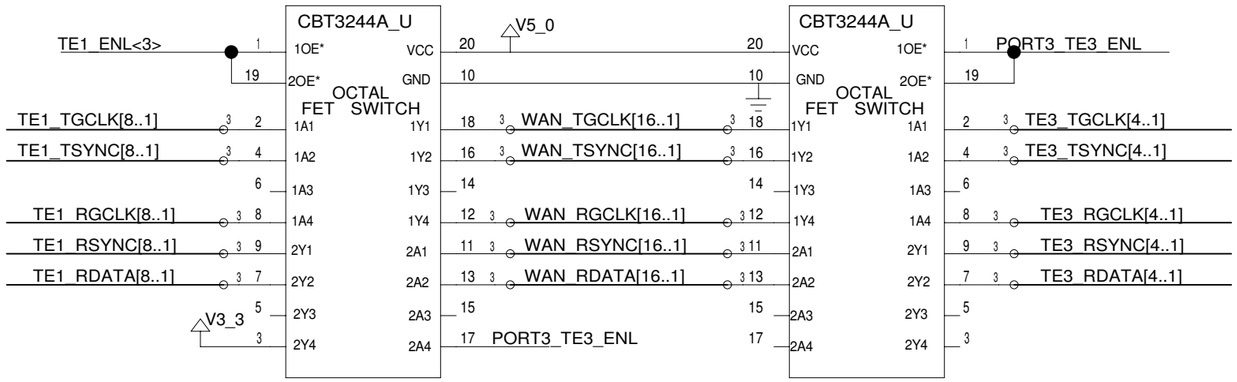






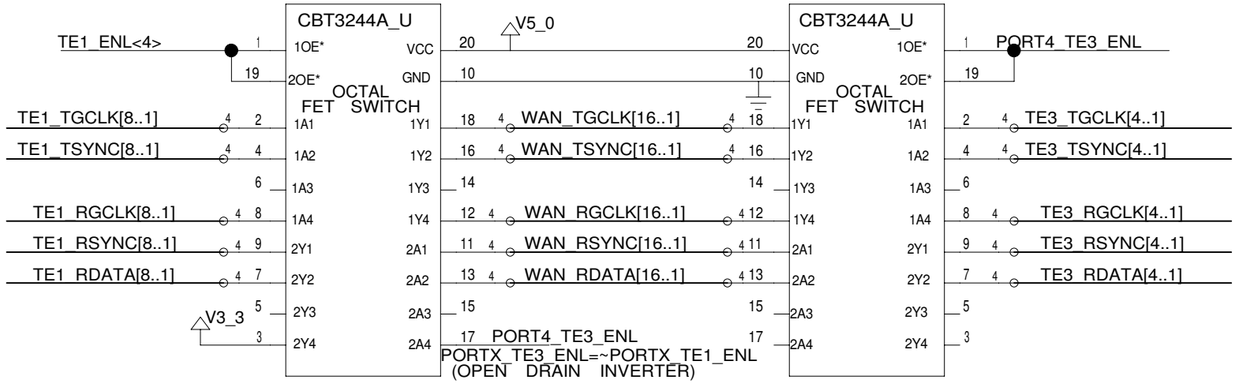
TITLE: DS33X42X82X162EE01A0 WAN SECTION. P.25-30	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 26/76(TOTAL)

U06



UB13

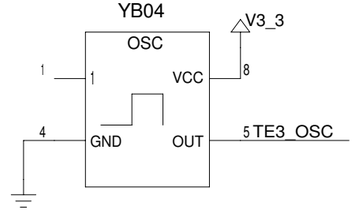
UB20



U09

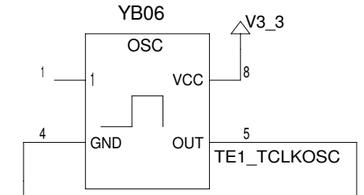
44.736MHZ_5.0V

YB04



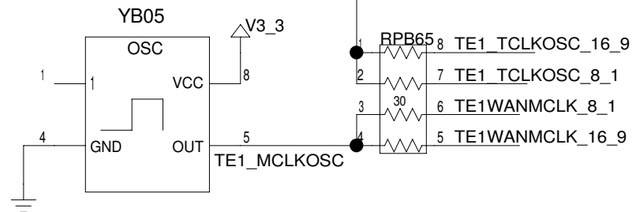
1.544MHZ_5.0VS

YB06



2.048MHZ_3.3VS

YB05

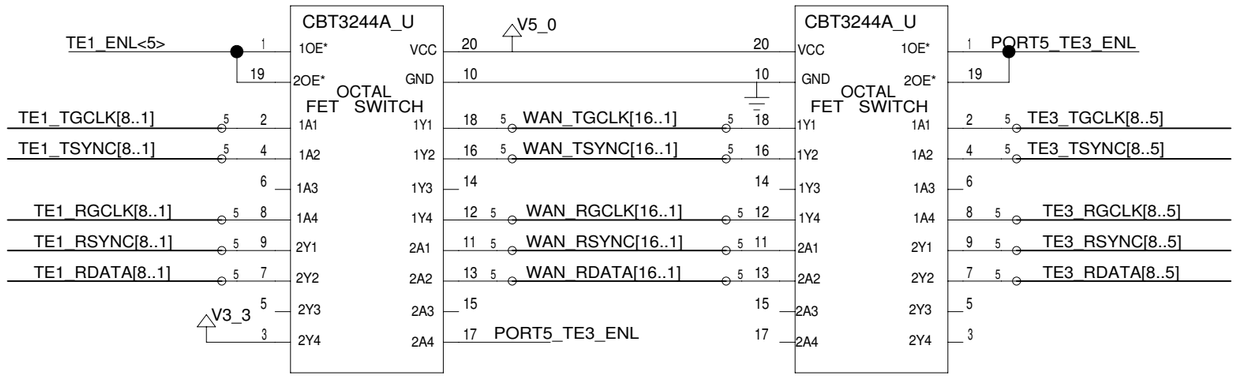


TITLE: DS33X42X82X162EE01A0 WAN SECTION. P.25-30	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 27/76(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

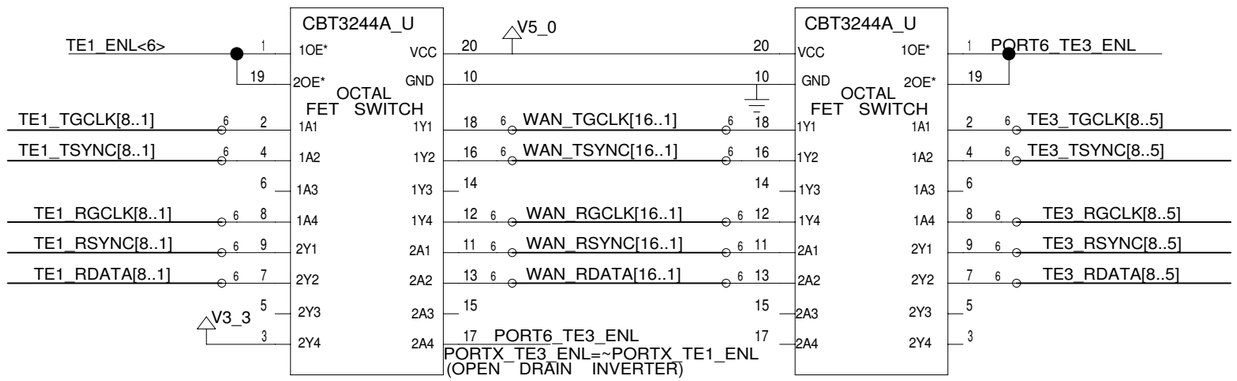
CR-5 : @_RC_LIB_RC_TOP_DN_\(SCH_1):PAGE1_I2@_RC_LIB_DS33X162_DN\(SCH_1):PAGE2

UB19



U12

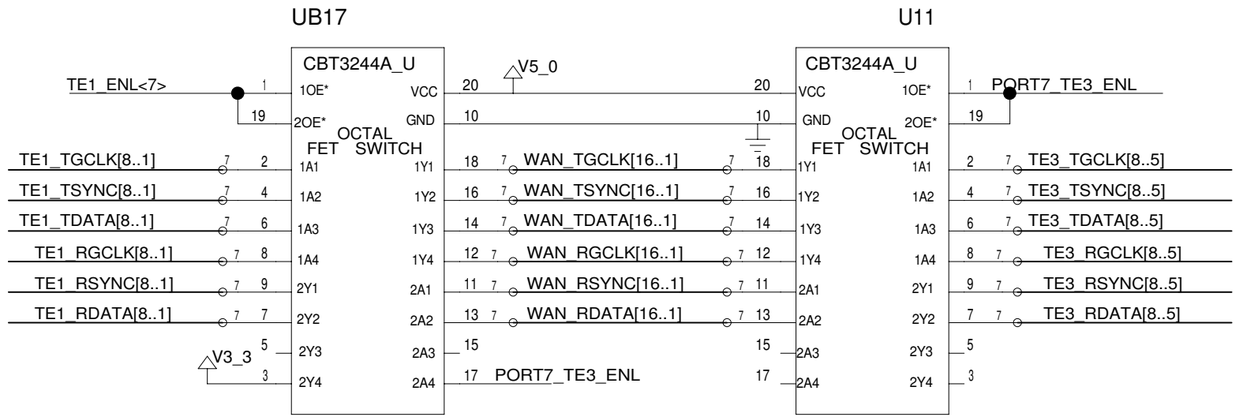
UB18

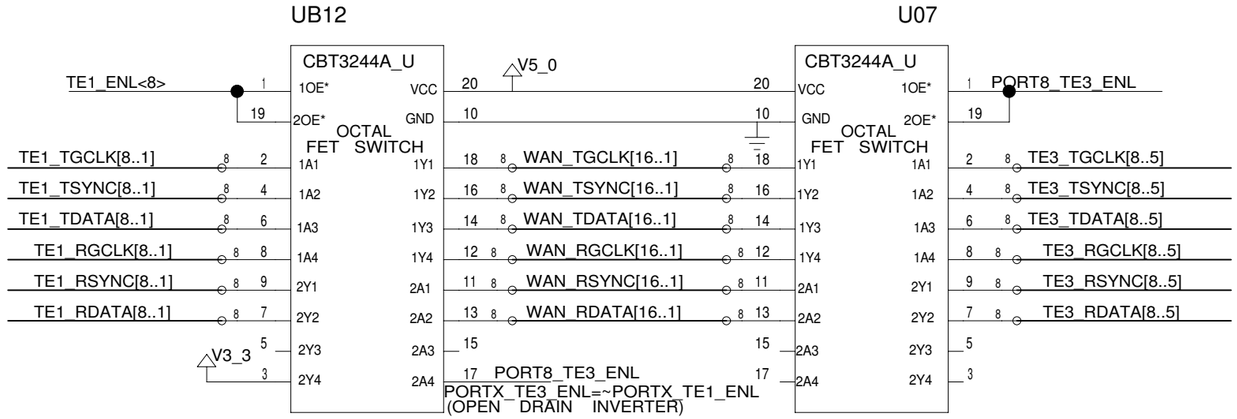


U10

TITLE: DS33X42X82X162EE01A0 WAN SECTION. P.25-30	DATE: 03/28/2006
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 28/76(TOTAL)

BLOCK_NAME: ds33x162dk_dn, PARENT_BLOCK: \ rc_top_dn \





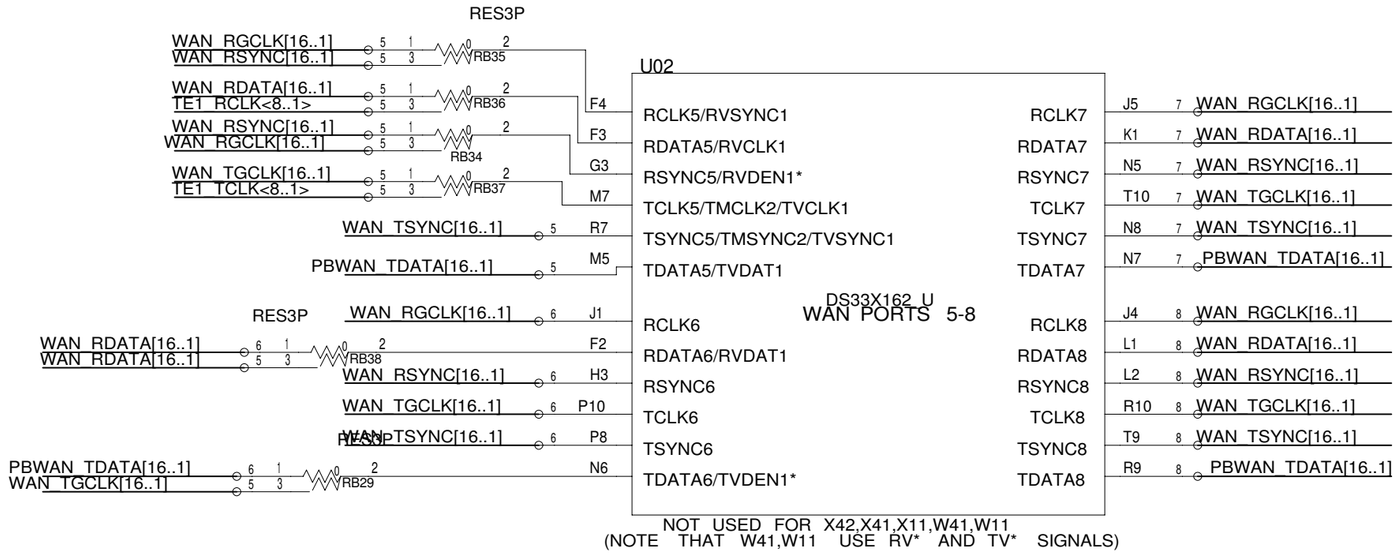
TITLE: DS33X42X82X162EE01A0 WAN SECTION. P.25-30	DATE: 03/28/2006
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 29/76(TOTAL)

DS33X162/X82, DS26528

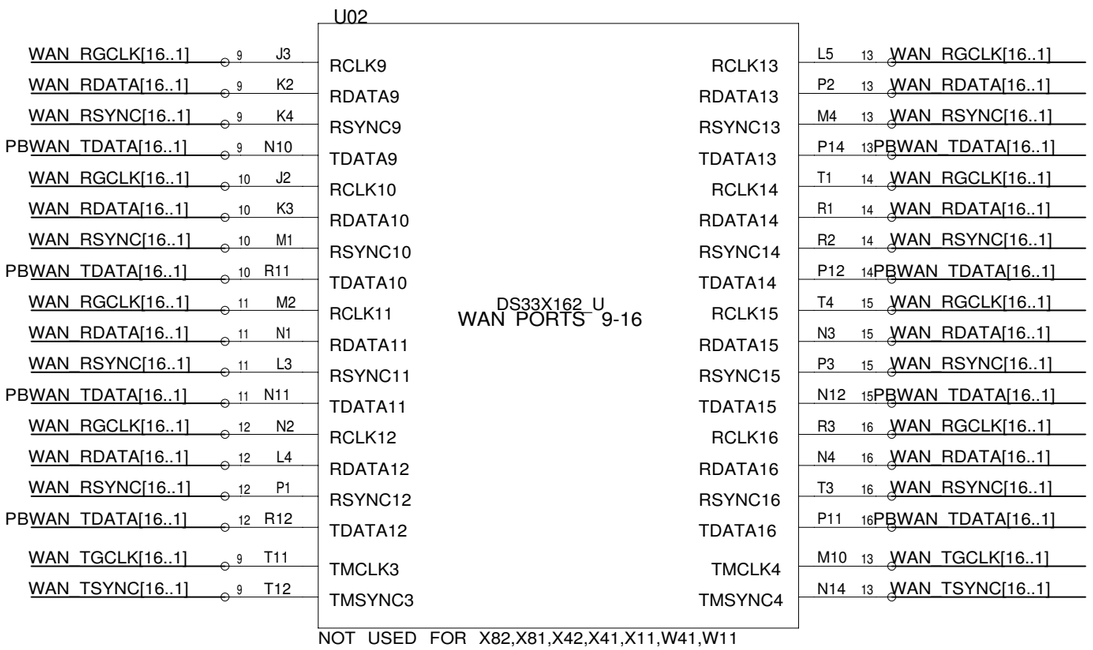
RCLK5	<-	RGCLK5
RDATA5	<-	RDATA5
RSYNC5	<-	RSYNC5
TCLK5	<-	TGCLK5
TSYNC5	<-	TSYNC5
TDATA5	->	TDATA5
RDATA6	<-	RDATA6
TDATA6	->	TDATA6

DS33W41/W11, DS26528

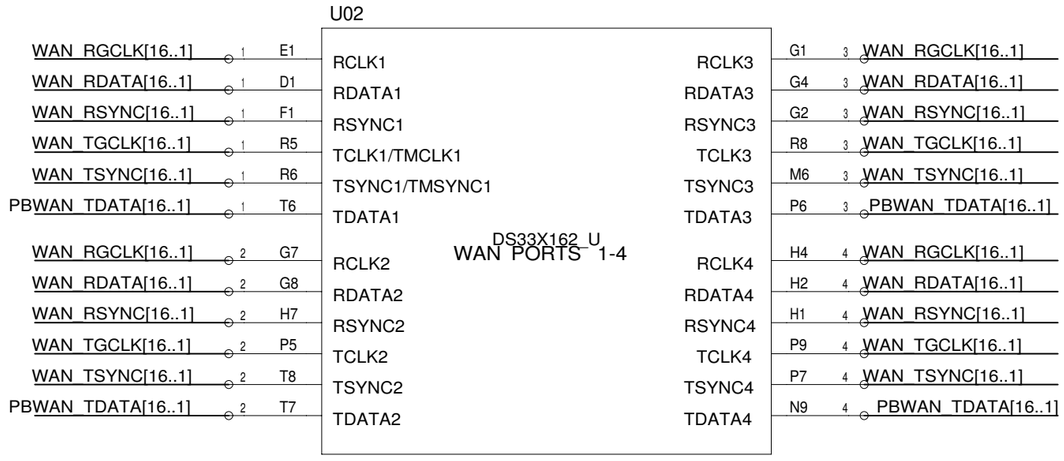
RVSYNC1	<-	RSYNC5
RVCLK1	<-	RCLK5, NOT GAPPED
RVDEN1	<-	RGCLK/RCHBLK5
TVCLK1	<-	TCLK5, NOT GAPPED
TVSYNC1	<-	TSYNC5
TDATA1	->	TDATA5
RVDAT1	<-	RDATA5
TVDEN1	->	TGCLK/TCHBLK5



NOT USED FOR X42,X41,X11,W41,W11
(NOTE THAT W41,W11 USE RV* AND TV* SIGNALS)



NOT USED FOR X82,X81,X42,X41,X11,W41,W11



TITLE: DS33X42X82X162EE01A0 WAN SECTION. P.25-30	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 7/12(BLOCK) 30/76(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

RESISTOR DIVIDER COMPONENT VALUES
OF 4.87K 1% WAS CHOSEN TO SIMPLIFY BOM
(THE DP83848 PHY USES THE SAME VALUE RESISTOR)

V2_5
R1 4.87K
.01UF C32
C268 4.7UF
VREF_FROM_VREG
TPB01
R2 4.87K
CB69 .01UF
CB14 4.7UF

V1_8 V2_5 VREF_FROM_VREG
E5 A16 A15 D14 C14 A12 A11 D10 B8 E7 E5 B9
AVDD_1.8V VDDQ_2.5V VDDQ_2.5V VDDQ_2.5V VDDQ_2.5V VDDQ_2.5V VDDQ_2.5V VDDQ_2.5V VDDP_2.5V VDDP_2.5V VDDP_2.5V VREF

DDR_A<12..0>
0 C3 SD_A[0]
1 C2 SD_A[1]
2 B2 SD_A[2]
3 A2 SD_A[3]
4 D3 SD_A[4]
5 D4 SD_A[5]
6 B5 SD_A[6]
7 C5 SD_A[7]
8 D5 SD_A[8]
9 B6 SD_A[9]
10 A3 SD_A[10]
11 C6 SD_A[11]
12 A5 SD_A[12]
DDR_BA0 B4 SD_BA[0]
DDR_BA1 B3 SD_BA[1]
DDR_CAS B7 SD_CAS*
DDR_RAS A6 SD_RAS*
DDR_WE A7 SD_WE*
DDR_CKE C4 SD_CLKEN
DDR_CKINV A9 SD_CLK*
DDR_CK A8 SD_CLK
DDR_CS A4 SD_CS*
DDR_LDM D13 SD_LDM
DDR_UDM D7 SD_UDM

U02
DS33X162_U
DDR INTERFACE

SD_UDQS D8 DDR_UDQS
SD_LDQS C13 DDR_LDQS
DDR_DQ<15..0>
SD_DQ[15] B12 15
SD_DQ[14] C11 14
SD_DQ[13] B11 13
SD_DQ[12] B10 12
SD_DQ[11] C10 11
SD_DQ[10] D12 10
SD_DQ[9] C9 9
SD_DQ[8] D9 8
SD_DQ[7] B13 7
SD_DQ[6] A13 6
SD_DQ[5] C12 5
SD_DQ[4] A14 4
SD_DQ[3] C15 3
SD_DQ[2] B15 2
SD_DQ[1] B16 1
SD_DQ[0] C16 0

VSSO VSSO VSSO VSSO VSSO VSSO VSSO AVSS
D6 E6 C8 B14 D15 E15 D16 E11

V2_5
18 33 15 55 9 3 61 49
VDD VDD VDD VDDQ VDDQ VDDQ VDDQ VREF

DDR_UDM 47 UDM
DDR_LDM 20 LDM
DDR_CKINV 46 CK_INV
DDR_CS 24 CS
DDR_CK 45 CK
DDR_CKE 44 CKE
DDR_WE 21 WE
DDR_RAS 23 RAS
DDR_CAS 22 CAS
DDR_BA1 27 BA1
DDR_BA0 26 BA0
12 42 A12
11 41 A11
10 28 A10/AP
9 40 A9
8 39 A8
7 38 A7
6 37 A6
5 36 A5
4 35 A4
3 32 A3
2 31 A2
1 30 A1
0 29 A0
DDR_A<12..0>

UB03
MT46V16M16BG75

UDQS 51 DDR_UDQS
LDQS 16 DDR_LDQS
DQ15 65 15
DQ14 63 14
DQ13 62 13
DQ12 60 12
DQ11 59 11
DQ10 57 10
DQ9 56 9
DQ8 54 8
DQ7 13 7
DQ6 11 6
DQ5 10 5
DQ4 8 4
DQ3 7 3
DQ2 5 2
DQ1 4 1
DQ0 2 0
DDR_DQ<15..0>

DNU 19 DNU 50
NC 14 NC 53 NC 43 NC 25 NC 17
VSSQ 58 VSSQ 6 VSSQ 64 VSSQ 12 VSSQ 52
VSS 48 VSS 34 VSS 66

V2_5 FOR DDR
CB74 4.7UF
C11 4.7UF
CB51 0.1UF
C27 .1UF
CB106 .1UF
C26 .1UF
CB111 .1UF
CB16 4.7UF
CB60 4.7UF
CB37 4.7UF
CB61 .01UF

TITLE: DS33X42X82X162EE01A0 DDR MEMORY. P.31-32	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 8/12(BLOCK) 31/76(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

SCHEMATICS FOR GIGABIT AND DUAL PHY CARDS AT
ARE PLACED AT THE END OF THE DS33X162DK SCHEMATIC

SINGLE 50 PIN
I.M. CARD PLUG-CONNECTORS
USED ON BOTTOM OF MOTHERBOARD
FOR CONNECTION TO ETHERNET CARD

THIS CONNECTOR IS INTENED TO ATTACH TO THE GIG PHY OR DUAL PHY CARD.

_phy_imbus_mb_dn

ETHERNET (LAN) CONNECTORS

PT1_COL_DET	AVP1_COL_DET
PT1_RXD<3..0>	AV_RXD<3..0>
PT1_RXDV	AVP1_RXDV
PT1_RX_CLK	AVP1_RX_CLK
PT1_RX_CRS	AVP1_RX_CRS
PT1_RX_ERR	AVP1_RX_ERR
PT1_TXD<3..0>	AV_TXD<3..0>
PT1_TX_CLK	AVP1_TX_CLK
PT1_TX_EN	AVP1_TX_EN
PT2_COL_DET	AVP2_COL_DET
PT2_RXD<3..0>	AV_RXD<7..4>
PT2_RXDV	AVP2_RXDV
PT2_RX_CLK	AVP2_RX_CLK
PT2_RX_CRS	AVP2_RX_CRS
PT2_RX_ERR	AVP2_RX_ERR
PT2_TXD<3..0>	AV_TXD<7..4>
PT2_TX_CLK	AVP2_TX_CLK
PT2_TX_EN	AVP2_TX_EN
REF_CLK	AV_REF_CLK
OSC25M	PY25MHZOSC
MDC	AV_MDC
MDIO	AV_MDIO
RESET_B	RESET_SYS
PHY_INT	PHY_INT
SPARE	
GMII_CLKFROM_MAC	CLOCK_TO_MAC
GMII_TX_ER	AVP1_GMII_TX_ER
GMII_CLKTOMAC_BUF	AV_GMII_CLKFROM_MAC

NOTE: GMII_CLKTOMAC_BUF
EXPECTING THAT THIS WILL BE USED INSTEAD OF 125M_OSC

125.000MHZ_3.3V_SOCKET
YB01
OSC
V3_3
VCC
GND
OUT
R03 30
DUT_SYSCLK

25.000MHZ_3.3V_SOCKET
YB02
OSC
V3_3
VCC
GND
OUT
RB14 30
PY25MHZOSC
RB28 30
JMP_3
JP08
R8 0.0
DUT_REF_CLK
RB26 30
AV_REF_CLK
AV_REF_CLK IS ONLY USED IN RMII MODE (50 MHZ)
CLOCK_TO_MAC (FROM GMII PHY)

V3_3
R6 10K

U02

AVP1_COL_DET	E14	COL1	
	G14	RXD[0]	
	F13	RXD[1]	
	F14	RXD[2]	
AV_RXD<7..0>	H14	RXD[3]	
AVP1_RXDV	G15	RXDV1	
AVP1_RX_CRS	E13	CRS1	
AVP1_RX_ERR	H15	RXER1	
AVP2_COL_DET	L16	COL2	
	N16	RXD[4]	
	M16	RXD[5]	
	L15	RXD[6]	
AV_RXD<7..0>	K16	RXD[7]	
AVP2_RXDV	M11	RXDV2	
AVP2_RX_CRS	J14	CRS2	
AVP2_RX_ERR	M12	RXER2	
		RXCLK1	G16
		TXD[0]	J13
		TXD[1]	K15
		TXD[2]	J15
		TXD[3]	H13
		TXCLK1	M15
		TXEN1	K14
		TXER1	L14
		RXCLK2	N13
		TXD[4]	N15
		TXD[5]	P15
		TXD[6]	R15
		TXD[7]	T15
		TXCLK2	T16
		TXEN2	P16
		TXER2	R16
	P13	DCE_SEL	
	M14	RMII_SEL	
	F15	MDC	
	G13	MDIO	
	T13	REFCLK	
	R14	GTX_CLK1	

LAN PORTS 1+2 COMBINE TO FORM GIGABIT PORT (AVAILABLE TO ALL X/W DEVICES)

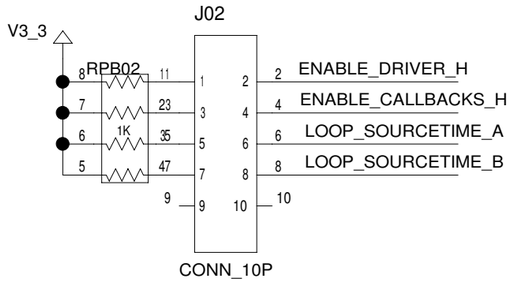
LAN PORT 2 NOT USED IN 10/100 MODE WITH X161,X81,X41,W41,W11

RB09 30 AVP1_RX_CLK
RPB09 AV_TXD<7..0>
RPB08 AVP1_TX_CLK, AVP1_TX_EN, AVP1_GMII_TX_ER
AVP2_RX_CLK
RPB11 AV_TXD<7..0>
RPB05 AVP2_TX_CLK, AVP2_TX_EN, TXER2 NOT USED, AV_GMII_CLKFROM_MAC

DUT_DCE_SEL
DUT_RMII_SEL
AV_MDC
AV_MDIO
DUT_REF_CLK

TITLE:	DS33X42X82X162EE01A0 ETHERNET. P.51,87
DATE:	06/07/2006
ENGINEER:	STEVE SCULLY
PAGE:	9/12(BLOCK) 32/76(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

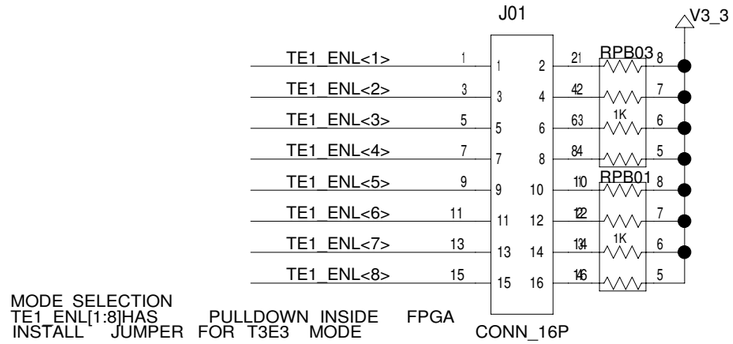


DEVICE DRIVER SETTINGS

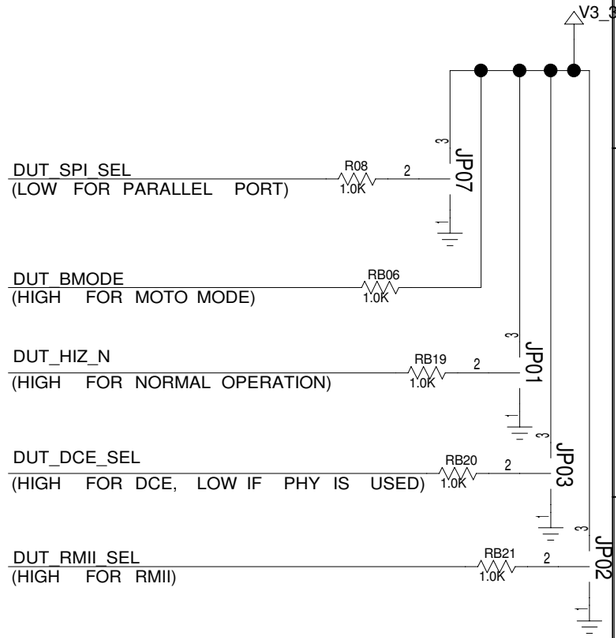
ENABLE_DRIVER_H: ENABLES DEVICE DRIVERS WHEN JUMPER IS INSTALLED
ENABLE_CALLBACKS_H: ENABLES INTERRUPT HANDLING WHEN JUMPER IS INSTALLED

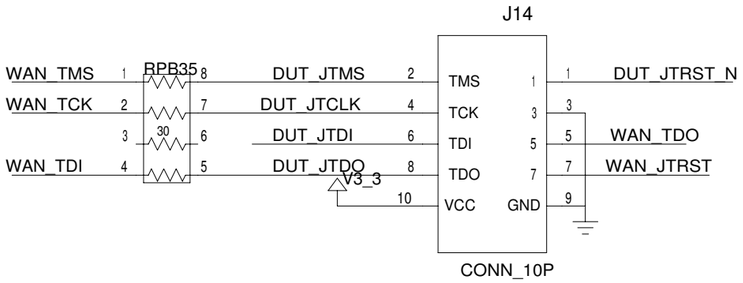
LOOP_SOURCETIME_A: (IN DRIVER MODE ONLY)
WHEN JUMPER IS INSTALLED WAN PORTS 1-8 HAVE TCLK<=RCLK
WHEN JUMPER IS NOT INSTALLED WAN PORTS 1-8 HAVE TCLK<=REFCLKIO

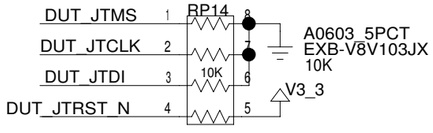
LOOP_SOURCETIME_B: (IN DRIVER MODE ONLY)
WHEN JUPMPER IS INSTALLED WAN PORTS 9-16 HAVE TCLK<=RCLK
WHEN JUPMPER IS NOT INSTALLED WAN PORTS 9-16 HAVE TCLK<=REFCLKIO



MODE SELECTION
TE1_ENL[1:8]HAS PULLDOWN INSIDE FPGA
INSTALL JUMPER FOR T3E3 MODE

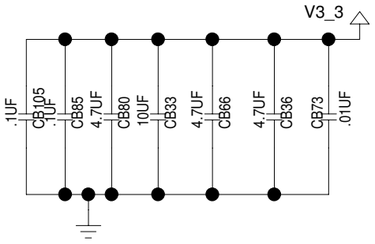


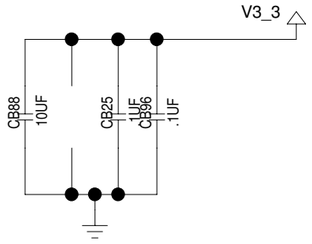


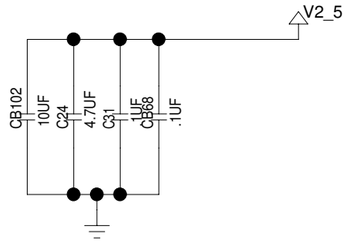


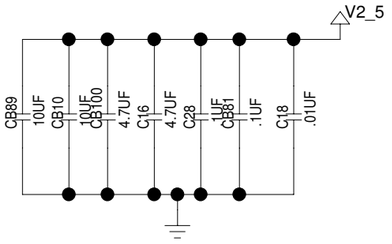
TITLE: DS33X42X82X162EE01A0 BIAS+CONFIG. P.33	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 10/12(BLOCK) 33/76(TOTAL)

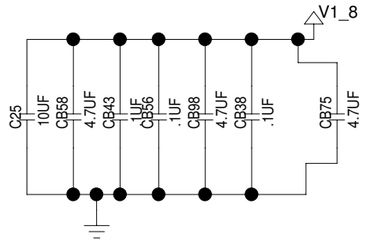
BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

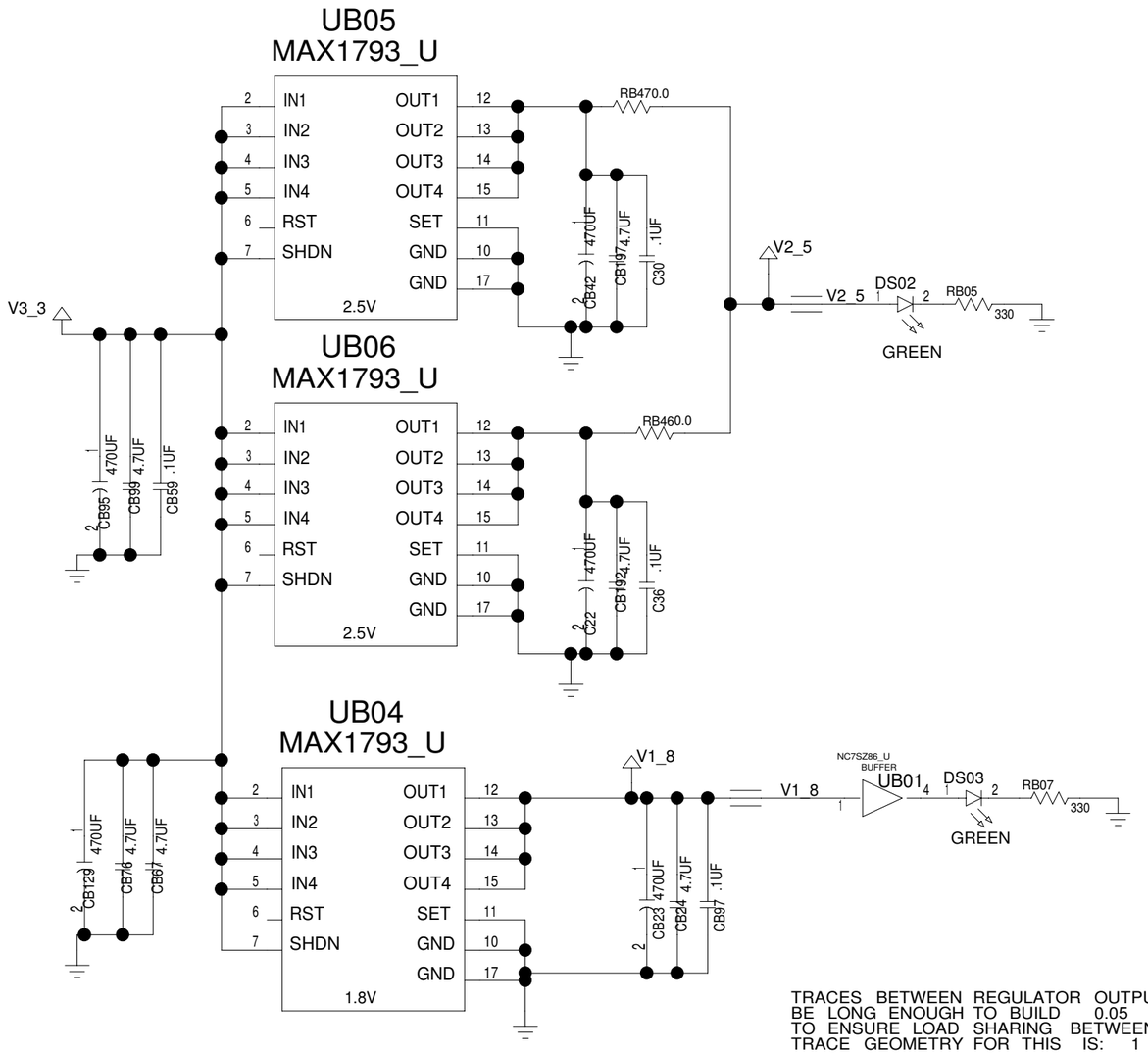




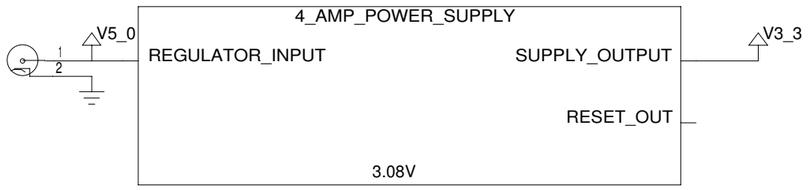




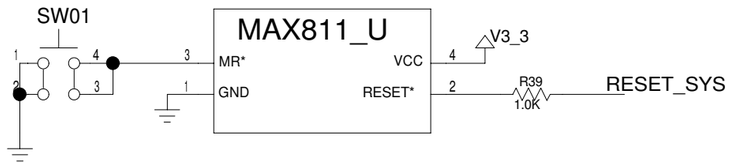




J15



U2



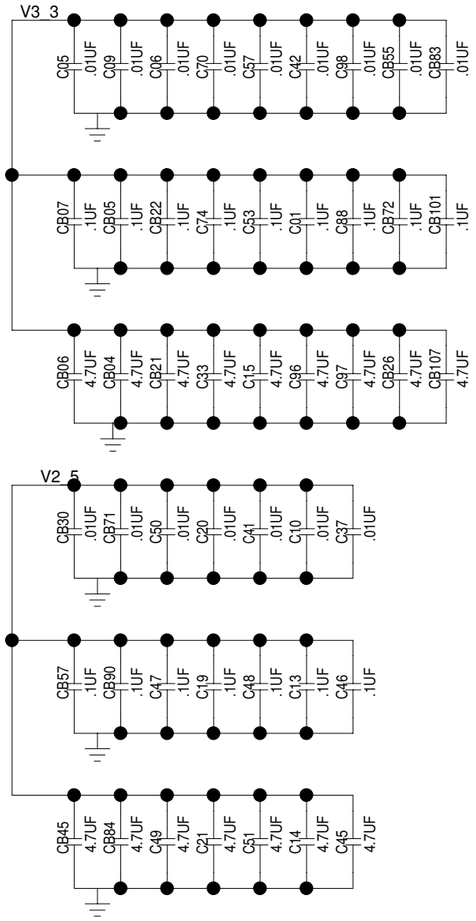
TRACES BETWEEN REGULATOR OUTPUT AND V2.5 SHOULD BE LONG ENOUGH TO BUILD 0.05 OHM OF RESISTANCE TO ENSURE LOAD SHARING BETWEEN THE 2.5V 1% REGULATORS
TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

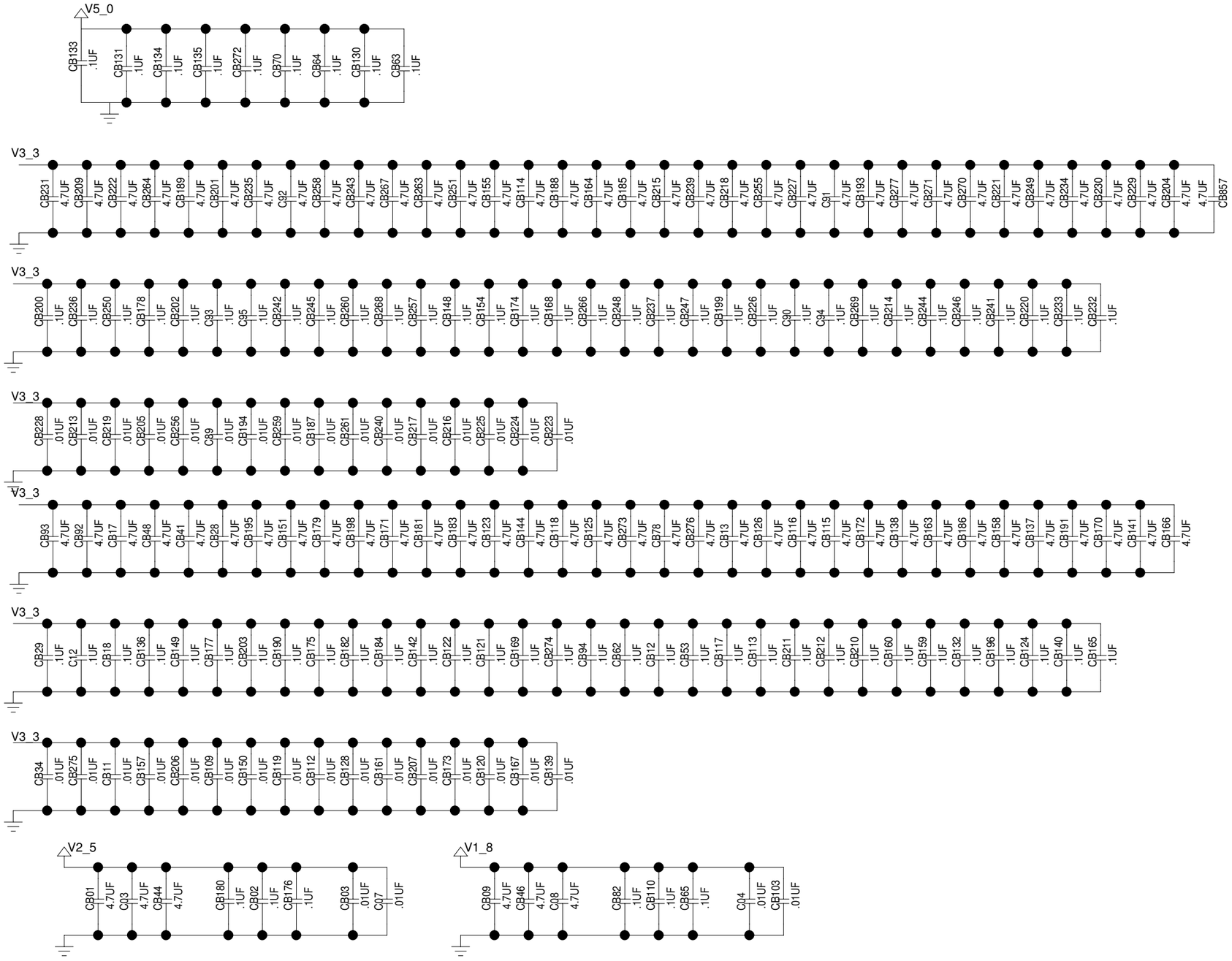
POWER. P.34-35,67

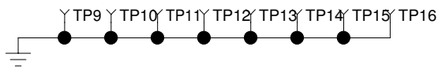
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 11/12(BLOCK) 34/76(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\

DECOUPLING CAPS, PLACED CLOSE TO DUT



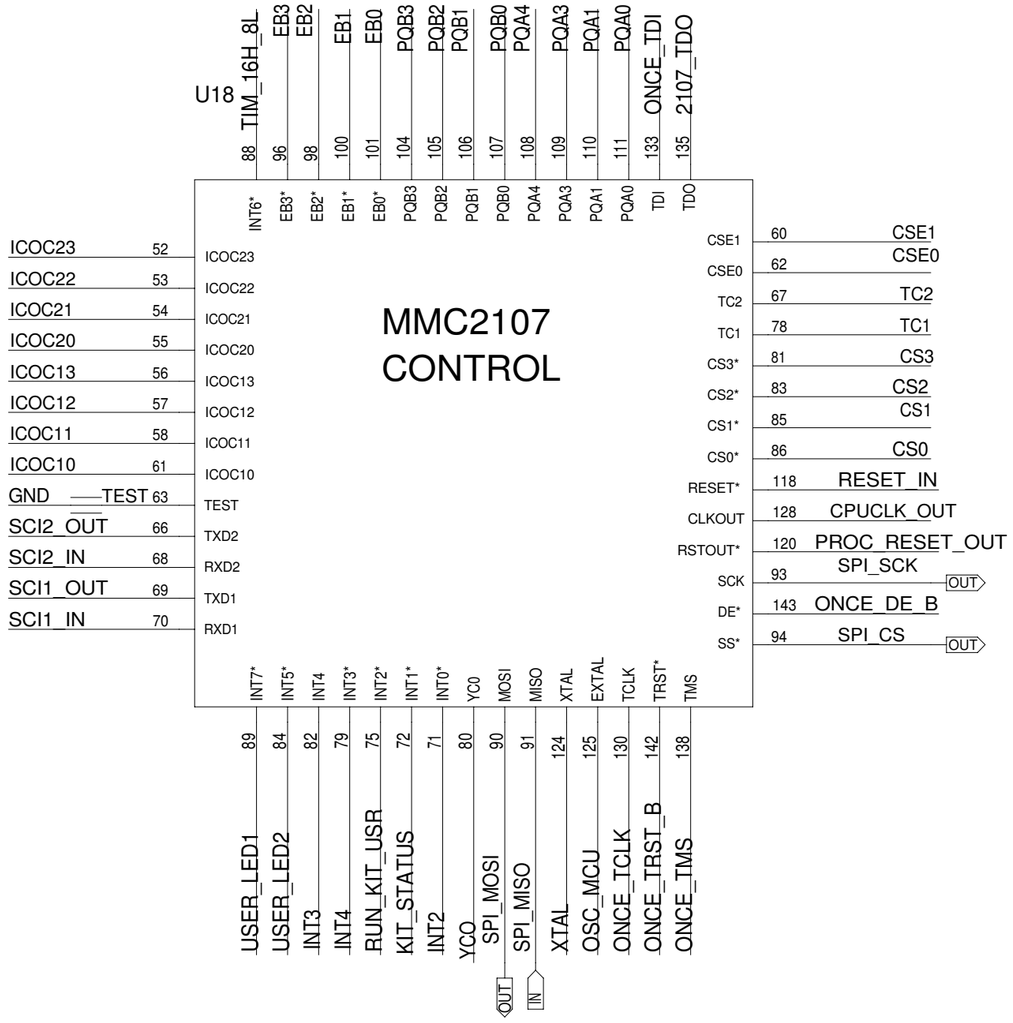


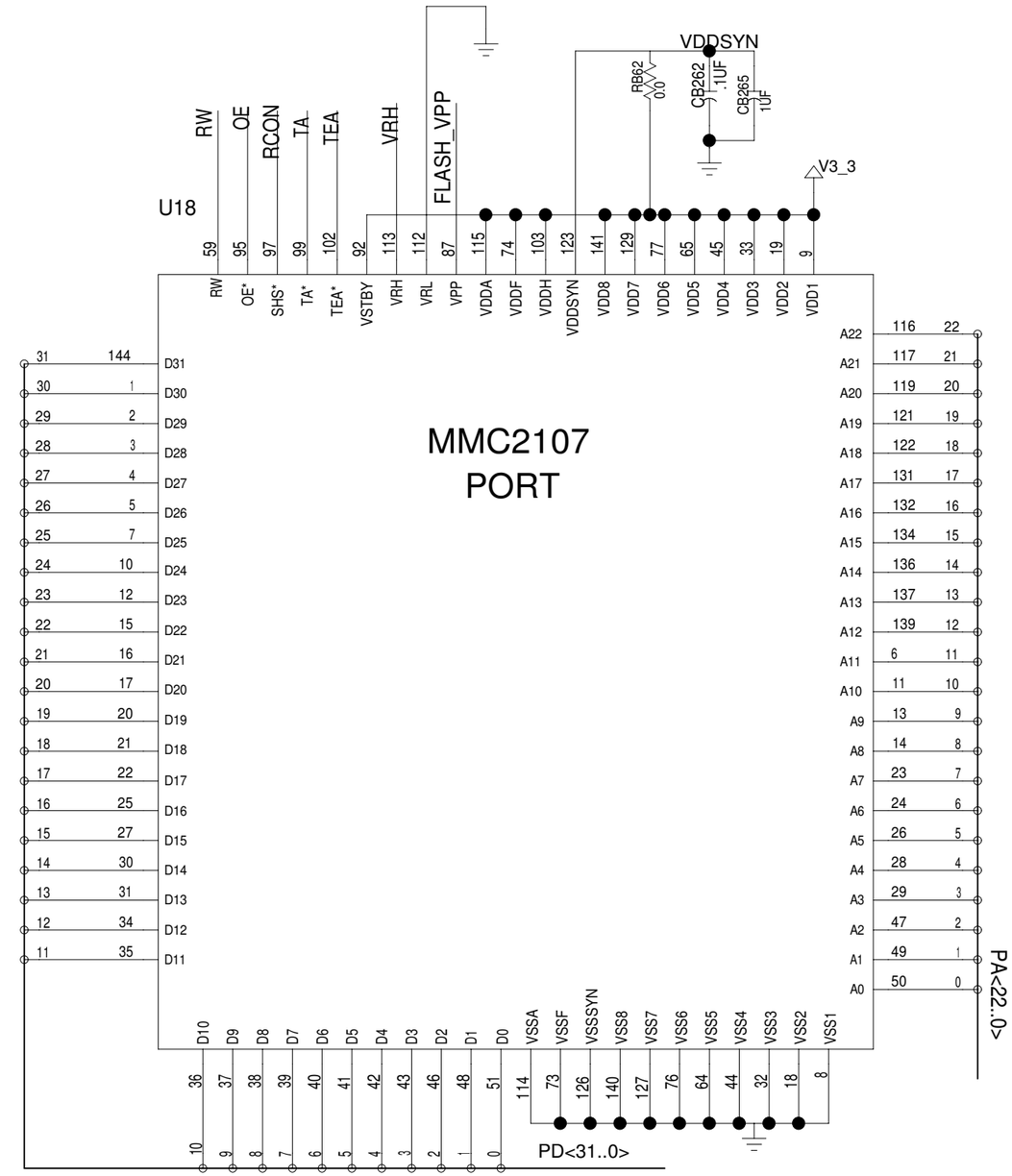


H01 H04 H03 H11 H02 H05

TITLE: DS33X42X82X162EE01A0 POWER. P.34-35,67	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 12/12(BLOCK) 28/110(TOTAL)

BLOCK NAME: _ds33x162dk_dn. PARENT BLOCK: _rc_top_dn_\





BEGINNING OF PROCESSOR HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/5(BLOCK) 36/76(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:03:56 2007

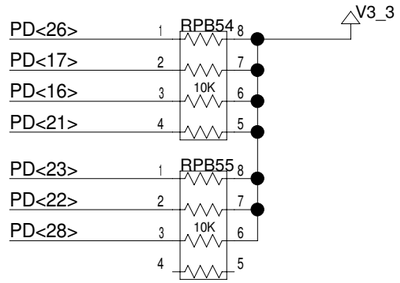
RESET CONFIGURATION

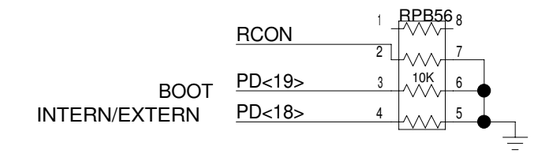
MASTER MODE

FULL DRIVE

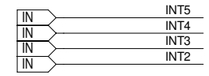
XTAL W/ PLL

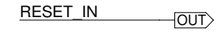
INTERNAL
FLASH ENABLE

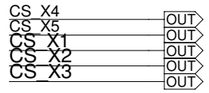


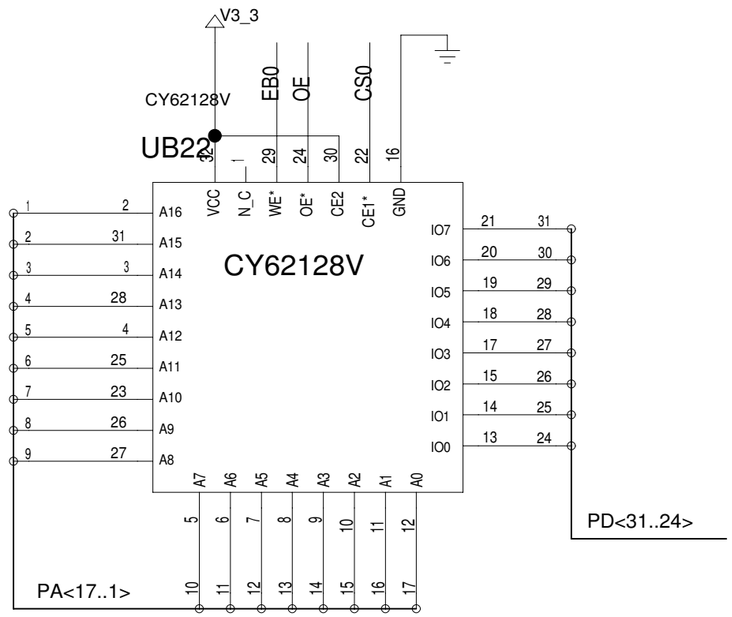


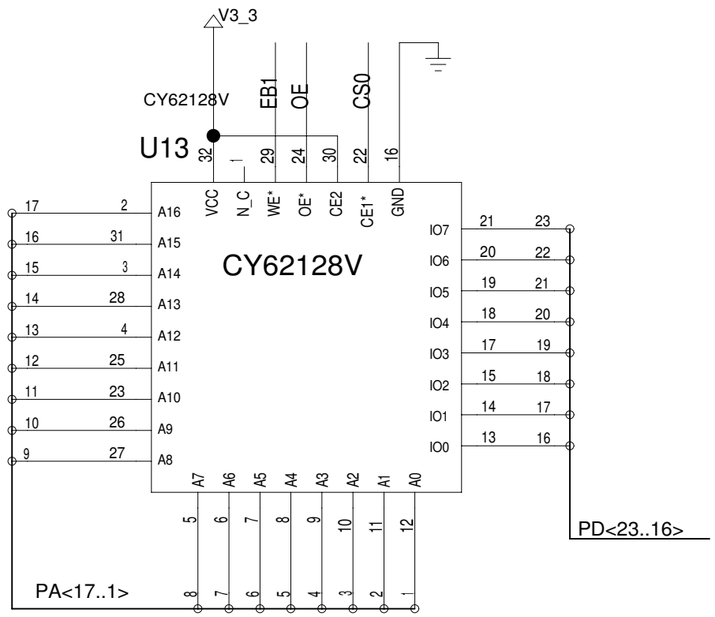
WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND







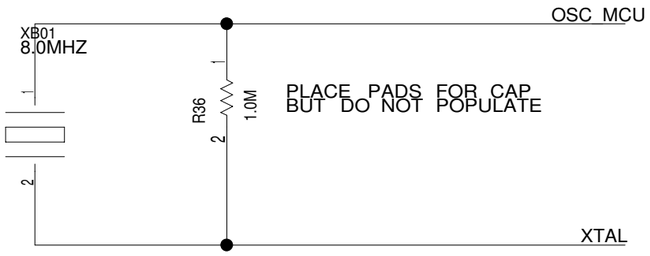


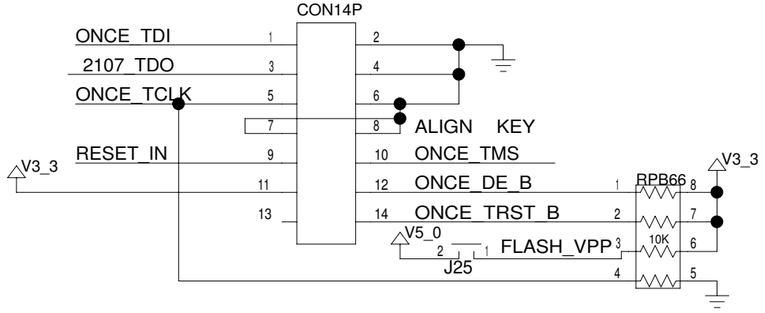


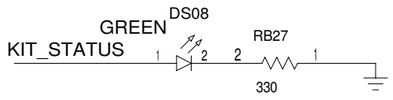
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/5(BLOCK) 37/76(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x162dk_dn\

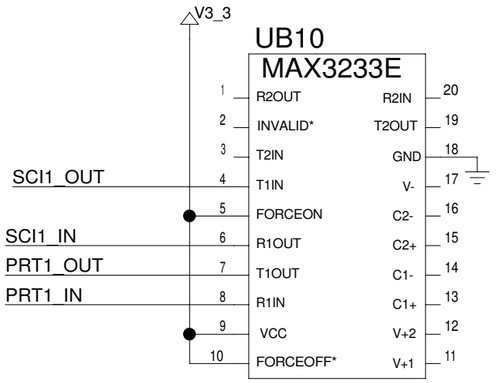
J42
CON14P

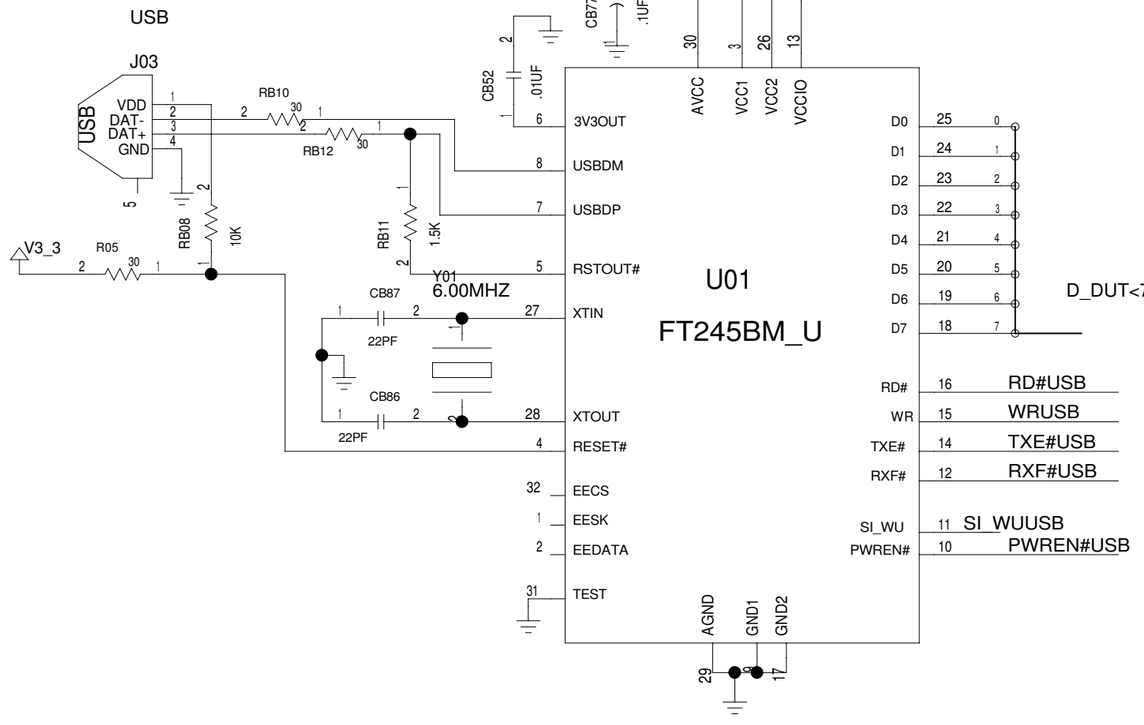


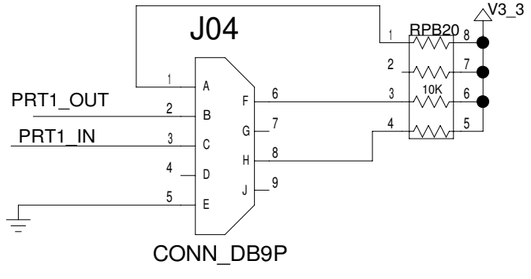




TODO_REMOVETHISNOTE: 330OHM AVCC RES USED TO BE 470OHM (BOM CONSOLDIATE)

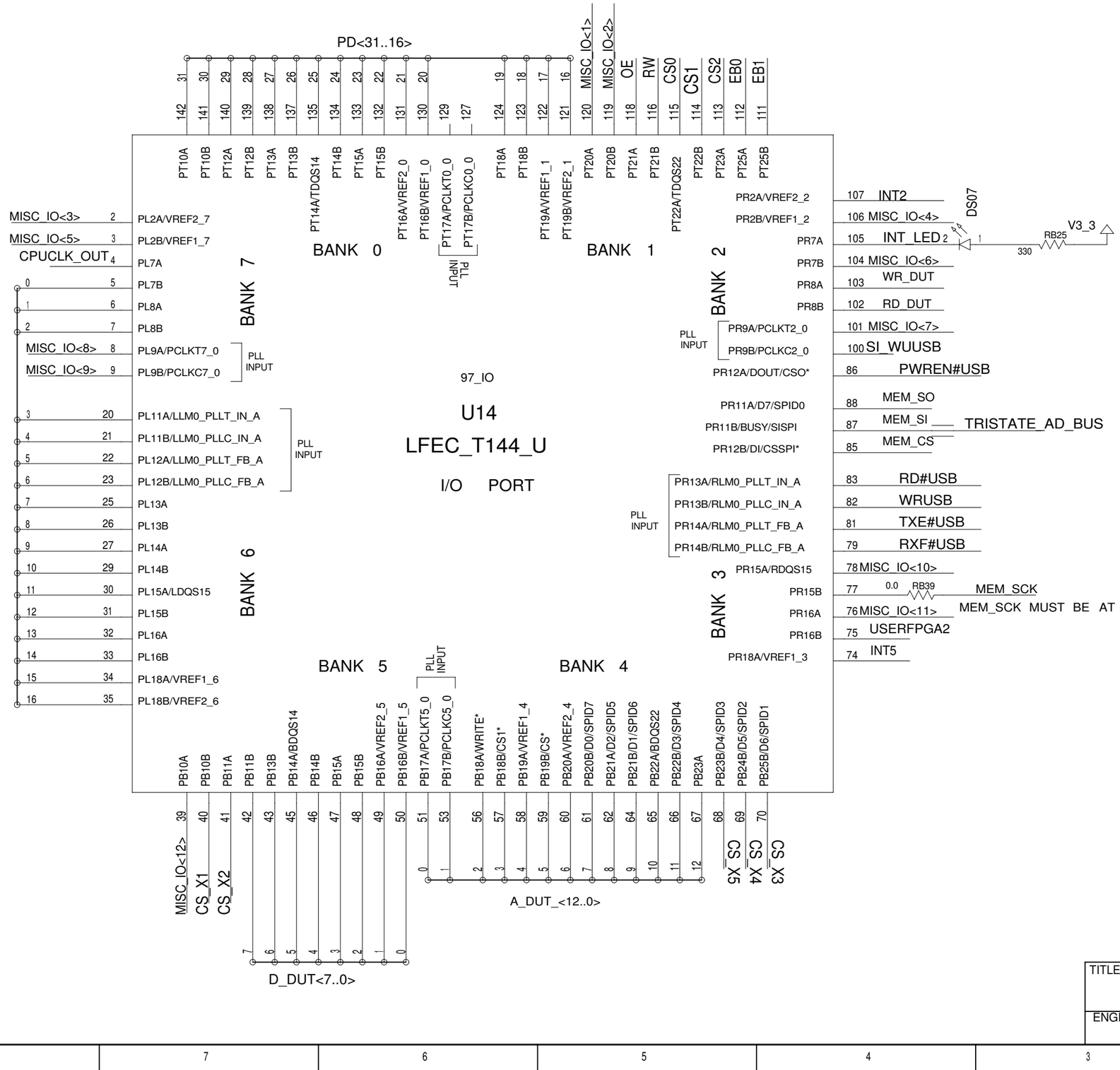


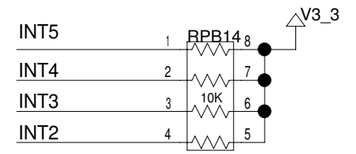


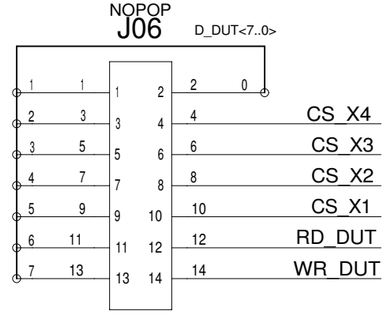


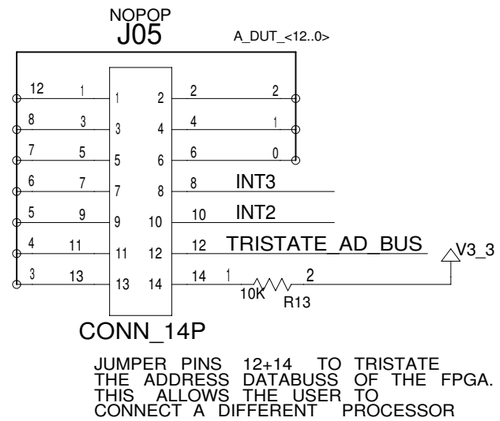
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 38/76(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x162dk_dn\





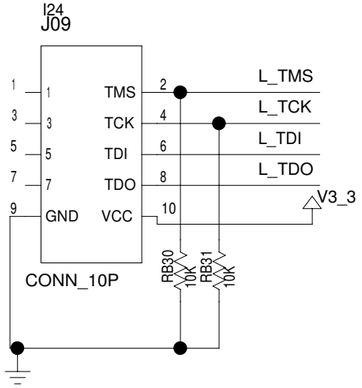




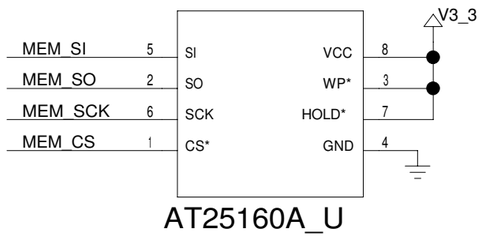
JUMPER PINS 12+14 TO TRISTATE THE ADDRESS DATABUSS OF THE FPGA. THIS ALLOWS THE USER TO CONNECT A DIFFERENT PROCESSOR

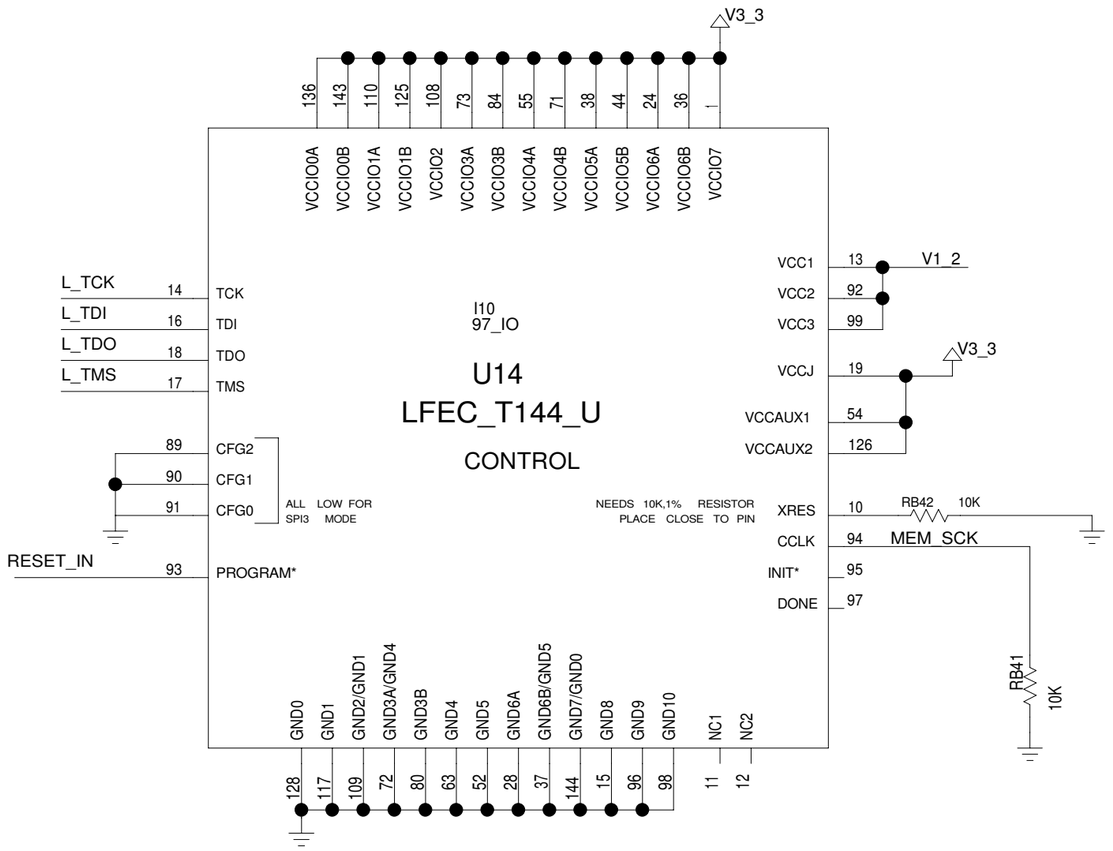
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/5(BLOCK) 39/76(TOTAL)

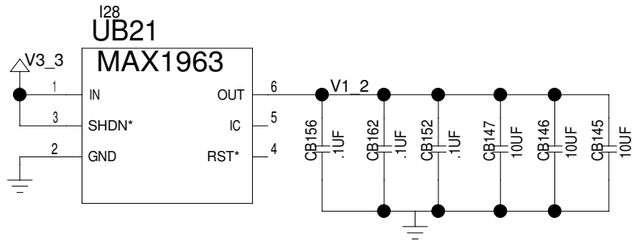
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x162dk_dn\



I26
2.7V



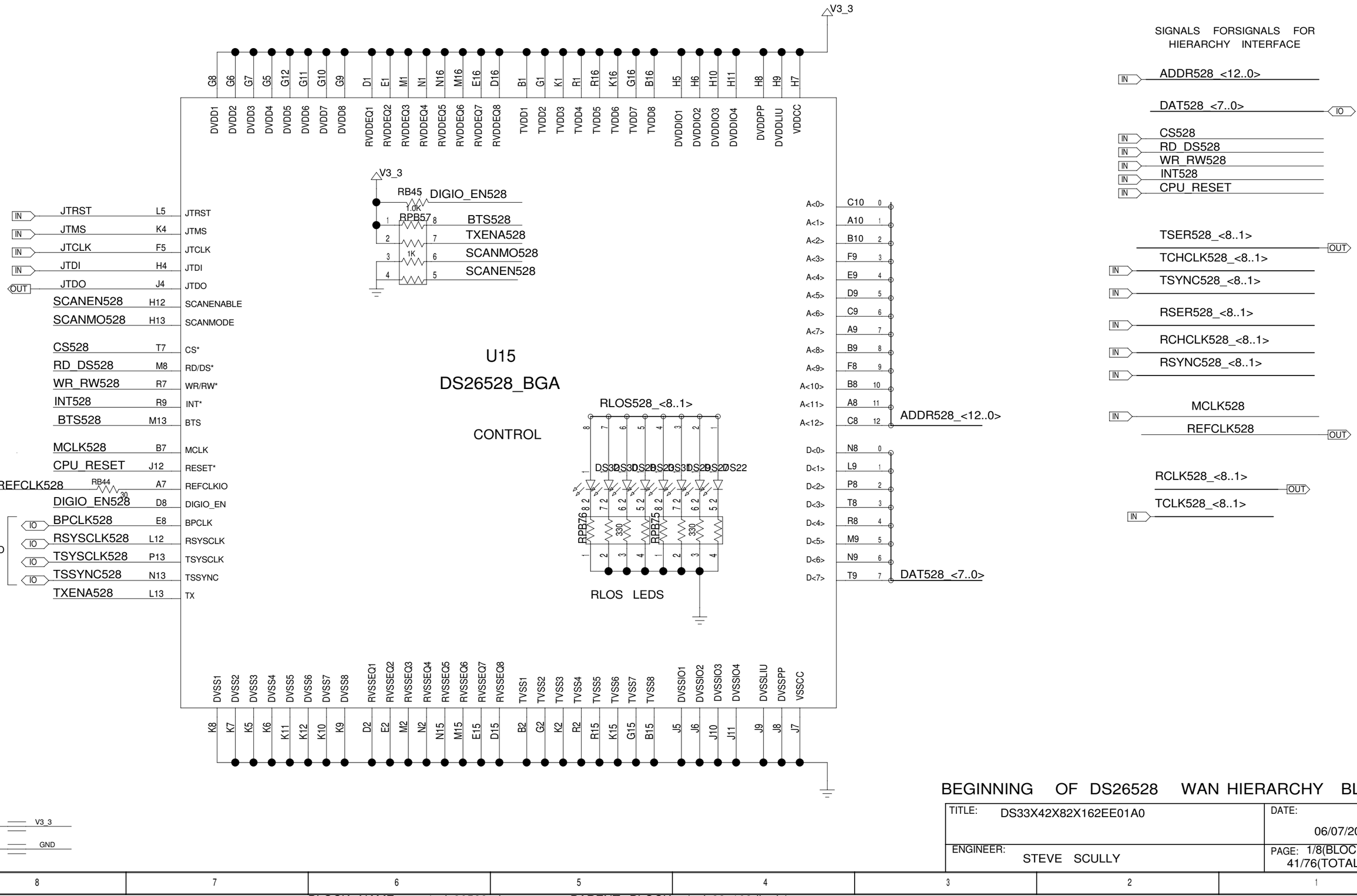


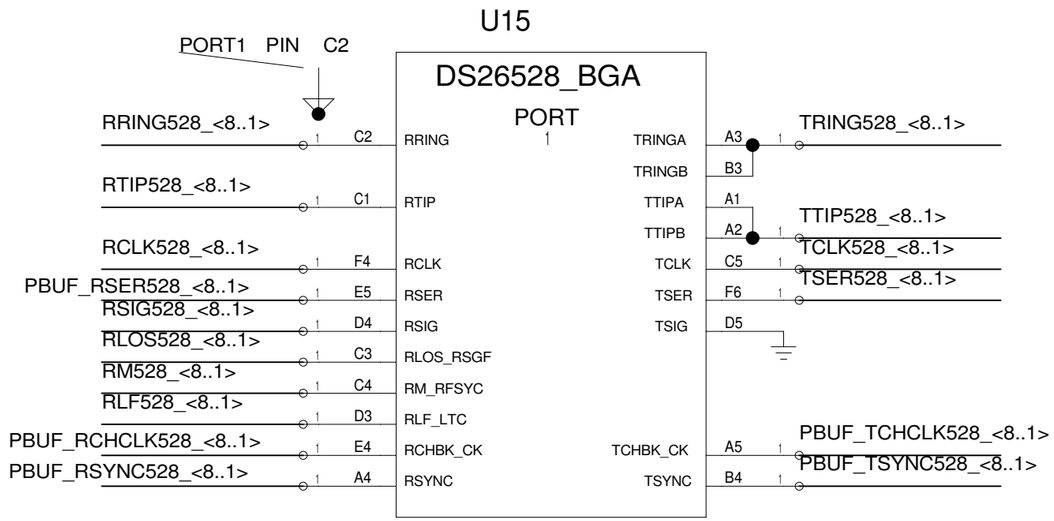


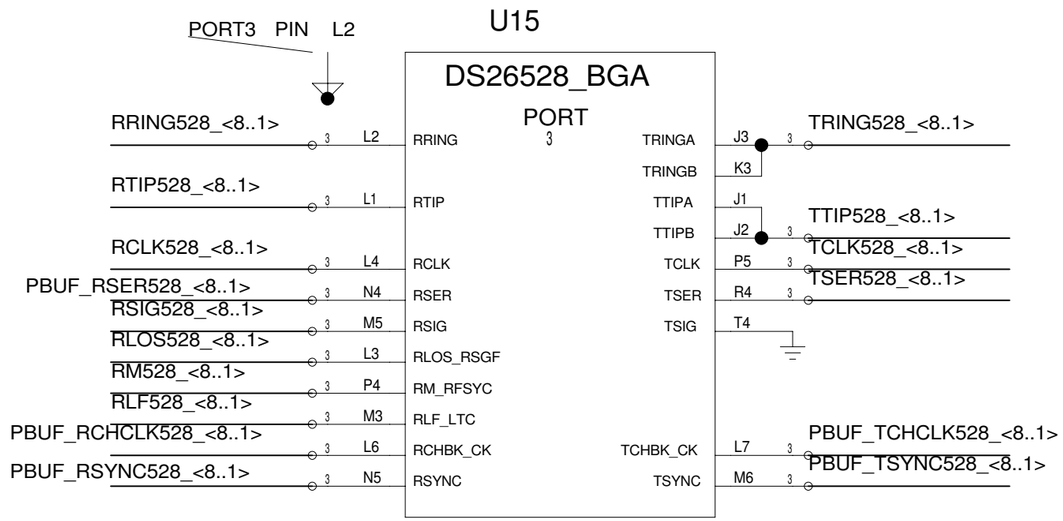
END OF PROCESSOR HIERARCHY BLOCK

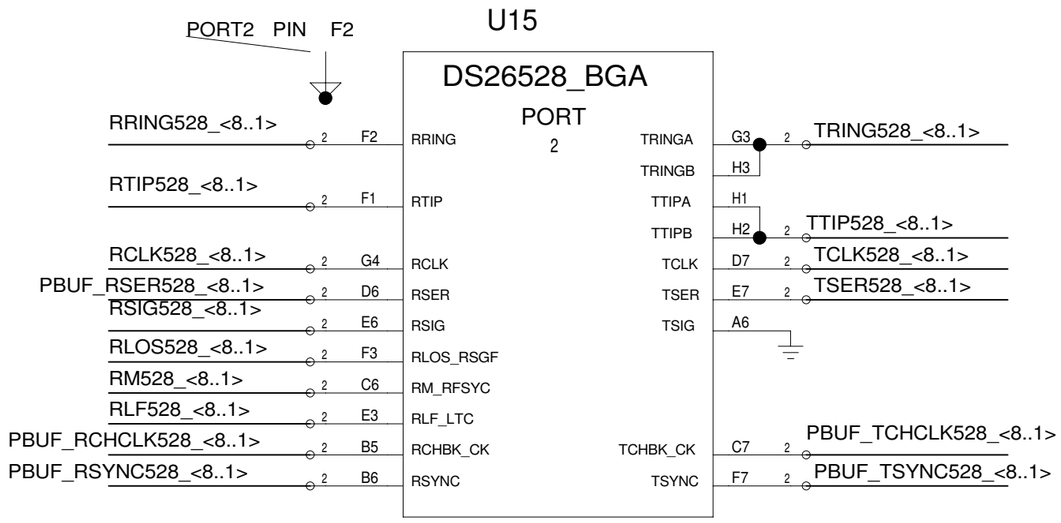
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 40/76(TOTAL)

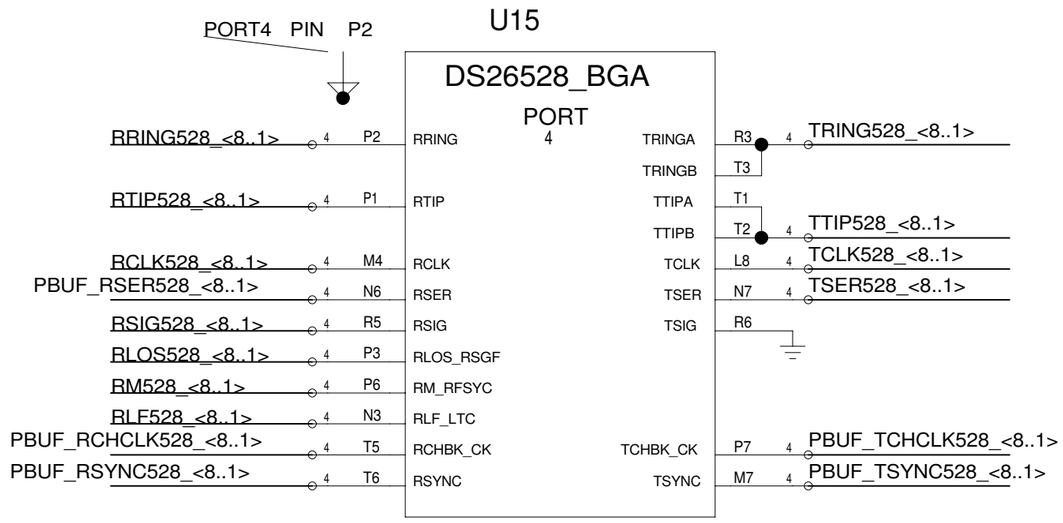
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x162dk_dn\


V3_3
G8 G6 G7 G5 G12 G11 G10 G9 D1 E1 M1 N1 N16 M16 E16 D16 B1 G1 K1 R1 R16 K16 G16 B16 H5 H6 H10 H11 H8 H9 H7
DVDD1 DVDD2 DVDD3 DVDD4 DVDD5 DVDD6 DVDD7 DVDD8 RVDDEQ1 RVDDEQ2 RVDDEQ3 RVDDEQ4 RVDDEQ5 RVDDEQ6 RVDDEQ7 RVDDEQ8 TVDD1 TVDD2 TVDD3 TVDD4 TVDD5 TVDD6 TVDD7 TVDD8 DVDDIO1 DVDDIO2 DVDDIO3 DVDDIO4 DVDDPP DVDDLIU VDDCC
SIGNALS FORSIGNALS FOR HIERARCHY INTERFACE
IN ADDR528_<12..0>
DAT528_<7..0> IO
IN CS528
IN RD_DS528
IN WR_RW528
IN INT528
IN CPU_RESET
V3_3
RB45 DIGIO_EN528
1.0K
RPB57
1K
BTS528
TXENA528
SCANMO528
SCANEN528
IN JTRST L5 JTRST
IN JTMS K4 JTMS
IN JTCLK F5 JTCLK
IN JTDI H4 JTDI
OUT JTDO J4 JTDO
SCANEN528 H12 SCANENABLE
SCANMO528 H13 SCANMODE
CS528 T7 CS*
RD_DS528 M8 RD/DS*
WR_RW528 R7 WR/RW*
INT528 R9 INT*
BTS528 M13 BTS
MCLK528 B7 MCLK
CPU_RESET J12 RESET*
REFCLK528 RB44 30 A7 REFCLKIO
DIGIO_EN528 D8 DIGIO_EN
UNUSED
IO BPCLK528 E8 BPCLK
IO RSYSCLK528 L12 RSYSCLK
IO TSYSCLK528 P13 TSYSCLK
IO TSSYNC528 N13 TSSYNC
TXENA528 L13 TX
U15
DS26528_BGA
CONTROL
RLOS528_<8..1>
DS33 DS32 DS31 DS30 DS29 DS28 DS27 DS26 DS25 DS24 DS23 DS22
RPB76 RPB75 330
RLOS LEDS
A<0> C10 0
A<1> A10 1
A<2> B10 2
A<3> F9 3
A<4> E9 4
A<5> D9 5
A<6> C9 6
A<7> A9 7
A<8> B9 8
A<9> F8 9
A<10> B8 10
A<11> A8 11
A<12> C8 12
ADDR528_<12..0>
D<0> N8 0
D<1> L9 1
D<2> P8 2
D<3> T8 3
D<4> R8 4
D<5> M9 5
D<6> N9 6
D<7> T9 7
DAT528_<7..0>
TSER528_<8..1> OUT
IN TCHCLK528_<8..1>
IN TSYNC528_<8..1>
IN RSER528_<8..1>
IN RCHCLK528_<8..1>
IN RSYNC528_<8..1>
IN MCLK528
REFCLK528 OUT
RCLK528_<8..1> OUT
IN TCLK528_<8..1>
DVSS1 DVSS2 DVSS3 DVSS4 DVSS5 DVSS6 DVSS7 DVSS8 RVSSEQ1 RVSSEQ2 RVSSEQ3 RVSSEQ4 RVSSEQ5 RVSSEQ6 RVSSEQ7 RVSSEQ8 TVSS1 TVSS2 TVSS3 TVSS4 TVSS5 TVSS6 TVSS7 TVSS8 DVSSIO1 DVSSIO2 DVSSIO3 DVSSIO4 DVSSLIU DVSSPP VSSCC
K8 K7 K5 K6 K11 K12 K10 K9 D2 E2 M2 N2 N15 M15 E15 D15 B2 G2 K2 R2 R15 K15 G15 B15 J5 J6 J10 J11 J9 J8 J7
V3_3
V3_3
GND
BEGINNING OF DS26528 WAN HIERARCHY BLOCK
TITLE: DS33X42X82X162EE01A0
DATE: 06/07/2006
ENGINEER: STEVE SCULLY
PAGE: 1/8(BLOCK) 41/76(TOTAL)
BLOCK NAME: _te1_ds26528_dn.
PARENT BLOCK: _ds33x162dk_dn\
PRINTED Mon Feb 11 13:57:23 2008





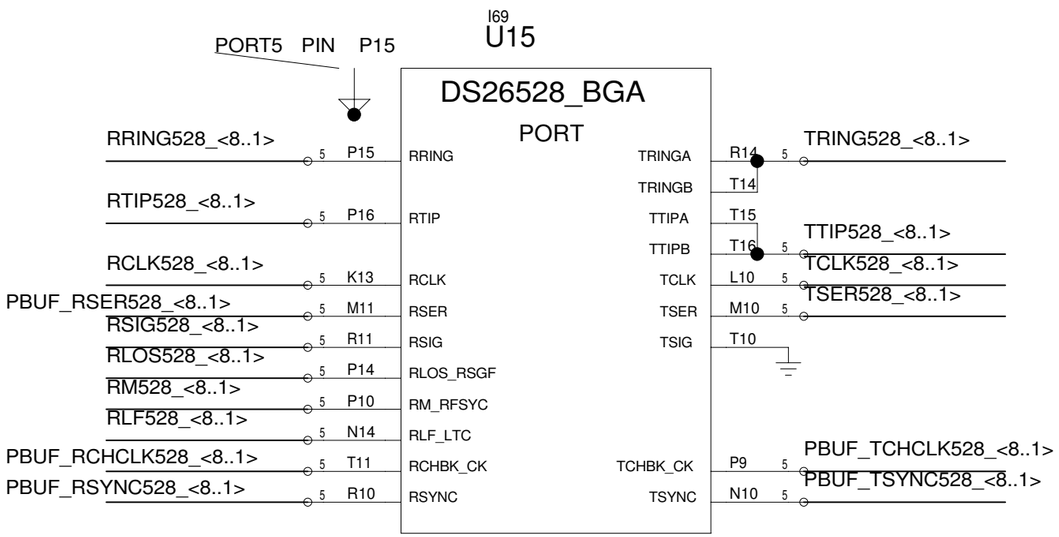


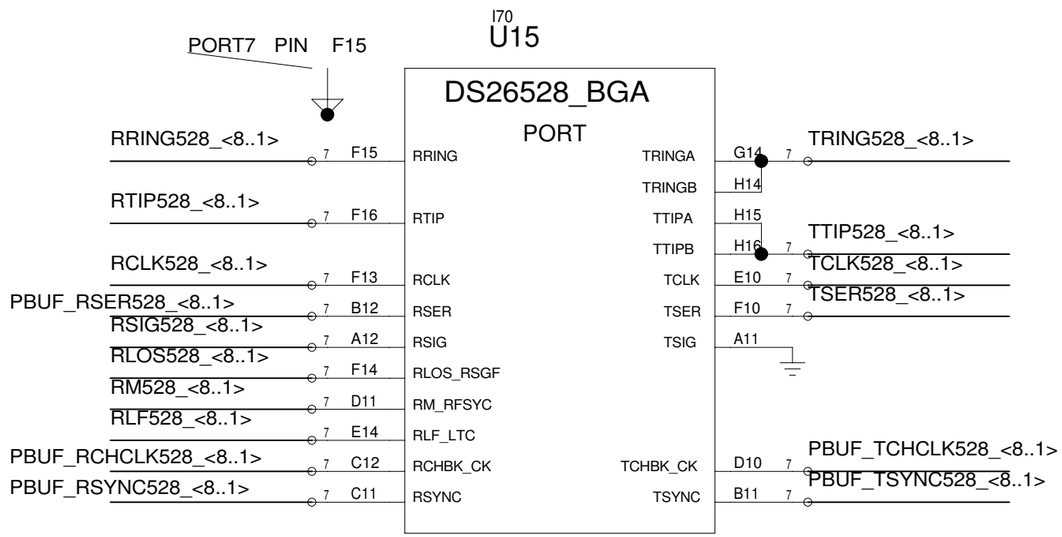


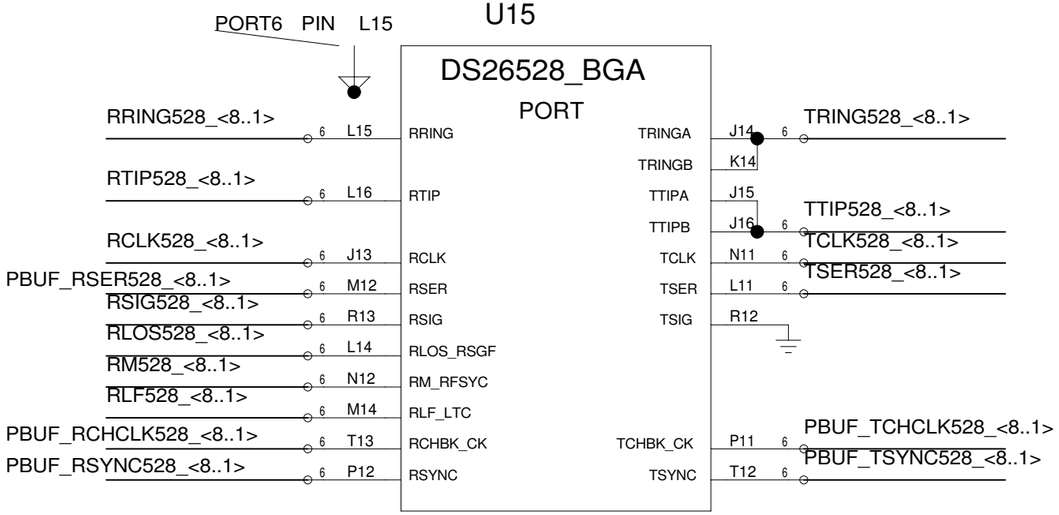
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/8(BLOCK) 42/76(TOTAL)

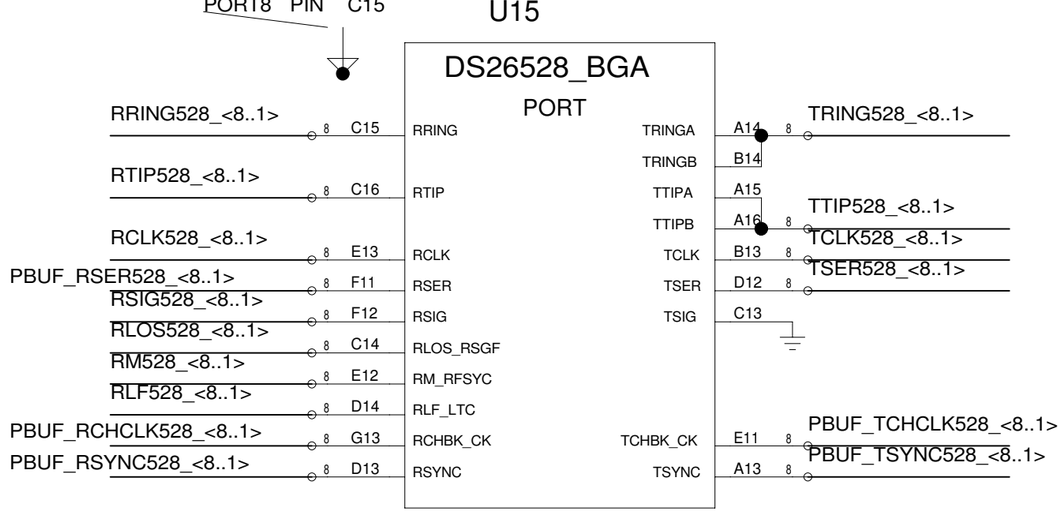
BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:08 2007





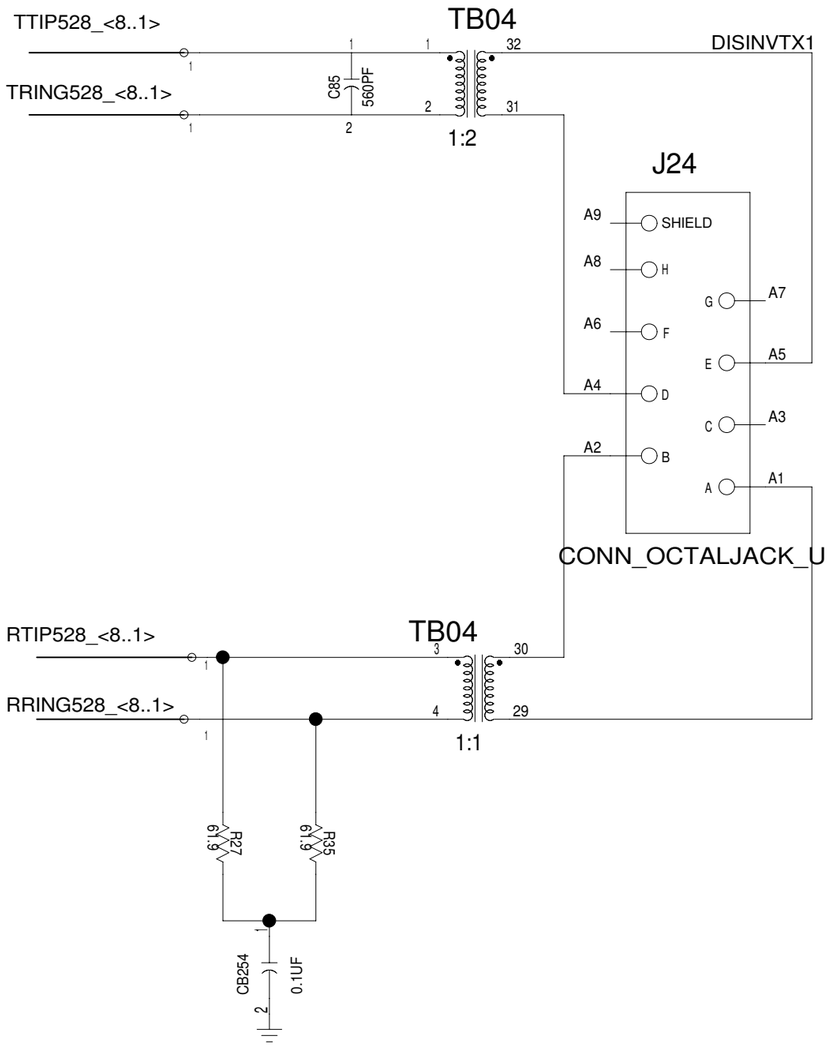


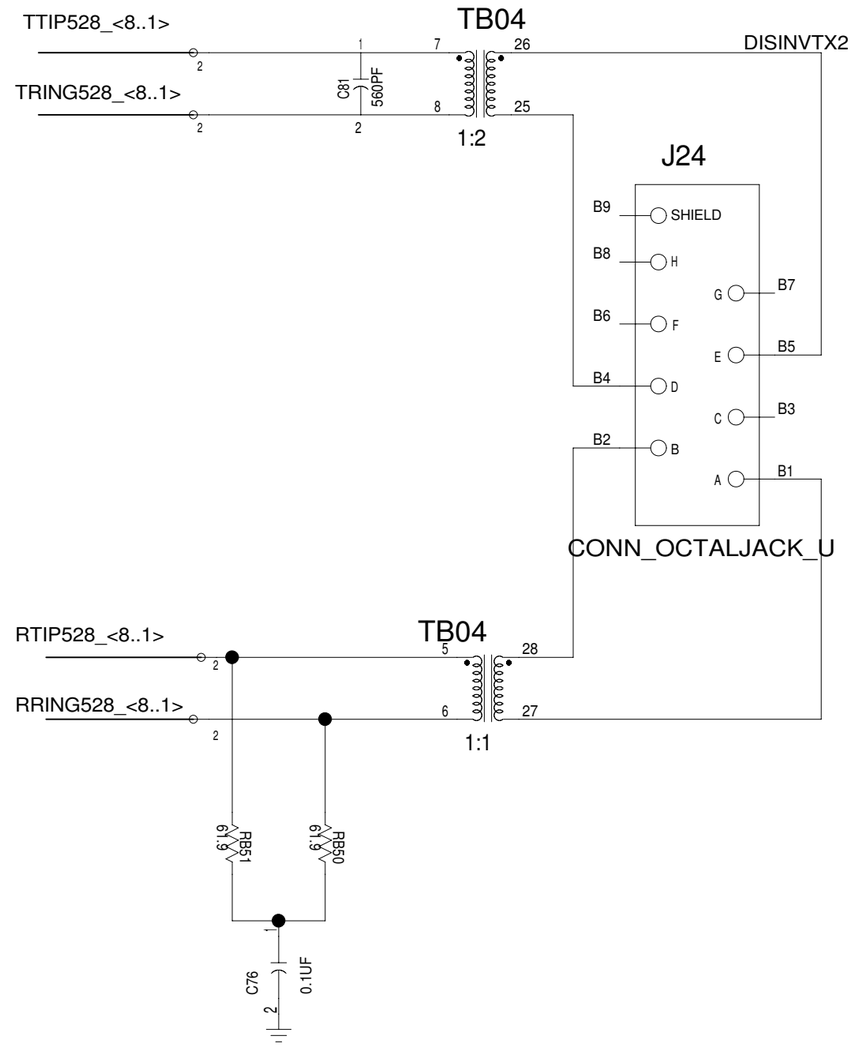


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/8(BLOCK) 43/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:08 2007





TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/8(BLOCK) 44/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

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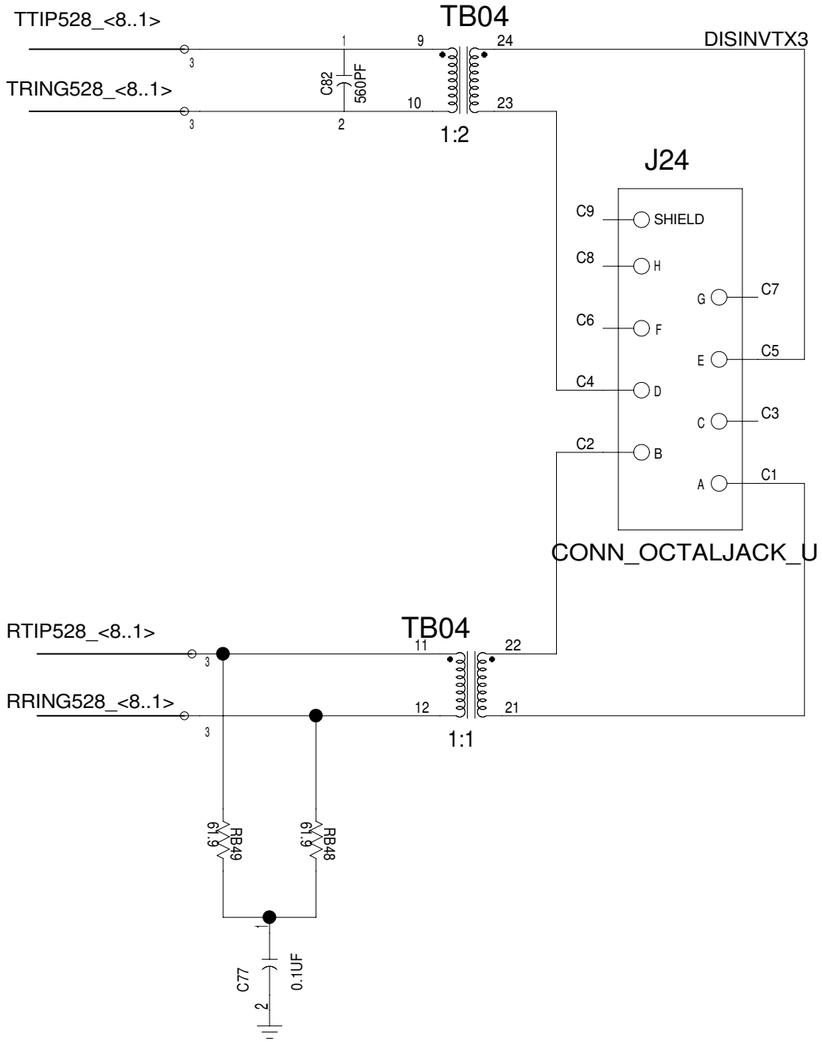

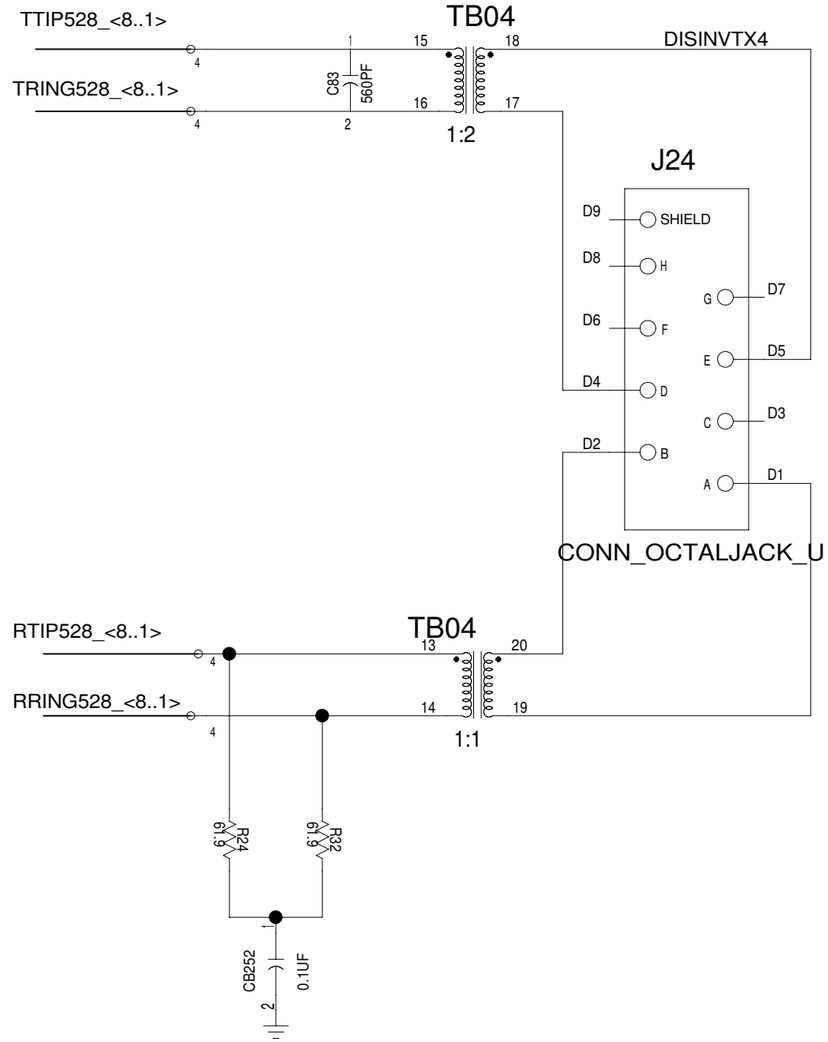

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/8(BLOCK) 45/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

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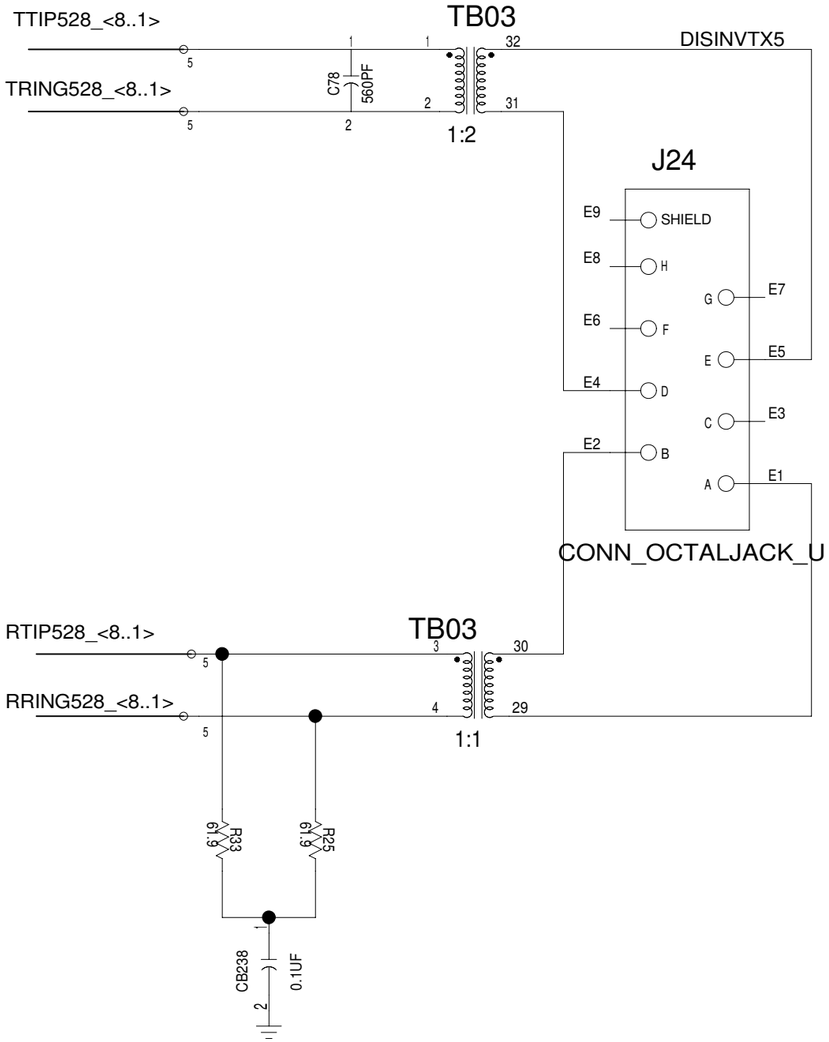
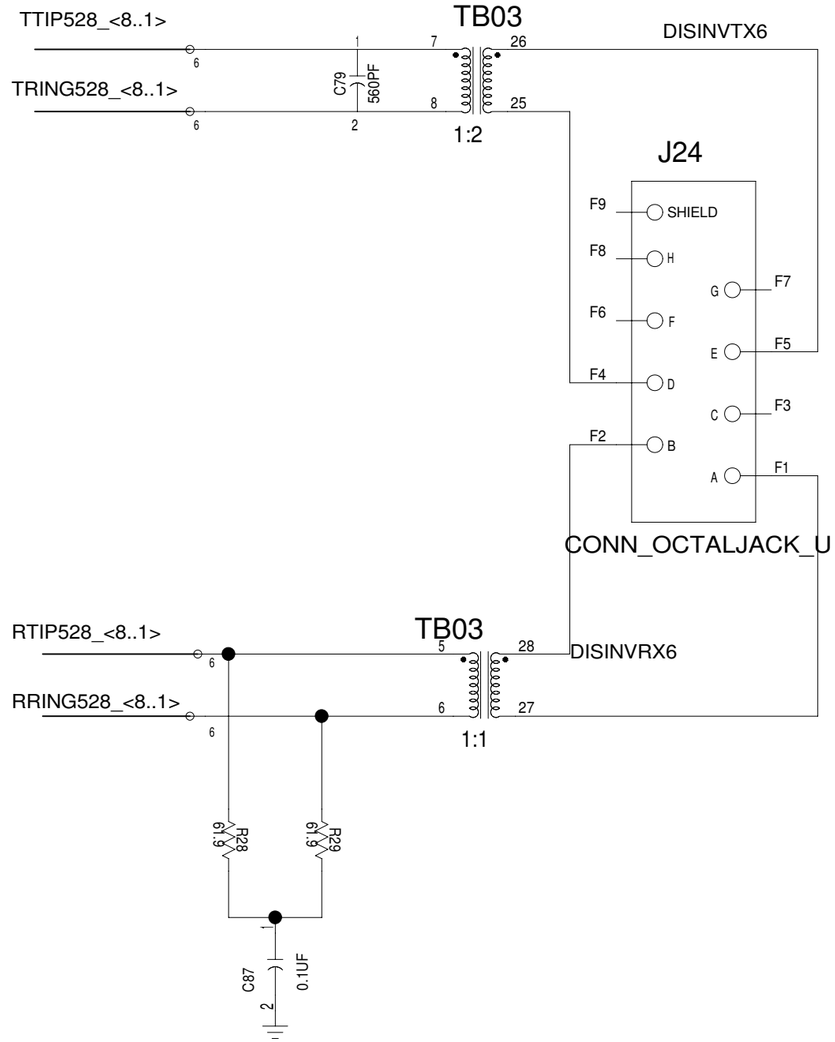
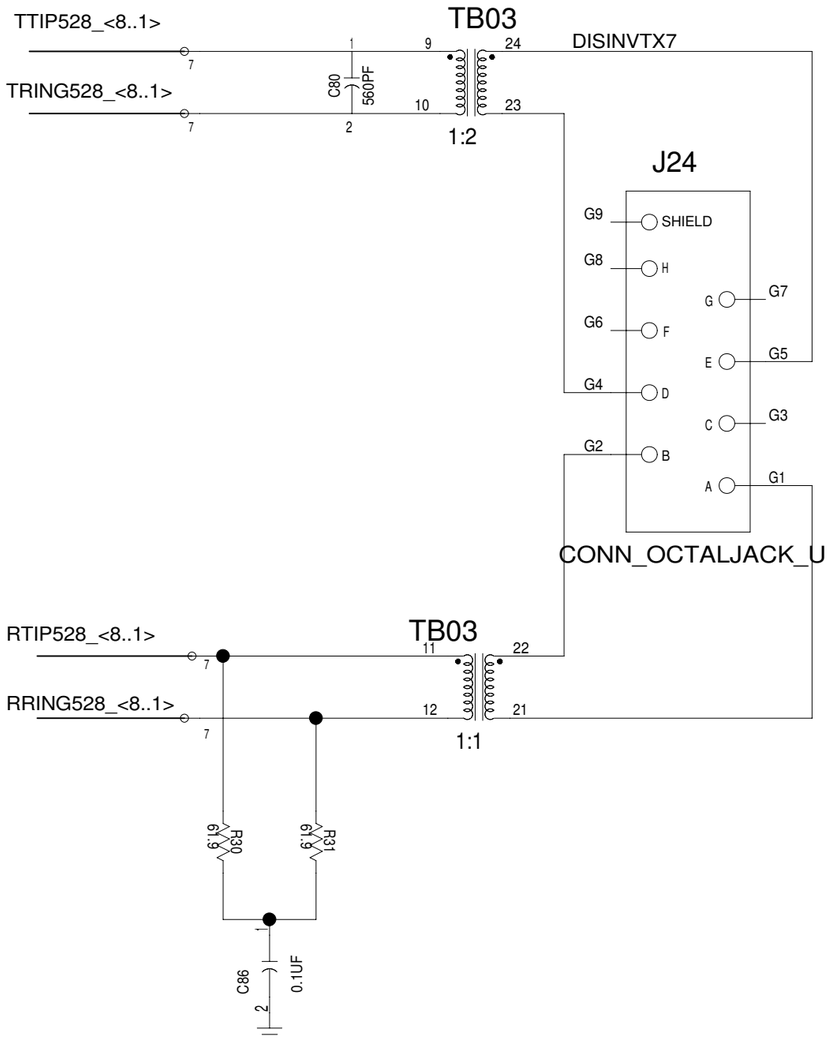


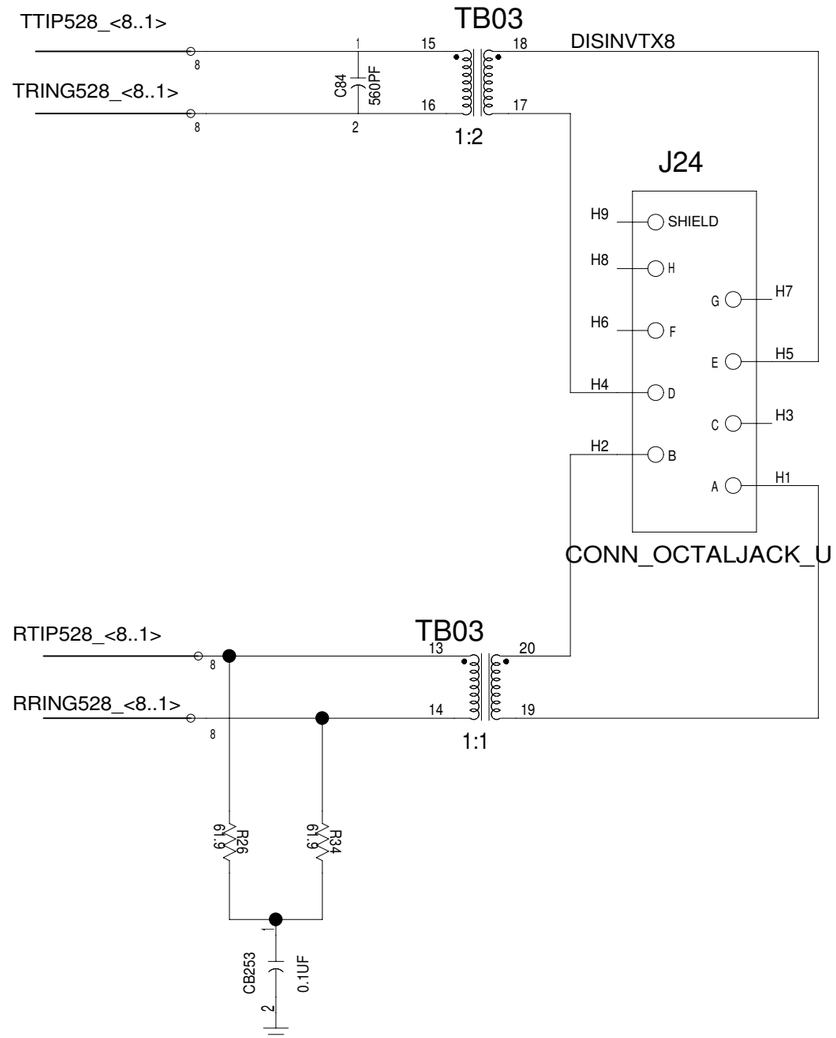


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 6/8(BLOCK) 46/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:08 2007





TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 47/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

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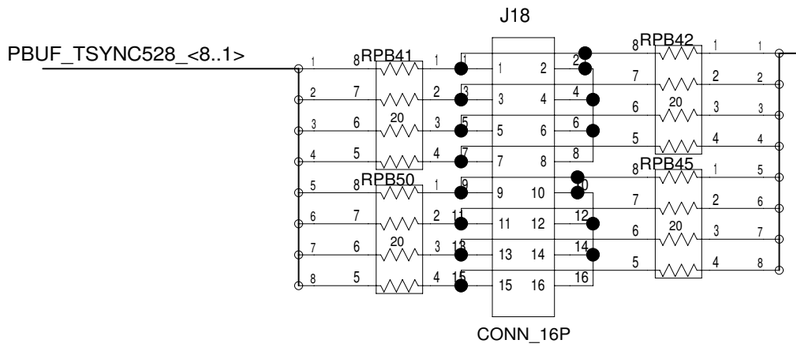
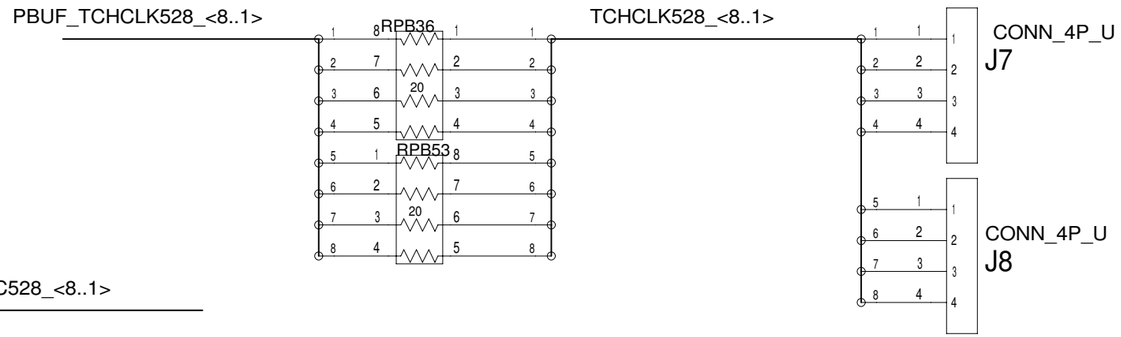
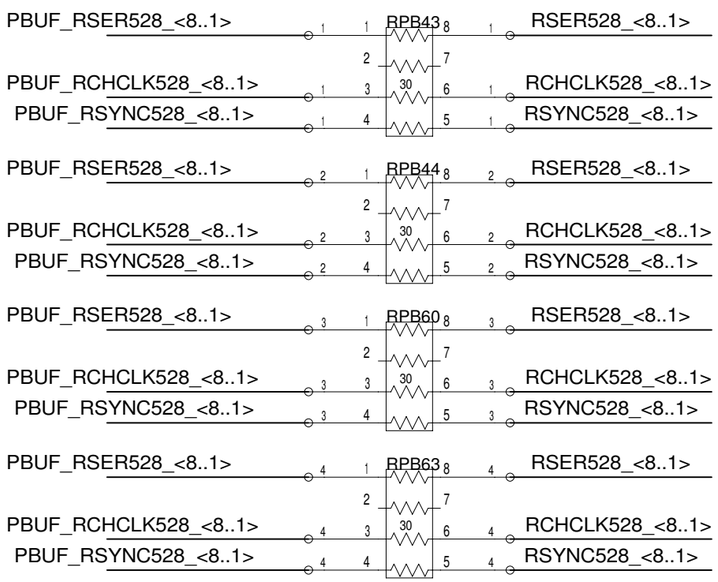
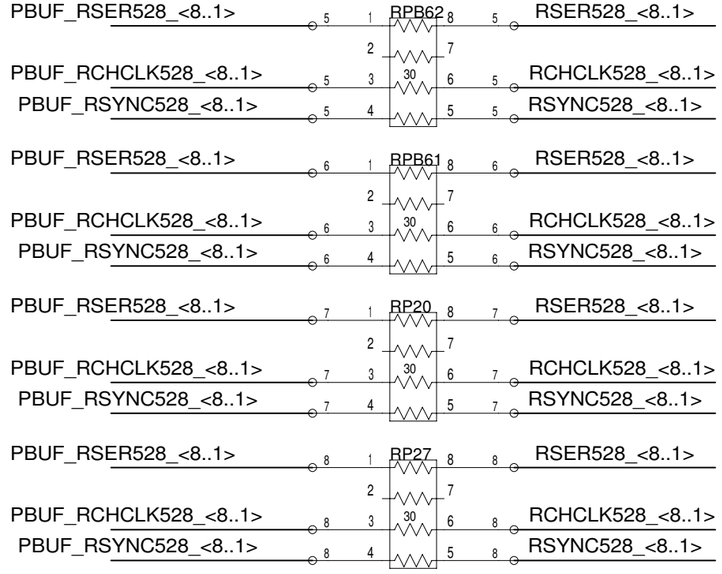




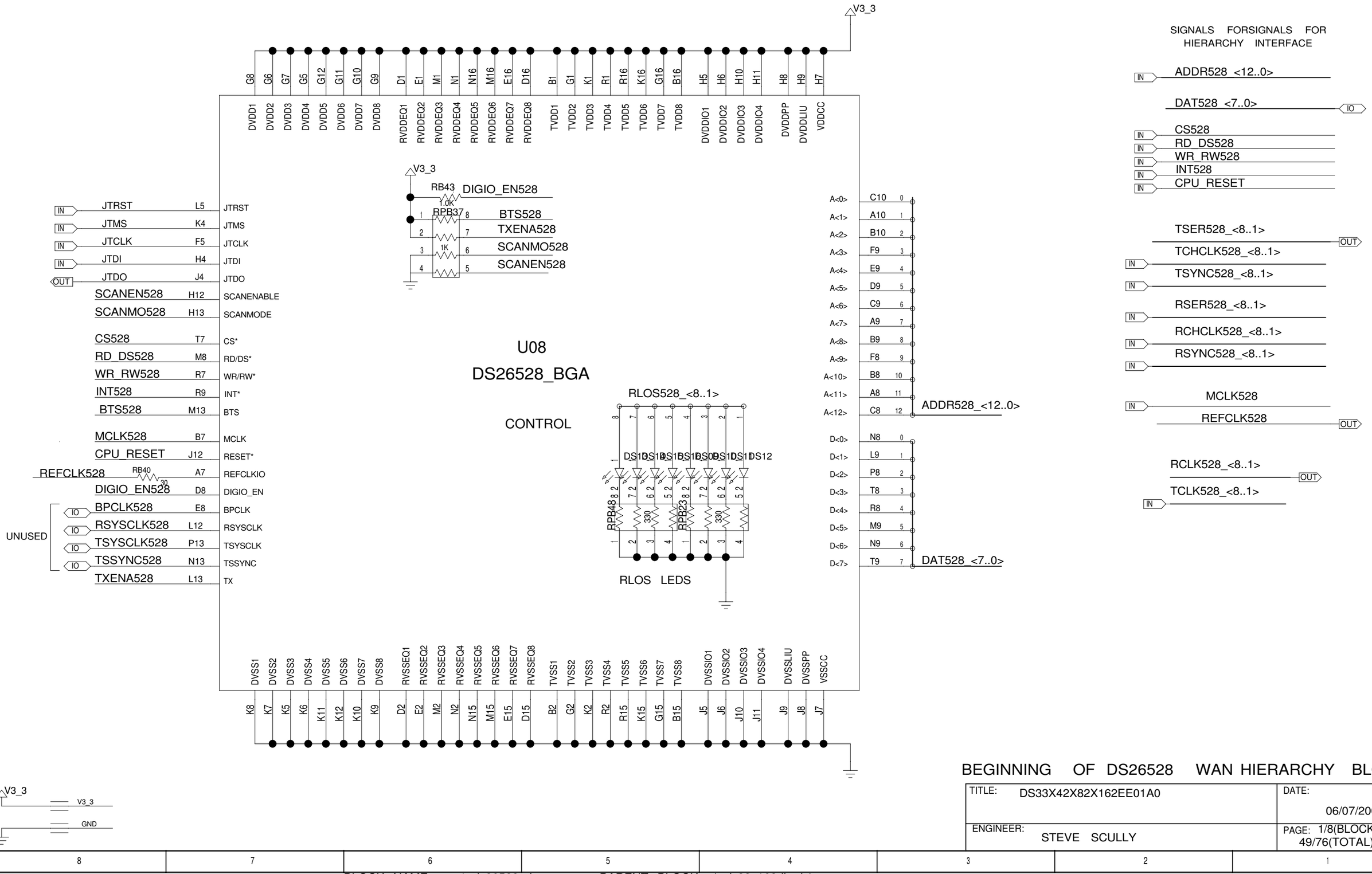


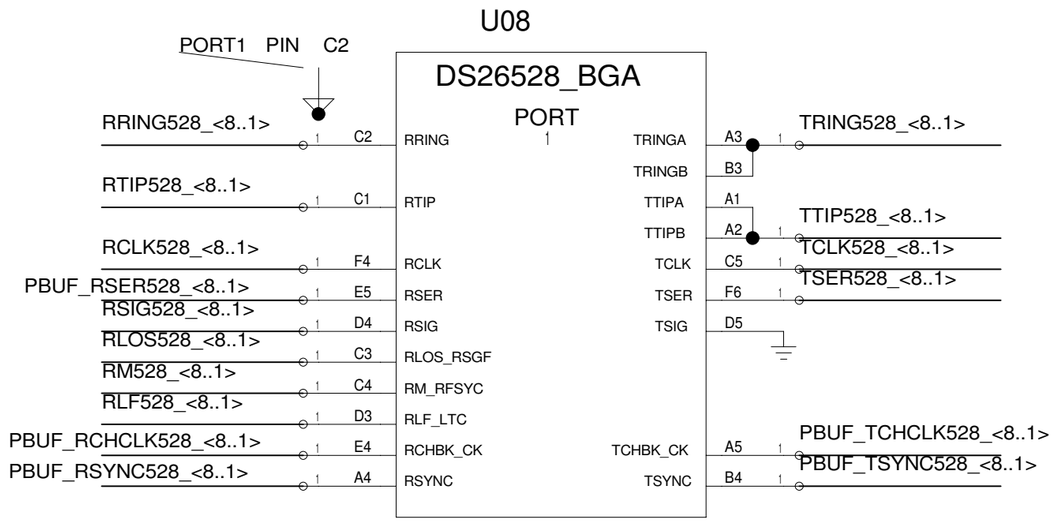


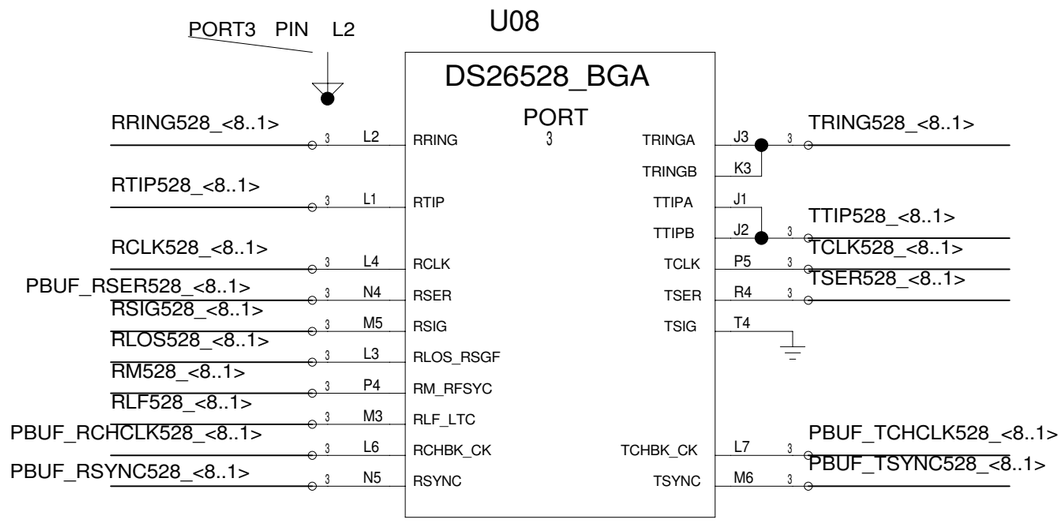
JUMPERS FOR GAPCLK AND SYNC
TO BE PLACED CLOSE TO
THE OTHER EIGHT T1E1 PORTS
TO ALLOW CONNECTION WITH JUMPER

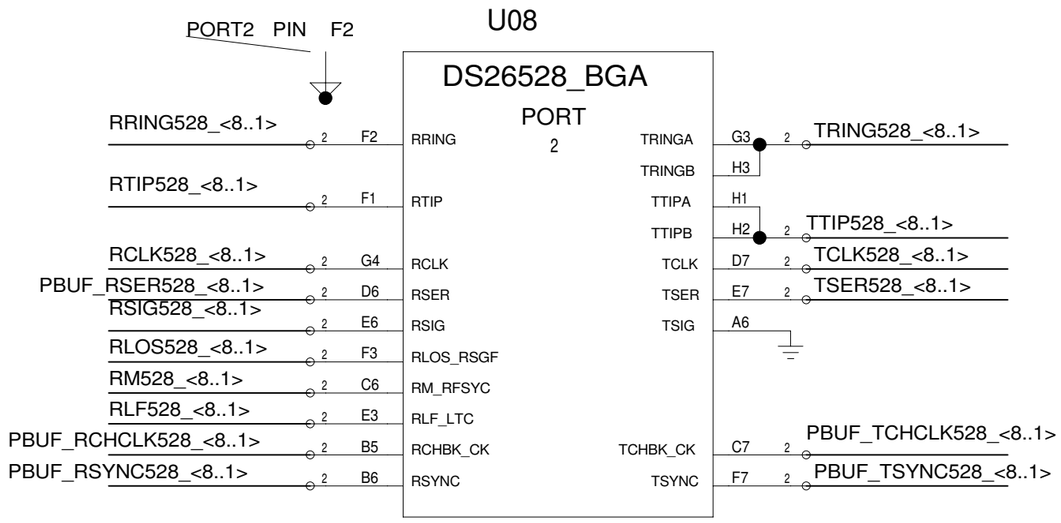
END OF DS26528 WAN HIERARCHY BLOCK

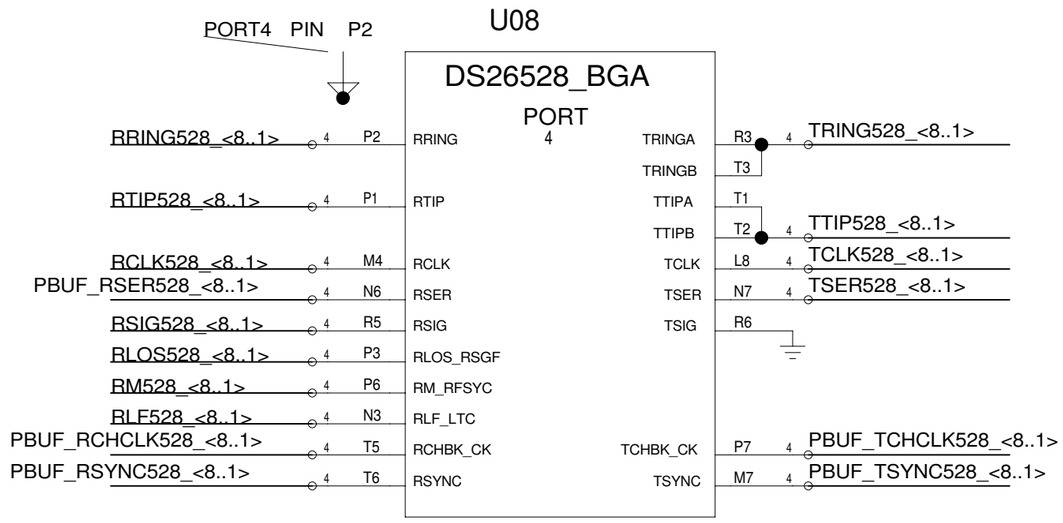
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 48/76(TOTAL)


V3_3
G8 G6 G7 G5 G12 G11 G10 G9 D1 E1 M1 N1 N16 M16 E16 D16 B1 G1 K1 R1 R16 K16 G16 B16 H5 H6 H10 H11 H8 H9 H7
DVDD1 DVDD2 DVDD3 DVDD4 DVDD5 DVDD6 DVDD7 DVDD8 RVDDEQ1 RVDDEQ2 RVDDEQ3 RVDDEQ4 RVDDEQ5 RVDDEQ6 RVDDEQ7 RVDDEQ8 TVDD1 TVDD2 TVDD3 TVDD4 TVDD5 TVDD6 TVDD7 TVDD8 DVDDIO1 DVDDIO2 DVDDIO3 DVDDIO4 DVDDPP DVDDLIU VDDCC
SIGNALS FORSIGNALS FOR HIERARCHY INTERFACE
IN ADDR528_<12..0>
DAT528_<7..0> IO
IN CS528
IN RD_DS528
IN WR_RW528
IN INT528
IN CPU_RESET
TSER528_<8..1> OUT
TCHCLK528_<8..1>
IN TSYNC528_<8..1>
IN
RSER528_<8..1>
IN RCHCLK528_<8..1>
IN RSYNC528_<8..1>
IN
MCLK528
IN REFCLK528 OUT
RCLK528_<8..1> OUT
TCLK528_<8..1> IN
IN JTRST L5 JTRST
IN JTMS K4 JTMS
IN JTCLK F5 JTCLK
IN JTDI H4 JTDI
OUT JTDO J4 JTDO
SCANEN528 H12 SCANENABLE
SCANMO528 H13 SCANMODE
CS528 T7 CS*
RD_DS528 M8 RD/DS*
WR_RW528 R7 WR/RW*
INT528 R9 INT*
BTS528 M13 BTS
MCLK528 B7 MCLK
CPU_RESET J12 RESET*
REFCLK528 RB40 30 A7 REFCLKIO
DIGIO_EN528 D8 DIGIO_EN
UNUSED
IO BPCLK528 E8 BPCLK
IO RSYSCLK528 L12 RSYSCLK
IO TSYSCLK528 P13 TSYSCLK
IO TSSYNC528 N13 TSSYNC
TXENA528 L13 TX
V3_3
RB43 1.0K DIGIO_EN528
RPB37 1K
1 8 BTS528
2 7 TXENA528
3 6 SCANMO528
4 5 SCANEN528
U08
DS26528_BGA
CONTROL
RLOS528_<8..1>
DS1 DS2 DS3 DS4 DS5 DS6 DS7 DS8
RPB48 RPB23 330
RLOS LEDS
A<0> C10 0
A<1> A10 1
A<2> B10 2
A<3> F9 3
A<4> E9 4
A<5> D9 5
A<6> C9 6
A<7> A9 7
A<8> B9 8
A<9> F8 9
A<10> B8 10
A<11> A8 11
A<12> C8 12
ADDR528_<12..0>
D<0> N8 0
D<1> L9 1
D<2> P8 2
D<3> T8 3
D<4> R8 4
D<5> M9 5
D<6> N9 6
D<7> T9 7
DAT528_<7..0>
DVSS1 DVSS2 DVSS3 DVSS4 DVSS5 DVSS6 DVSS7 DVSS8 RVSSEQ1 RVSSEQ2 RVSSEQ3 RVSSEQ4 RVSSEQ5 RVSSEQ6 RVSSEQ7 RVSSEQ8 TVSS1 TVSS2 TVSS3 TVSS4 TVSS5 TVSS6 TVSS7 TVSS8 DVSSIO1 DVSSIO2 DVSSIO3 DVSSIO4 DVSSLIU DVSSPP VSSCC
K8 K7 K5 K6 K11 K12 K10 K9 D2 E2 M2 N2 N15 M15 E15 D15 B2 G2 K2 R2 R15 K15 G15 B15 J5 J6 J10 J11 J9 J8 J7
V3_3
V3_3
GND
BEGINNING OF DS26528 WAN HIERARCHY BLOCK
TITLE: DS33X42X82X162EE01A0
DATE: 06/07/2006
ENGINEER: STEVE SCULLY
PAGE: 1/8(BLOCK) 49/76(TOTAL)
BLOCK NAME: _te1_ds26528_dn.
PARENT BLOCK: _ds33x162dk_dn\
PRINTED Mon Feb 11 13:57:23 2008

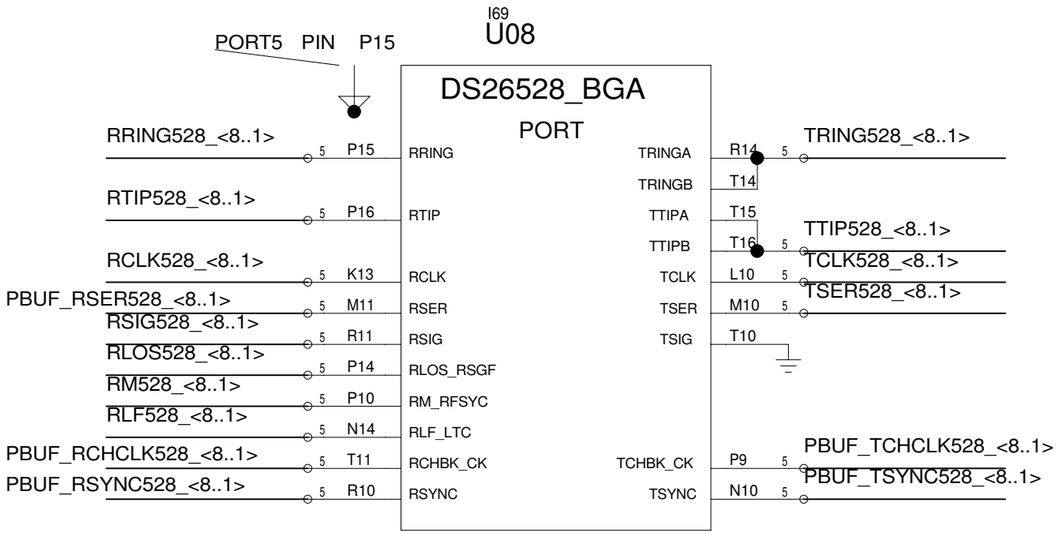


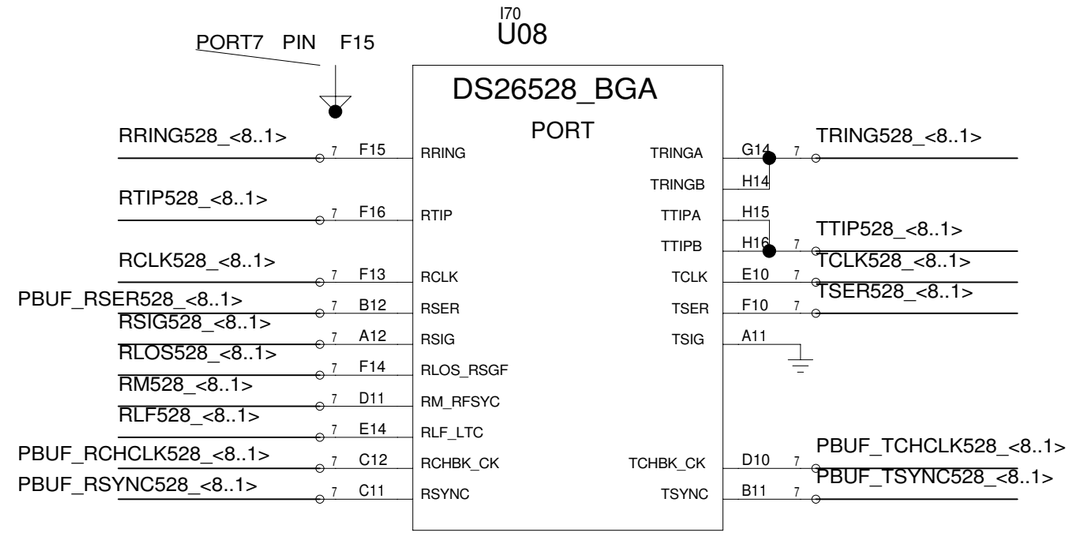


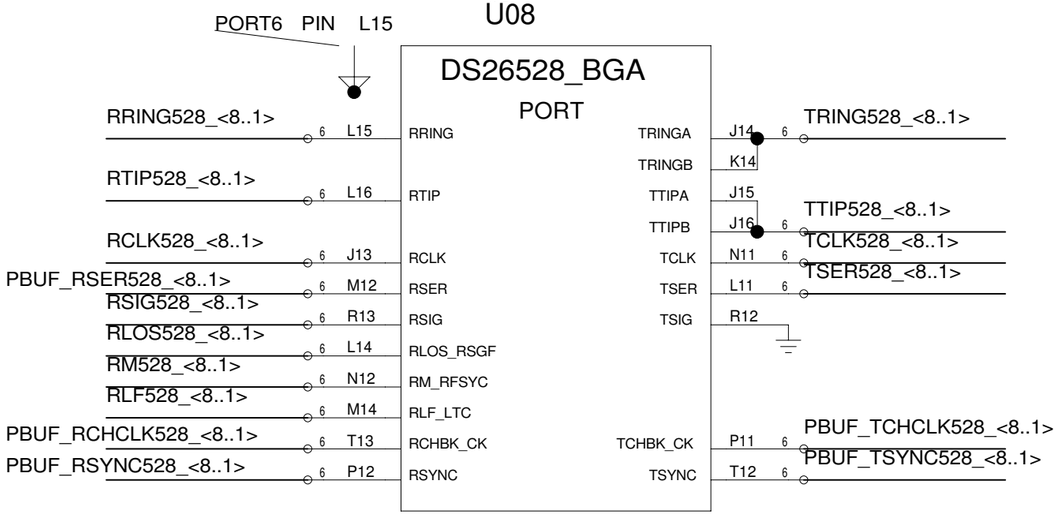


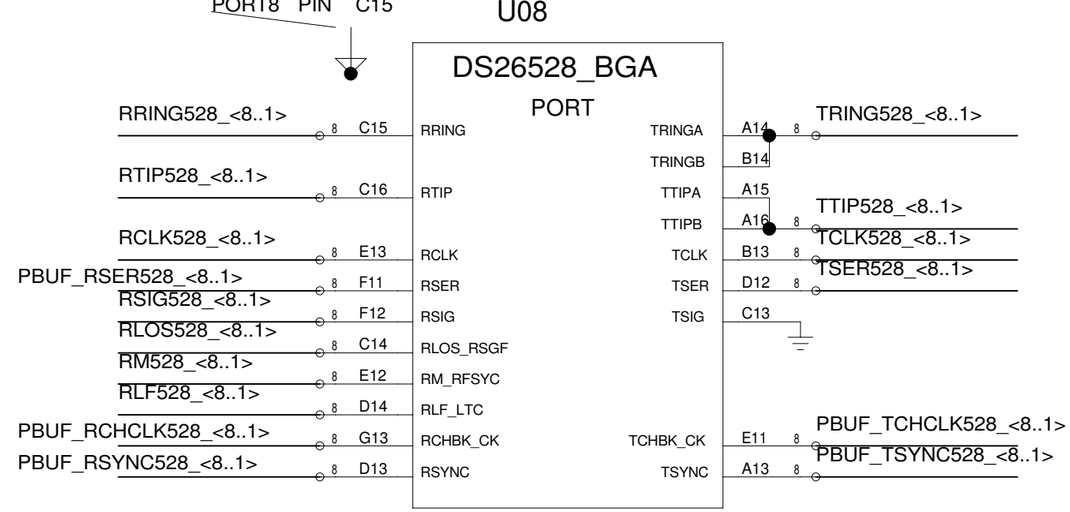


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/8(BLOCK) 50/76(TOTAL)





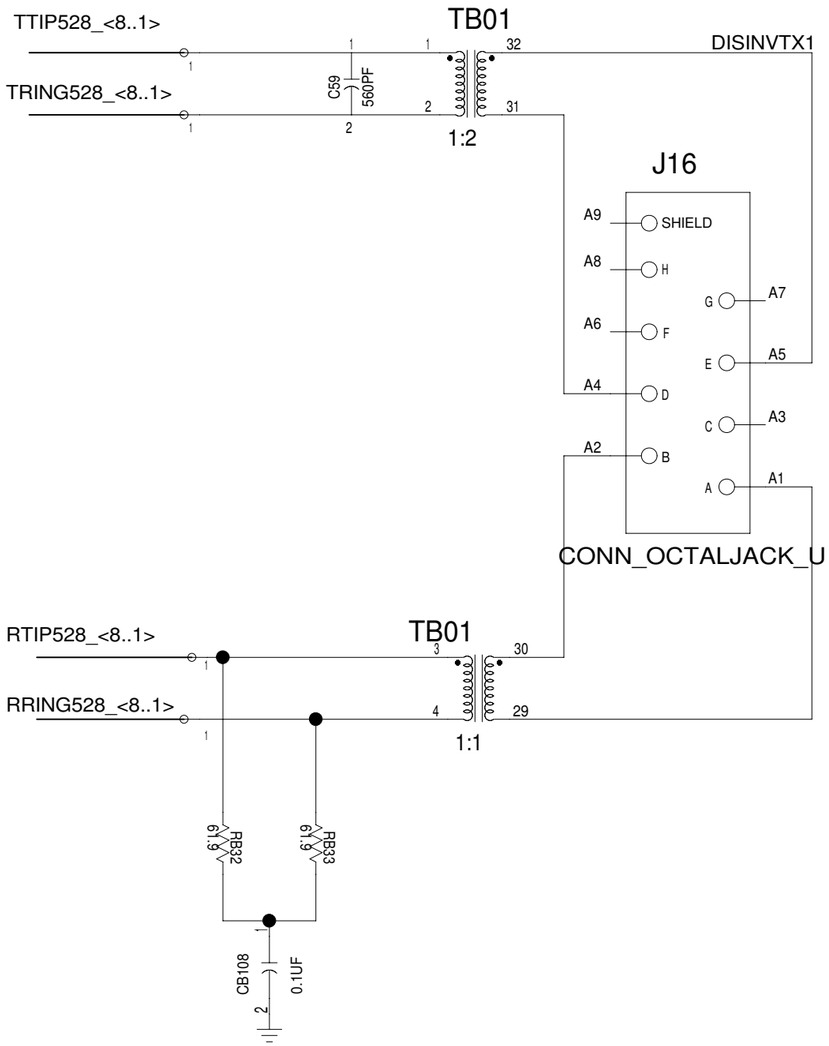


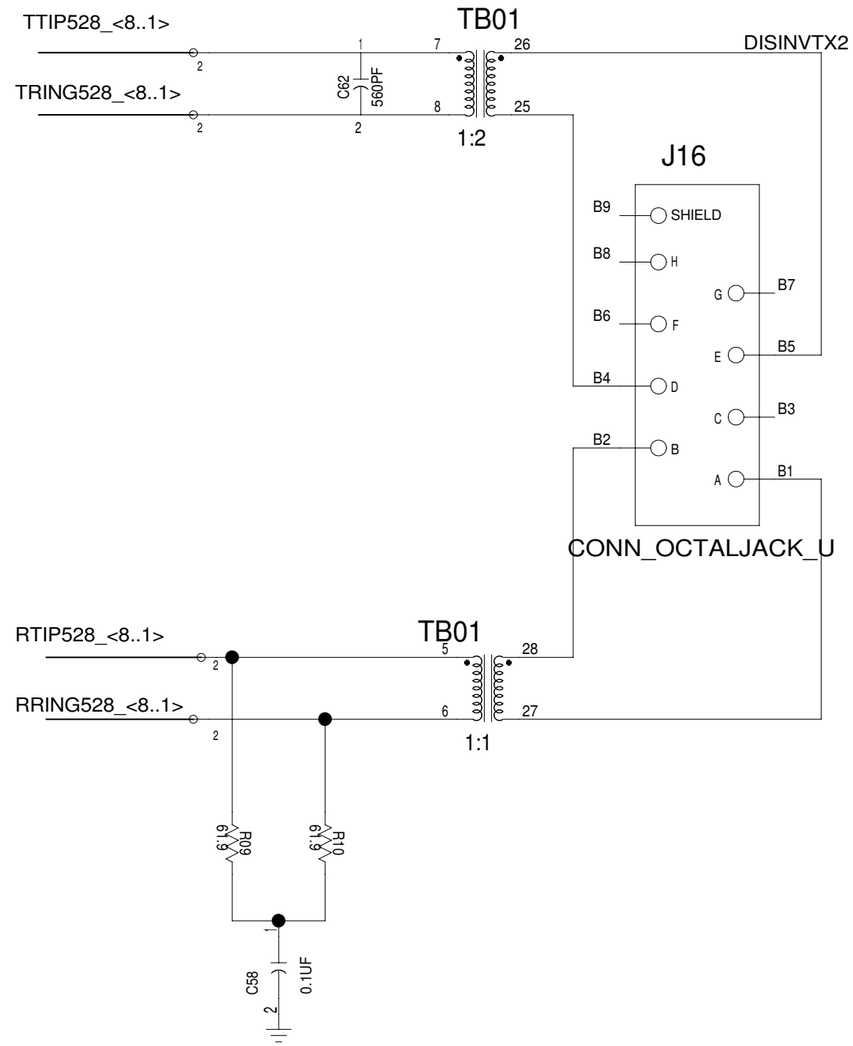


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/8(BLOCK) 51/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:08 2007

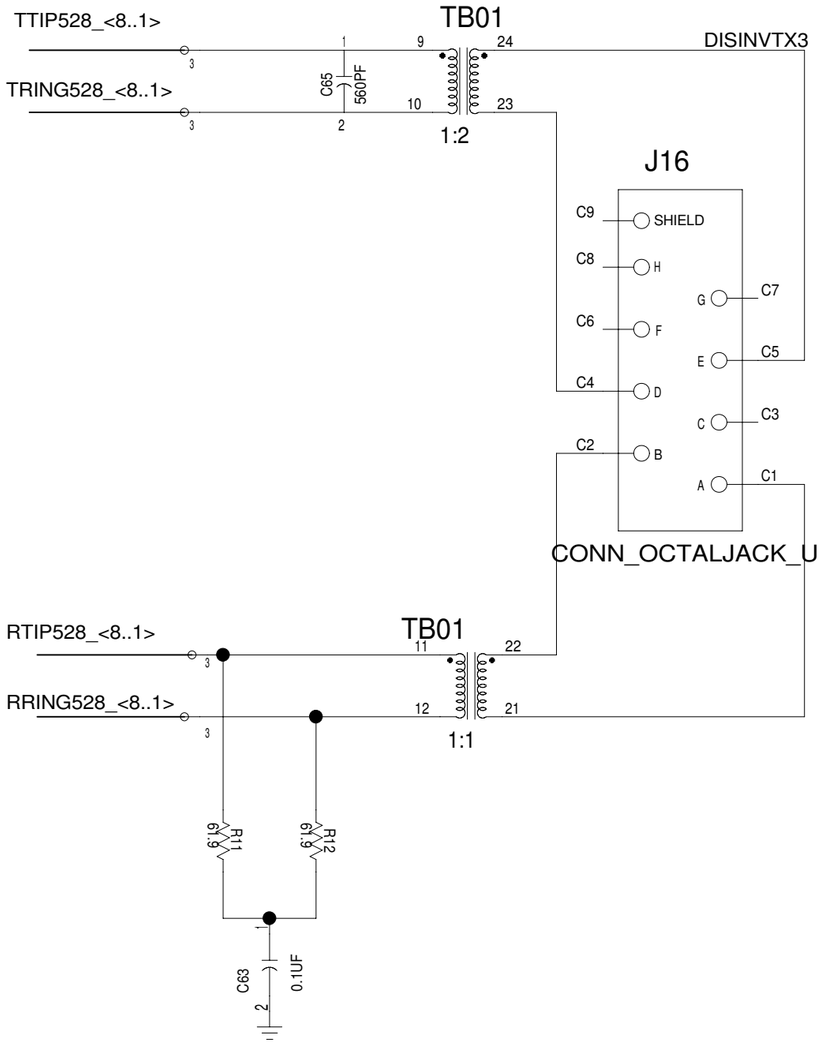


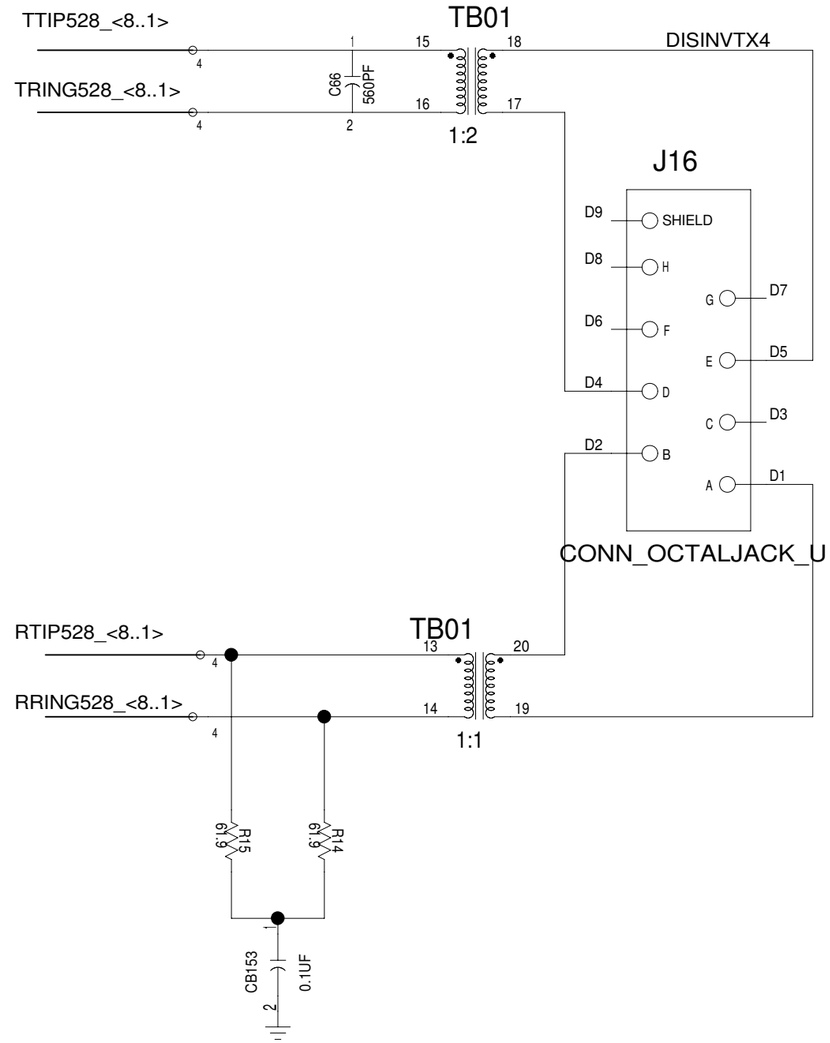


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/8(BLOCK) 52/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:07 2007

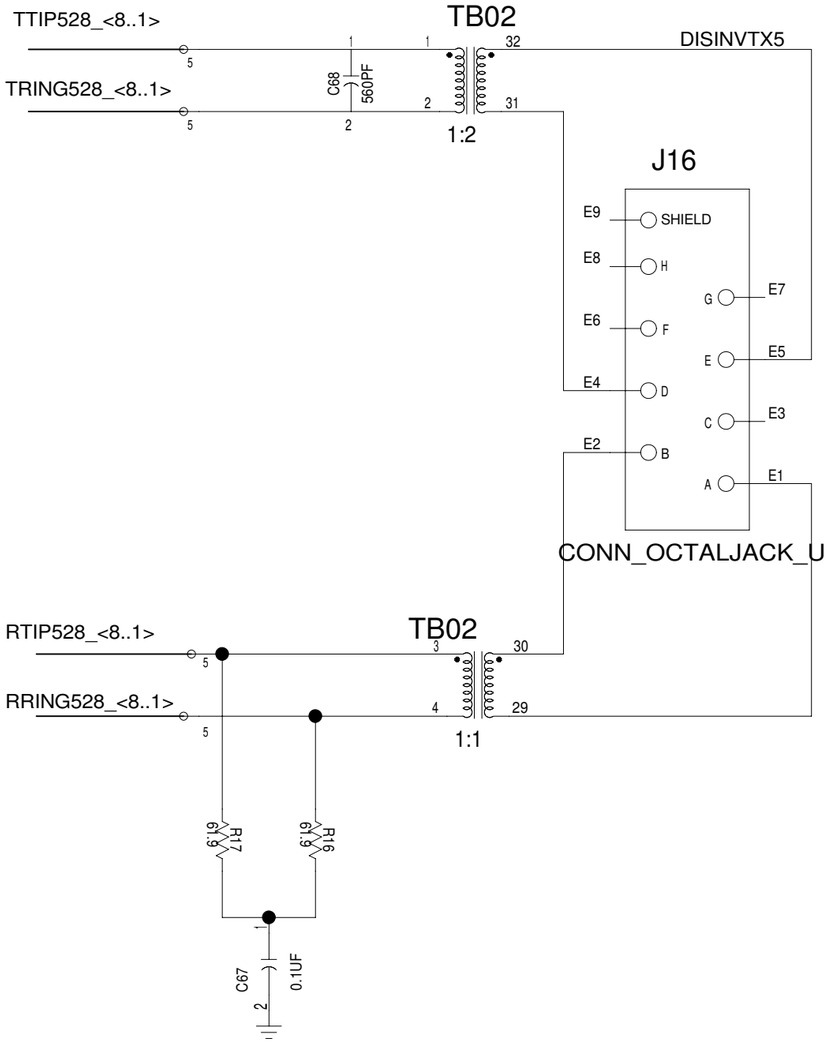


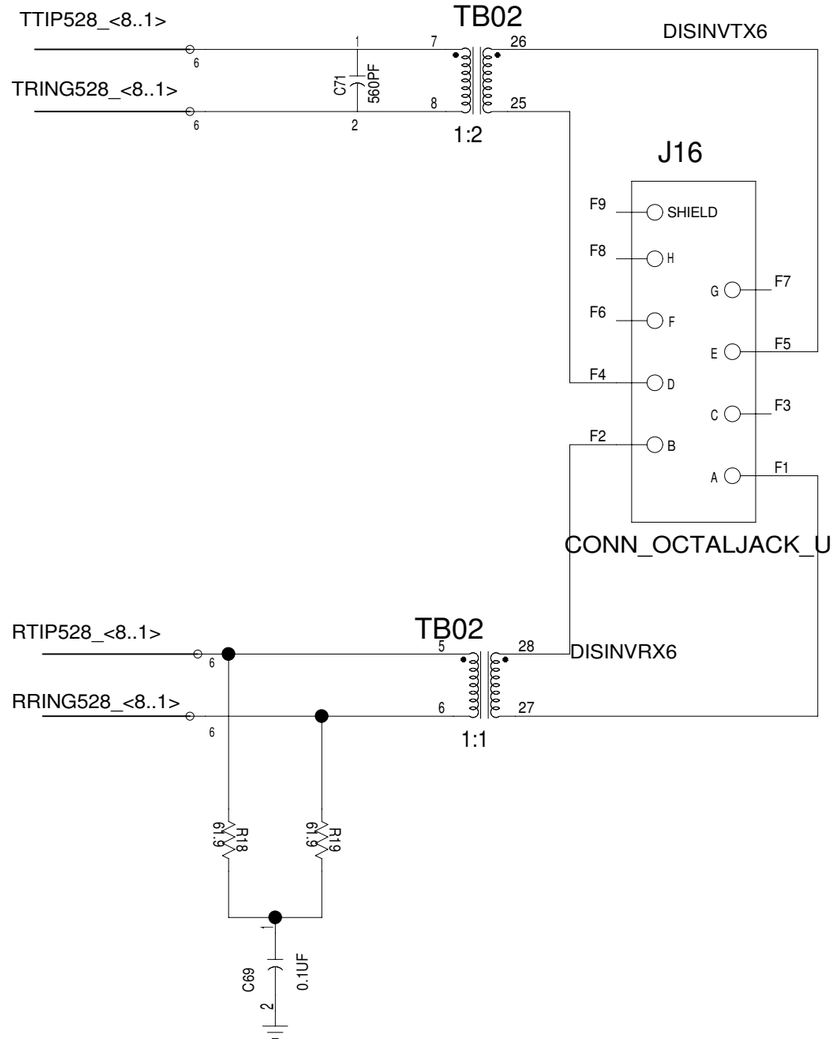


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/8(BLOCK) 53/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:07 2007

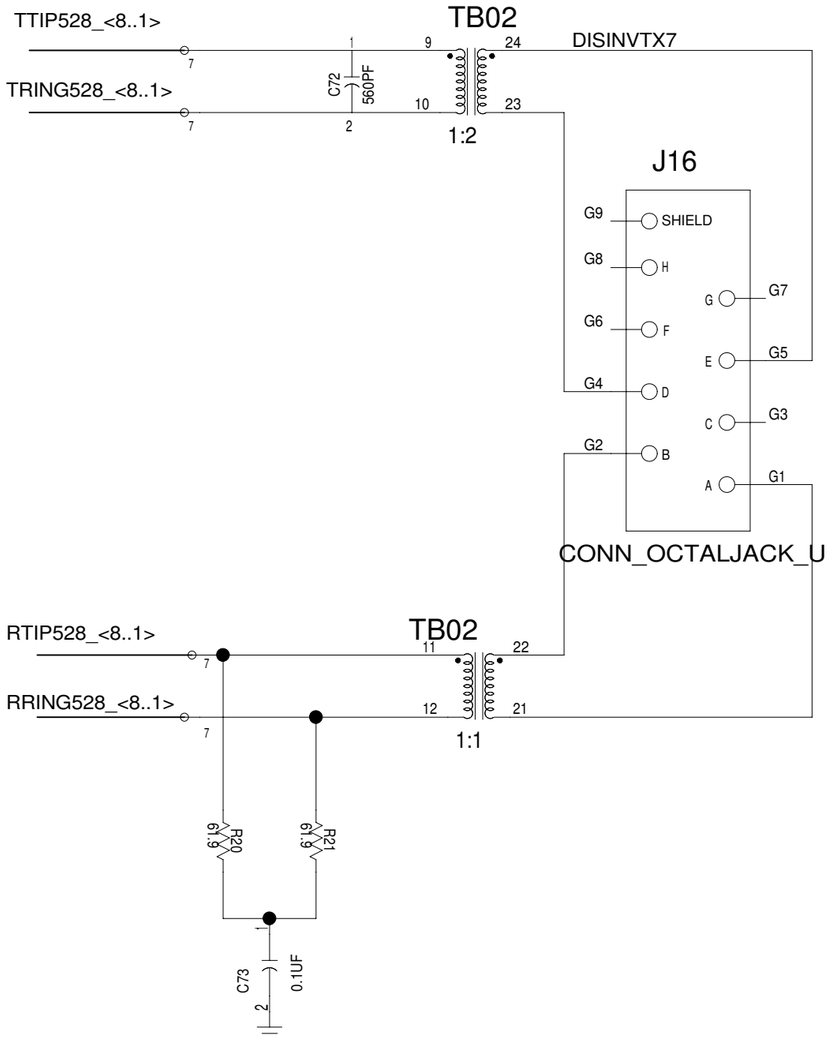


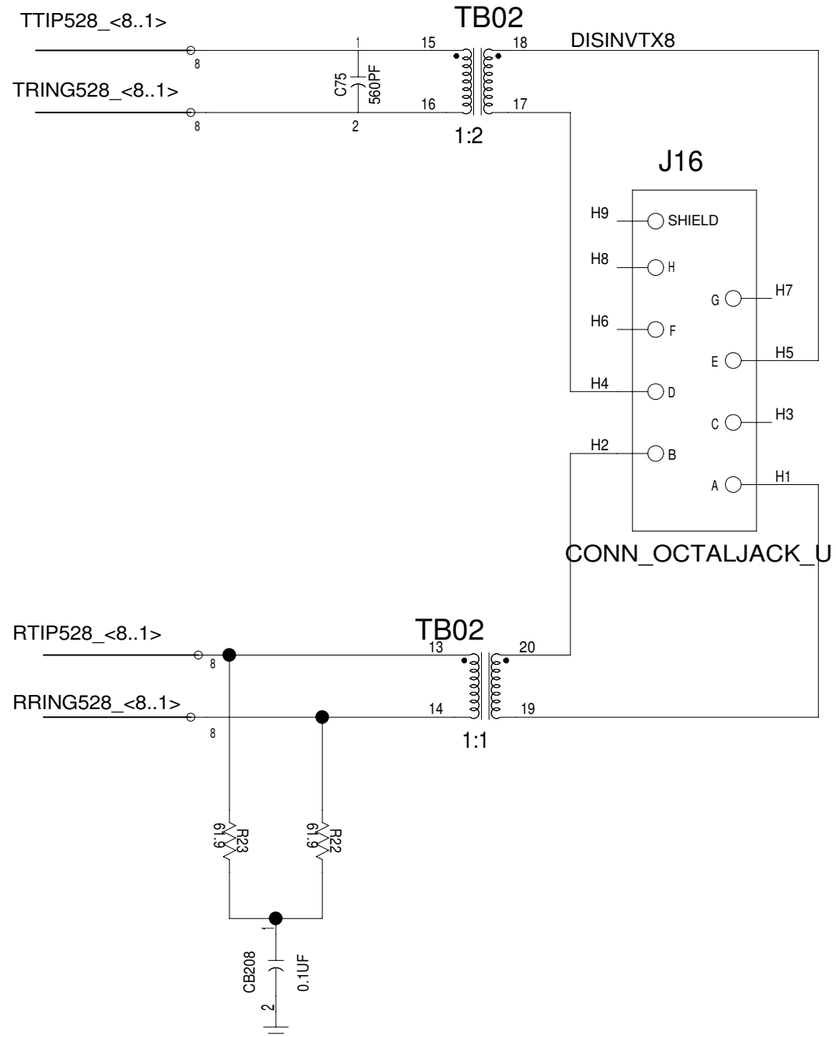


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 6/8(BLOCK) 54/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon May 14 11:04:08 2007





TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 55/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

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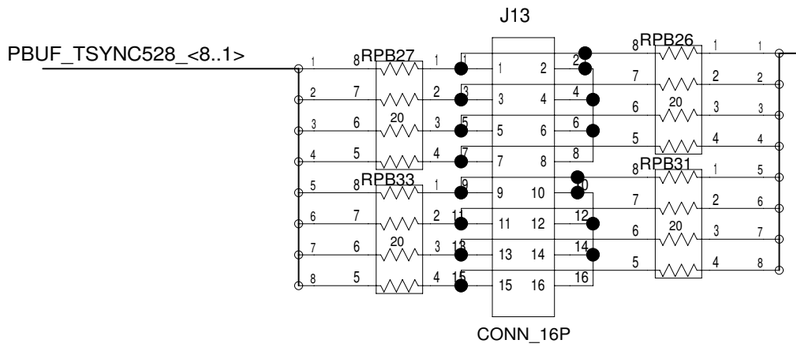
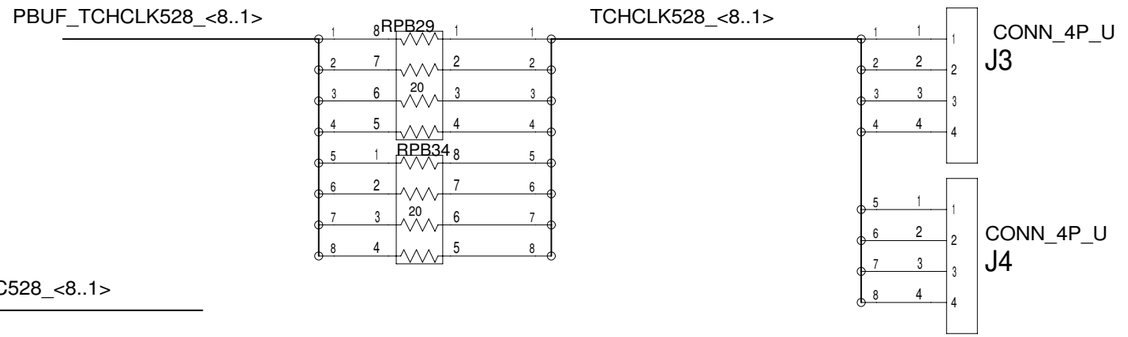
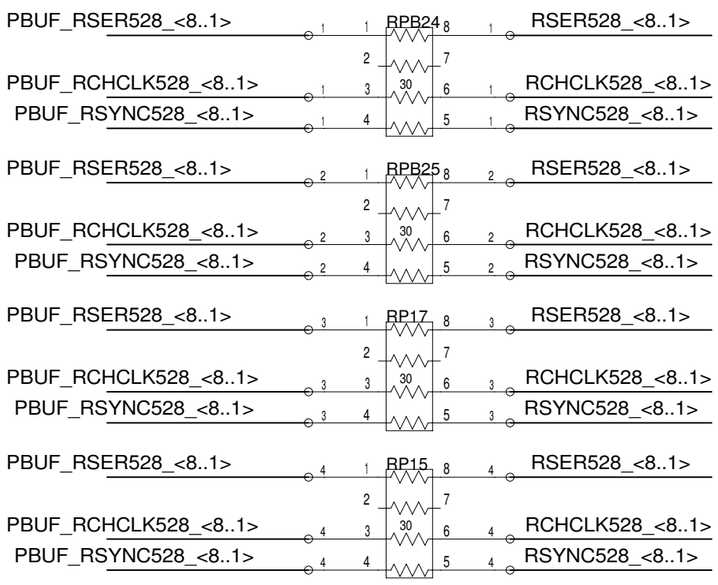
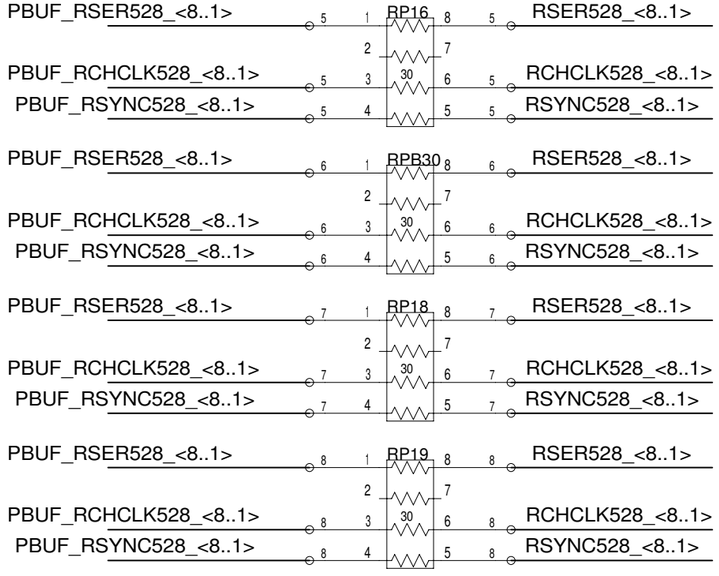








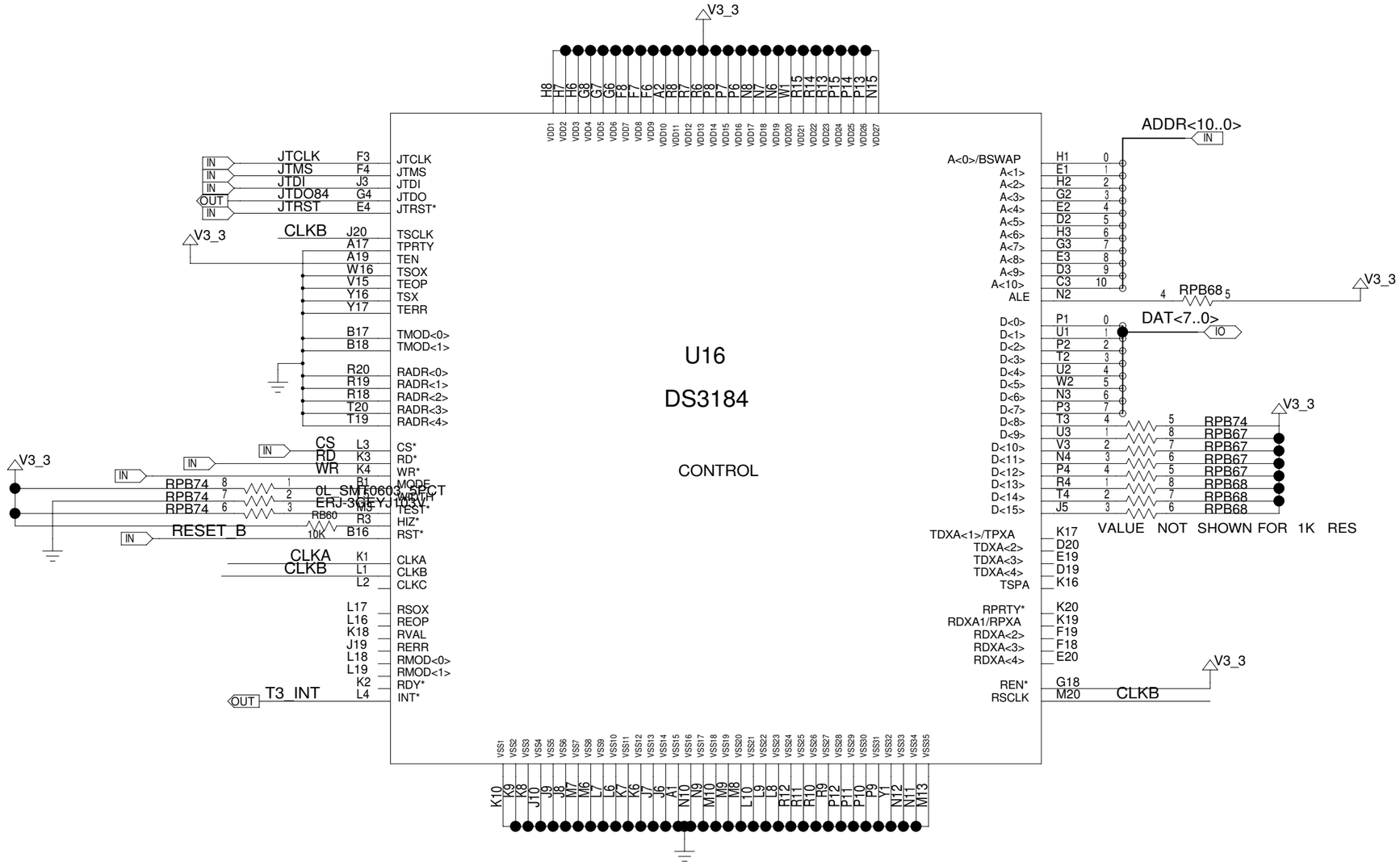
JUMPERS FOR GAPCLK AND SYNC
TO BE PLACED CLOSE TO
THE OTHER EIGHT T1E1 PORTS
TO ALLOW CONNECTION WITH JUMPER

END OF DS26528 WAN HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 56/76(TOTAL)

BLOCK NAME: _te1_ds26528_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon Feb 11 13:57:55 2008

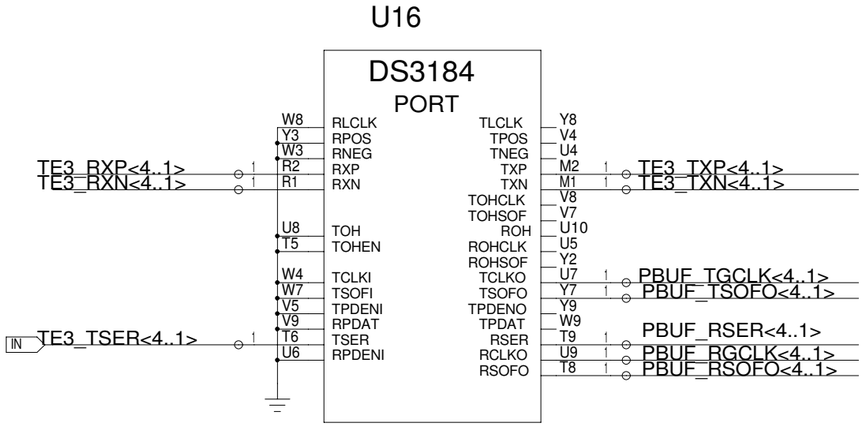


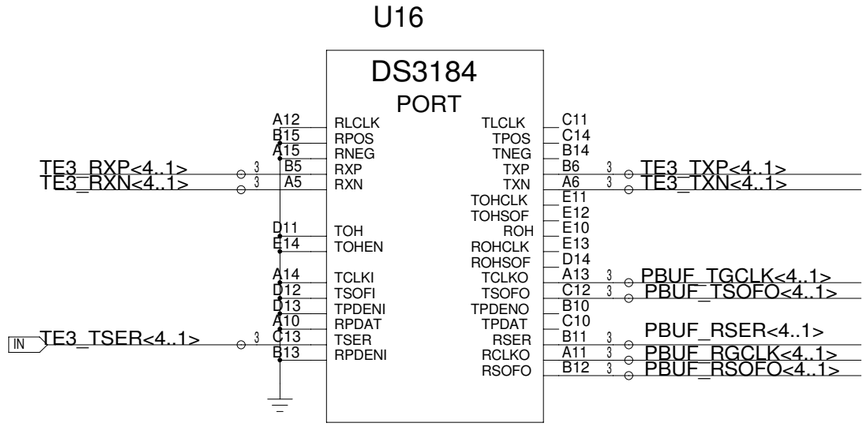
BEGINNING OF DS3184 WAN HIERARCHY BLOCK

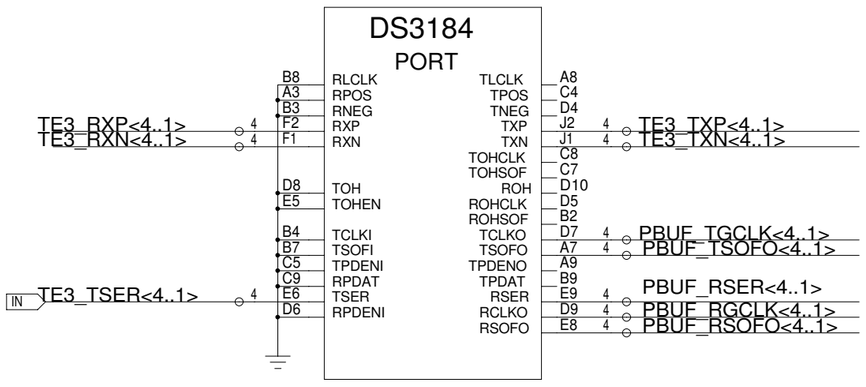
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/5(BLOCK) 57/76(TOTAL)

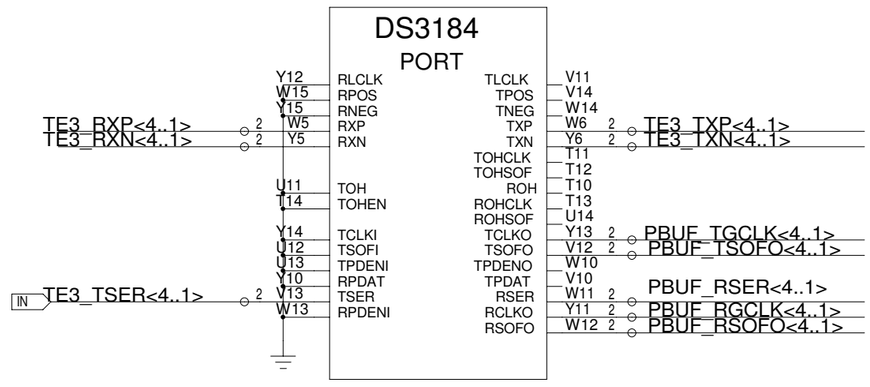
BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\

PRINTED Mon Feb 11 13:56:05 2008







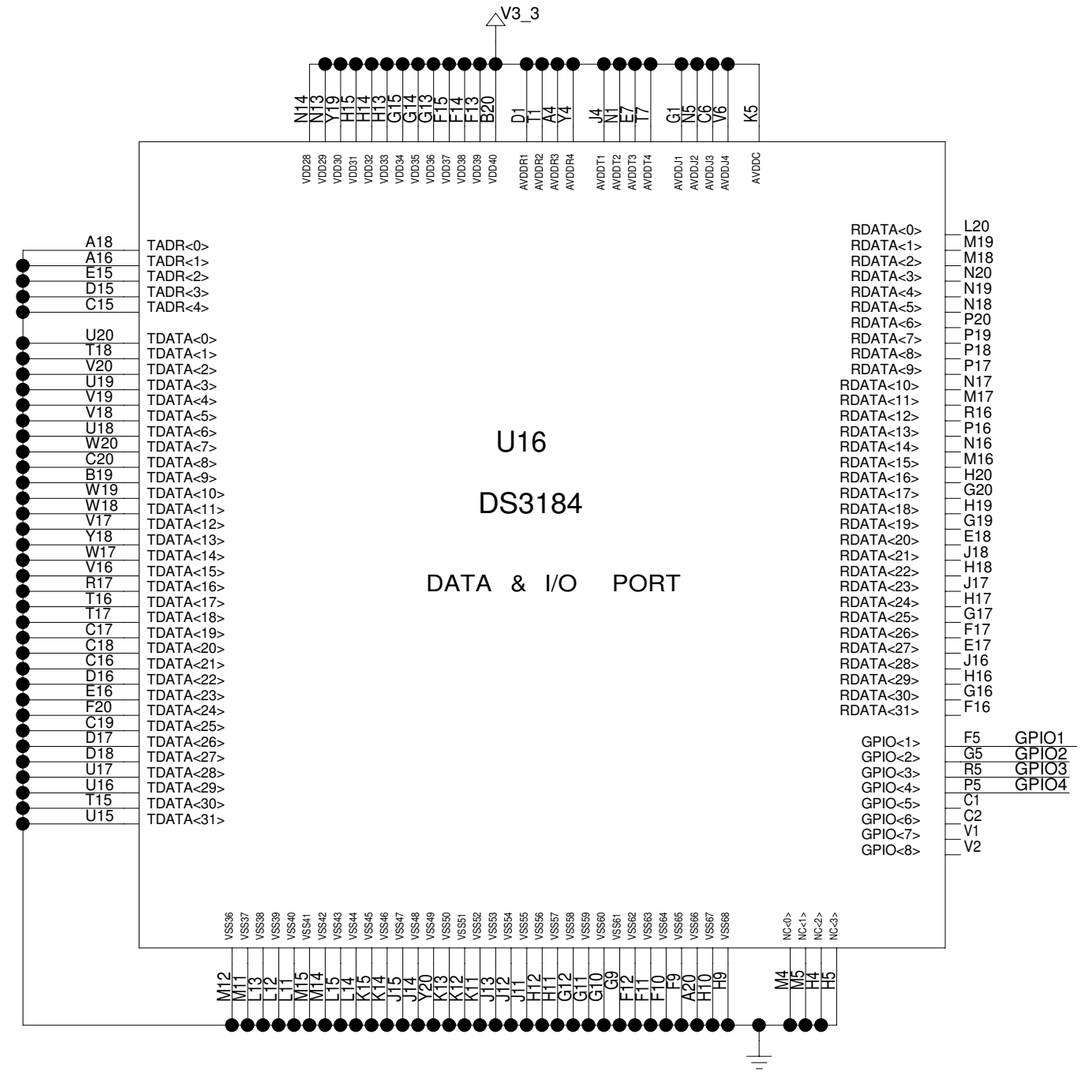


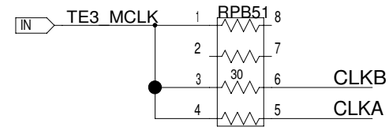
DS3184 PORT NUMBERS DO NOT MATCH DS33X162 PORT NUMBERS
PORT MAPPING IS AS FOLLOWS:
DS33X162_PORT: 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8
DS3184 PORT: 2A, 4A, 3A, 1A, 2B, 4B, 3B, 1B
ALL PCB SILKSCREEN CORRESPONDS TO THE DS33X162 PORT NUMBER
THIS MAP IS ONLY NEEDED FOR DS3184 REGISTER ACCESS

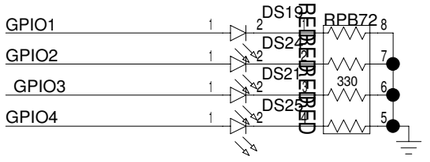
DS3184 PORT#/RCLK_PIN#
PORT1=PINB8
PORT3=PINA12
PORT2=PINW8
PORT4=PINY12

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/5(BLOCK) 58/76(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\

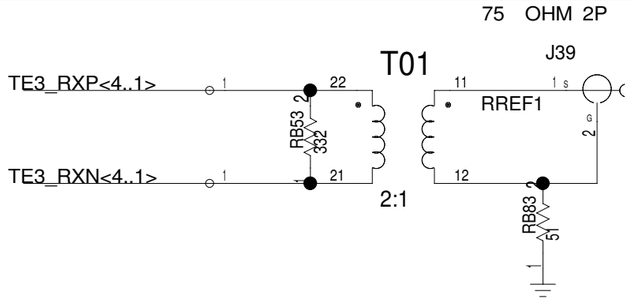


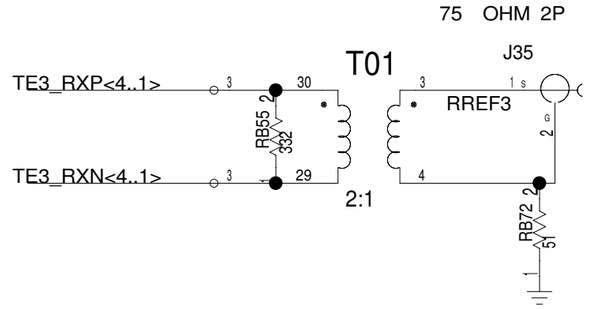


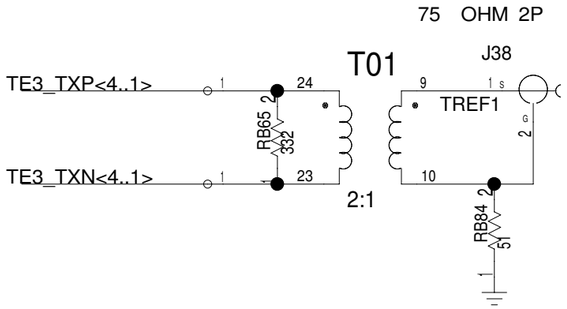


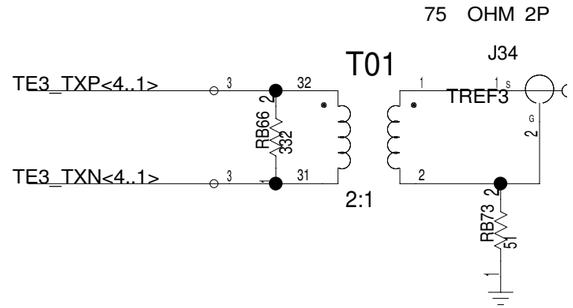
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 59/76(TOTAL)

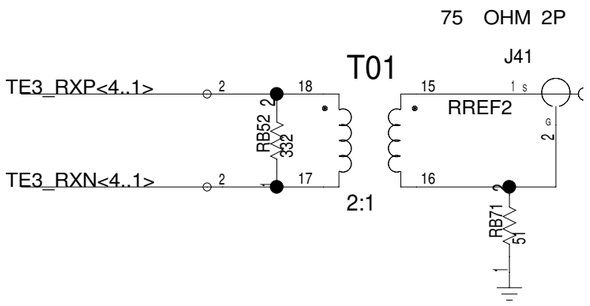
BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\

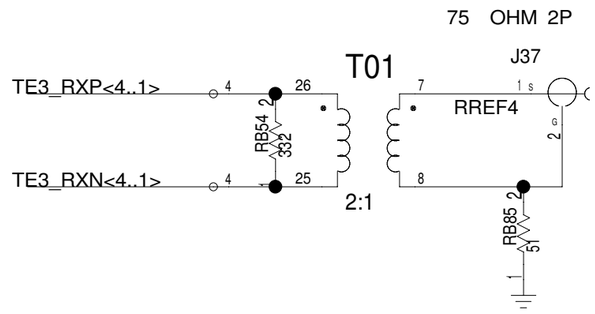


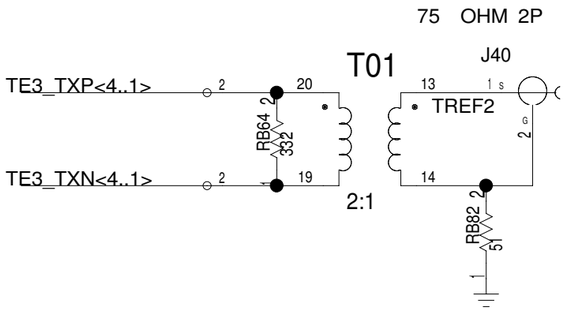


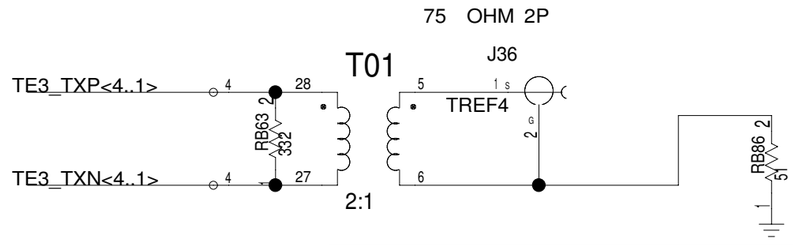






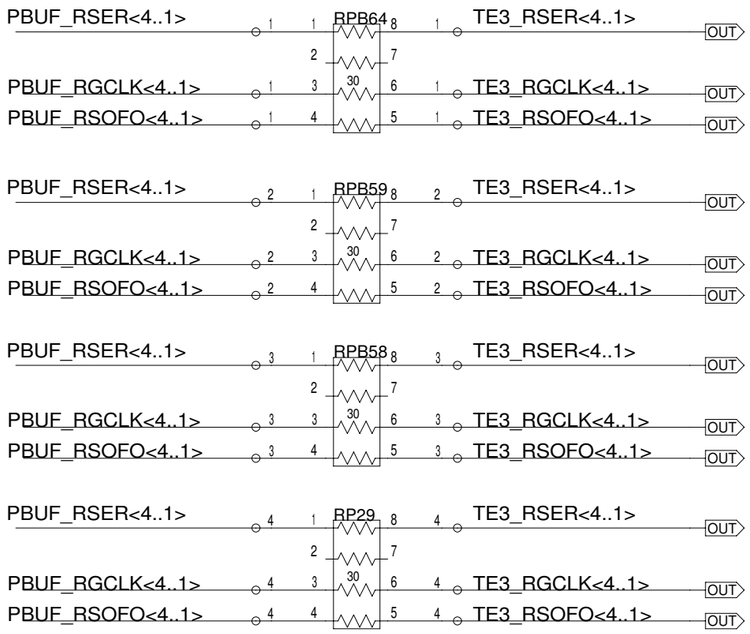


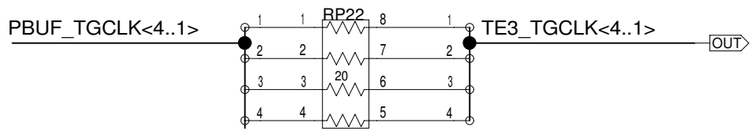


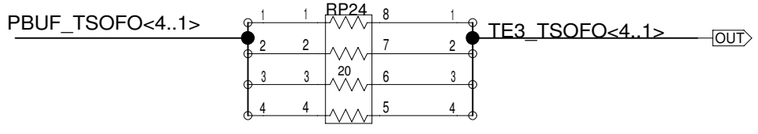


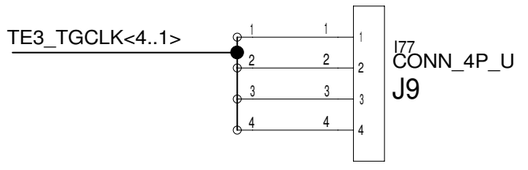
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/5(BLOCK) 60/76(TOTAL)

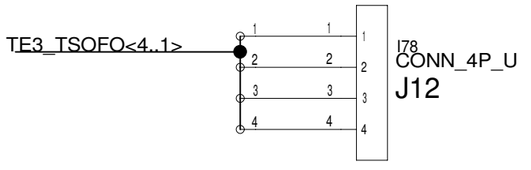
BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\









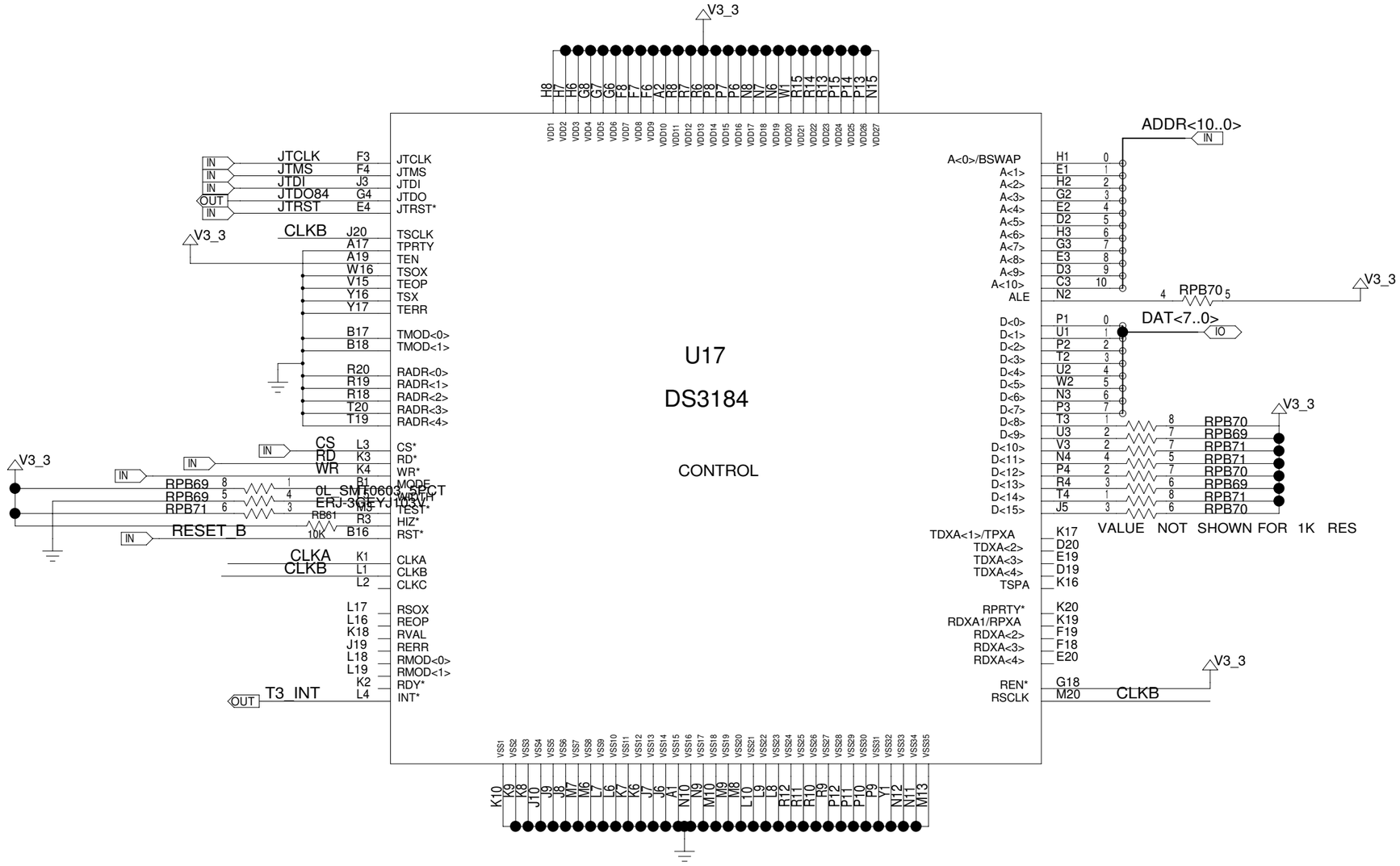


JUMPERS FOR GAPCLK AND SOFO
TO BE PLACED CLOSE TO
THE OTHER FOUR T3E3 PORTS
TO ALLOW CONNECTION WITH JUMPER

END OF DS3184 WAN HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 61/76(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\



BEGINNING OF DS3184 WAN HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/5(BLOCK) 62/76(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\

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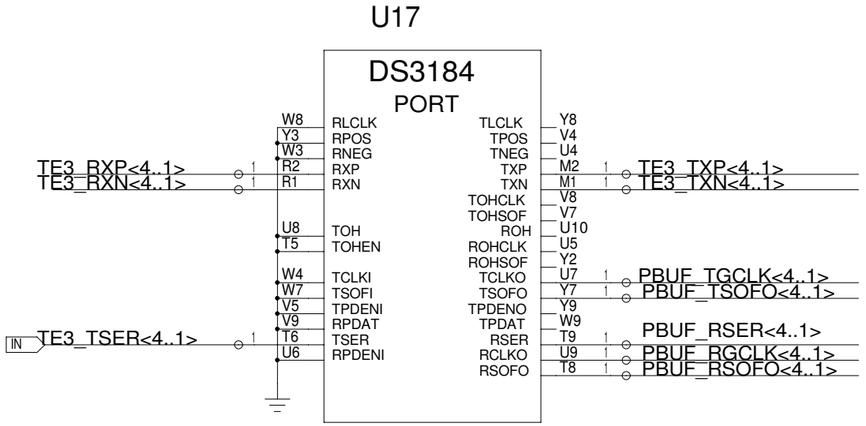
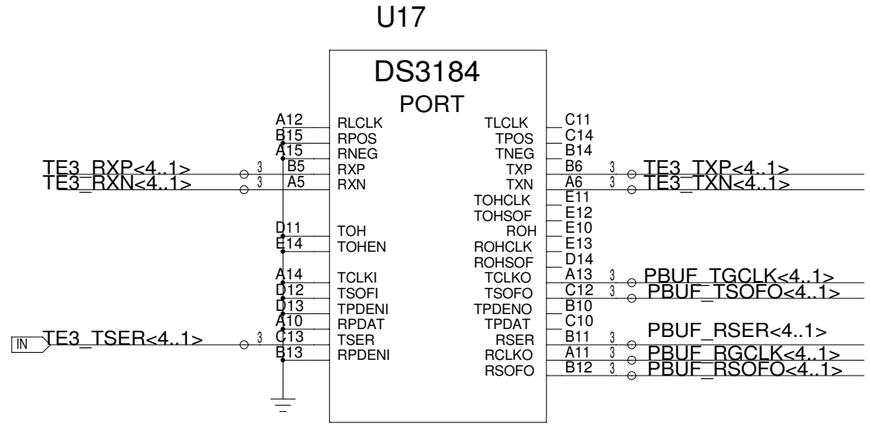
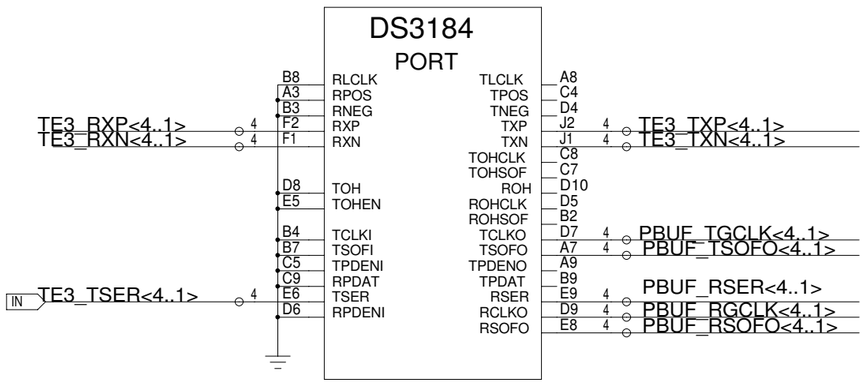
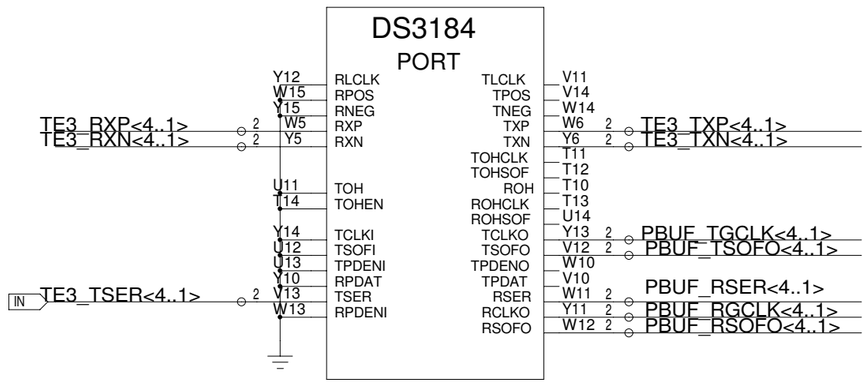






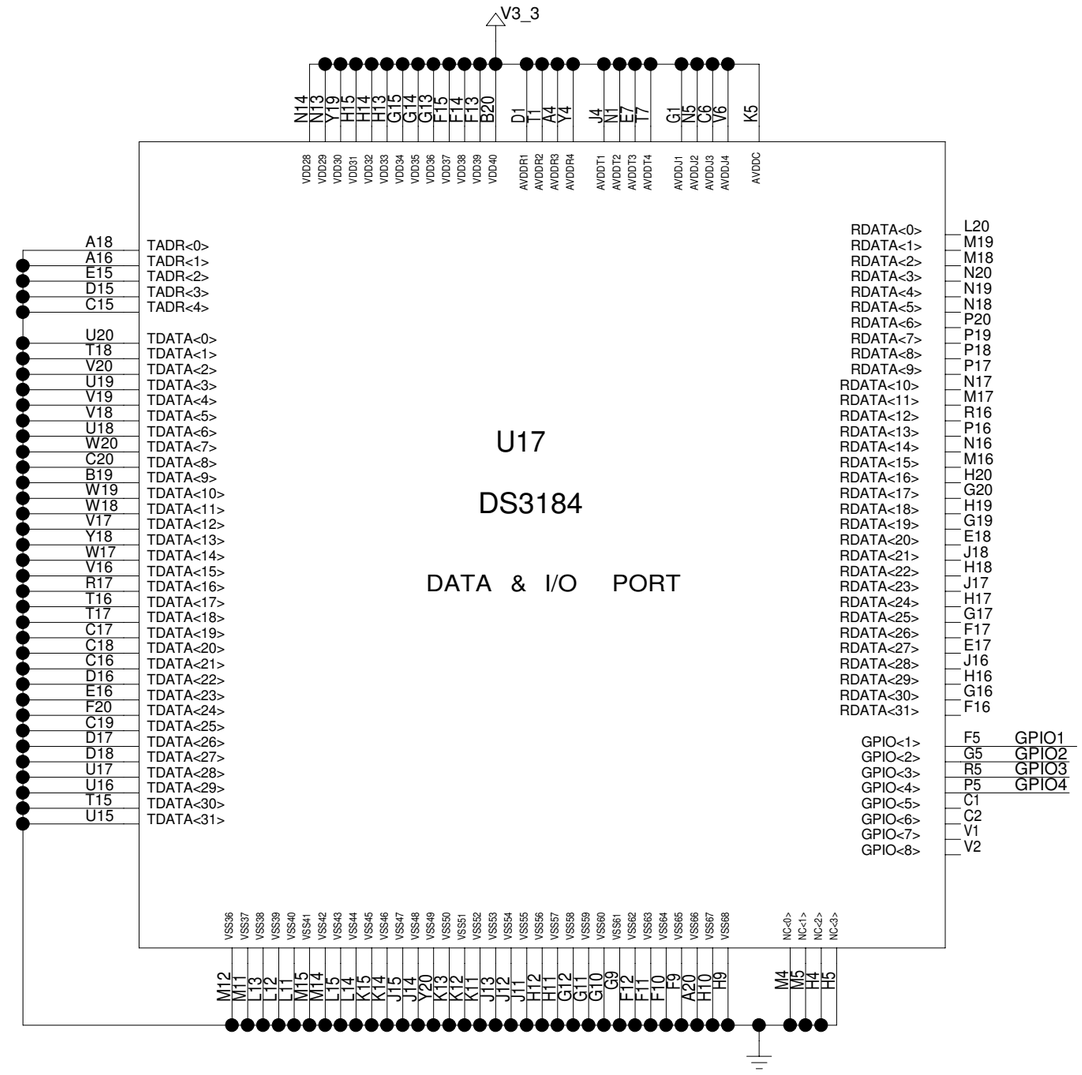


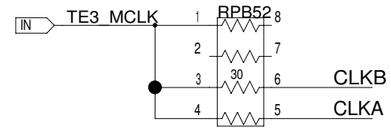
DS3184 PORT NUMBERS DO NOT MATCH DS33X162 PORT NUMBERS
PORT MAPPING IS AS FOLLOWS:
DS33X162_PORT: 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8
DS3184 PORT: 2A, 4A, 3A, 1A, 2B, 4B, 3B, 1B
ALL PCB SILKSCREEN CORRESPONDS TO THE DS33X162 PORT NUMBER
THIS MAP IS ONLY NEEDED FOR DS3184 REGISTER ACCESS

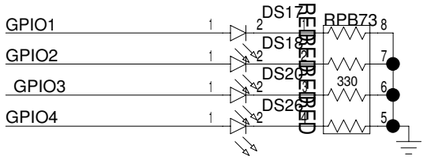
DS3184 PORT#/RCLK_PIN#
PORT1=PINB8
PORT3=PINA12
PORT2=PINW8
PORT4=PINY12

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/5(BLOCK) 63/76(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\



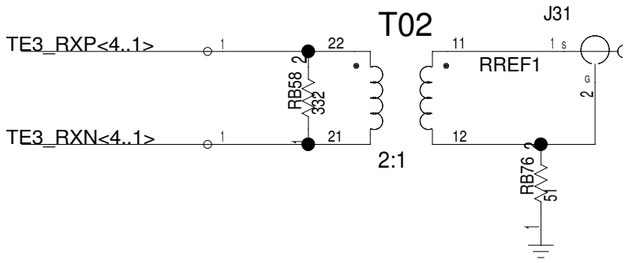




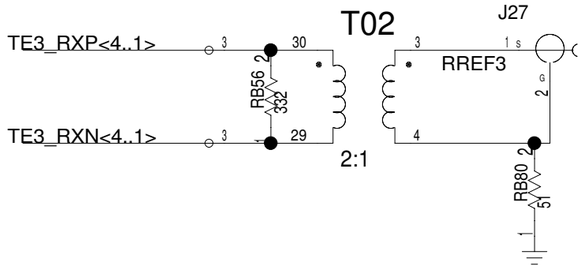
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 64/76(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\

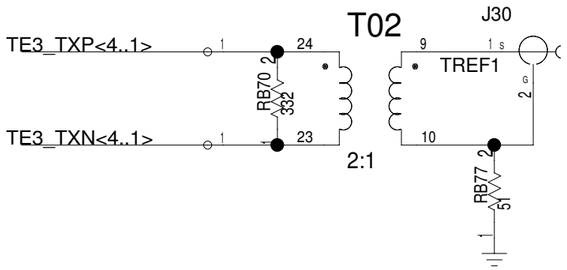
75 OHM 2P



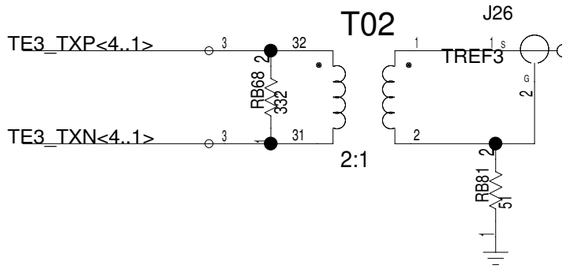
75 OHM 2P



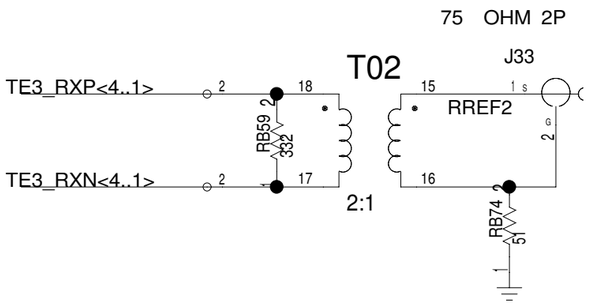
75 OHM 2P



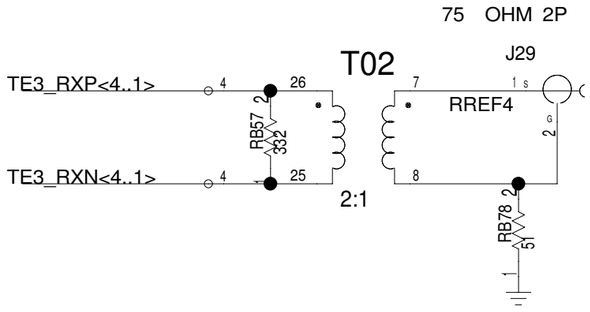
75 OHM 2P



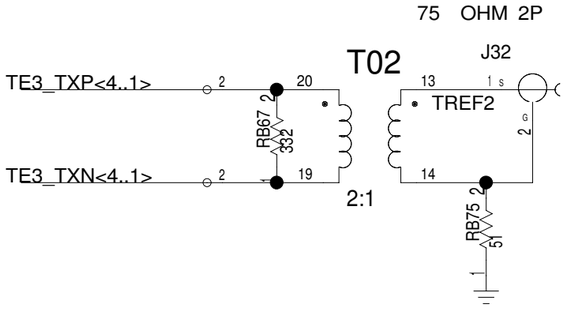
75 OHM 2P



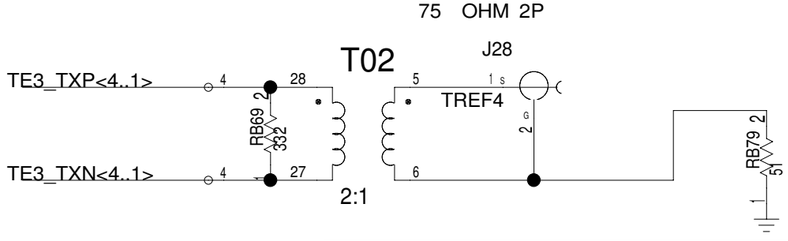
75 OHM 2P



75 OHM 2P

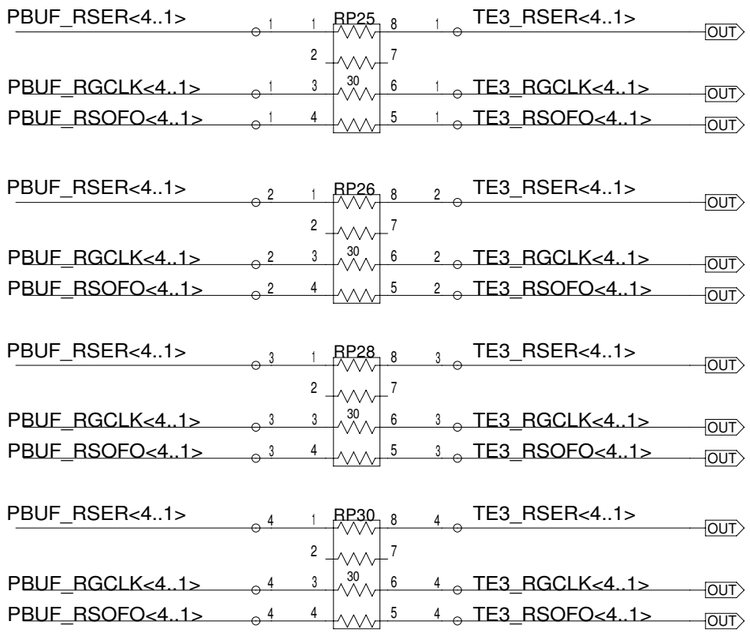


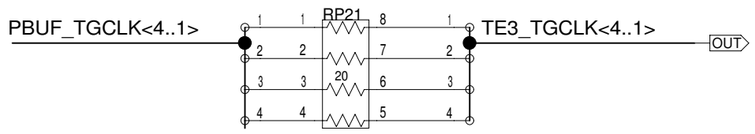
75 OHM 2P

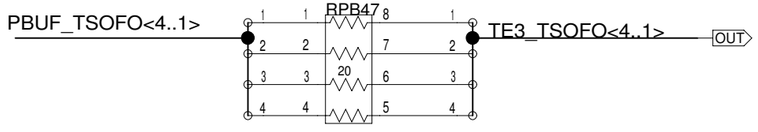


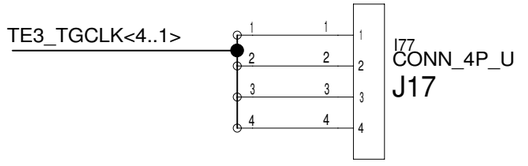
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/5(BLOCK) 65/76(TOTAL)

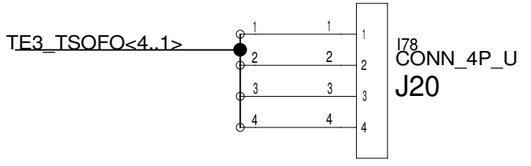
BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\









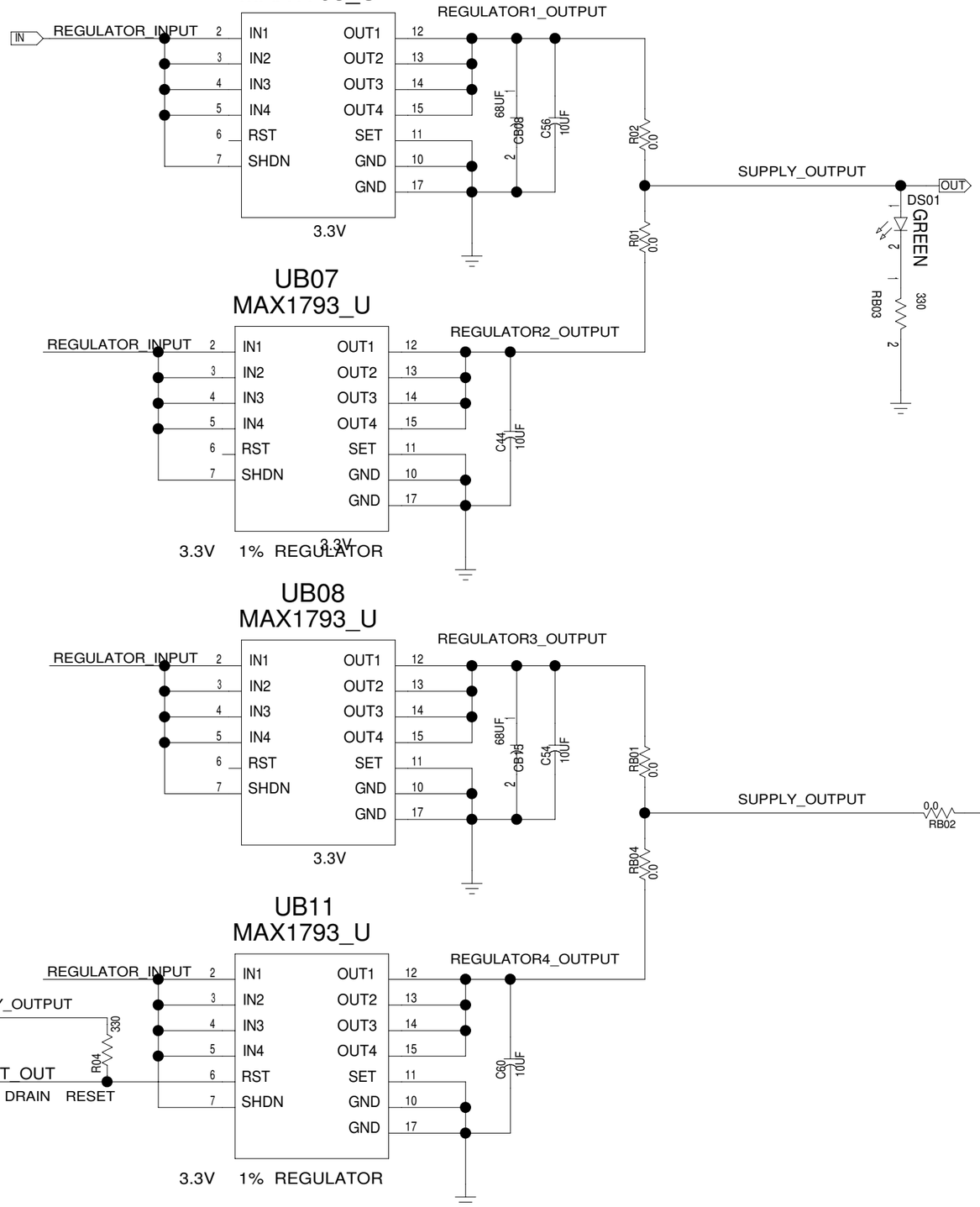


JUMPERS FOR GAPCLK AND SOFO
TO BE PLACED CLOSE TO
THE OTHER FOUR T3E3 PORTS
TO ALLOW CONNECTION WITH JUMPER

END OF DS3184 WAN HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 66/76(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _ds33x162dk_dn\



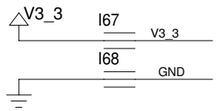
TRACES BETWEEN REGULATOR OUTPUT AND V3.3 SHOULD
BE LONG ENOUGH TO BUILD 0.06 OHM OF RESISTANCE
TO ENSURE LOAD SHARING BETWEEN THE 3.3V 1% REGULATORS
TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

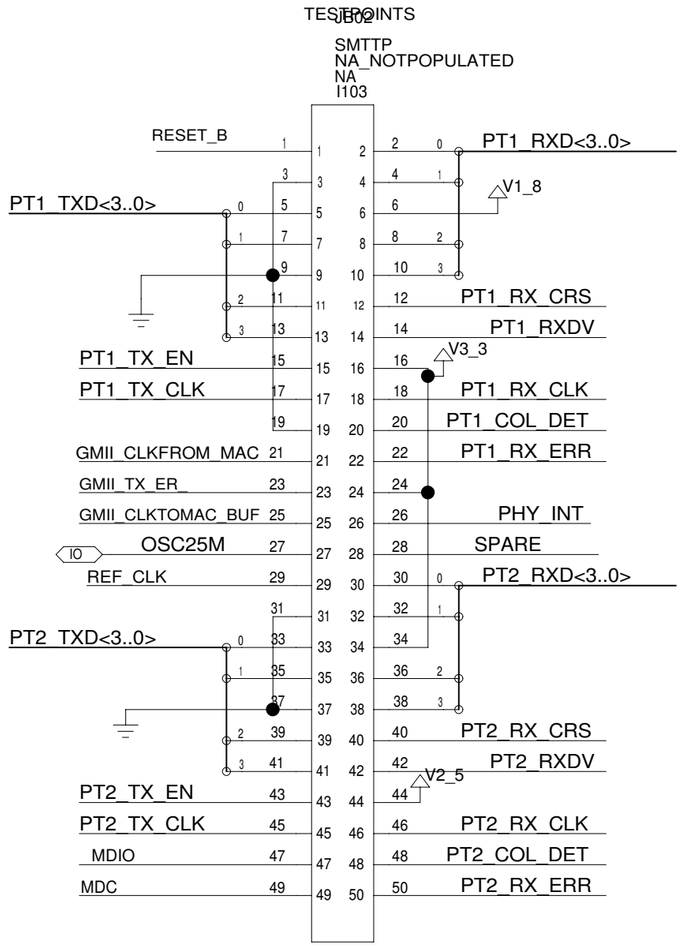
5V DC POWER SUPPLY
REVERSE BIAS PROTECTION

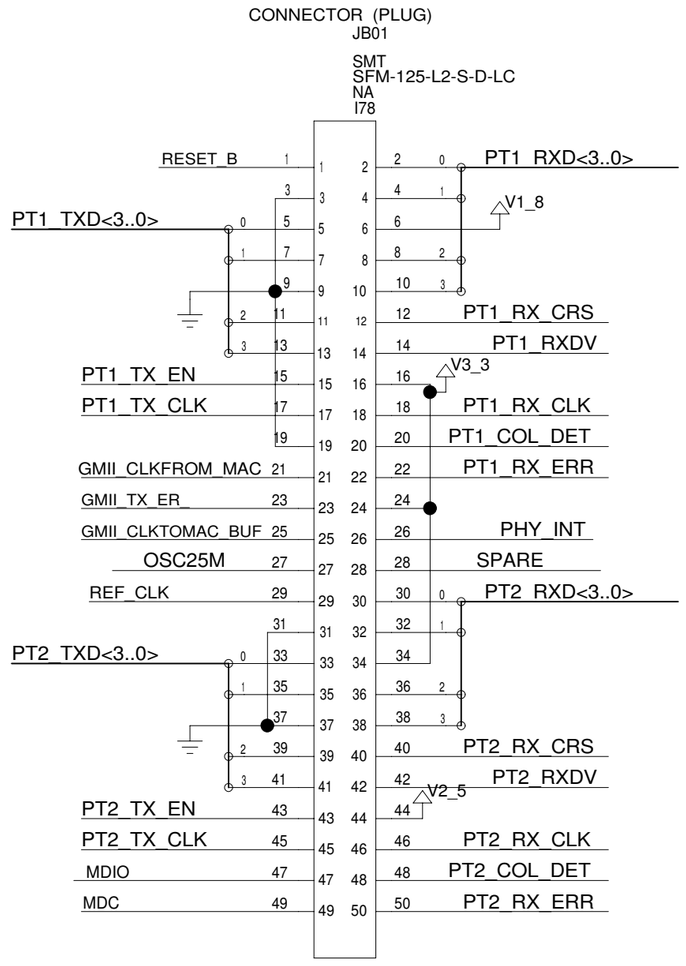
BEGINNING / END OF PHY
POWER SUPPLY HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 67/76(TOTAL)

BLOCK NAME: power_supply_4amp_dn. PARENT BLOCK: _ds33x162dk_dn\







PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

REF_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

SPARE IO

GMII_CLKFROM_MAC IO
GMII_TX_ER_ IO
GMII_CLKTOMAC_BUF IO

CONNECTORS FOR LAN MOTHERBOARD TO RESOURCE CARD

BEGINNING & END OF PHY CONNECTOR + TESTPOINT HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 68/76(TOTAL)

BLOCK NAME: _phy_imbus_mb_dn. PARENT BLOCK: _ds33x162dk_dn\

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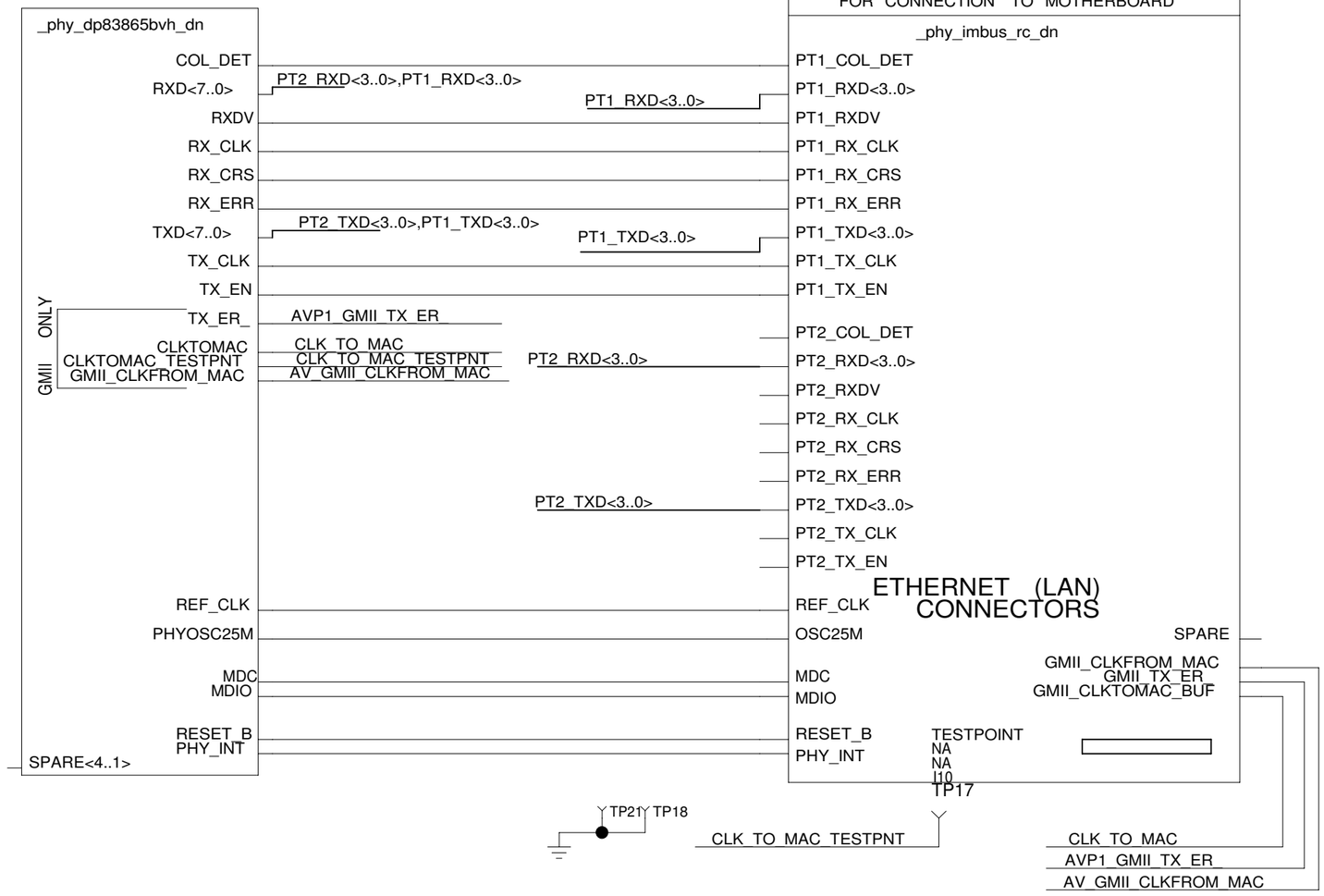
GIGABIT PHY CARD CONTENTS / INDEX



TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/3(BLOCK) 2/76(TOTAL)

BLOCK NAME: _rc_top_dn_. PARENT BLOCK: <CON_PARENT_NAME>

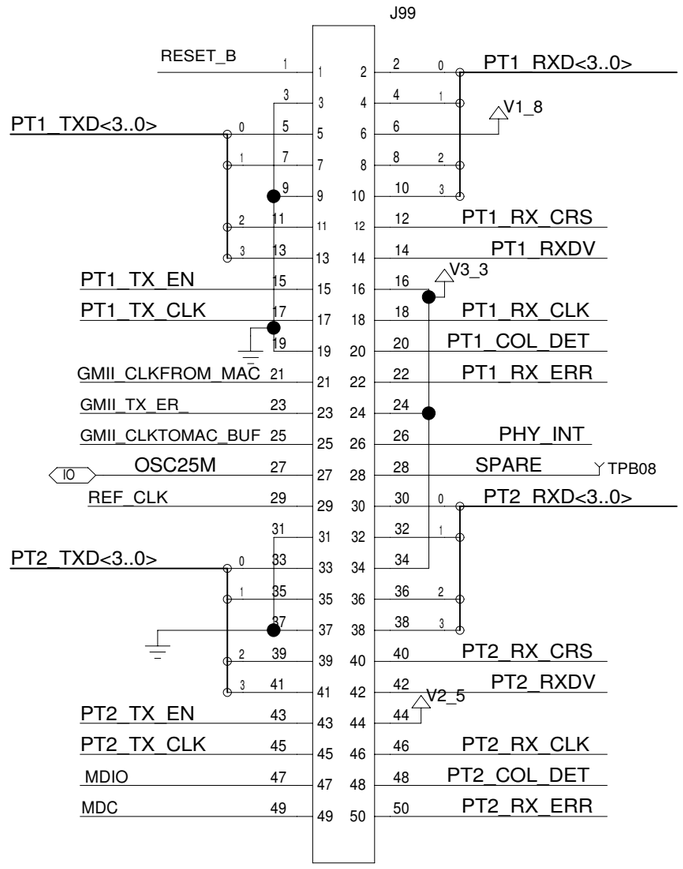
PRINTED Mon Feb 11 14:09:11 2008

V3_3

V3_3

GND

P2 CONNECTOR (RECEPTICAL)



RESOURCE CARD CONNECTOR FOR LAN TO MOTHERBOARD

PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

REF_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

SPARE IO

GMII_CLKFROM_MAC IO
GMII_TX_ER_ IO
GMII_CLKTOMAC_BUF IO

BEGINNING / END OF PHY CONNECTOR HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 69/76(TOTAL)

BLOCK NAME: _phy_imbus_rc_dn. PARENT BLOCK: _rc_top_dn_\

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<TXT_GIGABITPHYMOTHERBRDCONNECTOR>. SCHEMATIC ON <PGNM_GIGABITPHYMOTHERBRDCONNECTOR>

PLACE 9.76K RES CLOSE TO BG_REF

RESET_B — RB246 9.76K — BG_REF

V3_3 V1_8 V2_5 V1_8

33 RESET*
102 BG_REF
34 VDD_SEL_STRAP
90 IO_VDD<1..12>
92 CORE_VDD<1..8>
96 2V5_AVDD<1..2>
123 1V8_AVDD1_<1..5>
98 1V8_AVDD2
100 1V8_AVDD3

RB249 2.0K

RP89 30

32 TRST*
31 TDI
28 TDO
27 TMS
24 TCK

RX_CRS_BUF 40 CRS/RGMII_SEL1
COL_DET_BUF 39 COL
TX_CLK_BUF 60 TX_CLK/RGMII_SEL0

TXD<7..0>
76 TXD<0>/TX0
75 TXD<1>/TX1
72 TXD<2>/TX2
71 TXD<3>/TX3
68 TXD<4>
67 TXD<5>
66 TXD<6>
65 TXD<7>

TX_EN 62 TX_EN/TXEN_ER
GMII_CLKFROM_MAC 79 GTX_CLK/TCK
TX_ER 61 TX_ER
RX_CLK_BUF 57 RX_CLK

RXD<7..0>
RP92 30
56 RXD<0>/RX0
55 RXD<1>/RX1
52 RXD<2>/RX2
51 RXD<3>/RX3
RP91 30
50 RXD<4>
47 RXD<5>
46 RXD<6>
45 RXD<7>

RX_ERR_BUF 41 RX_ER/RXDV_ER
RXDV_BUF 44 RX_DV/RCK

U33
DP83865_U

OUTPUT
COL PIN39
CRS PIN40
RXER PIN41
RXDV PIN44
RXD[0:7] [PIN56:PIN45]
RXCLK PIN57
TXCLK PIN60
CLKTOMAC PIN85
CLKOUT PIN87

INPUT
TXERR PIN61
TXEN PIN62
TXD[0:7] [PIN76:PIN65]
GTXCLK PIN79
MDC PIN81
CLKIN PIN86

MDC 81 MDC
MDIO 80 MDIO
INTERRUPT* 3 PHY_INT
MDIA_P 108 MDIA_P1
MDIA_N 109 MDIA_N2
MDIB_P 114 MDIB_P3
MDIB_N 115 MDIB_N4
MDIC_P 120 MDIC_P1
MDIC_N 121 MDIC_N2
MDID_P 126 MDID_P3
MDID_N 127 MDID_N4
CLK_IN 86 PHYOSC25M
CLK_OUT 87 CLKOUT_BUF
CLK_TO_MAC 85 CLKTOMAC_BUF
NON_IEEE_STRAP 1 NON_IEEE_STRAP
MAN_MDIX_STRAP/TX_TCLK 6 MAN_MDIX_STRAP__TX_TCLK
ACTIVITY_LED/SPEED0_STRAP 7 ACTIVITYLED_SPEED0
LINK10_LED/SPEED1_STRAP 8 LINK10LED_SPEED1
LINK100_LED/DUPLEX_STRAP 9 LINK100LED_DUPLEX
LINK1000_LED/AN_EN_STRAP 10 LINK1000LED_ANEN
DUPLEX_LED/PHYADDR<0>_STRAP 13 A0_DUPLEX
PHYADDR<1>_STRAP 14
PHYADDR<2>_STRAP 17
PHYADDR<3>_STRAP 18
PHYADDR<4>_STRAP 95
MULTI_EN_STRAP/TX_TRIGGER 94 MULTI_EN_STRAP__TX_TRIGGER
MDIX_EN_STRAP 89 MDIX_EN_STRAP
MAC_CLK_EN_STRAP/TX_SYN_CLK 88 MAC_CLK_EN_STRAP__TX_SYN_CLK

RPB144 RPB145 50
PLACE MDI RESISTORS CLOSE TO PHY
V2_5
MAINTAIN 50OHM STIPLINE TO V2_5PHY

RPB149 1K

VSS<1..35>
128

PHYOSC25M IN
REF_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO
SPARE<4..1> IO

GMII_CLKFROM_MAC IO
TX_ER IO
CLKTOMAC_TESTPNT IO
CLKTOMAC IO
TXD<7..0> IO
TX_EN IO
TX_CLK IO
RX_CLK IO
COL_DET IO
RX_ERR IO
RX_CRS IO
RXDV IO
RXD<7..0> IO

RP94 30
RX_CLK_BUF — RX_CLK
TX_CLK_BUF — TX_CLK

CLKTOMAC_BUF — RP88 30 — CLKTOMAC, CLKTOMAC_TESTPNT
CLKOUT_BUF — TPB09 — CLKOUT
COL_DET_BUF — RP93 30 — COL_DET
RX_CRS_BUF — RX_CRS
RX_ERR_BUF — RX_ER
RXDV_BUF — RXDV

V3_3 — V3_3 — GND

TX_ER — RP90 1K

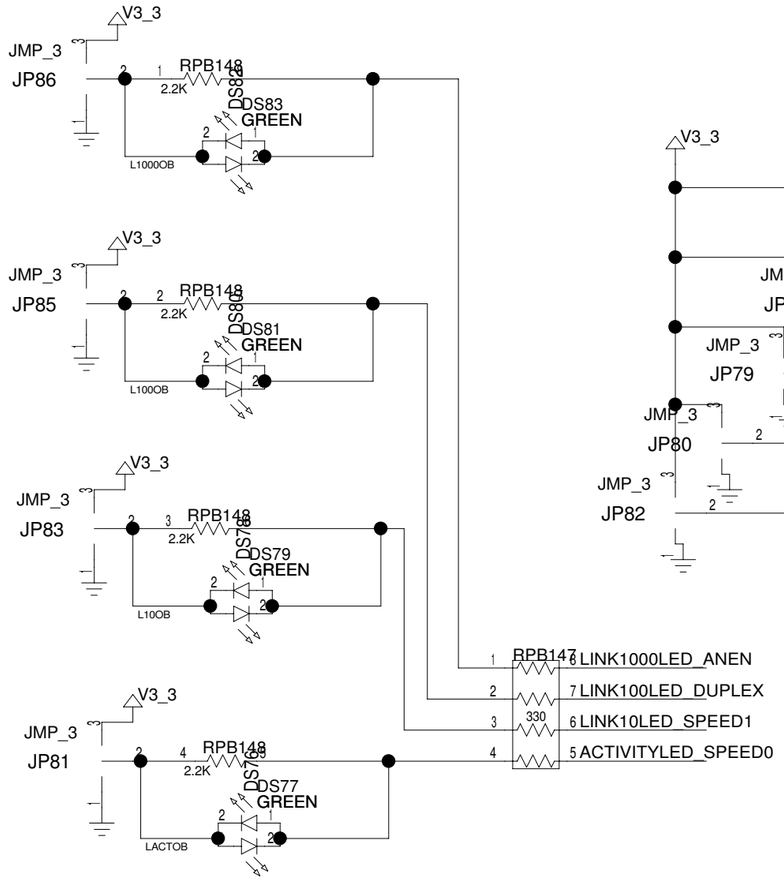
RB247 330 — DS75 GREEN — RB248 2.0K — A0_DUPLEX — V3_3

BEGINNING OF GIGABIT PHY HIERARCHY BLOCK

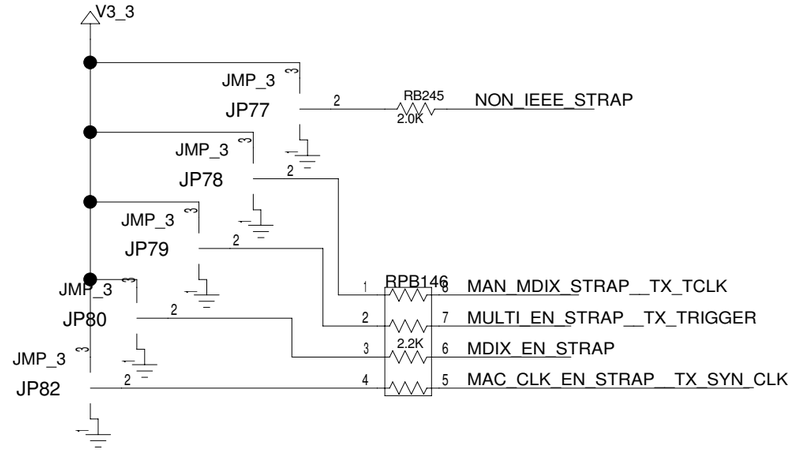
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 70/76(TOTAL)

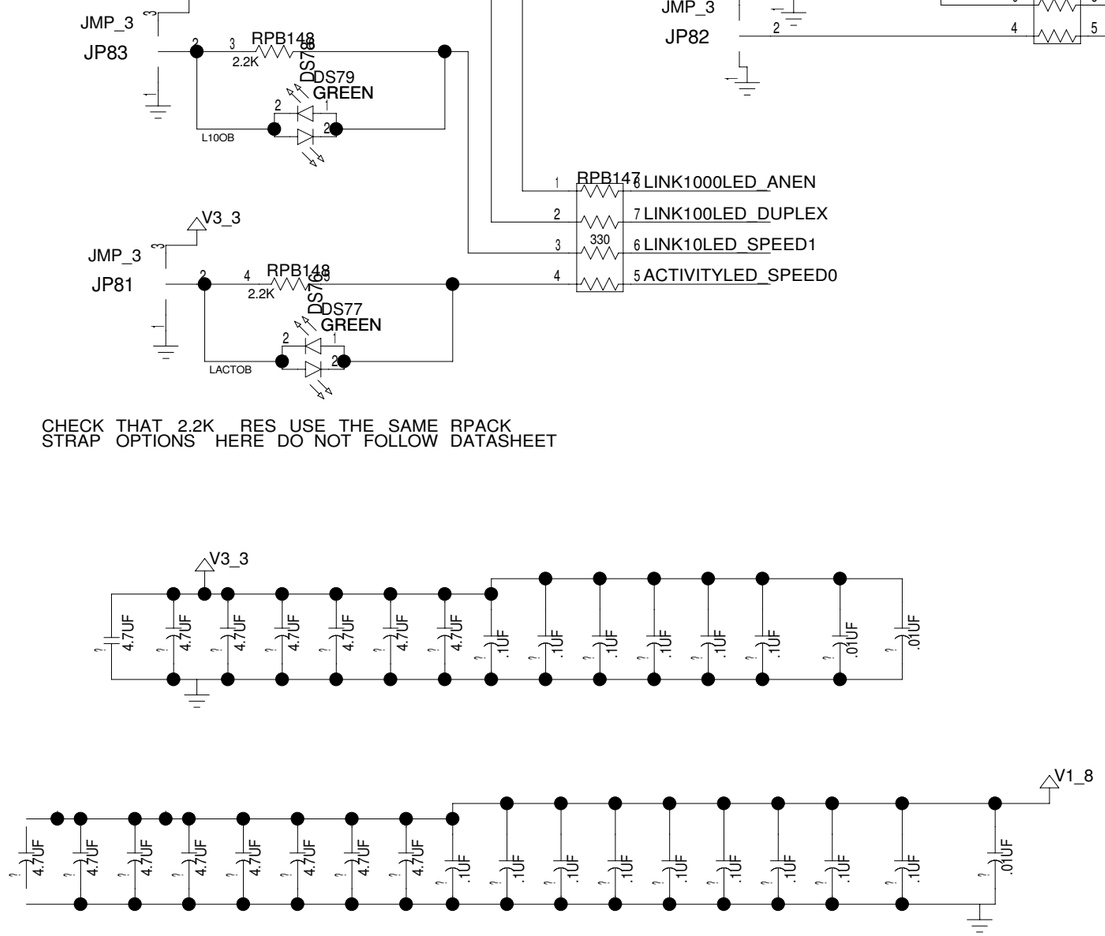
BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _rc_top_dn_\

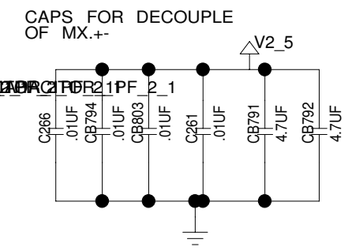
PRINTED Mon Feb 11 13:39:44 2008

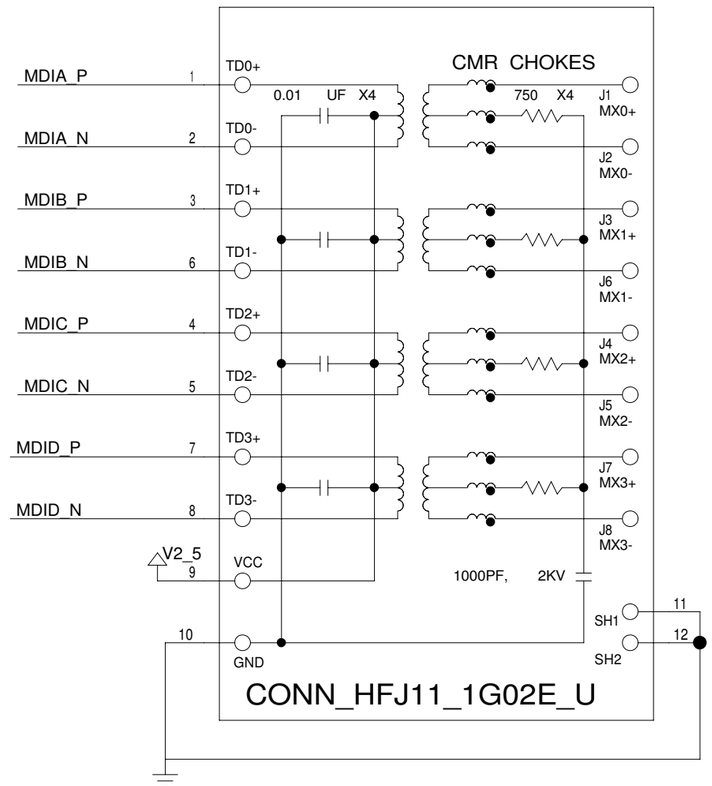


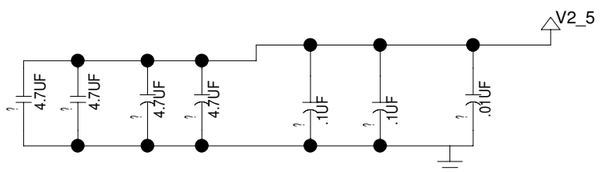
CHECK THAT 2.2K RES USE THE SAME RPACK
STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET







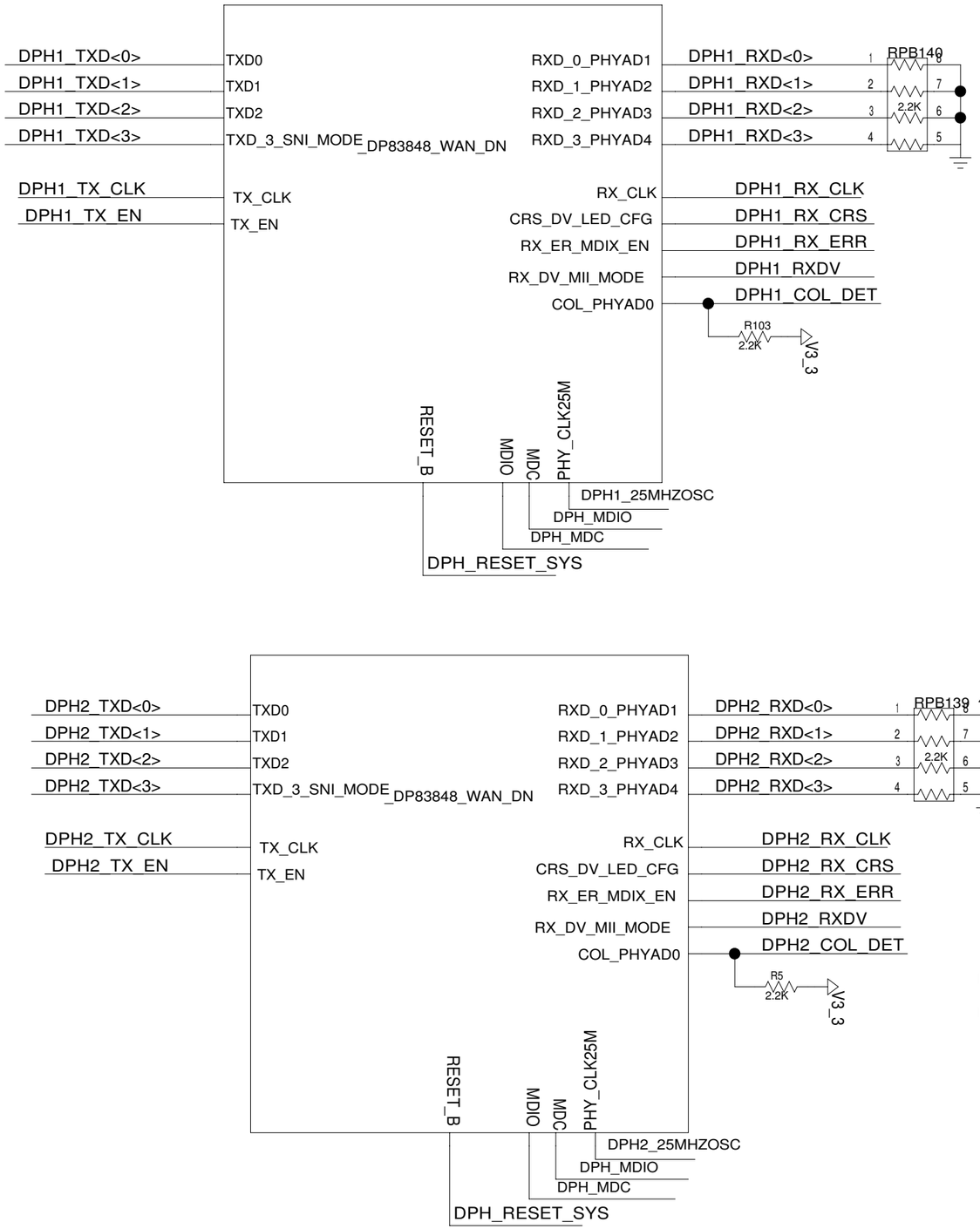


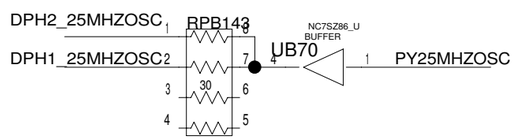


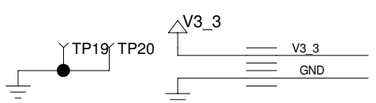
END OF GIGABIT PHY HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 71/76(TOTAL)

DUAL PHY CARD CONTENTS / INDEX







SINGLE 50 PIN
I.M. CARD RECEPTICAL-CONNECTORS
USED ON TOP OF ETHERNET CARD
FOR CONNECTION TO MOTHERBOARD

_phy_imbus_rc_dn

DPH1_COL_DET	PT1_COL_DET
DPH1_RXD<3..0>	PT1_RXD<3..0>
DPH1_RXDV	PT1_RXDV
DPH1_RX_CLK	PT1_RX_CLK
DPH1_RX_CRS	PT1_RX_CRS
DPH1_RX_ERR	PT1_RX_ERR
DPH1_TXD<3..0>	PT1_TXD<3..0>
DPH1_TX_CLK	PT1_TX_CLK
DPH1_TX_EN	PT1_TX_EN
DPH2_COL_DET	PT2_COL_DET
DPH2_RXD<3..0>	PT2_RXD<3..0>
DPH2_RXDV	PT2_RXDV
DPH2_RX_CLK	PT2_RX_CLK
DPH2_RX_CRS	PT2_RX_CRS
DPH2_RX_ERR	PT2_RX_ERR
DPH2_TXD<3..0>	PT2_TXD<3..0>
DPH2_TX_CLK	PT2_TX_CLK
DPH2_TX_EN	PT2_TX_EN
DPH_REF_CLK	REF_CLK
PY25MHZOSC	OSC25M
DPH_MDC	MDC
DPH_MDIO	MDIO
DPH_RESET_SYS	RESET_B
DPH_PHY_INT	PHY_INT

ETHERNET (LAN)
CONNECTORS

SPARE

GMII_CLKFROM_MAC
GMII_TX_ER
GMII_CLKTOMAC_BUF

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/3(BLOCK) 3/76(TOTAL)

V3_3

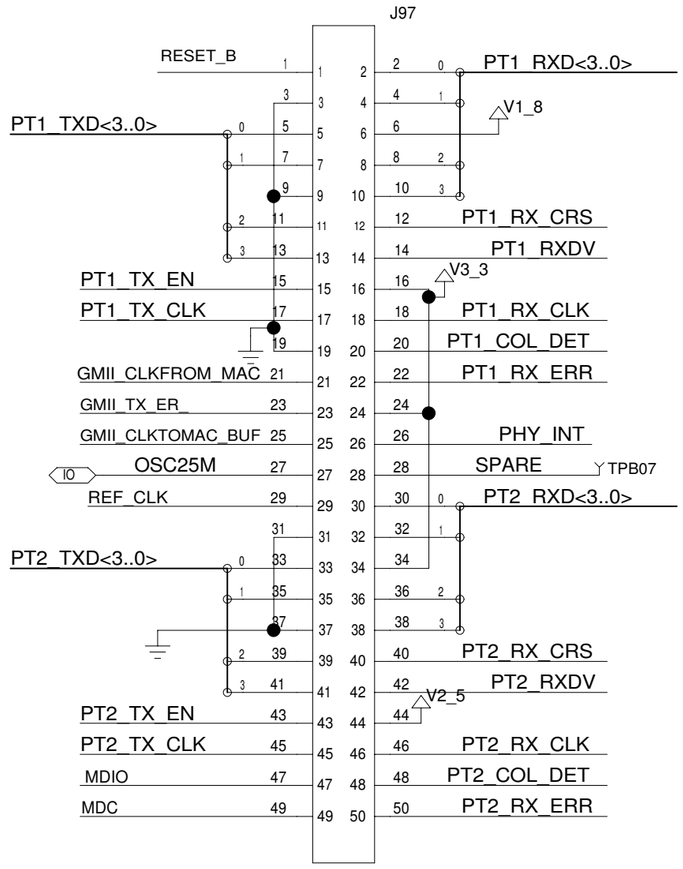
V3_3

GND

PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

P2 CONNECTOR (RECEPTICAL)



RESOURCE CARD CONNECTOR FOR LAN TO MOTHERBOARD

REF_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

SPARE IO

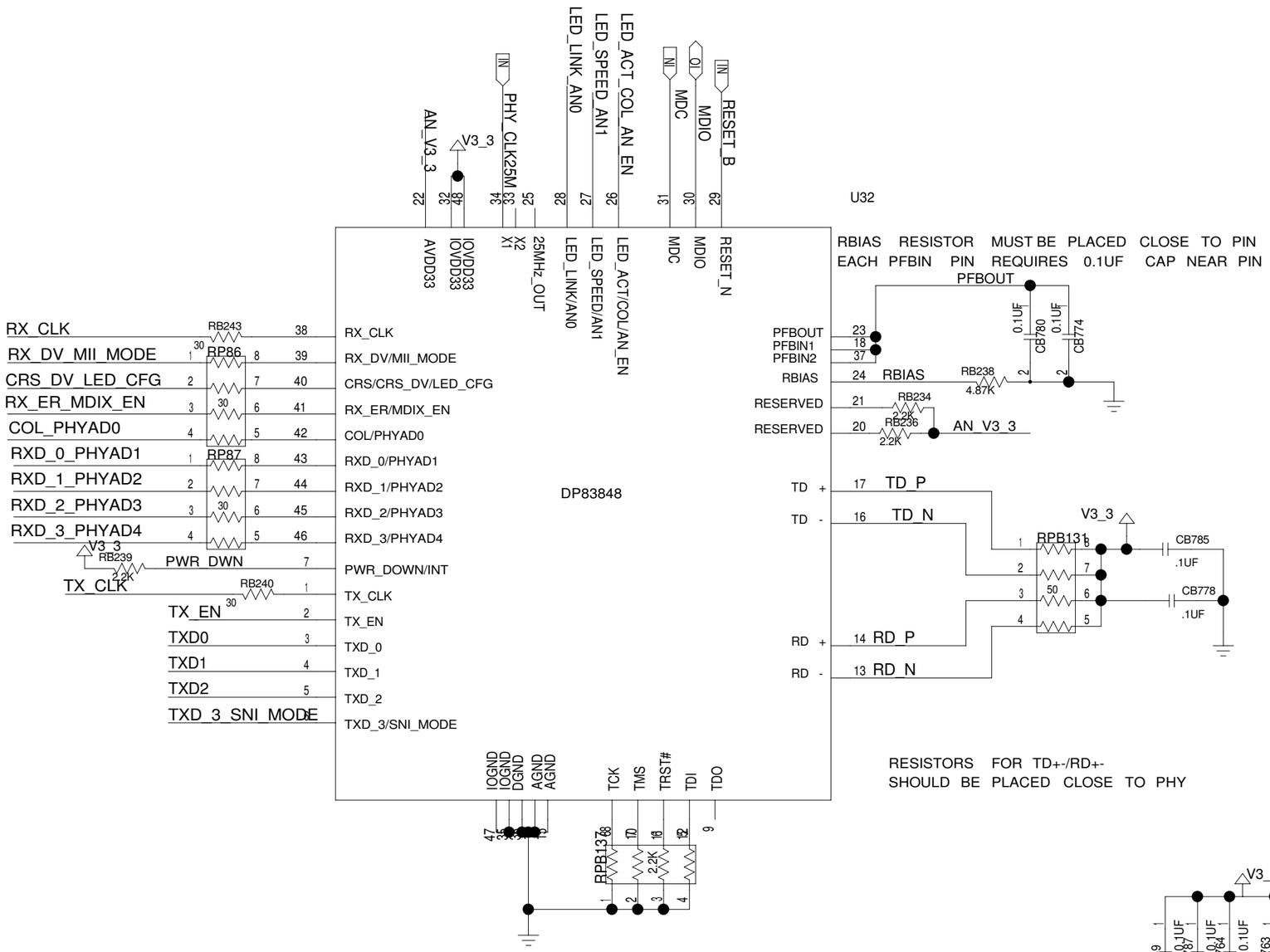
GMII_CLKFROM_MAC IO
GMII_TX_ER_ IO
GMII_CLKTOMAC_BUF IO

BEGINNING / END OF PHY CONNECTOR HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 72/76(TOTAL)

BLOCK NAME: _phy_imbus_rc_dn. PARENT BLOCK: _rc_top_dn_\

PRINTED Mon Feb 11 13:59:49 2008

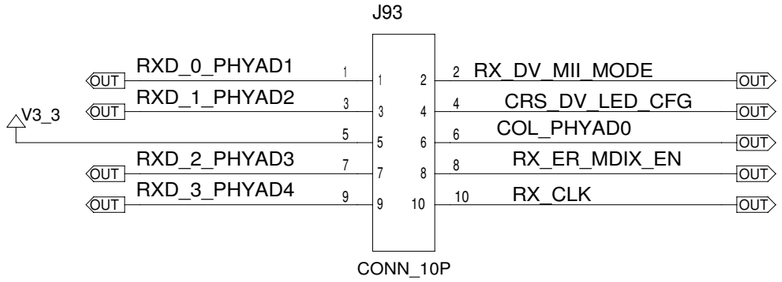


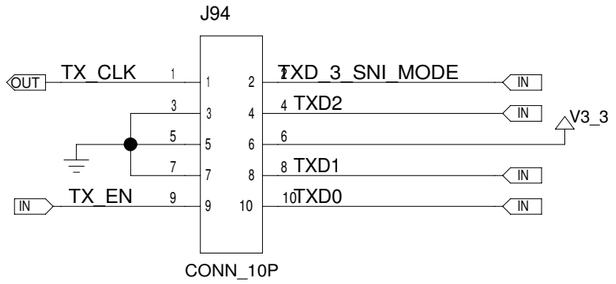
PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW 0.2 BETWEEN CONNECTORS.

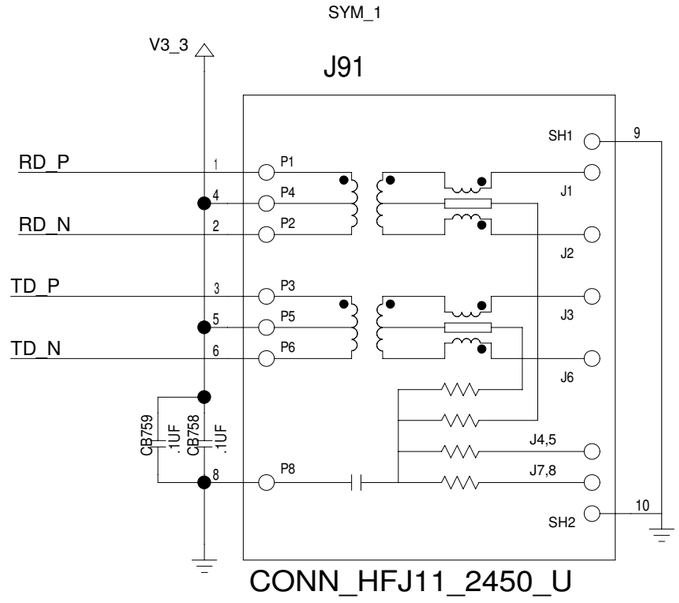
ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

BEGINNING OF PHY HIERARCHY BLOCK

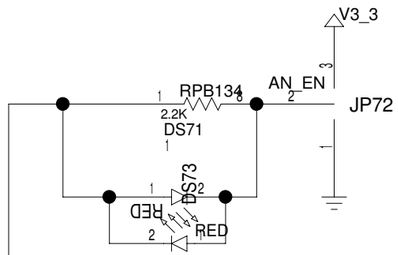
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 73/76(TOTAL)

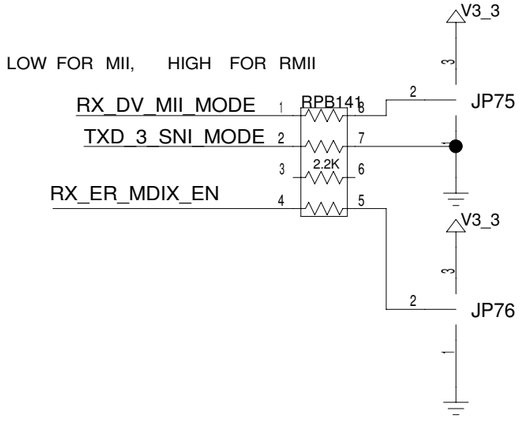






CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM





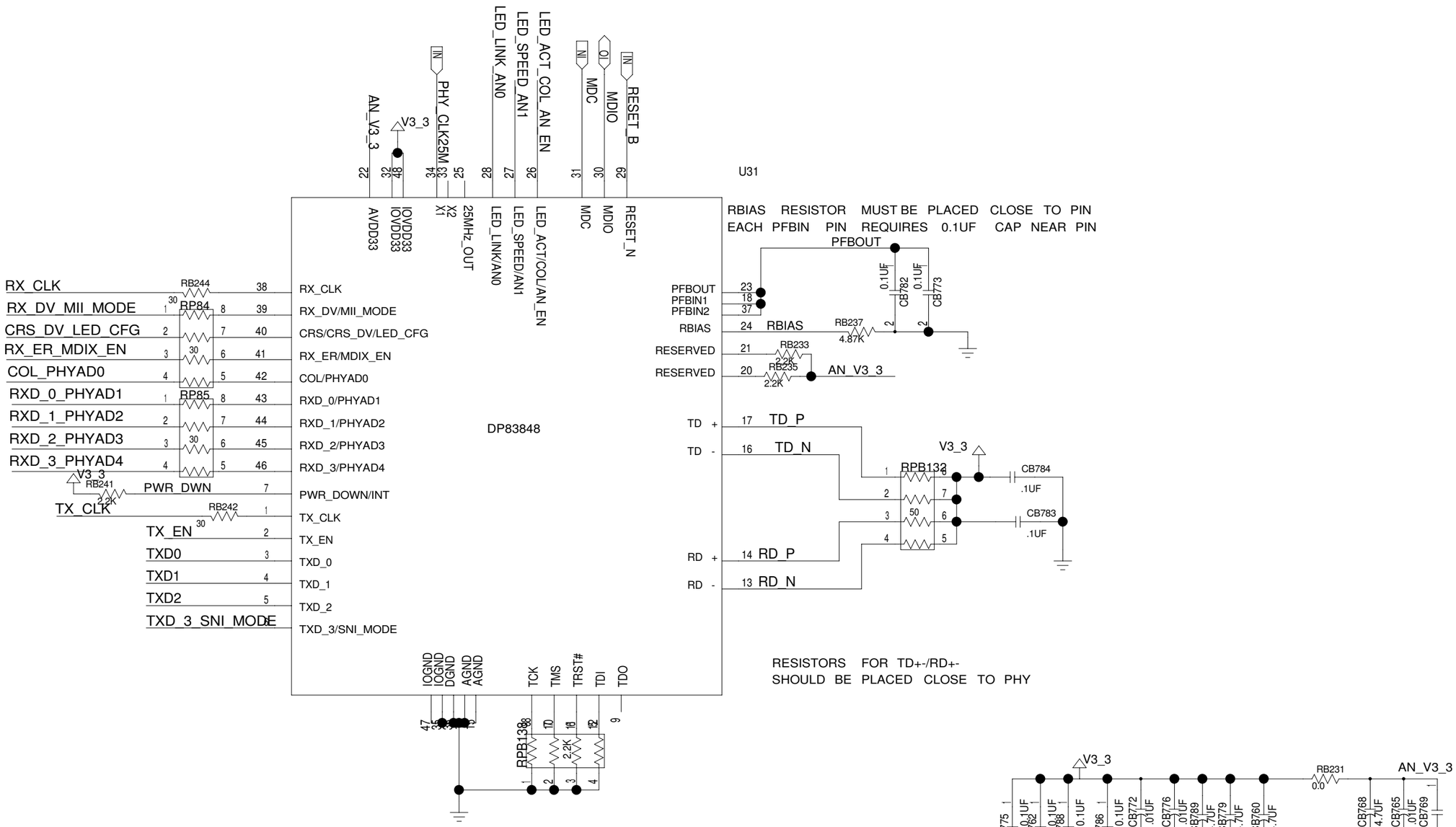
STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET

ENSURE THAT SAME RPACK
IS USED FOR LED

END OF PHY HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 74/76(TOTAL)

BLOCK NAME: _dp83848_wan_dn. PARENT BLOCK: _rc_top_dn_\

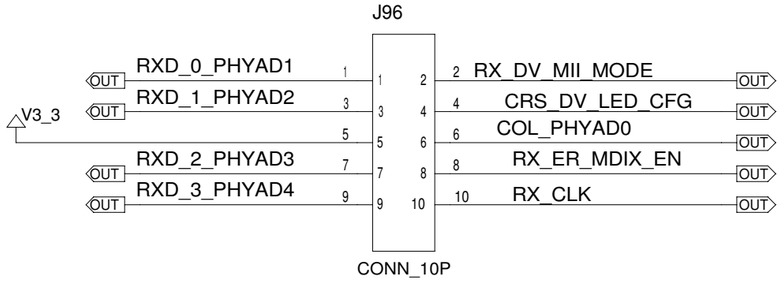


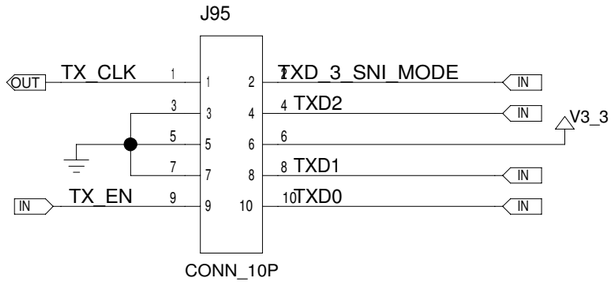
PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW 0.2 BETWEEN CONNECTORS.

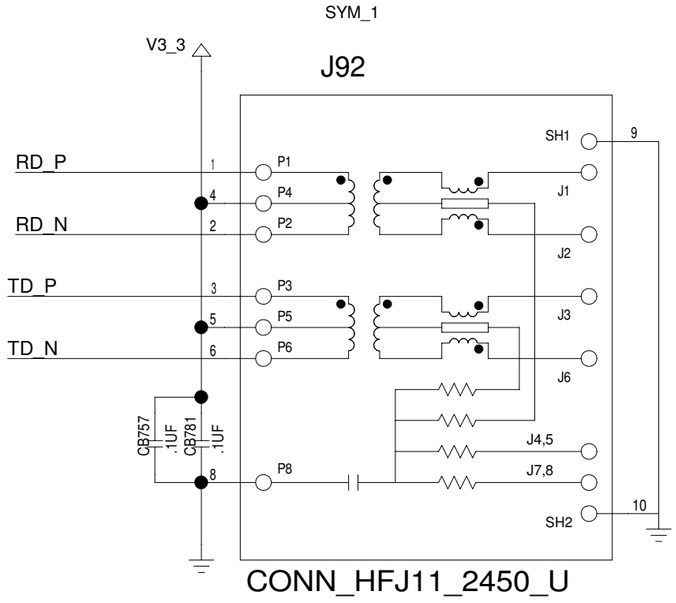
ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

BEGINNING OF PHY HIERARCHY BLOCK

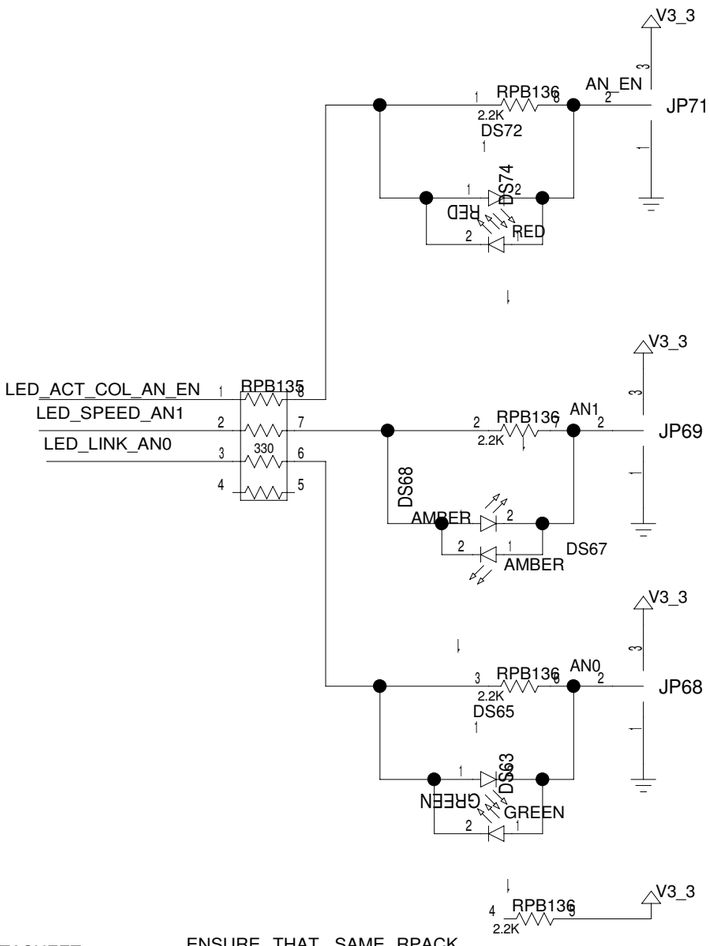
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 75/76(TOTAL)







CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM



STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET

ENSURE THAT SAME RPACK
IS USED FOR LED

END OF PHY HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 76/76(TOTAL)

BLOCK NAME: _dp83848_wan_dn. PARENT BLOCK: _rc_top_dn_\