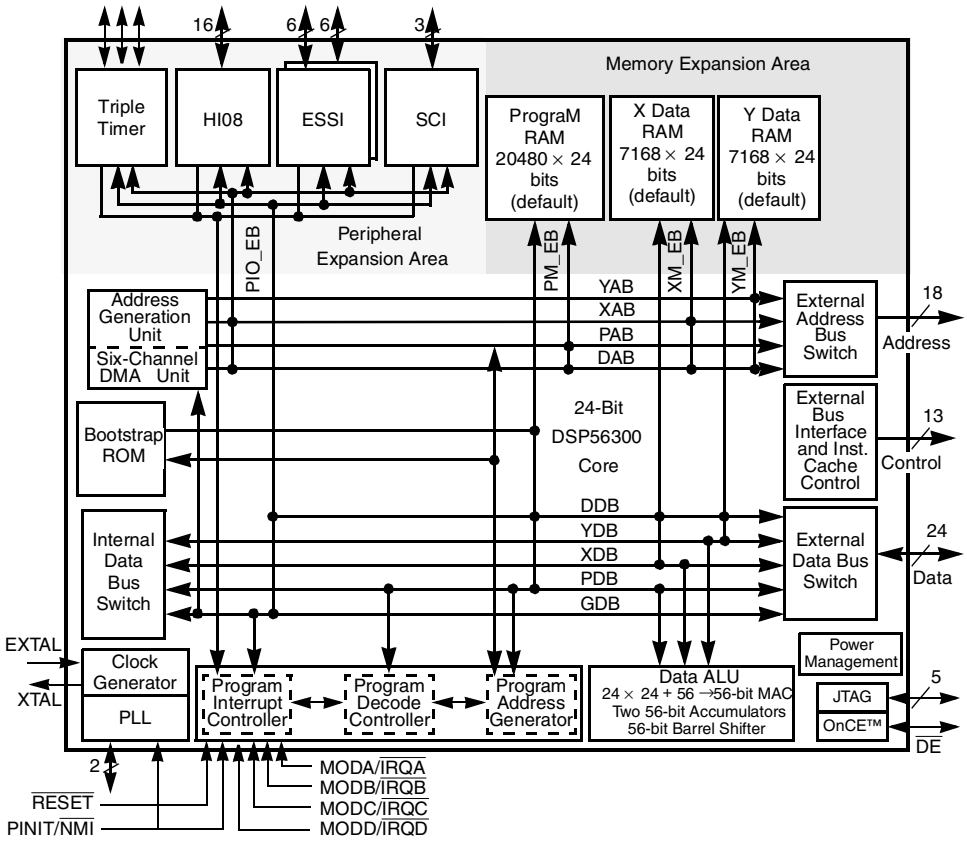
# DSP56309

## 24-Bit Digital Signal Processor




*The DSP56309 is intended for applications benefiting from a large amount of internal memory, such as wireless infrastructure applications.*

**Figure 1.** DSP56309 Block Diagram

The DSP56309 is a member of the DSP56300 core family of programmable CMOS DSPs. The DSP56300 core includes a barrel shifter, 24-bit addressing, an instruction cache, and direct memory access (DMA). The DSP56309 offers 100 million multiply-accumulates per second (MMACS) at 3.0–3.6 V using an internal 100 MHz clock. The large internal memory is ideal for wireless infrastructure and wireless local-loop applications. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low-power dissipation, thus enabling a new generation of wireless, multimedia, and telecommunications products.

**Note**: This document contains information on a new product. Specifications and information herein are subject to change without notice.

# Features

**Table 1** lists the features of the DSP56309 device.

**Table 1.** DSP56309 Features

| Feature | Description |
|---|---|
| **High-Performance DSP56300 Core** | • 100 million multiply-accumulates per second (MMACS) with a 100 MHz clock at 3.3 V nominal<br>• Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control<br>• Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts<br>• Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two- and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals<br>• Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination<br>• Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP) |
| **Internal Peripherals** | • Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs<br>• Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)<br>• Serial communications interface (SCI) with baud rate generator<br>• Triple timer module<br>• Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled |
| **Internal Memories** | • 192 × 24-bit bootstrap ROM<br>• 8 K × 24-bit RAM total<br>• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:<br>**Program RAM Size** / **Instruction Cache Size** / **X Data RAM Size** / **Y Data RAM Size** / **Instruction Cache** / **Switch Mode**<br>20480 × 24 bits / 0 / 7168 × 24 bits / 7168 × 24 bits / disabled / disabled<br>19456 × 24 bits / 1024 × 24-bit / 7168 × 24 bits / 7168 × 24 bits / enabled / disabled<br>24576 × 24 bits / 0 / 5120 × 24 bits / 5120 × 24 bits / disabled / enabled<br>23552 × 24 bits / 1024 × 24-bit / 5120 × 24 bits / 5120 × 24 bits / enabled / enabled |
| **External Memory Expansion** | • Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines<br>• Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines<br>• External memory expansion port<br>• Chip select logic for glueless interface to static random access memory (SRAMs)<br>• Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs) |
| **Power Dissipation** | • Very low-power CMOS design<br>• Wait and Stop low-power standby modes<br>• Fully static design specified to operate down to 0 Hz (dc)<br>• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent) |
| **Packaging** | • 144-pin TQFP package in lead-free or lead-bearing versions<br>• 196-pin molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions |

# Target Applications

The DSP56309 is intended for applications benefiting from a large amount of internal memory, such as wireless infrastructure applications.

# Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56309 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

**Table 2.** DSP56309 Documentation

| Name | Description | Order Number |
|---|---|---|
| *DSP56309 Technical Data* | Description, features list, and specifications of the DSP56309 | DSP56309 |
| *DSP56309 User's Manual* | Detailed functional description of the DSP56309 memory configuration, operation, and register programming | DSP56309UM |
| *DSP56300 Family Manual* | Detailed description of the DSP56300 family processor core and instruction set | DSP56300FM |
| Application Notes | Documents describing specific applications or optimized device operation including code examples | See the DSP56309 product website |

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