



PESD5V0F1BSF

Extremely low capacitance bidirectional ESD protection diode

12 April 2021

Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DSN0603-2 (SOD962) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance $C_d = 0.25$ pF
- Minimized capacitance variation over voltage
- ESD protection up to ± 10 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals


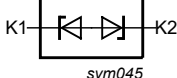
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	0.2	0.25	0.3	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view</p> <p>DSN0603-2 (SOD962)</p>	 <p><i>sym045</i></p>
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0F1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 x 0.3 x 0.3 mm body	SOD962

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0F1BSF	F

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PPM}	rated peak pulse power	$t_p = 8/20 \mu s$	[1]	-	28	W
I_{PPM}	rated peak pulse current		[1]	-	2.2	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2]	-	10	kV
		IEC 61000-4-2 (air discharge)	[2]	-	10	kV
		MIL-STD-883 (human body model)		-	10	kV

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.

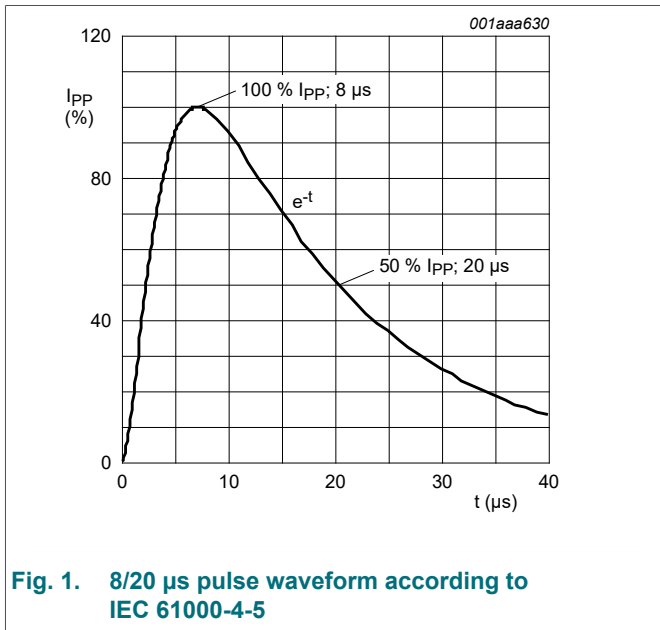


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

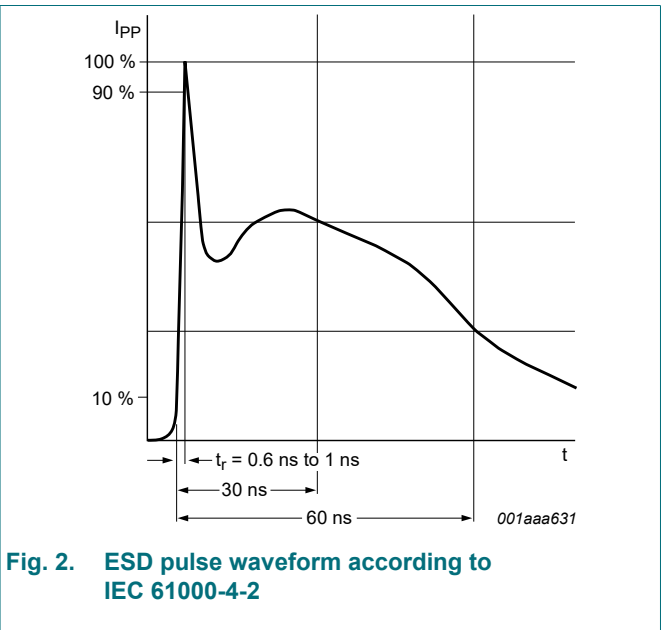


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

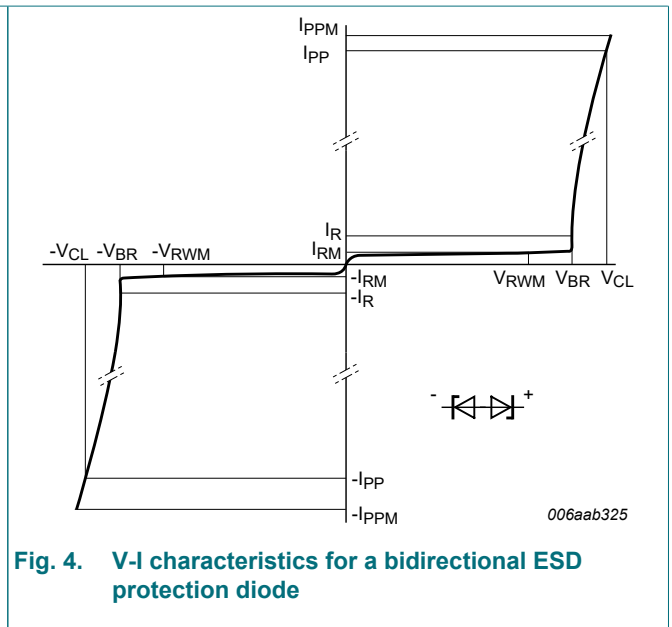
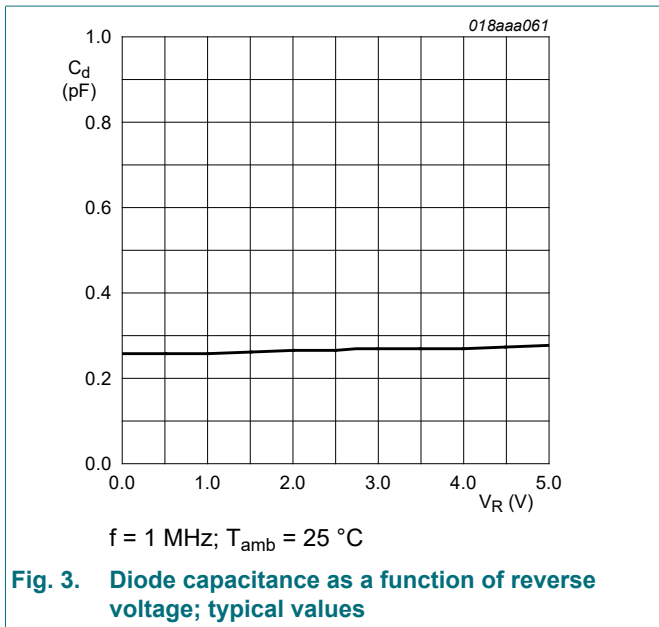
9. Characteristics

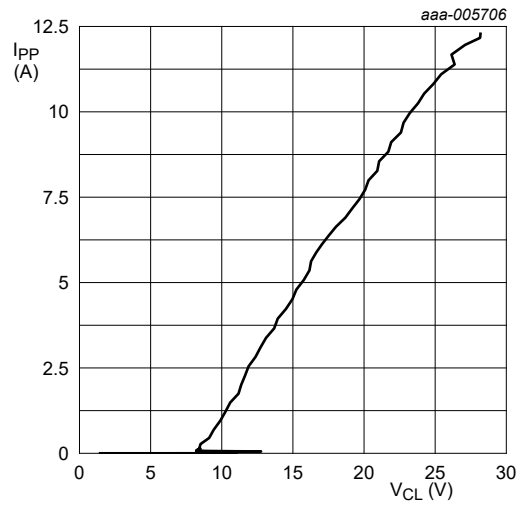
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	5	V
V_{BR}	breakdown voltage	$I_R = 1\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	6	-	10	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	0.2	0.25	0.3	pF
V_{CL}	clamping voltage	$I_{PP} = 0.5\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	10	V
		$I_{PPM} = 2.2\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	12.8	V
R_{dyn}	dynamic resistance	$I_R = 10\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	1.3	-	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANS/IESD STM5.5.1-2008.





$t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP)

Fig. 5. Dynamic resistance; typical values

Extremely low capacitance bidirectional ESD protection diode

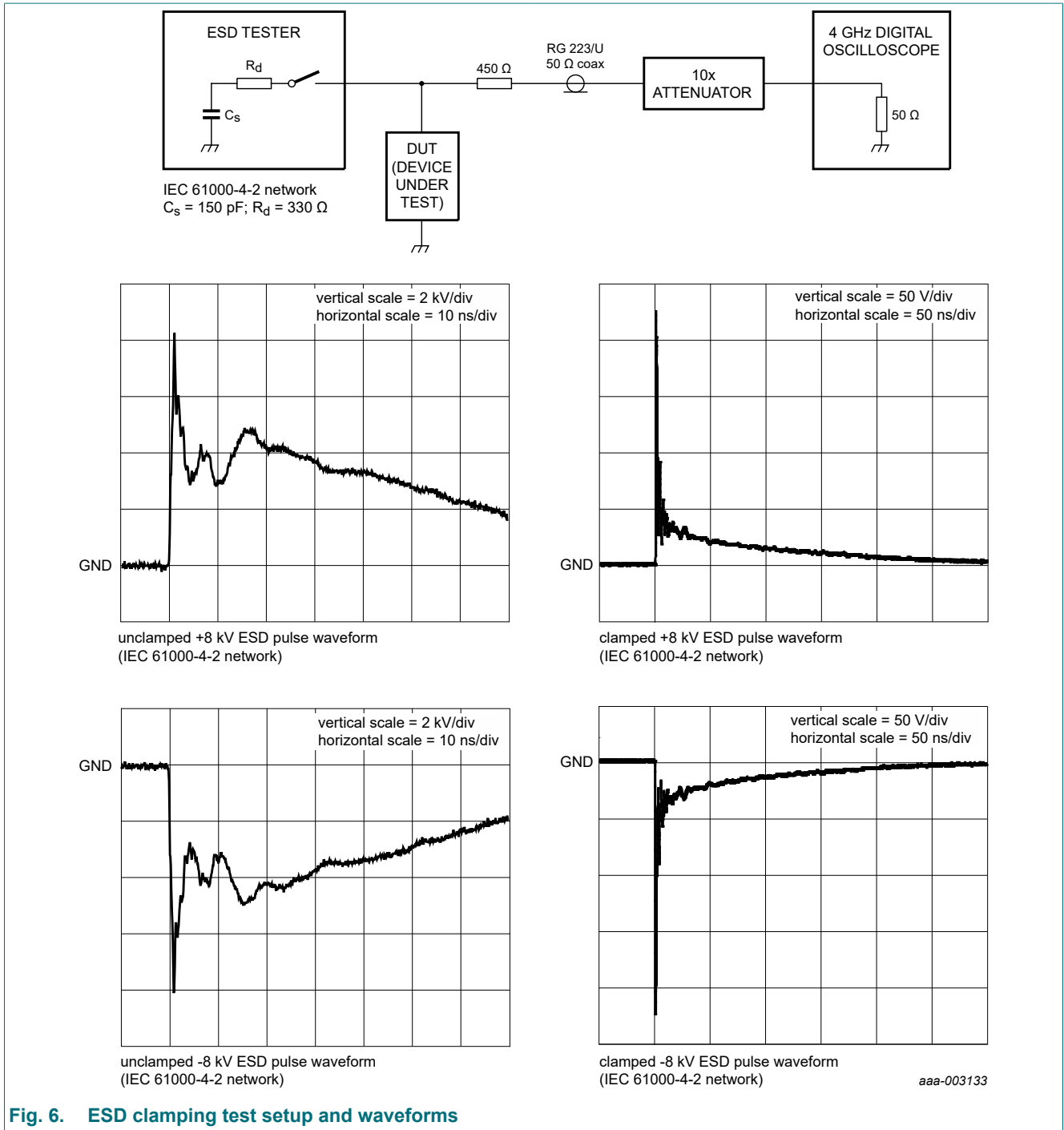


Fig. 6. ESD clamping test setup and waveforms

10. Application information

The PESD5V0F1BSF is designed for the protection of one data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground. It provides protection against surges with up to 28 W per line.

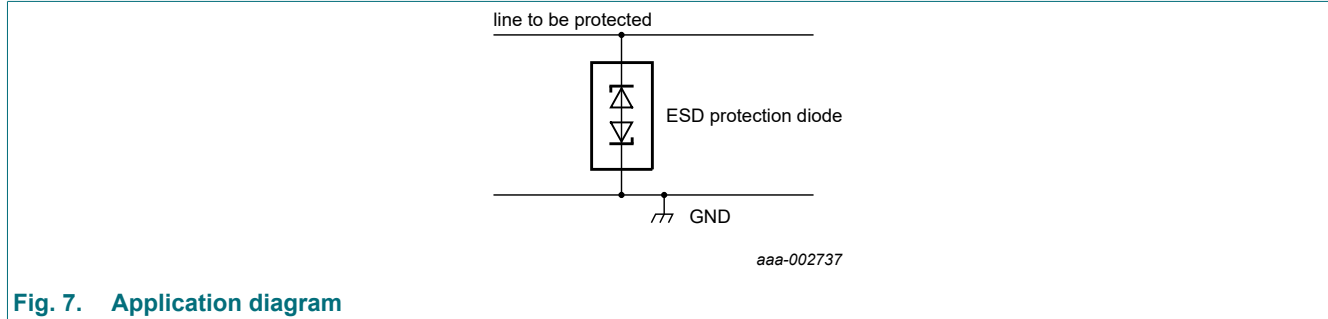


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

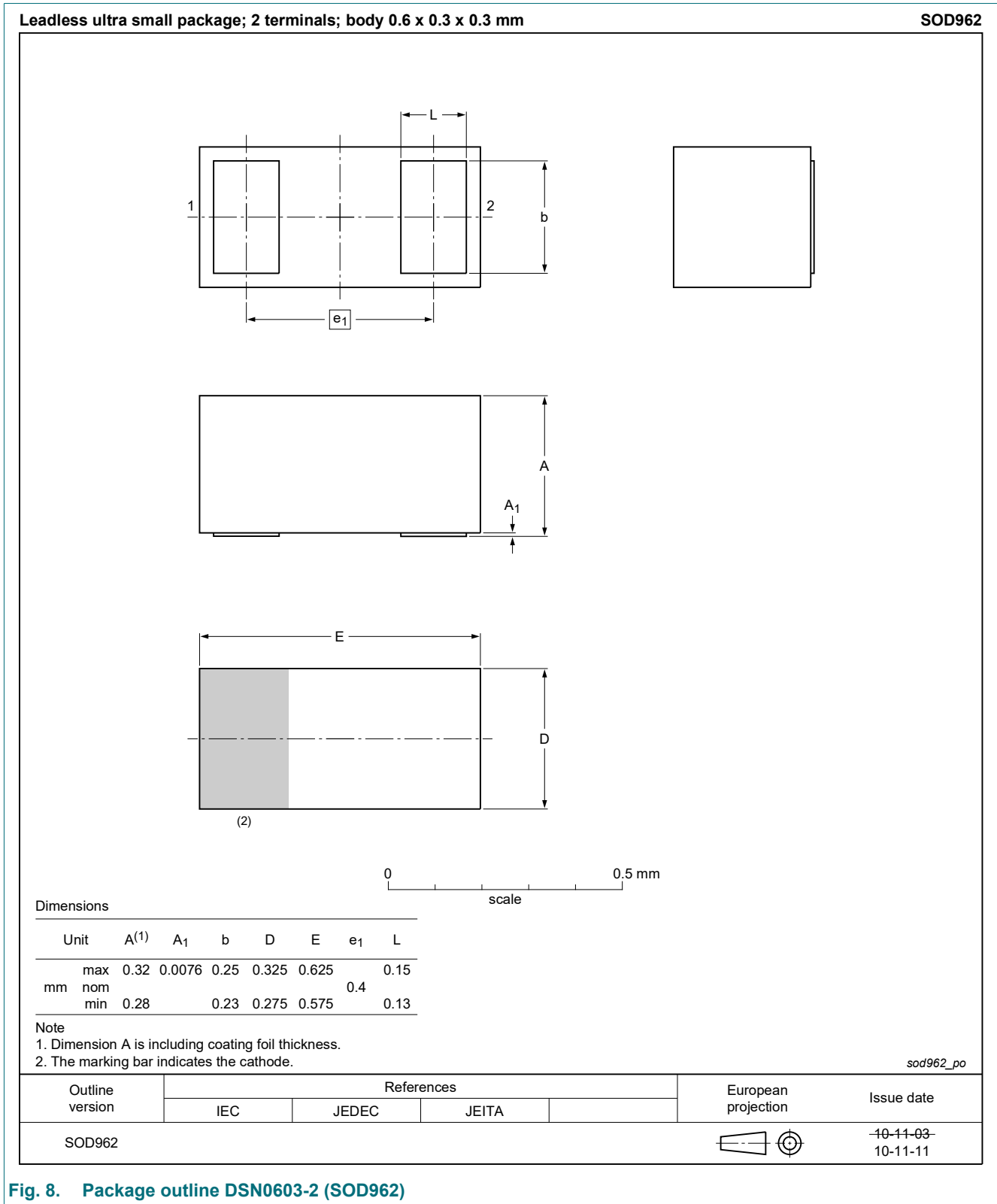


Fig. 8. Package outline DSN0603-2 (SOD962)

12. Soldering

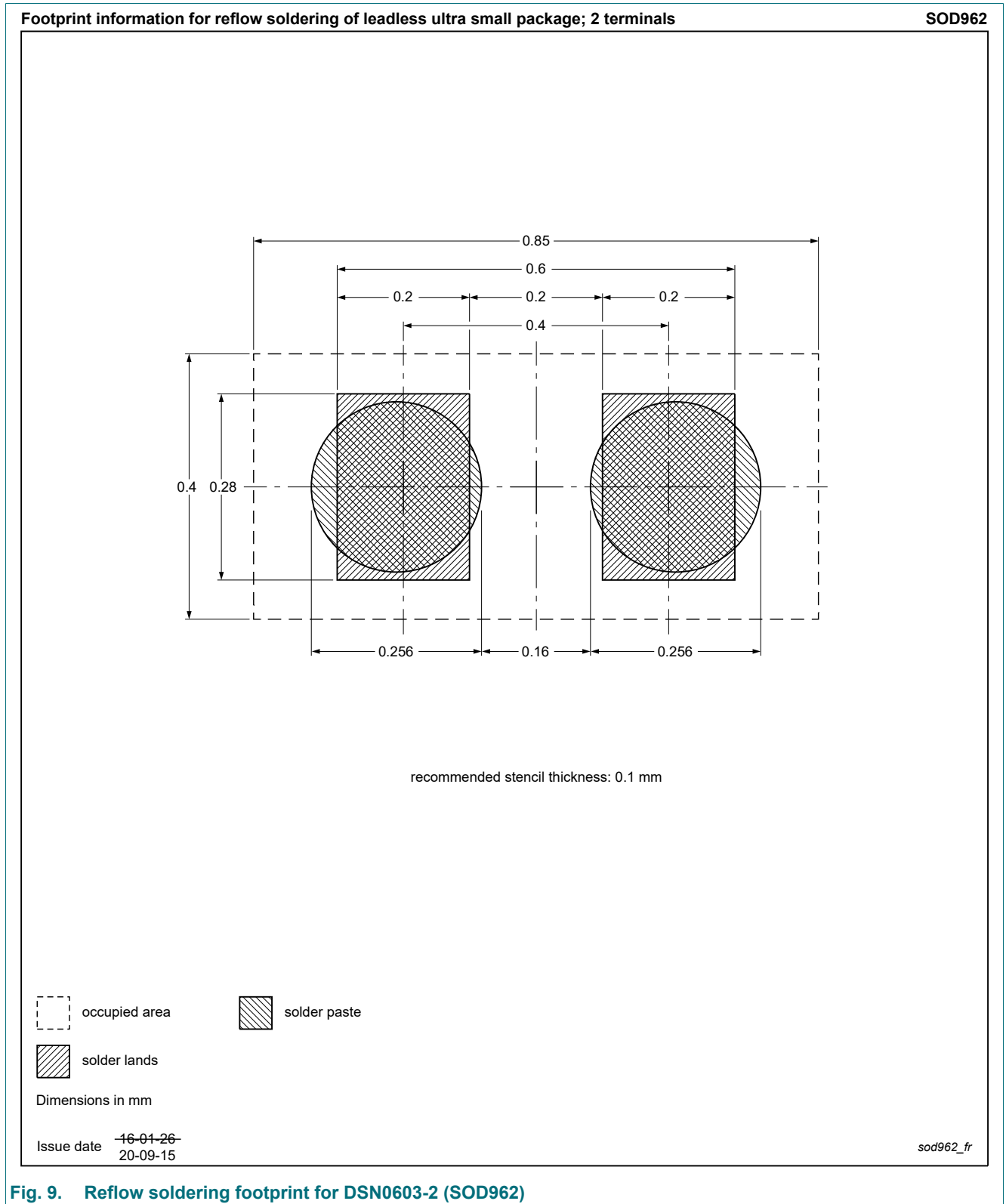


Fig. 9. Reflow soldering footprint for DSN0603-2 (SOD962)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0F1BSF v.3	20210412	Product data sheet	-	PESD5V0F1BSF v.2
Modifications:	• Figure "Reflow soldering footprint" updated			
PESD5V0F1BSF v.2	20180410	Product data sheet	-	PESD5V0F1BSF v.1
PESD5V0F1BSF v.1	20121210	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 12 April 2021
