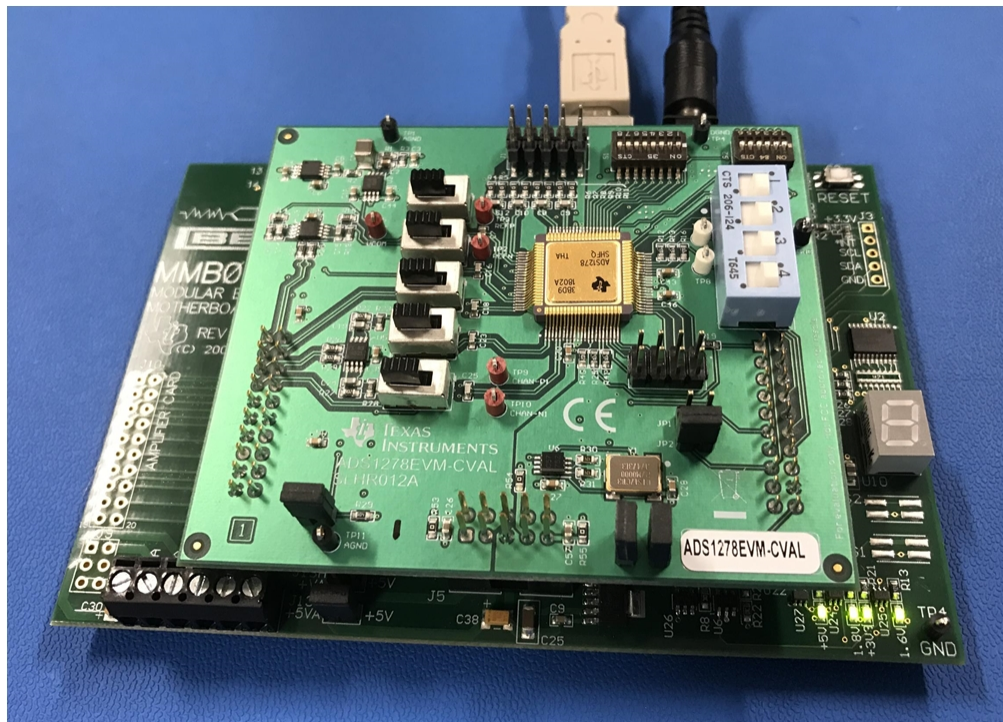


ADS1278EVM-CVAL Evaluation Module User's Guide



ADS1278EVM-CVAL Evaluation Module Kit

This user's guide describes the characteristics, operation, and use of the ADS1278EVM-CVAL kit. This evaluation kit is an evaluation system for the [ADS1278-SP](#), a 24-bit, radiation hardened, 8 channel, delta-sigma analog-to-digital converter (ADC).

This document includes an EVM QuickStart, hardware and software details, bill of materials, and schematic.

The following related documents are available through the Texas Instruments web site at <http://www.ti.com>.

Table 1. EVM-Compatible Device Data Sheets

Device	Literature Number	Device	Literature Number
ADS1278-SP	SBAS937	SN74LVC2G157	SCES207
REF5025	SBOS410	TPS65131	SLVS493
OPA2350	SBOS099	PCA9535	SCPS129
OPA1632	SBOS286		

Trademarks

ADCPro is a trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

1 EVM Overview

The ADS1278EVM-CVAL is an evaluation module kit that includes an EVM, MMB0 motherboard, a USB cable, and a barreled power supply cable as shown in [ADS1278EVM-CVAL Evaluation Module Kit](#) above. When used with the MMB0 EVM, the ADS1278-SP can be evaluated quickly using software GUI ADCPro™. As a standalone PCB, the ADS1278EVM-CVAL is useful for prototyping designs and firmware as it can be connected to any modular EVM system interface card.

1.1 Features

ADS1278EVM-CVAL Features:

- Contains all support circuitry needed for the ADS1278-SP
- Voltage reference options: external or onboard
- Clock options: External clock source (PLL or DSP supplied) or 27-MHz onboard crystal oscillator
- GPIO access
- Compatible with the TI Modular EVM System

2 Quick Start

This section provides a QuickStart guide to quickly begin evaluating the ADS1278EVM-CVAL with ADCPro.

2.1 Default Jumper/Switch Configuration

Figure 1 and Table 2 show the factory default jumper positions for the MMB0 motherboard EVM.

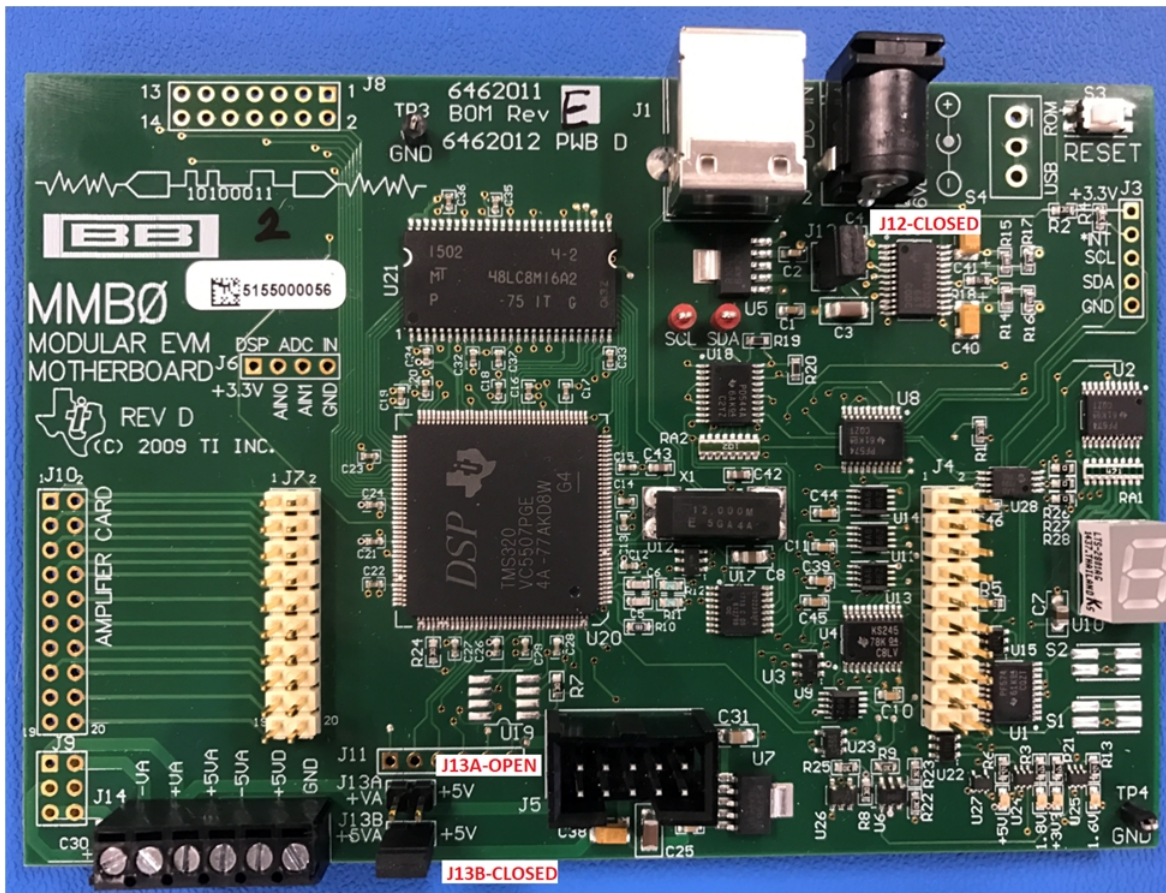


Figure 1. MMB0 Default Jumper Positions

Table 2. MMB0 Default Jumper Positions

Jumper	Position
J12	CLOSED
J13A	OPEN
J13B	CLOSED

Figure 2 and Table 3 show the factory default jumper and switch positions for the ADS1278EVM-CVAL.

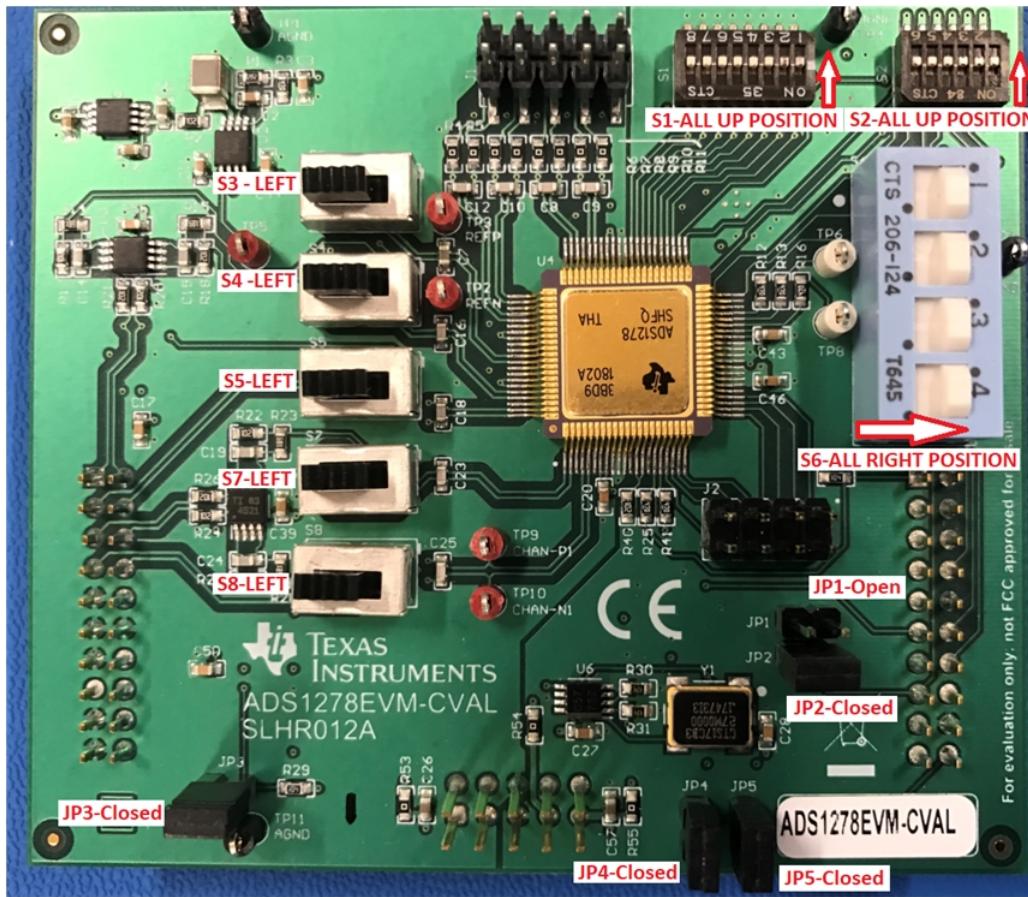


Figure 2. ADS1278EVM-CVAL Default Jumper/Switch Positions

Table 3 lists the jumpers and switches and the factory default conditions.

Table 3. Default Jumper/Switch Configuration

Switch	Default Position	Switch Description
S1	All OFF (Up)	Power-down channel DIP switches (hardware control).
S2	All OFF (Up)	Mode, Format, and CLKDIV DIP switches (hardware control).
S3	INT (Left)	On-board voltage reference selected.
S4	Header connected to converter (Left)	Channel 4 header connected to converter (not buffered).
S5	Header connected to converter (Left)	Channel 3 header connected to converter (not buffered).
S6	[1-2], [4-5], [7-8], [10-11](Right)	Jumpers installed to select FS serial interface format.
S7	Header connected to converter (Left)	Channel 2 header connected to converter (not buffered).
S8	Header connected to converter (Left)	Channel 1 header connected to converter (not buffered).
Jumper	Default Position	Jumper Description
JP1	Open	FSX NOT connected to SYNC/DRDY.
JP2	Short	FSR connected to SYNC/DRDY.
JP3	Short	Input buffer op-amps are powered-down.
JP4	Short	Clock source selection using software control.
JP5	Short	External clock source selected (invalid since using software control).

2.2 ADS1278EVM-CVAL Operation

Perform the following steps to ensure proper hardware setup as shown in [Figure 3](#).

- Install ADCPro software GUI per the instructions in **ADCPro™ Hardware and Software Installation Manual (SLAU372)**.
- Install the ADS1278EVM-CVAL plug-in GUI software per the instructions in [Appendix A](#).
- Mate ADS1278EVM-CVAL to MMB0 EVM through connectors **J3**, **J4**, and **J5**.

CAUTION

Do not misalign the pins when plugging the ADS1278EVM-CVAL into the MMB0. Check the pin alignment of **J3**, **J4**, and **J5** carefully before applying power.

- Connect USB cable from MMB0 **J1** to PC.
- Connect +6-V power supply to **J2** on MMB0 EVM with current limit no lower than 1 A.
- Confirm that four green LEDs on MMB0 EVM light up when powered as shown in [Figure 3](#).

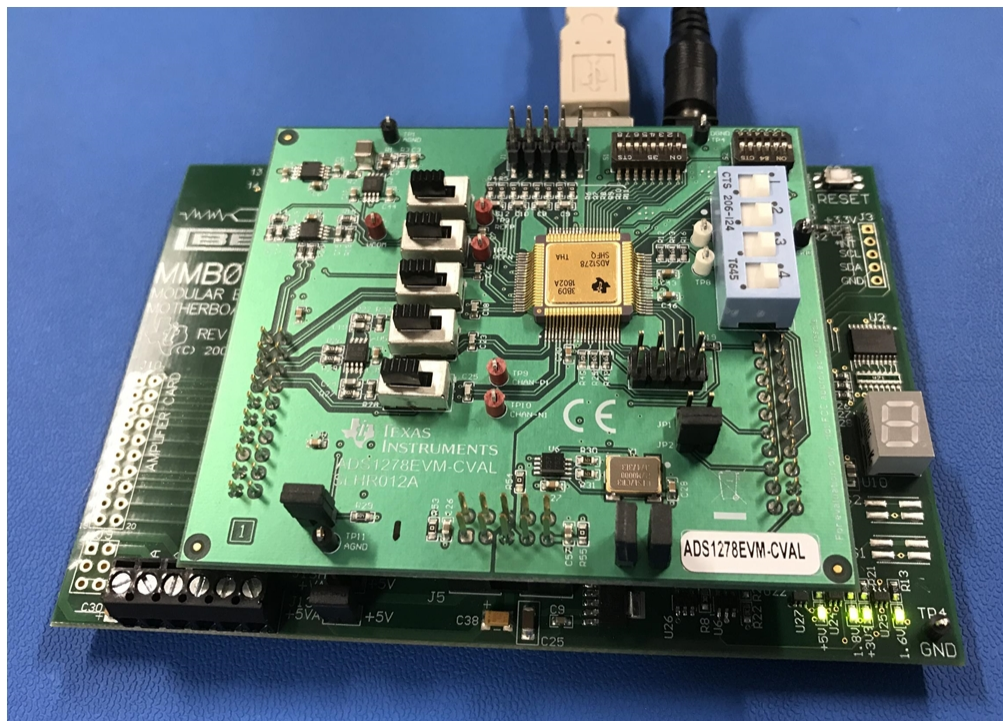


Figure 3. EVM Setup

- Launch ADCPro and then load the ADS1278EVM-CVAL plug-in by clicking on the EVM menu item and selecting ADS1278EVM-CVAL.
- Verify that the plug-in loaded correctly by observing that the black box at the top of the plug-in screen reads “Connected to EVM” as shown in [Figure 4](#).

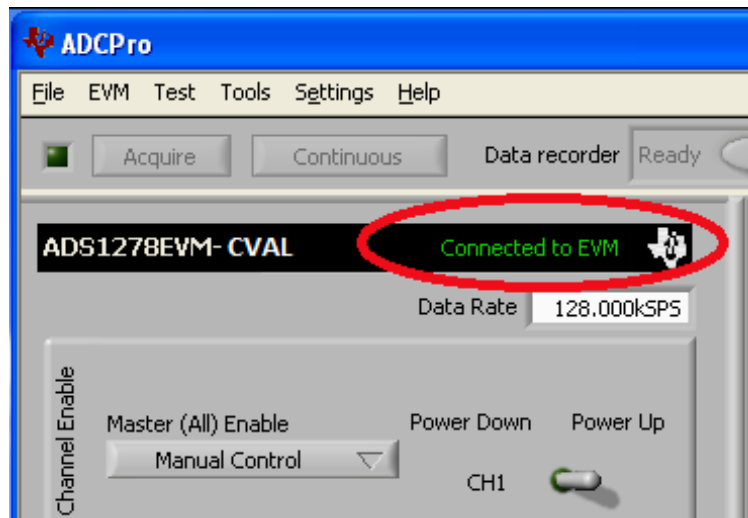


Figure 4. Connected to EVM Status

To capture Channel 1 waveform configure ADS1278EVM-CVAL PCB as follows and as shown in [Figure 5](#).

- Remove jumper **JP3**, Power down Buffer.
- Set switches **S8** to right position to enable buffers in analog input signal paths.
- Using jumper cable, ground the complementary analog input of Channel 1 by connecting test point **TP1, AGND**, to **J3.7, ANN1**.
- Set function generator to High Z mode, sine wave output, frequency = 500 Hz, Amplitude = 1 V_{pp}-diff, DC offset = 500 mV, and enable the output.
- Connect function generator negative output to **TP1, AGND**, and positive output to **J3.8, ANP1**, on ADS1278EVM-CVAL.

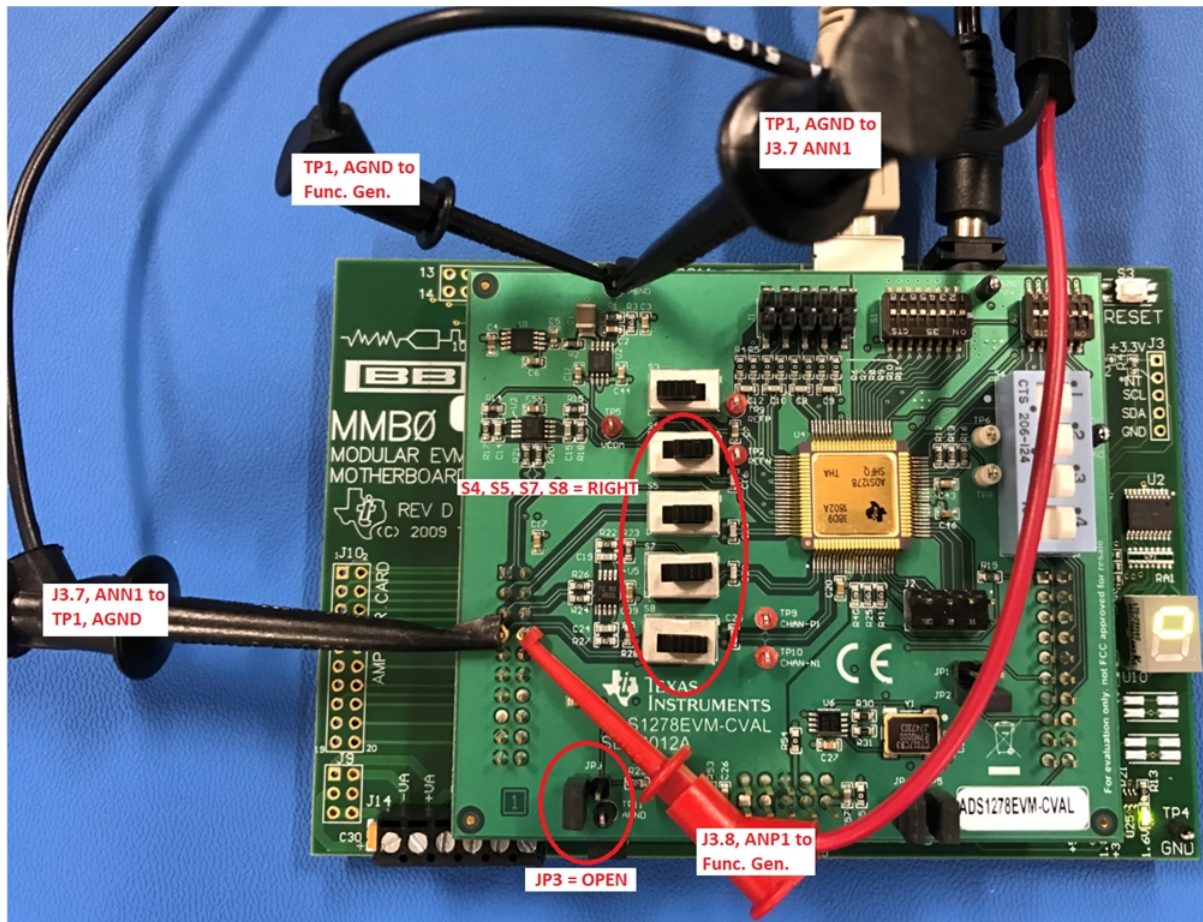


Figure 5. EVM Setup AC Testing Channel 1

- On the EVM plug-in GUI, select the *SETTINGS* tab, set the Operating Mode to *High Resolution* as shown below, leaving all other settings in the default state.

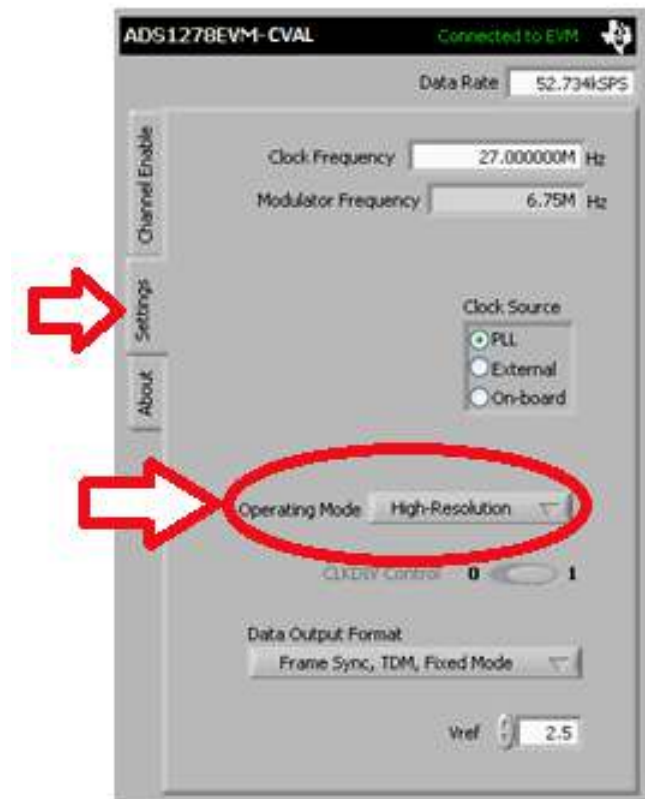


Figure 6. Set Operating Mode to *High-Resolution*

- In ADCPro, select the *MultiScope* plug-in in the *Test* drop-down menu as shown in Figure 7.

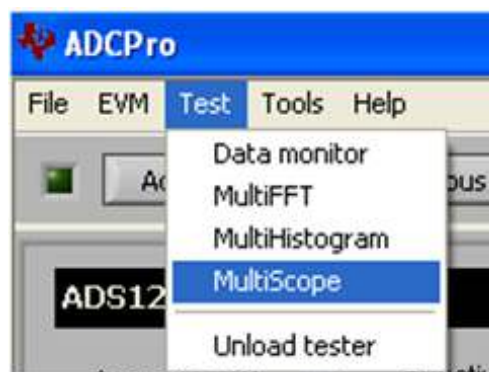


Figure 7. Select *Test=>MultiScope*

- In ADCPro, select the *Continuous* button to begin continuous conversions. Confirm that the signal being applied to Channel 1 is being captured and displayed in the *Multichannel Scope* window as shown below and that the signal is roughly 1 Vpp-diff.

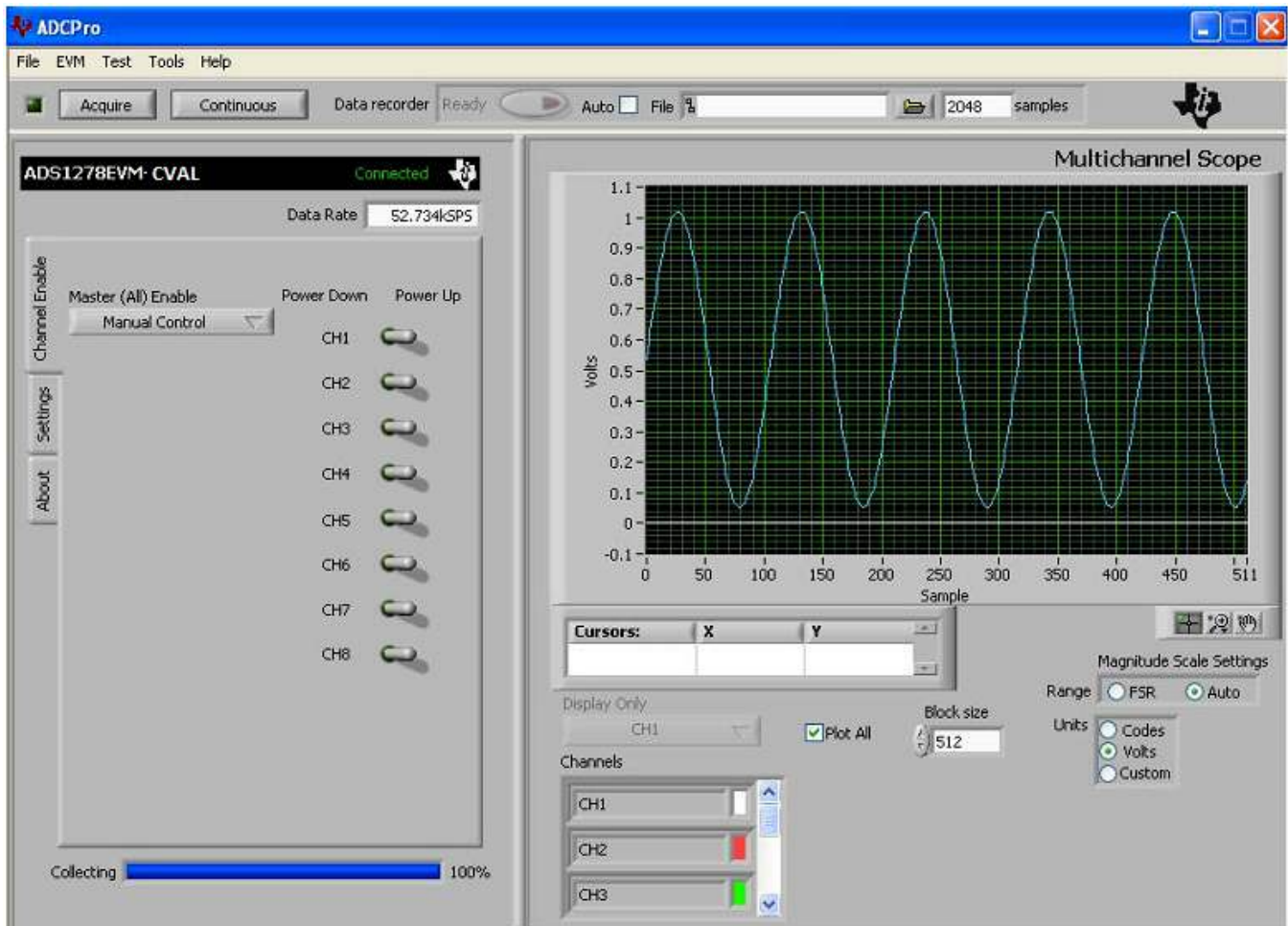


Figure 8. Multichannel Scope Capture of Analog Channel 1

3 Quick Reference

Table 4 provides a quick summary of the connections required for operation of the EVM as a standalone.

Table 4. Critical Connections

Function	Header/Pin	Pin Name	Description	
Interface	SCLK	J4.3	CLKX	SCLK
	DIN	J4.11	DX	Data In
	DOUT	J4.13	DR	Data Out
	Interrupt	J4.15	$\overline{\text{INT}}$	$\overline{\text{DRDY}}/\text{FSYNC}$
Power	1.8 V	J5.7	+1.8VD	Digital supply
	3.3 V	J5.9	+3.3VD	Digital supply
	5.0 V	J5.3	+5VA	Analog supply
Analog Inputs	Channels 1-4	J3.1-8		Analog Inputs
	Channels 5-8	J1.3-10		Analog Inputs

CAUTION

When using the ADS1278EVM-CVAL with the MMB0 EVM, the DIP switches **S1** and **S2** must all be switched up, away from the center of the board. Failure to do so may damage the EVM.

3.1 Analog Inputs

The analog inputs for the ADS1278EVM-CVAL are connected to **J1** and **J3**. Channels 1-4 connect to **J3** and provisions are provided to buffer these signals before being connected to the converter. Switches **S4**, **S5**, **S7**, and **S8** control whether the buffered or unbuffered signal is connected to the ADS1278-SP. Channels 5-8 connect to **J1** and have an RC filter available to filter the input before connecting to the converter. Channels 5-8 do not have provisions for buffering the signal.

3.2 Digital Control

The digital control signals can be applied directly to **J4** (top or bottom side).

3.3 Power Supply

The ADS1278EVM-CVAL requires power rails as follows:

- 5.0-V analog supply - supplied by MMB0 motherboard via **J13B**
- 3.3-V digital supply - supplied by MMB0 motherboard
- 1.8-V digital supply - supplied by MMB0 motherboard

3.4 Voltage Reference

The ADS1278EVM-CVAL has two options for the reference voltage. Switch **S3** selects the reference voltage from either the buffered REF5025 or an external reference voltage that is connected to the reference pins of **J3** (**J3.18** = REFN and **J3.20** = REFP). Regardless of the reference source, the voltage being provided to the ADS1278-SP can be monitored at testpoints **TP2**, **REFN**, and **TP3**, **REFP**, as shown in Figure 9 below.

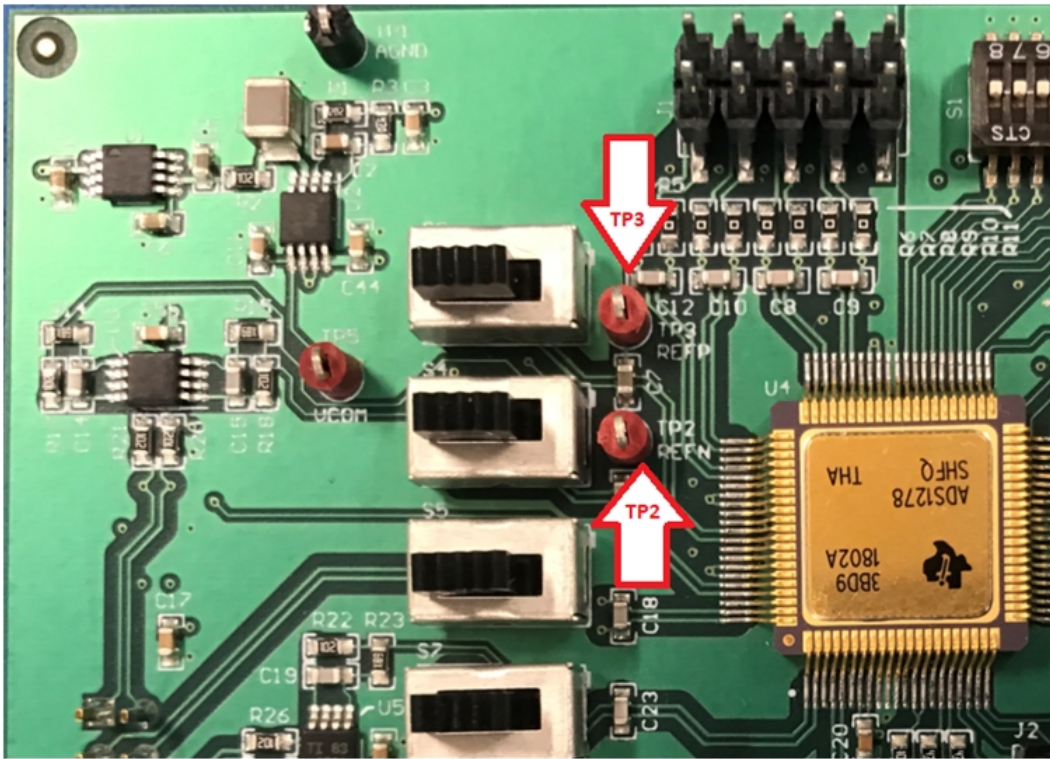


Figure 9. TP2, REFN, and TP3, REFP, Test Points

4 Using the ADS1278EVM-CVAL Plug-in ADCPro

The ADS1278EVM-CVAL plug-in for ADCPro provides complete control over all settings of the ADS1278-SP. It consists of a tabbed interface (see [Figure 10](#)) with different functions available on different tabs. The tabs are:

- Channel Enable
- Settings
- About

The user can adjust the ADS1278EVM-CVAL settings when not acquiring data. During acquisition, all controls are disabled and settings may not be changed. When a setting is changed on the ADS1278EVM-CVAL plug-in, the setting immediately updates on the board.

Settings on the ADS1278EVM-CVAL correspond to settings described in the [ADS1278-SP product data sheet](#) product data sheet.

4.1 Top Level Controls

You can adjust the ADS1278EVM-CVAL settings when you are not acquiring data. During acquisition, all controls are disabled and settings may not be changed.

The effective data rate of the ADS1278-SP depends upon settings of the Clock Freq and Operating Mode. The *Data Rate* indicator in the upper right corner of the plug-in interface (see [Figure 10](#)) is always visible and updates whenever a setting changes that affects the data rate.

4.2 Channel Enable Tab

The ADS1278-SP can acquire data from one to eight channels simultaneously. The *Channel Enable* tab (as shown in [Figure 10](#)) provides the control to power on or off each channel.

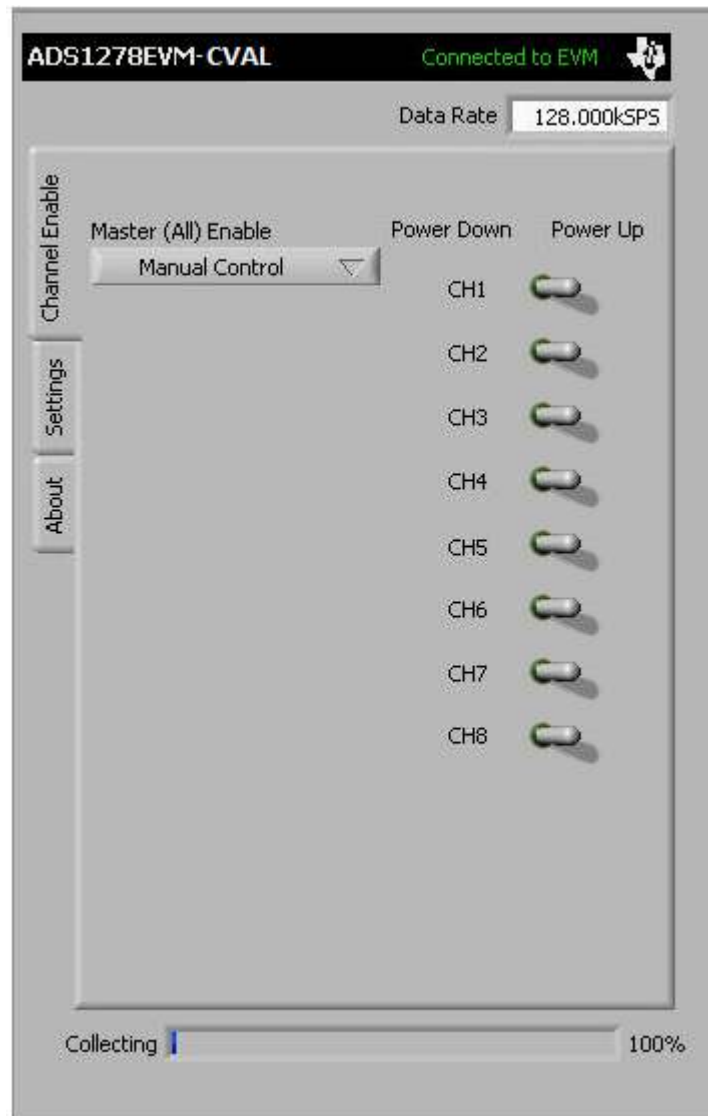


Figure 10. Channel Enable

The *Master (All) Enable* control allows for the selection of channels to convert. *Manual Control* allows channel enable control via *CH1* through *CH8* selector switches. *All Channels Enabled* and *All Channels Disabled* turn all the selector switches either ON or OFF.

4.3 Settings Tab

The *Settings* tab as shown below allows for the selection of the various clock frequencies, operating mode, data format, and other settings.

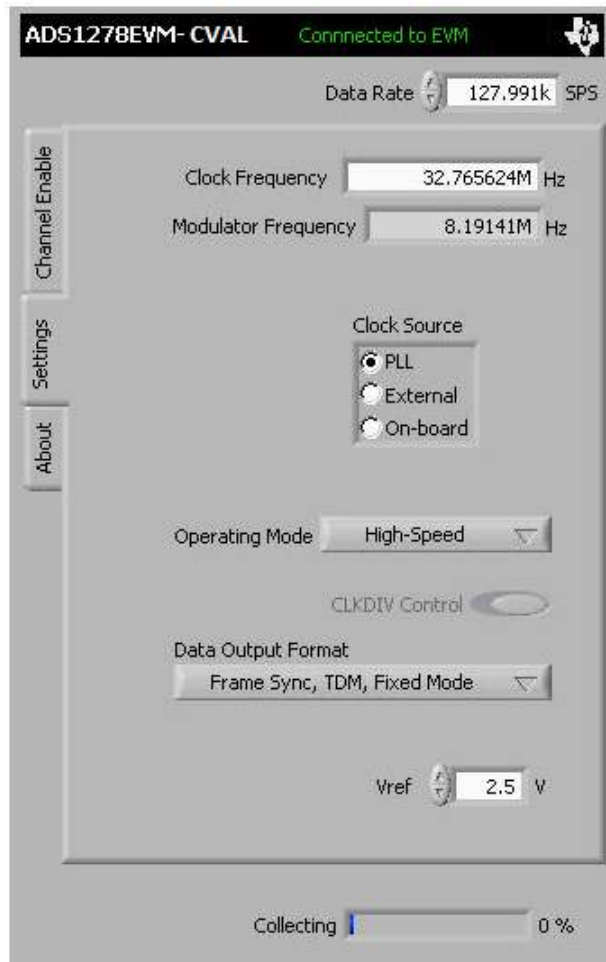


Figure 11. Clock Settings and Mode

The *Clock Source* control selects the input clock source for the ADS1278-SP. The clock can be selected from the MMB0 PLL, an *External* source, or use the *On-board* oscillator.

The *Modulator Frequency* indicator shows the ADS1278-SP modulator frequency based on the clock source.

The *Clock Frequency* control allows the user to input the desired clock frequency when the *PLL* clock source is selected. Once the frequency is entered, the software finds the closest frequency for the PLL to synthesize (and which is within the maximum allowable frequency for the mode selected). This clock frequency is configured in the PLL and overwrites the user entered value in the *Clock Frequency* indicator.

The *Operating Mode* control allows selection of the converter operating mode: *High-Speed*, *High-Resolution*, *Low-Power*, or *Low-Speed*.

The *CLKDIV* control can be set to **0** or **1**.

The *Data Output Format* allows selection of the data output formats. For the ADS1278EVM-CVAL software, the formats are limited to the *Frame-Sync*, *TDM Format*. The available options select whether the software collects data for all channels *Fixed Mode* or only channels that are powered up *Dynamic Mode*.

The *Vref* control allows the user to input the current Vref value being used by the data converter. This control does not change the actual reference voltage, but is required for the software to process the data correctly for display.

The maximum clock frequency is shown for the different converter options in [Table 5](#).

Table 5. Operating Modes: Clock Frequency

Operating Mode	CLKDIV	Frequency (MHz)
High-Speed	1	32.768
High-Resolution	1	27
Low-Power	1	27
Low-Power	0	13.5
Low-Speed	1	27
Low-Speed	0	5.4

4.4 About Tab

The *About* tab provides information on the EVM hardware and software versions.

Plug-in Version is software version of ADCPro plug-in.

Firmware Version is firmware version loaded and running on the processor.

5 ADS1278EVM-CVAL Hardware Details

The ADS1278EVM-CVAL is designed to easily interface with multiple control platforms. Dual-row, header/socket combinations at **J3**, **J4**, and **J5** allow connection to external circuitry for evaluation and debug.

5.1 Jumpers and Switches

Jumpers and Switches function shown in [Table 6](#) below.

Table 6. Jumper and Switch Descriptions

Jumper/Switch	Functions	Descriptions
JP1	FSYNC/ $\overline{\text{DRDY}}$ Source	Short to select FSR as the source ⁽¹⁾
JP2	FSYNC/ $\overline{\text{DRDY}}$ Source	Short to select FSX as the source ⁽¹⁾
JP3	Analog Input Buffers Power-down	Short - input buffers powered-down Open - input buffers powered-up
JP4	Hardware/Software Control of Clock Source	Short - Software control Open - Hardware control
JP5	Internal/External Clock Select (Hardware control)	Short - External clock source selected Open - Internal clock source selected
S1	Power down Channel 1	Hardware control for PWDN1 (set to OFF position for use with software)
	Power down Channel 2	Hardware control for PWDN2 (set to OFF position for use with software)
	Power down Channel 3	Hardware control for PWDN3 (set to OFF position for use with software)
	Power down Channel 4	Hardware control for PWDN4 (set to OFF position for use with software)
	Power down Channel 5	Hardware control for PWDN5 (set to OFF position for use with software)
	Power down Channel 6	Hardware control for PWDN6 (set to OFF position for use with software)
	Power down Channel 7	Hardware control for PWDN7 (set to OFF position for use with software)
	Power down Channel 8	Hardware control for PWDN8 (set to OFF position for use with software)
S2	GPIO2	Hardware control for GPIO2 (set to OFF position for use with software)
	GPIO3	Hardware control for GPIO3 (set to OFF position for use with software)
	GPIO4	Hardware control for GPIO4 (set to OFF position for use with software)
	GPIO0	Hardware control for GPIO0 (set to OFF position for use with software)
	GPIO1	Hardware control for GPIO1 (set to OFF position for use with software)
	CLKDIV	Hardware control for CLKDIV (set to OFF position for use with software)
S3	Converter voltage reference source selector	Selects source for reference voltage - buffered on-board reference (Left) or header to external source (Right)
S4	Channel 4 input source selector	Selects Channel 4 input source - header or input buffer Left - header Right - input buffer
S5	Channel 3 input source selector	Selects Channel 3 input source - header or input buffer Left - header Right - input buffer

⁽¹⁾ Only one of FSYNC/ $\overline{\text{DRDY}}$ signals should be connected at a time (**JP1** or **JP2**).

Table 6. Jumper and Switch Descriptions (continued)

Jumper/Switch	Functions	Descriptions
S6	Serial Interface format	FS - Frame Sync format. [1-2], [4-5], [7-8], [10-11] installed. ⁽²⁾ SPI - SPI-compatible mode. [2-3], [5-6], [8-9], [11-12] installed. ⁽²⁾
S7	Channel 2 input source selector	Selects Channel 2 input source - header or input buffer Left - header Right - input buffer
S8	Channel 1 input source selector	Selects Channel 1 input source - header or input buffer Left - header Right - input buffer

⁽²⁾ Refer to [Section 5.5.1](#) for more details.

5.2 Power-Down, MODE, and FORMAT Control

The ADS1278-SP has several pins to control the power-down of individual channels and select the mode and format for the digital interface.

For users of the ADS1278EVM-CVAL as a stand-alone module, these pins may be pulled high or low through DIP switches **S1** and **S2** (see [Table 6](#)). Refer to the [ADS1278-SP product data sheet](#) for complete details on these pins and which state sets which options.

For use with the MMB0 motherboard, the state of these pins is controlled by software, using the I²C port expanders (U7 and U8) on the EVM. With this configuration, the DIP switches **S1** and **S2** must all be switched up (away from the center of the board). The ADS1278EVM-CVAL software checks at startup to verify that these switches are set correctly, and generates an error message for incorrect settings. The software cannot detect if the switches are changed after startup.

CAUTION

When using the ADS1278EVM-CVAL with the MMB0 motherboard, the DIP switches **S1** and **S2** must all be switched up (away from the center of the board). Failure to do so may damage the EVM.

5.3 Clock Source

The ADS1278-SP clock can come from one of several sources: the onboard 27-MHz crystal oscillator, a clock supplied by a processor on the TOUT pin (**J4.17**), or an external clock source connected between **J4.17** (TOUT) and **J4.18** (DGND).

If the onboard 27-MHz oscillator is selected, the device can be run in high-speed mode, high-resolution mode, low-power mode, or low-speed modes with *CLKDIV* set to 1.

If the performance of the device must be explored with *CLKDIV* set to 0 in the low-power and low-speed modes, an external clock must be provided to the board, either using the TOUT connection or having an external clock source connected to **J4.17**. The same condition is true if frequencies other than the 27 MHz provided by the onboard oscillator must be investigated.

5.4 Analog Headers, J1 and J3

For maximum flexibility, the ADS1278EVM-CVAL is designed for easy interfacing to multiple analog sources. These headers/socket provide access to the analog input pins of the ADS1278-SP.

Four of the analog input sources (Channels 1–4) connect directly to **J3** (top or bottom side) or through signal-conditioning modules available for the modular EVM system. These inputs have provisions to buffer the inputs using THS4521 before connecting to the converter. Switches **S4**, **S5**, **S7**, and **S8** provide the capability to connect either the header directly or through a buffer. When the buffers are not selected, the op-amps used for buffering can be powered down by shorting **JP3**.

Analog input sources (Channels 5-8) are connected directly to **J1**. These inputs can be filtered by installing passive components in the option filter circuitry. By default, the resistors are populated with 0-Ω resistors and the capacitors are not installed. No circuitry is provided to buffer these signals before connecting to the converter.

Table 7. J3: Primary Analog Interface Pinout

Description	Signal	Designator		Signal	Description
Analog Input Channel 4 Negative	AINN4	J3.1 ⁽¹⁾	J3.2	AINP4	Analog Input Channel 4 Positive
Analog Input Channel 3 Negative	AINN3	J3.3	J3.4	AINP3	Analog Input Channel 3 Positive
Analog Input Channel 2 Negative	AINN2	J3.5	J3.6	AINP2	Analog Input Channel 2 Positive
Analog Input Channel 1 Negative	AINN1	J3.7	J3.8	AINP1	Analog Input Channel 1 Positive
Analog Ground	AGND	J3.9	J3.10	Not Connected	Not used for this design
Analog Ground	AGND	J3.11	J3.12	Analog Ground	AGND
Analog Ground	AGND	J3.13	J3.14	Not Connected	Not used for this design
Not used for this design	Not Connected	J3.15	J3.16	Not Connected	Not used for this design
Analog Ground	AGND	J3.17	J3.18	EXTREFN	External Reference negative input
Analog Ground	AGND	J3.19	J3.20	EXTREFP	External Reference positive input

⁽¹⁾ Pin 1 is top left-hand corner, located next to reference designator.

Table 8. J1: Secondary Analog Interface Pinout

Description	Signal	Designator		Signal	Description
Not used for this design	Not Connected	J1.1 ⁽¹⁾	J1.2	Not Connected	Not used for this design
Analog Input Channel 8 Negative	AINN8	J1.3	J1.4	AINP8	Analog Input Channel 8 Positive
Analog Input Channel 7 Negative	AINN7	J1.5	J1.6	AINP7	Analog Input Channel 7 Positive
Analog Input Channel 6 Negative	AINN6	J1.7	J1.8	AINP6	Analog Input Channel 6 Positive
Analog Input Channel 5 Negative	AINN5	J1.9	J1.10	AINP5	Analog Input Channel 5 Positive

⁽¹⁾ Pin 1 is top right-hand corner, located next to reference designator.

5.5 Digital Interface

The digital signals are controlled via DSP interface or I²C ICs on the EVM. Some of the digital control pins allow control via hardware or software methods. See [Section 5.2](#) for details on these pins and their operation. The digital control signals can be applied directly to the EVM or by connecting the EVM to a DSP or micro controller interface board, the [5-6K Interface](#), or [HPA-MCUInterface](#) boards which are available from Texas Instruments.

5.5.1 Digital Format Control

The ADS1278-SP allows the serial interface to be used in two different formats: an SPI-compatible mode and a frame-sync format. Switch **S6** is populated with jumpers to select between these two formats:

- **SPI** format configures the signals as follows:
 - The SCLK input of the converter is driven by the serial port signal CLKX, pin **J4.3**.
 - The signal from the selected source for the clock (see [Clock Source](#)) is connected to the CLKR pin (**J4.5**) allowing the serial port of a processor to be synchronized to the converters master clock.
 - The signal from the selected clock source is routed to the CLK input of the converter.
 - Port P10 of the I²C port expander U8 is connected to a logic high level, so that the position of switch **S12** can be read back by software.

- **FS** format configures the signals as follows:
 - The SCLK input of the converter is driven by the serial port signal CLKR, pin **J4.5**.
 - The signal from the selected clock source is connected to the CLKX pin (**J4.3**), allowing the serial port of a processor to be synchronized to the converter's master clock.
 - The CLK input of the converter is driven by the CLKR signal (**J4.5**). This ensures that the CLK and SCLK signals have the same phase and the correct ratio as outlined in the data sheet of the device.
 - Port P10 of the I²C port expander U8 is connected to a logic low level, so that the position of S6 can be read back by software.

For use with the MMB0 motherboard, the jumpers on **S6** must be installed in the **FS** positions, which is the factory default setting. See [Figure 2](#).

Switching to **SPI** format will allow users to connect the EVM to any SPI-compatible processor not supporting the frame-sync mode. If this format is selected, keep in mind that the high-speed mode will not operate at full speed (32.768 MHz) because of the limitations outlined in the device product data sheet.

5.5.2 Serial Data Interface, J4

This header/socket provides access to the digital control and serial data pins of the ADC.

All logic levels on **J4** are 3.3-V CMOS, except for the I²C pins. These pins conform to 3.3-V I²C rules. [Table 9](#) describes the **J4** serial interface pins.

Table 9. J4: Serial Interface Header

Function	Signal Name	Designator		Signal Name	Function
Synchronize channels input	SYNC	1 ⁽¹⁾	2	MODE0	Select bit 0 of converter MODE
SPI clock	SCLK	3	4	DGND	Digital ground
SCLK clock	CLKR	5	6	MODE1	Select bit 1 of converter MODE
DRDY/FSYNC source 1	DRDY/FSYNC	7	8	FORMAT0	Select bit 0 of FORMAT to select Frame-Sync/SPI Protocol
DRDY/FSYNC source 2	DRDY/FSYNC	9	10	DGND	Digital ground
ADS1278 SPI data in	DIN	11	12	FORMAT1	Select bit 1 of FORMAT to select Frame-Sync/SPI Protocol
ADS1278 data out	DOUT1 ⁽²⁾	13	14	FORMAT2	Select bit 2 of FORMAT to select Frame-Sync/SPI Protocol
DRDY/FSYNC to DSP (interrupt)	DRDY/FSYNC	15	16	SCL	I ² C clock
Can be used to provide a clock from a processor	CLK	17	18	DGND	Digital ground
Clock source select (SW mode)	CLK Select	19	20	SDA	I ² C data

⁽¹⁾ Pin 1 is top left-hand corner, located next to reference designator.

⁽²⁾ **DOUT1** buffered through a D flip-flop. See [Section 5.5.3.1](#) below.

Some pins on **J5** have weak pull-up/down resistors. These resistors provide default settings for many of the control pins. Many pins on **J5** correspond directly to ADS1278-SP pins. See the [ADS1278-SP product data sheet](#) for complete details on these pins.

5.5.3 Data Output Signals

5.5.3.1 DOUT on Digital Interface J4

In TDM mode, the data from all eight channels can be observed on the DOUT1 pin of the converter. The DOUT1 signal is used by the MMB0 motherboard to read back and display all the channels. The digital data output pin on the digital interface header **J4** is connected to DOUT1 signal via a D flip-flop. The D flip-flop provides a half cycle delay in order to align the data correctly to reach the higher speeds of the device. Otherwise, the propagation delay from the MSB in Frame Sync mode may result in missing the MSB out of the data word.

5.5.3.2 DOUTx Header, J2

All the data output signals (DOUT1 to DOUT8) can be monitored on **J2**. [Table 10](#) illustrates the pinout for **J2**.

Table 10. J2: DOUTx Header

Data Out Line	Designator		Data Out Line
DOUT1	1 ⁽¹⁾	2	DOUT2
DOUT3	3	4	DOUT4
DOUT5	5	6	DOUT6
DOUT7	7	8	DOUT8

⁽¹⁾ Pin 1 is top right-hand corner, located next to reference designator.

5.6 Power Supply Header, J5

J5 is the power-supply input connector. [Table 11](#) lists the configuration details for **J5**. Supplies of 1.8 V, 3.3 V, and 5.0 V are required for operation of the EVM. When using the EVM with the MMB0, these voltages are generated by the MMB0 and no external supplies are required. For operation as a stand-alone EVM, the power supplies should be connected as shown below.

Table 11. J5 Configuration: Power-Supply Input

Function	Pin Name	Designator		Pin Name	Function
Not used for this design	Not used	1 ⁽¹⁾	2	Not used	Not used for this design
+5-V analog supply	+5VA	3	4	Not used	Not used for this design
Digital ground	DGND	5	6	AGND	Analog ground input
1.8-V digital supply	+1.8VD	7	8	Not used	Not used for this design
3.3-V digital supply	+3.3VD	9	10	N/A	Do not use

⁽¹⁾ Pin 1 is bottom left-hand corner, located next to reference designator.

NOTE: For monitoring the current from each supply, **CM1**, **CM2**, and **CM3** (0-Ω resistors) can be removed and replaced with sense resistors or ammeters.

The ADS1278-SP digital supplies are connected as follows:

- IOVDD supply is connected to the +1.8VD pin of the **J3** header.
- DVDD supply is connected to the +3.3VD pin of the **J3** header.

The ADS1278-SP analog supply, AVDD, is connected to the +5VA pin of the **J5** header.

6 Schematic and Bill of Materials

This section provides EVM schematics for the ADS1278EVM-CVAL as well as the bill of materials (BOM). Gerber files are available on request. Please e-mail support@ti.com or [E2E Community Forums](#) and ask for details on how to receive the files.

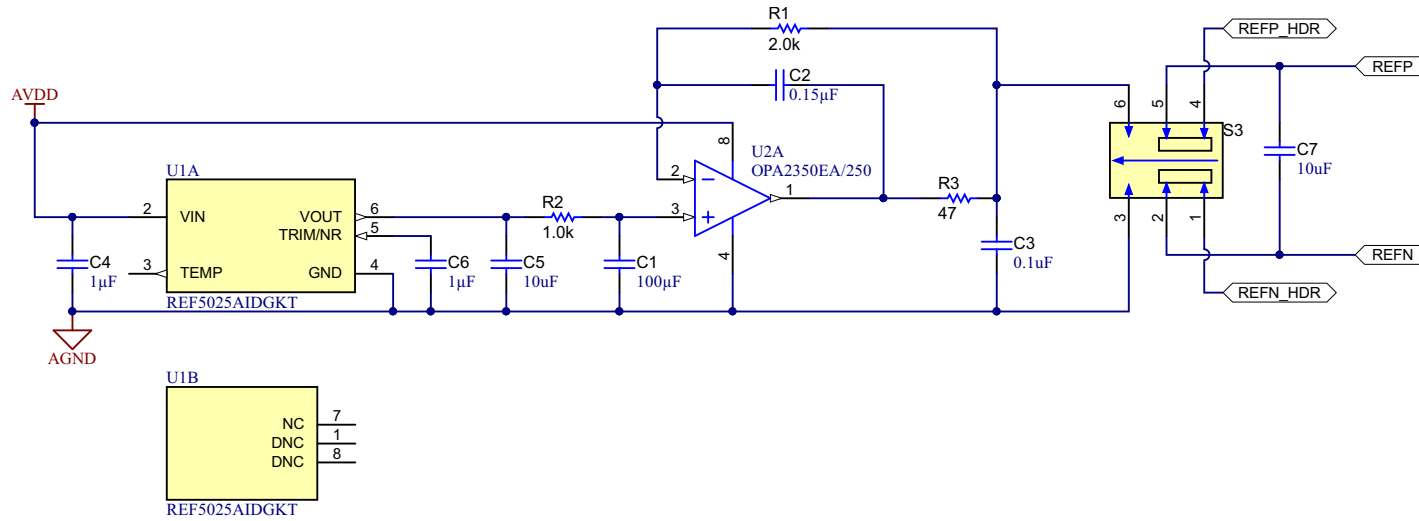
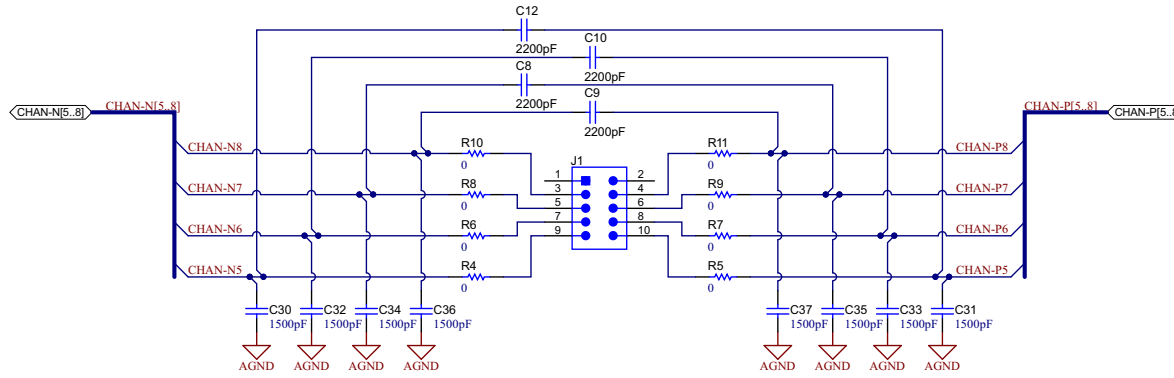


Figure 13. Schematic02

Channels 5-8 Analog Connections



GPIO/Logic Connections

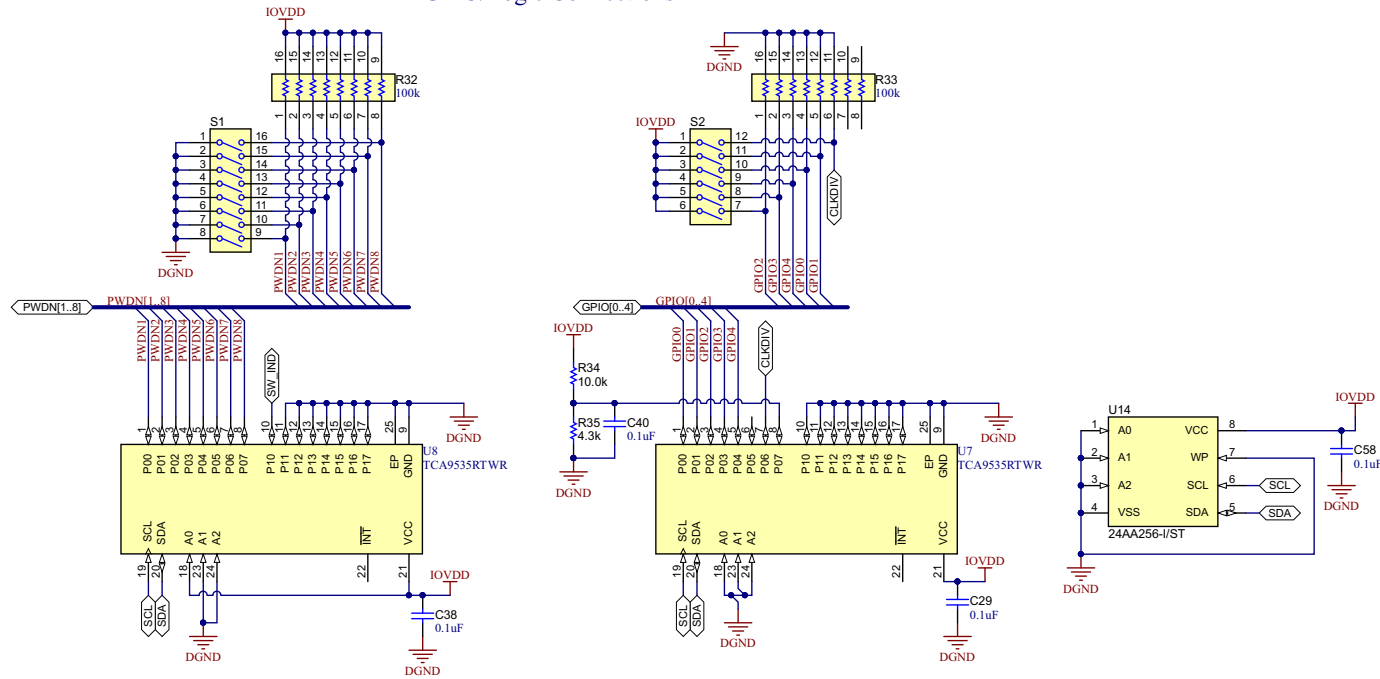


Figure 15. Schematic04

6.2 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the <http://www.ti.com>.)

Table 12. ADS1278EVM-CVAL Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board		SLHR012	Any
C1	1	100 μ F	CAP, CERM, 100 μ F, 10 V, \pm 20%, X5R, 1210	1210	CL32A107MPVNNNE	Samsung
C2	1	0.15 μ F	CAP, CERM, 0.15 μ F, 25 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603X154K3RAC7867	Kemet
C3, C11, C13, C17, C20, C21, C22, C27, C28, C29, C38, C39, C40, C41, C42, C44, C45, C46, C49, C50, C51, C54, C55, C56, C58	25	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, \pm 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C4, C6, C43	3	1 μ F	CAP, CERM, 1 μ F, 25 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105K080AD	TDK
C5, C7, C26, C57	4	10 μ F	CAP, CERM, 10 μ F, 10 V, \pm 20%, X5R, 0603	0603	C1608X5R1A106M080AC	TDK
C8, C9, C10, C12, C16, C18, C23, C25	8	2200 pF	CAP, CERM, 2200 pF, 50 V, \pm 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
C14, C15, C19, C24, C30, C31, C32, C33, C34, C35, C36, C37, C47, C48, C52, C53	16	1500 pF	CAP, CERM, 1500 pF, 25 V, \pm 5%, X7R, 0603	0603	C0603C152J3RACTU	Kemet
J1	1		Header, 100 mil, 5x2, Tin, SMT	500x180x290 mil	TSM-105-01-T-DV-P	Samtec
J2	1		Header, 100 mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
J3, J4	2		Receptacle, 2.54 mm, 10x2, Gold, TH	Receptacle, 2.54 mm, 10x2, TH	SSW-110-02-G-D	Samtec
J5	1		Receptacle, 2.54 mm, 5x2, Gold, TH	Receptacle, 2.54 mm, 5x2, TH	SSW-105-03-G-D	Samtec
JP1, JP2, JP3, JP4, JP5	5		Header, 100 mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 in	THT-14-423-10	Brady
R1	1	2.0k	RES, 2.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06032K00JNEA	Vishay-Dale
R2, R17, R18, R20, R21, R22, R24, R26, R27, R38, R39, R40, R42, R43, R45, R46, R47, R48	18	1.0k	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R3, R12, R13, R16, R25, R41	6	47	RES, 47, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347R0JNEA	Vishay-Dale
R4, R5, R6, R7, R8, R9, R10, R11	8	0	RES, 0, 5%, 0.1 W, 0603	0603	MCR03EZPJ000	Rohm
R14, R15, R23, R28, R36, R37, R49, R50	8	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo
R19, R29, R44	3	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R30, R31	2	470k	RES, 470 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470KJNEA	Vishay-Dale

Table 12. ADS1278EVM-CVAL Bill of Materials (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
R32, R33	2	100k	RES, 100 k, 5%, 0.0625 W, AEC-Q200 Grade 1, Resistor Array - 8x1	Resistor Array - 8x1	EXB-2HV104JV	Panasonic
R34	1	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R35	1	4.3k	RES, 4.3 k, 5%, 0.1 W, 0603	0603	RC0603JR-074K3L	Yageo
R51, R52	2	47k	RES, 47 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347K0JNEA	Vishay-Dale
R53, R54, R55	3	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
S1	1		Switch, SPST, 8 Pos, 25 mA, 24 VDC, SMD	11.33x5.8 mm	218-8LPST	CTS Electrocomponents
S2	1		Switch, SPST, Slide, Off-On, 6 Pos, 0.025 A, 24 V, SMD	5.8x8.79 mm	218-6LPST	CTS Electrocomponents
S3, S4, S5, S7, S8	5		Switch, Slide, DPDT, On-On, 0.1 A, 30 V, TH	TH, 6-Leads, Body 9.25x5.65 mm, Pitch 2 mm	SSB22	TE Connectivity
S6	1		DIP SWITCH, SPDT x 4, TH	DIPSWITCH, 16 PIN	206-124	CTS Electrocomponents
TP1, TP4, TP7, TP11	4		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP2, TP3, TP5, TP9, TP10	5		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP6, TP8	2		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1		3 μ Vpp/V Noise, 3 ppm/ $^{\circ}$ C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	DGK0008A	REF5025AIDGKT	Texas Instruments
U2	1		High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier™ Series, DGK0008A (VSSOP-8)	DGK0008A	OPA2350EA/250	Texas Instruments
U3, U5, U9, U11	4		Very low power rail-to-rail output fully differential amplifier, DGK0008A (VSSOP-8)	DGK0008A	THS4521IDGKR	Texas Instruments
U4	1		OCTAL SIMULTANEOUS-SAMPLING 24-BIT ANALOG-TO-DIGITAL CONVERTER, HFQ0084A (CFP-84)	HFQ0084A	ADS1278HFQ/EM	Texas Instruments
U6	1		Single 2-Line to 1-Line Data Selector/Multiplexer, DCT0008A, LARGE T-and-R	DCT0008A	SN74LVC2G157DCTR	Texas Instruments
U7, U8	2		Remote 16-Bit I2C and SMBus, Low-Power I/O Expander with Interrupt Output and Config Register, 1.65 to 5.5 V, -40 to 85 degC, 24-pin QFN (RTW), Green (RoHS -and- no Sb/Br)	RTW0024B	PCA9535RTWR	Texas Instruments
U10	1		Enhanced Product Single Inverter Gate, DBV0005A, LARGE T-and-R	DBV0005A	SN74LVC1G04MDBVREP	Texas Instruments
U12	1		Enhanced Product Single Positive Edge Triggered D-Type Flip-Flop With Clear And Preset, DCU0008A (VSSOP-8)	DCU0008A	SN74LVC2G74MDCUTEP	Texas Instruments
U13	1		Enhanced Product Configurable Multiple-Function Gate, DCK0006A (SOT-SC70-6)	DCK0006A	SN74LVC1G97IDCKREP	Texas Instruments
U14	1		256K I2C™ CMOS Serial EEPROM, TSSOP-8	TSSOP-8	24AA256-I/ST	Microchip
Y1	1		Oscillator, 27 MHz, 50 pF, SMD	SMD, 4-Leads, Body 7.2x5.2 mm	CB3LV-3I-27M0000	CTS Electrocomponents

ADS1278EVM-CVAL Plug-in GUI installation

This appendix provides detailed instructions for installing the ADS1278EVM-CVAL GUI which plugs into the ADCPro GUI. Before proceeding, ensure that ADCPro software GUI has been installed per the instructions in **ADCPro™ Hardware and Software Installation Manual (SLAU372)**.

1. From Tool folder for ADS1278EVM-CVAL download the ADS1278EVM-CVAL GUI and unzip file.
2. Right click on installer executable and *Run as administrator* as shown below:

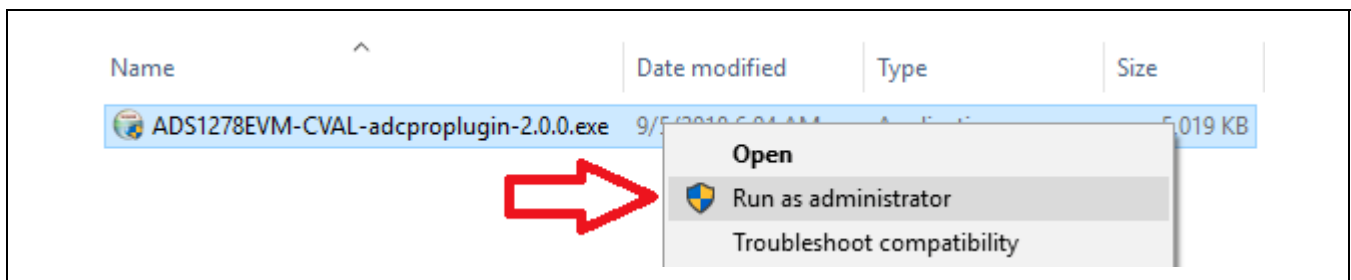


Figure 16.

3. Click *Next*.

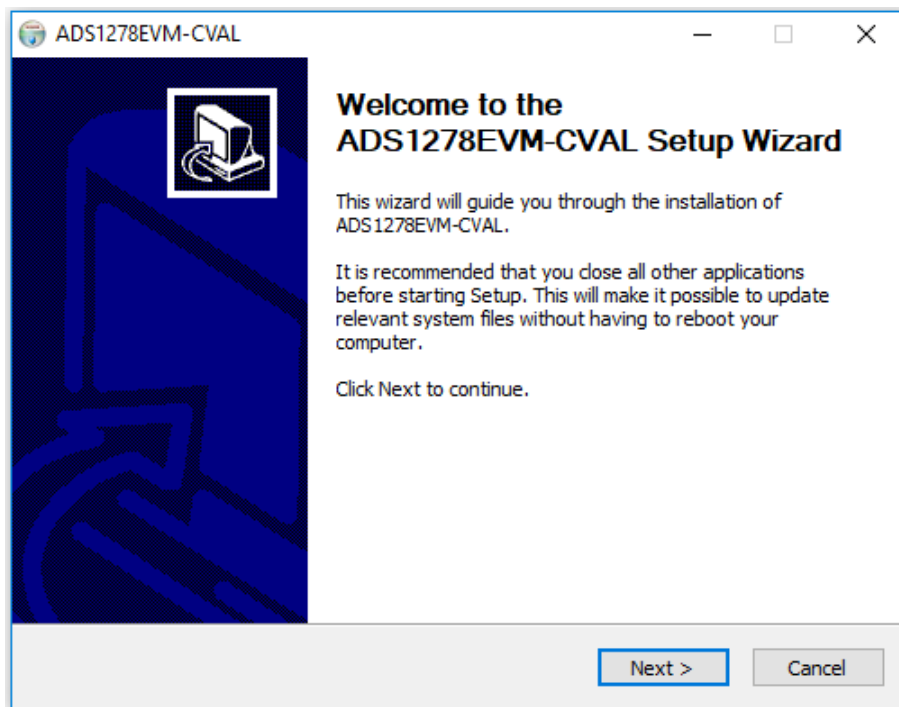


Figure 17.

4. Read the License Agreement and then click *I Agree*.

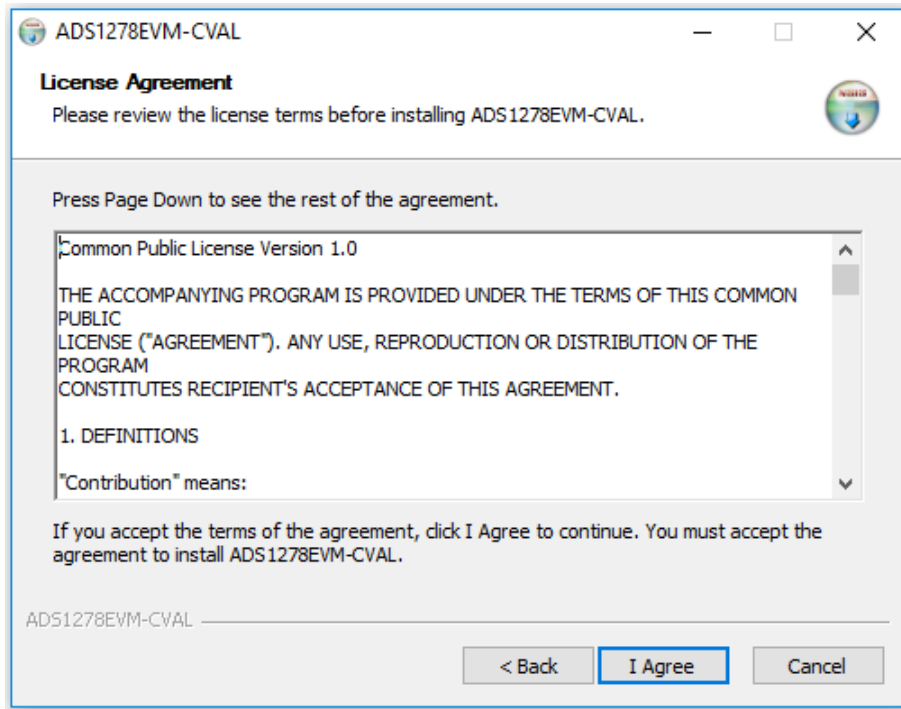


Figure 18.

5. 5. Click *Next*.

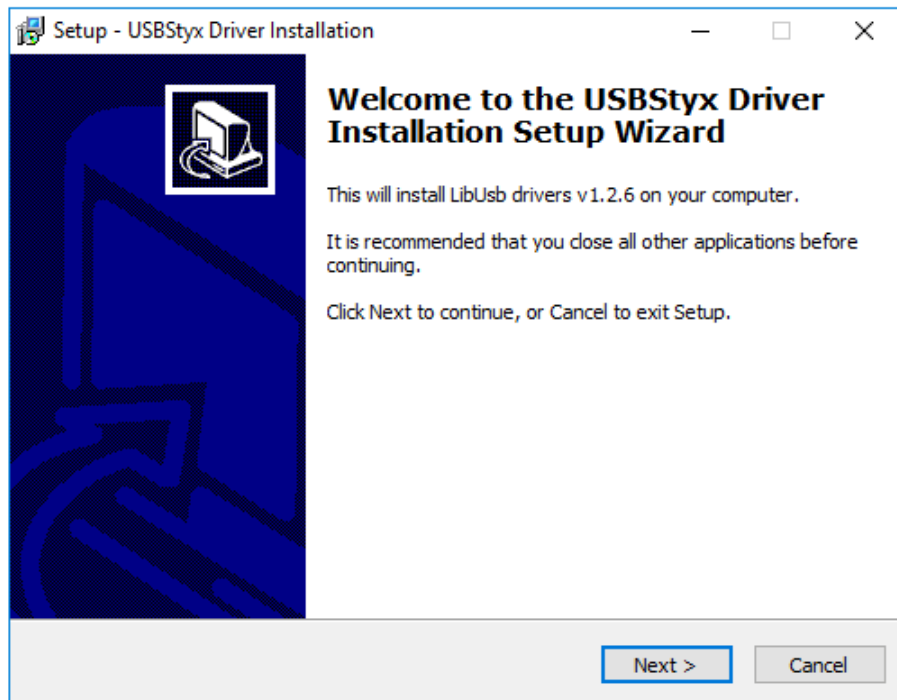


Figure 19.

6. Click *Install* to begin installation of USBStyx Driver.

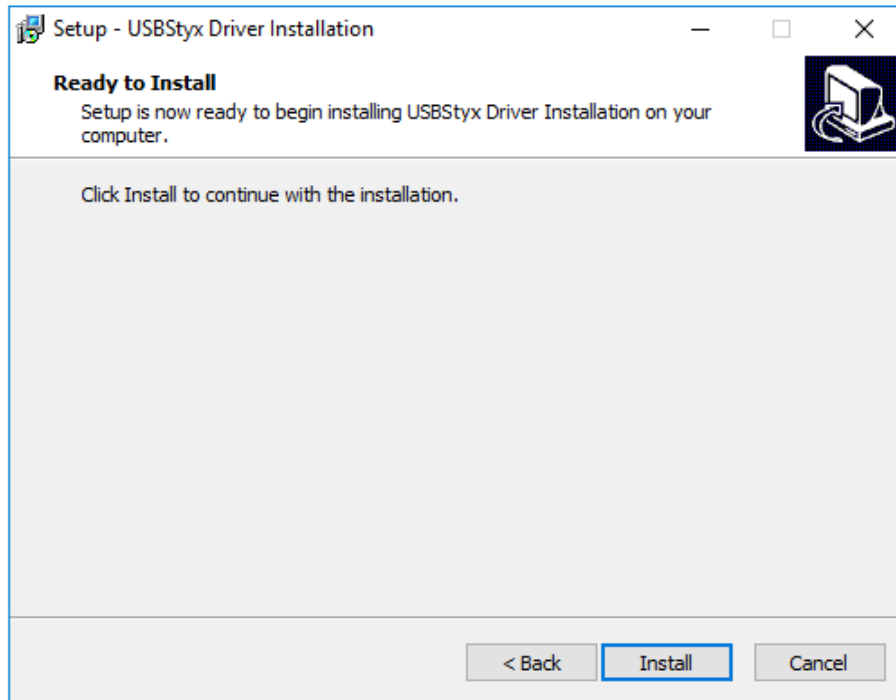


Figure 20.

7. Click *Finish*.

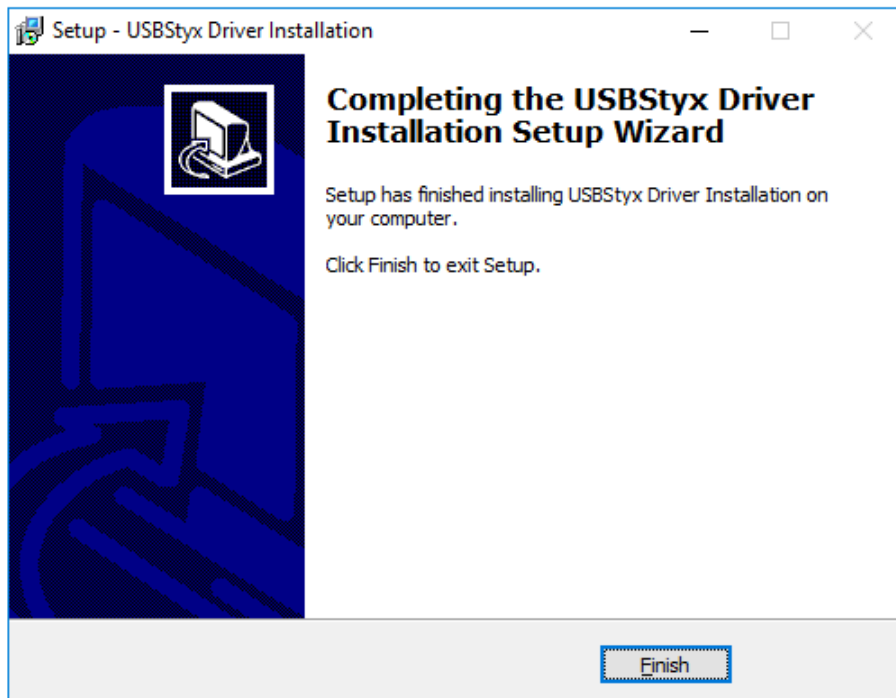


Figure 21.

8. Click *Finish*.

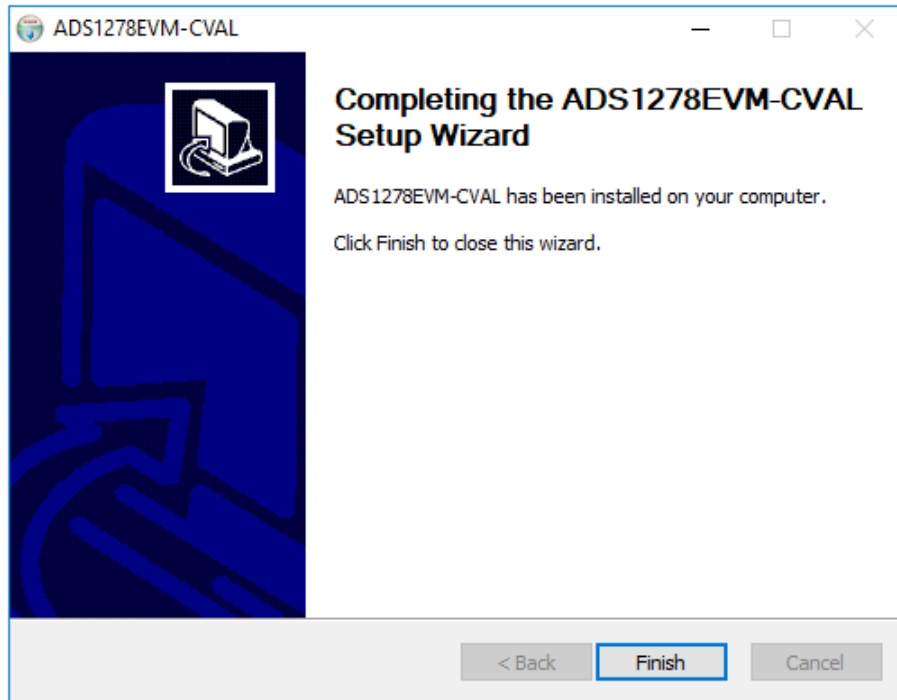


Figure 22.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated