Atmel SAM4SP32A

CORTEX-M4 PRIME SoC

PRELIMINARY DATASHEET

Features

- Core
  - ARM® Cortex™-M4 with a 2Kbytes cache running at 120MHz
  - Memory Protection Unit (MPU)
  - DSP Instruction Set
  - Thumb®-2 instruction set
- Memories
  - 2048 Kbytes embedded Flash with optional dual bank and cache memory
  - 160 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded boot loader routines (UART, USB) and IAP routines
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low-power 32.768 kHz for RTC or device clock
  - RTC with Gregorian and Persian Calendar mode, waveform generation in low power modes
  - RTC clock calibration circuitry for 32.768 kHz crystal frequency compensation
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
  - Slow Clock Internal RC oscillator as permanent low-power mode device clock
  - Two PLLs up to 240 MHz for device clock and for USB
  - Temperature Sensor
  - Up to 22 Peripheral DMA (PDC) Channels
- Low Power Modes
  - Sleep and Backup Modes, down to 1 µA in Backup Mode
  - Ultra low-power RTC
- Peripherals
  - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver
  - 2 USARTs with ISO7816, IrDA ®, RS-485, Manchester and Modem Mode
  - Two 2-wire UARTs
  - 2 Two Wire Interface (I2C compatible), 1 Synchronous Serial Controller (SSC)
  - 2 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter

- 32-bit Real-time Timer and RTC with calendar and alarm features
  - One Analog Comparator with flexible input selection
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Write Protected Registers
- I/O
  - Up to 38 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode
- PRIME PLC Modem
  - Power Line Carrier Modem for 50 and 60 Hz mains
  - 97-carrier OFDM PRIME compliant
  - Baud rate Selectable: 21400 to 128600 bps
  - Differential BPSK, QPSK, 8-PSK modulations
  - Automatic Gain Control and signal amplitude tracking
  - Embedded on-chip DMAs
  - Media Access Control
  - Viterbi decoding and CRC PRIME compliant
  - 128-bit AES encryption
  - Channel sensing and collision pre-detection
- Package
  - 128-Lead LQFP
  - Pb-free and RoHS compliant
- Typical Applications
  - PRIME Smart Meters
  - PRIME Data Concentrator

Description

The SAM4SP32A is a new evolution of SAM4SD32 Flash microcontroller based on the high performance 32-bit ARM Cortex-M4 RISC processor with a PRIME Power Line Communication Modem SoC integrated.

The SAM4SP32A operates at a maximum speed of 120 MHz and features with a 2048 Kbytes of Flash, with optional dual bank implementation and 2Kbytes of cache memory, 160 Kbytes of SRAM, and 32Kbytes embedded SRAM memory available for PRIME specification requirements.

The peripheral set mainly includes a Certified PRIME Power line communication transceiver with a featured Class D power amplifier and a set of hardware accelerators blocks to execute the heavy tasks of the PRIME protocol without the interruption of the Cortex-M4 CPU. Furthermore, the SAM4SP32A includes a Full Speed USB Device port with embedded transceiver, , 2x USARTs, 2x UARTs, 2x TWIs, an I2S, as well as 1 PWM timer, 2x three channel general-purpose 16-bit timers (with stepper motor and quadrature decoder logic support), an RTC, a Synchronous Serial Controller (SSC) and an analog comparator.

The Atmel SAM4SP32A SoC device combines robust and high performances PRIME PLC Modem with a powerfull Cortex-M4 microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM4SP32A to sustain a wide range of applications including PRIME Smart Grid and data concentrator solutions.

SAM4SP32A operates from 3.0V to 3.6V

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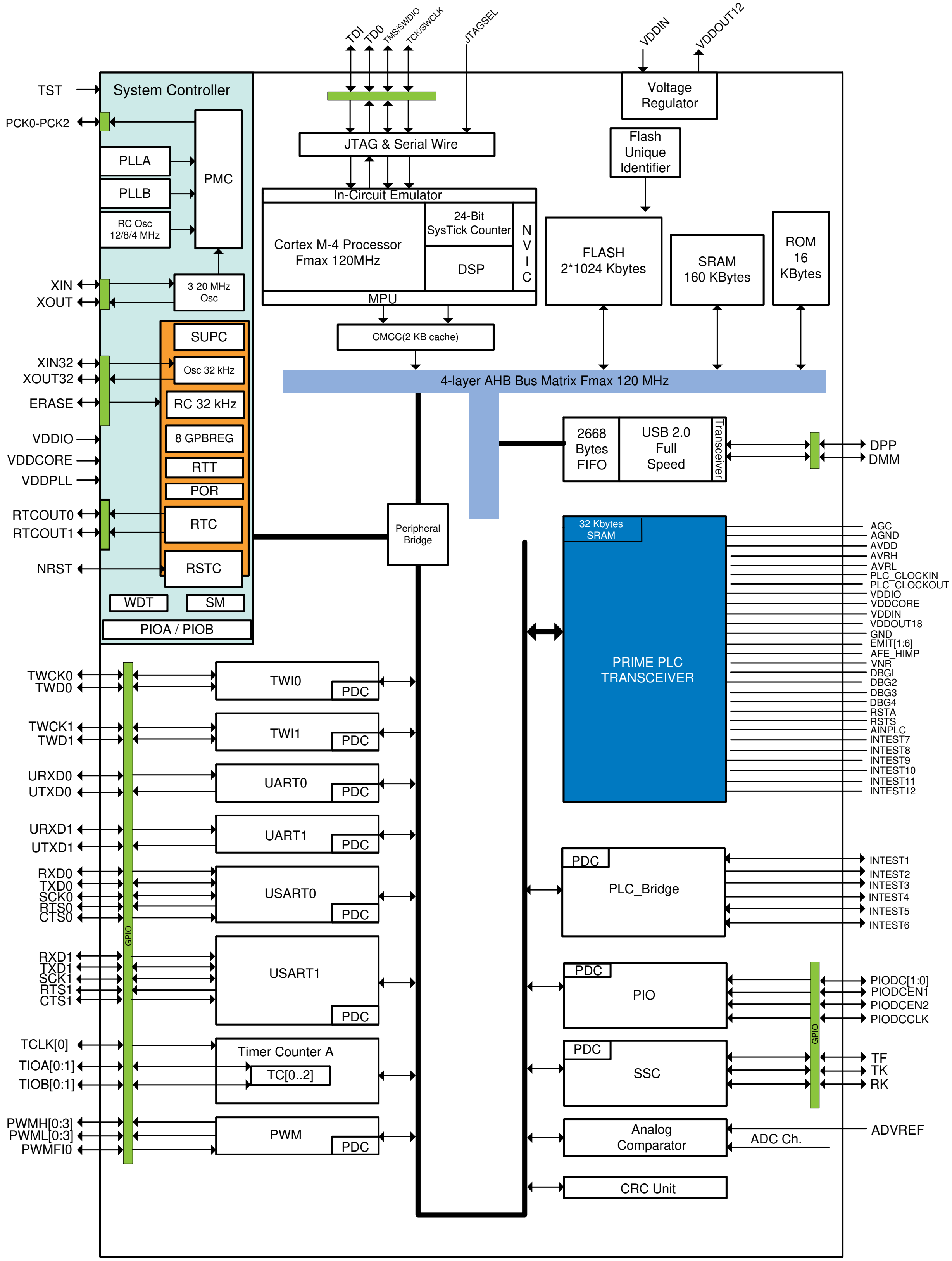
1. Block Diagram

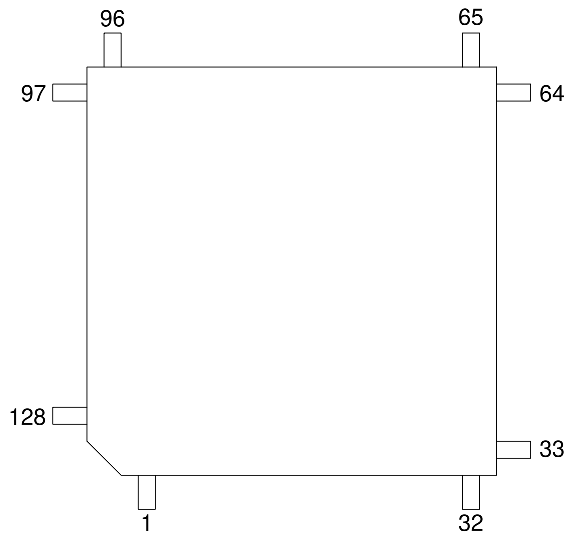
Figure 1-1. SAM4SP32A Block Diagram



2. Package and Pinout

2.1 128-Lead LQFP Package Outline

Figure 2-1. Orientation of the 128-Lead Package



2.2 128-Lead LQFP Pinout

Table 2-1. **SAM4SP32A 128-Lead LQFP pinout**

1	ADVREF	**33**	PC0	**65**	INTEST7	**97**	TDO/TRACESWO/ PB5
2	GND	**34**	GND	**66**	INTEST10	**98**	DBG0
3	GND	**35**	VDDIO	**67**	INTEST12	**99**	JTAGSEL
4	AGC	**36**	PA16/PGMD4	**68**	INTEST11	**100**	DBG1
5	GND	**37**	NC	**69**	TDI/PB4	**101**	DBG2
6	VDDIO	**38**	PA15/PGMD3	**70**	VDDIO	**102**	GND
7	AGND	**39**	INTEST1	**71**	PA6/PGMNOE	**103**	VDDIO
8	PB0	**40**	INTEST2	**72**	PA5/PGMRDY	**104**	DBG3
9	AVDD	**41**	PA24/PGMD12	**73**	PA4/PGMNCMD	**105**	TMS/SWDIO/PB6
10	PB1	**42**	PC5	**74**	GND	**106**	DBG4
11	AGND	**43**	NC	**75**	EMIT1	**107**	RSTA
12	AVDD	**44**	NC	**76**	VDDIO	**108**	RSTS
13	VRH	**45**	VDDCORE	**77**	NRST	**109**	TCK/SWCLK/PB7
14	PB2	**46**	GND	**78**	TST	**110**	GND
15	AINPLC	**47**	PA25/PGMD13	**79**	EMIT2	**111**	VDDOUT18
16	PB3	**48**	VDDOUT18	**80**	EMIT3	**112**	GND
17	VRL	**49**	NC	**81**	PA3	**113**	VDDCORE
18	VDDIN	**50**	INTEST3	**82**	EMIT4	**114**	VDDIN
19	VDDOUT12	**51**	INTEST4	**83**	PA2/PGMEN2	**115**	ERASE/PB12
20	PA17/PGMD5	**52**	INTEST5	**84**	GND	**116**	VDDIN
21	PC26	**53**	PA10/PGMM2	**85**	VDDIO	**117**	DDM/PB10
22	PA18/PGMD6	**54**	GND	**86**	EMIT5	**118**	DDP/PB11
23	PA21/PGMD9	**55**	PA9/PGMM1	**87**	VDDIO	**119**	VDDIO
24	VDDCORE	**56**	INTEST6	**88**	VDDIO	**120**	VDDIO
25	PA19/PGMD7	**57**	GND	**89**	NC	**121**	PLC_CLOCKIN
26	PA22/PGMD10	**58**	VDDIO	**90**	EMIT6	**122**	PB13/DAC0
27	PA23/PGMD11	**59**	PA8/XOUT32/ PGMM0	**91**	GND	**123**	PLC_CLOCKOUT
28	PA20/PGMD8	**60**	INTEST9	**92**	VDDIO	**124**	GND
29	GND	**61**	GND	**93**	AFE_HIMP	**125**	PB8/XOUT
30	VDDIO	**62**	PA7/XIN32/ PGMNVALID	**94**	PA1/PGMEN1	**126**	GND
31	NC	**63**	INTEST8	**95**	PA0/PGMEN0	**127**	PB9/PGMCK/XIN
32	NC	**64**	VDDIO	**96**	VNR	**128**	VDDPLL

3. Signal Description

Table 3-1. **Signal Description List**

<table>
<tr><th>Signal Name</th><th>Function</th><th>Type</th><th>Active Level</th><th>Voltage Reference</th><th>Comments</th></tr>
<tr><td colspan="6">Power Supplies</td></tr>
<tr><td>VDDIO</td><td>Peripherals I/O Lines and USB transceiver Power Supply</td><td>Power</td><td></td><td></td><td>3.0V to 3.6V</td></tr>
<tr><td>VDDIN</td><td>Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply</td><td>Power</td><td></td><td></td><td>3.0V to 3.6V</td></tr>
<tr><td>VDDCORE</td><td>Power the core, the embedded memories and the peripherals</td><td>Power</td><td></td><td></td><td>1.08V to 1.32V</td></tr>
<tr><td>VDDPLL</td><td>Oscillator and PLL Power Supply</td><td>Power</td><td></td><td></td><td>1.08V to 1.32V</td></tr>
<tr><td>VDDOUT18</td><td>LDO Output Power Supply</td><td>Power</td><td></td><td></td><td>1.8V Ouput</td></tr>
<tr><td>VDDOUT12</td><td>Voltage Regulator Output</td><td>Power</td><td></td><td></td><td>1.2V Output</td></tr>
<tr><td>AVDD</td><td>Analog Converter Power Supply</td><td>Power</td><td></td><td></td><td>3.0V to 3.6V</td></tr>
<tr><td>AGND</td><td>Analog Ground</td><td>Ground</td><td></td><td></td><td></td></tr>
<tr><td>GND</td><td>Digital Ground</td><td>Ground</td><td></td><td></td><td></td></tr>
<tr><td colspan="6">Clocks, Oscillators and PLLs</td></tr>
<tr><td>XIN</td><td>Main Oscillator Input</td><td>Input</td><td></td><td rowspan="5">VDDIO</td><td rowspan="4">Reset State:
-PIO Input
-Internal Pull-up disabled
-Schmitt Trigger enabled[1]</td></tr>
<tr><td>XOUT</td><td>Main Oscillator Output</td><td>Output</td><td></td></tr>
<tr><td>XIN32</td><td>Slow Clock Oscillator Input</td><td>Input</td><td></td></tr>
<tr><td>XOUT32</td><td>Slow Clock Oscillator Output</td><td>Output</td><td></td></tr>
<tr><td>PCK0 - PCK2</td><td>Programmable Clock Output</td><td>Output</td><td></td><td>Reset State:
-PIO Input
-Internal Pull-up enabled
-Schmitt Trigger enabled[1]</td></tr>
<tr><td>PLC_CLOCKIN</td><td>External clock Input reference</td><td>Input</td><td></td><td></td><td></td></tr>
<tr><td>PLC_CLOCKOUT</td><td>External clock Output reference</td><td>Output</td><td></td><td></td><td></td></tr>
<tr><td colspan="6">Analog Input Voltage Reference</td></tr>
<tr><td>AINPLC</td><td>Direct-analog input voltage</td><td>Analog</td><td></td><td></td><td></td></tr>
<tr><td>AVRH</td><td>Analog input high voltage reference</td><td>Analog</td><td></td><td></td><td></td></tr>
<tr><td>AVRL</td><td>Analog input low voltage reference</td><td>Analog</td><td></td><td></td><td></td></tr>
<tr><td>ADVERF</td><td>Analog Comparator Reference</td><td>Analog</td><td></td><td></td><td></td></tr>
</table>

Table 3-1. **Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Real Time Clock					
RTCOUT0	Programmable RTC waveform output	Output		VDDIO	Reset State: -PIO Input -Internal Pull-up disabled -Schmitt Trigger enabled[1]
RTCOUT1	Programmable RTC waveform output	Output			
Serial Wire/JTAG Debug Port - SWJ-DP					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled[1]
TDI	Test Data In	Input			
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input/ I/O			
JTAGSEL	JTAG Selection	Input	High		Permanent Internal pull-down
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled[1]
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Input			Permanent Internal pull-down
PRIME PLC TRANSCEIVER Signal Controller					
AGC	Automatic Gain Control	Output			
EMITx	PLC Transmission ports	Output			See footnote [2]
VNR	PLC Zero Crossing Detection Signal	Input			
AFE_HIMP	Analog Front-End High-Impedance	Output			
RSTA	PLC Asynchronous reset	Input			Internal configuration: 33kΩ typ. pull-down resistor
RSTS	Initialization Signal	Input			

Table 3-1. **Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PRIME PLC TRANSCEIVER Configuration Pins					
DBGx	External Configuration Pins	I/O			See Pin Description for details
INTEST7 – INTEST12	External Configuration Pins	I/O			
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs[2] - Internal pull-up enabled - Schmitt Trigger enabled[1]
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
Synchronous Serial Controller - SSC					
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			Only output in complementary mode when dead time insertion is enabled.
PWMFI0	PWM Fault Input	Input			

Table 3-1. **Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PLC Brigde					
INTEST1 – INTEST6	External Configuration pins	I/O			
Two-Wire Interface- TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog Comparator - ACC					
AC0 - AC7	Analog Comparator Inputs	Analog			
USB Full Speed Device					
DMM	USB Full Speed Data -	Analog, Digital		VDDIO	Reset State: - USB Mode - Internal Pull-down[3]
DPP	USB Full Speed Data +				

Note:

1. Schmitt Triggers can be disabled through PIO registers.
2. Different configurations allowed depending on external topology and net behavior.
3. Refer to USB Section of the product Electrical Characteristics for information on Pull-down value in USB Mode.

4. Pin Description

Table 4-1. **Pin Description List**

Pin Number	Pin Name	Functions	Type	Comments
1	ADVREF		Analog	Analog Voltage Comparator reference
2, 3, 5, 29, 34, 46, 54, 57, 61, 74, 84, 91, 102, 110, 112, 124, 126	GND		Power	Digital Ground
4	AGC		Output	Automatic Gain Control • This digital output is managed by AGC hardware logic to drive external circuitry if input signal attenuation is needed
6, 30, 58, 64, 70, 76, 85, 88, 87, 92, 103, 119, 120,	VDDIO		Power	Digital power supply. Voltage range: 3.0V - 3.6 V Must be decoupled by external capacitors
7, 11	AGND		Power	Analog ground
8	PB0	PWMH0 AC4 RTCOUT0	I/O	PIO Controller B Multiplexing (PB0): • PWM Waveform Output High for channel 0 • Analog Comparator Input channel 4 • Programmable RTC waveform output • See Signal Description for details.
9, 12	AVDD		Power	Analog converter power supply. Voltage range: 3.0V - 3.6 V
10	PB1	PWMH1 AC5 RTCOUT1	I/O	PIO Controller B Multiplexing (PB1): • PWM Waveform Output High for channel 1 • Analog Comparator Input channel 5 • Programmable RTC waveform output • See Signal Description for details.
13	AVRH		Input	Analog input high voltage reference

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments

14	PB2	URXD1
		AC6
		WKUP12
			I/O	PIO Controller B Multiplexing (PB2):
				• UART1 Receive Input Data
				• Analog Comparator Input channel 6
				• Wake-up Source 12
				  • Fast start up of the Processor
				  • Active level: Low

15	AINPLC		Input	Direct-analog input voltage
16	PB3	UTXD1 PCK2 AC7	I/O	PIO Controller B Multiplexing (PB3): • UART1 Transmit Output Data • Programmable clock output 2 • Analog Comparator Input channel 7 • See Signal Description for details.
17	AVRL		Input	Analog input low voltage reference
18, 35, 114, 116	VDDIN		P	Voltage Regulator Input, Analog Comparator Power Supply. Voltage range: 3.0V – 3.6 V
19	VDDOUT12		P	Voltage output regulator of 1.2 volts
20	PA17/PGMD5	TD PCK1 PWMH3 AC0	I/O	PIO Controller A Multiplexing (PA17): • Synchronous Serial Controller (SSC) Transmit Output Data • Programmable clock output 1 • PWM Waveform Output High for channel 3 • Analog Comparator Input channel 0 • See Signal Description for details.
21	PC26	TIOA4	I/O	PIO Controller C Multiplexing (PC26): • Tmer/Counter Channel 4 I/O Line A • General purpose I/O
22	PA18/PGMD6	RD PCK2 AC1	I/O	PIO Controller A Multiplexing (PA18): • Synchronous Serial Controller (SSC) Receive Input Data • Programmable clock output 2 • Analog Comparator Input channel 1 • See Signal Description for details.

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
23	PA21/PGMD9	RXD1 PCK1	I/O	PIO Controller A Multiplexing (PA21): • USART1 Receive Input Data • Programmable clock output 1 • See Signal Description for details.
24, 45, 113	VDDCORE		P	Core, embedded memories and the peripherals power supply: Voltage range of 1.08V to 1.32V

25	PA19/PGMD7	RK
		PWML0
		AC2WKUP
		9
			I/O	PIO Controller A Multiplexing (PA19):
				• Synchronous Serial Controller (SSC) I/O Receive Clock
				• PWM Waveform Output Low for channel 0
				• Analog Comparator Input channel 2
				• Wake-up Source 9
				  ◦ Fast start up of the Processor
				  ◦ Active level: Low

26	PA22/PGMD10	TXD1	I/O	PIO Controller A Multiplexing (PA22): • USART1 Transmit I/O Data
27	PA23/PGMD11	SCK1 PWMH0 PIODCLLK	I/O	PIO Controller A Multiplexing (PA23): • USART1 I/O Serial Clock • PWM Waveform Output High for channel 0 • Parallel Capture Mode Input Clock ◦ Voltage reference: VDDIO

28	PA20/PGMD8	RF
		PWML1
		AC3
		WKUP10
			I/O	PIO Controller A Multiplexing (PA20):
				• Synchronous Serial Controller (SSC) I/O Receive Frame Sync
				• PWM Waveform Output Low for channel 1
				• Analog Comparator Input channel 3
				• Wake-up Source 10
				  ◦ Fast start up of the Processor
				  ◦ Active level: Low

31, 32, 37, 43, 44,	NC		-	No connect

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
33	PC0	PWML0	I/O	PIO Controller C Multiplexing (PC0): • PWM Waveform Output Low for channel 0 • General purpose I/O

36	PA16/PGMD4	TK
		TIOB1
		PWML2
		WKUP15
		PIODCEN2
			I/O	PIO Controller A Multiplexing (PA16):
				• Synchronous Serial Controller (SSC) I/O Transmit Clock
				• Timer/Counter (TC) Channel 1 I/O Line B
				• PWM Waveform Output Low for channel 2
				• Wake-up Source 15
				  • Fast start up of the Processor
				  • Active level: Low
				• PIO Controller - Parallel Capture Mode Enable 2
				  • Voltage reference: VDDIO

38	PA15/PGMD3	TF
		TIOA1
		PWML3
		WKUP14
		PIODCEN1
			I/O	PIO Controller A Multiplexing (PA15):
				• Synchronous Serial Controller (SSC) I/O Transmit Frame Sync
				• Timer/Counter (TC) Channel 1 I/O Line A
				• PWM Waveform Output Low for channel 3
				• Wake-up Source 14
				  • Fast start up of the Processor
				  • Active level: Low
				• PIO Controller - Parallel Capture Mode Enable 1
				  • Voltage reference: VDDIO

39	INTEST1		O	External configuration pin. This pin must connect to INTEST7 (pin 65)
40	INTEST2		O	External configuration pin. This pin must connect to INTEST8 (pin 63)
41	PA24/PGMD12	RTS1 PWMH1 PIODC0	I/O	PIO Controller A Multiplexing (PA24): • USART1 Request To Send • PWM Waveform Output High for channel 1 • PIO Controller-Parallel Capture Mode Data 0

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
42	PC5		I/O	PIO Controller C Multiplexing (PC5): • General purpose I/O
47	PA25/PGMD13	CTS1 PWMH2 PIODC1	I/O	PIO Controller A Multiplexing (PA25): • USART1 Clear To Send • PWM Waveform Output High for channel 2 • PIO Controller-Parallel Capture Mode Data 1
48, 111	VDDOUT18		Power	1.8V LDO Output Power Supply. Just Requires output capacitor. Not intended for external use
50	INTEST3		O	External configuration pin. This pin must connect to INTEST9 (pin 60)
51	INTEST4		O	External configuration pin. This pin must connect to INTEST10 (pin 66)
52	INTEST5		O	External configuration pin. This pin must connect to INTEST11 (pin 68)
53	PA10/PGMM2	UTXD0	I/O	PIO Controller A Multiplexing (PA10): • UART Transmit Output Data •

55	PA9/PGMM1	URXD0
		PWMFI0
		WKUP6
			I/O	PIO Controller A Multiplexing (PA9):
				• UART Receive Input Data
				• PWM Fault Input
				• Wake-up Source 6
				  • Fast start up of the Processor
				  • Active level: Low

56	INTEST6		O	External configuration pin. This pin must connect to INTEST12 (pin 67)

59	PA8/ XOUT32/PGMM0	CTS0
		WKUP5
		XOUT32
			I/O	PIO Controller A Multiplexing (PA8):
				• USART0 Clear To Send
				• Wake-up Source 5
				  • Fast start up of the Processor
				  • Active level: Low
				• Slow Clock Oscillator Output
				• See Signal Description for details.

60	INTEST9		I	External configuration pin. This pin must connect to INTEST3 (pin 50)

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
62	PA7/ XIN32/PGMNVALID	RTS0 PWMH3 XIN32	I/O	PIO Controller A Multiplexing (PA7): • USART0 Request To Send • PWM Waveform Output High for channel 3 • Slow Clock Oscillator Input • See Signal Description for details.
63	INTEST8		I	External configuration pin. This pin must connect to INTEST2 (pin 40)
65	INTEST7		I	External configuration pin. This pin must connect to INTEST1 (pin 39)
66	INTEST10		I	External configuration pin. This pin must connect to INTEST4 (pin 51)
67	INTEST12		I	External configuration pin. This pin must connect to INTEST6 (pin 56)
68	INTEST11		I	External configuration pin. This pin must connect to INTEST5 (pin 52)
69	TDI/PB4	TWD1 PWMH2 TDI	I/O	PIO Controller B Multiplexing (PB4): • Two-Wire Interface – TWI1 Two-wire I/O Serial Data • PWM Waveform Output High for channel 2 • Serial Wire/JTAG Debug Port (SWJ-DP) Test Data In • See Signal Description for details.
71	PA6/PGMNOE	TXD0 PCK0	I/O	PIO Controller A Multiplexing (PA6): • USART0 Transmit I/O Data • Programmable Clock Output • See Signal Description for details.

72	PA5/PGMRY	RXD0
		WKUP4
			I/O	PIO Controller A Multiplexing (PA5):
				• USART0 Receive Input Data
				• Wake-up Source 4
				  ◦ Fast start up of the Processor
				  ◦ Active level: Low

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
73	PA4/PGMNCMD	TWCK0 TCLK0 WKUP3	I/O	PIO Controller A Multiplexing (PA4): • Two-Wire Interface-TWI0 Two-wire I/O Serial Clock • Timer/Counter (TC) Channel 0 External Clock Input • Wake-up Source 3 ◦ Fast start up of the Processor ◦ Active level: Low
75, 79, 80, 82, 86, 90,	EMIT(1:6)		Output	PLC Transmission ports. • See Signal Description for details.
77	NRST		I/O	Synchronous PRIME PLC Reset • See Signal Description for details.
78	TST		I	Test Select • See Signal Description for details.
81	PA3	TWD0	I/O	PIO Controller A Multiplexing (PA3): • Two-Wire Interface - TWI0 Two-wire I/O Serial Data
83	PA2/PGMEN2	PWMH2 SCK0 WKUP2	I/O	PIO Controller A Multiplexing (PA2): • PWM Waveform Output High for channel 2 • USART0 I/O Serial Clock • Wake-up Source 2 ◦ Fast start up of the Processor ◦ Active level: Low

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
93	AFE_HIMP		Output	Analog Front-End High-Impedance • This digital output is used by the chip to select between low-impedance and high-impedance transmission branch (when working with a “two half-H-bridge branches” analog front end configuration). This way, the system adapts its transmission external circuitry to the net impedance, improving transmission behavior. The polarity of this pin can be inverted by hardware. Please refer to the Reference Design for further information.

94	PA1/PGMEN1	PWMH1
		TIOB0
		WKUP1
			I/O	PIO Controller A Multiplexing (PA1):
				• PWM Waveform Output High for channel 1
				• Timer/Counter (TC) Channel 0 I/O Line B
				• Wake-up Source 1
				  ◦ Fast start up of the Processor
				  ◦ Active level: Low

95	PA0/PGMEN0	PWMH0
		TIOA0
		WKUP0
			I/O	PIO Controller A Multiplexing (PA0):
				• PWM Waveform Output High for channel 0
				• Timer/Counter (TC) Channel 0 I/O Line A
				• Wake-up Source 0
				  ◦ Fast start up of the Processor
				  ◦ Active level: Low

96	VNR		Input	PLC Zero Crossing Detection Signal • This input detects the zero-crossing of the mains voltage, needed to determine proper switching times. Depending on whether an isolated or a non-isolated power supply is being used, isolation of this pin should be taken into account in the circuitry design. Please refer to the Reference Design for further information.

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments

97	TDO/ TRACESWO/PB5	TWCK1
		PWML0
		WKUP13
		TDO
		TRACESWO
			I/O	PIO Controller B Multiplexing (PB5):
				• Two-Wire Interface **-** TWI1 Two-wire I/O Serial Clock
				• PWM Waveform Output Low for channel 0
				• Wake-up Source 13
				  • Fast start up of the Processor
				  • Active level: Low
				• TDO - Test Data Out / Trace Asynchronous DataOut (TRACESWO)
				• See Signal Description for details.

98	DBG0		Input	Internal configuration: must connect 33kΩ typ. pull-up resistor
99	JTAGSEL		A-I	Analog input used to select the JTAG boundary scan when asserted at a high level. • See Signal Description for details.
100	DBG1		Input	Internal configuration: must 33kΩ typ. pull-up resistor
101	DBG2		Output	No connect
104	DBG3		Input	Internal configuration: must 33kΩ typ. pull-up resistor
105	TMS/ SWDIO/PB6	TMS SWDIO	I/O	PIO Controller B Multiplexing (PB6): • TMS - Test Mode Input Select / (SWDIO) Serial Wire I/O • See Signal Description for details.
106	DBG4		Input	No connect
107	RSTA		Input	PLC Asynchronous reset • RSTA is a digital input pin used to perform a hardware reset of the ASIC • RSTA is active high

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
108	RSTS		Input	Initialization Signal • During power-on, D_INIT should be released before asynchronous reset signal RSTA, in order to ensure proper system start up. Not minimum time is required between both releases, $\Delta t > 0$ • D_INIT is active high
109	TCK/SWCLK/ PB7	TCK SWCLK	I/O	PIO Controller B Multiplexing (PB7): • TCK -Test Clock/(SWCLK) Serial Wire Clock • See Signal Description for details.
115	ERASE/PB12	PWML1 ERASE	I/O	PIO Controller B Multiplexing (PB12): • PWM Waveform Output Low for channel 0 • Flash and NVM Configuration Bits Erase Command • See Signal Description for details.
117	DDM/PB10	DMM	A-I/O	PIO Controller B Multiplexing (PB10): • USB Full Speed Data – • See Signal Description for details.
118	DDP/PB11	DPP	A-I/O	PIO Controller B Multiplexing (PB11): • USB Full Speed Data + • See Signal Description for details.
121	PLC_CLOCKIN		Input	External clock reference • PLC_CLOCKIN must be connected to one terminal of a crystal (when a crystal is being used) or tied to ground if a compatible oscillator is being used

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments
123	PLC_CLOCKOUT		I/O	External clock reference • PLC_CLOCKOUT must be connected to one terminal of a crystal (when a crystal is being used) or to one terminal of a compatible oscillator (when a compatible oscillator is being used)
125	PB8/XOUT	XOUT	Output	PIO Controller B Multiplexing (PB8): • Main Oscilator Output
127	PB9/PGMCK/XIN	XIN	Input	PIO Controller B Multiplexing (PB9): • Main Oscilator Input
128	VDDPLL		Power	Oscillator and PLL Power Supply • 1.08V to 1.32V

5. Power Considerations

5.1 Power Supplies

The SAM4SP32A has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals. Voltage ranges from 1.08V to 1.32V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers), USB transceiver, Backup part, 32 kHz crystal oscillator and oscillator pads. Voltage ranges from 3.0V to 3.6V.
- VDDIN pin: Voltage Regulator Input, and Analog Comparator Power Supply. Voltage ranges from 3.0V to 3.6V.
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator. Voltage ranges from 1.08V to 1.32V.
- AVDD pin: PRIME PLC Analog Converter Power Supply. Voltage ranges from 3.0V to 3.6V.

5.2 Voltage Regulator

The SAM4SP32A embeds two voltage regulators that are managed by the Supply Controller.

The first internal regulator is designed to supply the internal core of SAM4SP32A It features two operating modes:

- In Normal mode, the voltage regulator consumes less than 500 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 5 µA.
- In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT12) is driven internally to GND. The default output voltage is 1.20V and the start-up time to reach Normal mode is less than 300 µs.

The second internal regulator is designed to supply the internal PRIME PLC Transceiver. Its output (VDDOUT18) is driven internally to GND and the default output voltage is 1.8V. The VDDOUT18 pin just requires an output capacitor in the range of 0.1µF-10µF and it is not intended for external use.

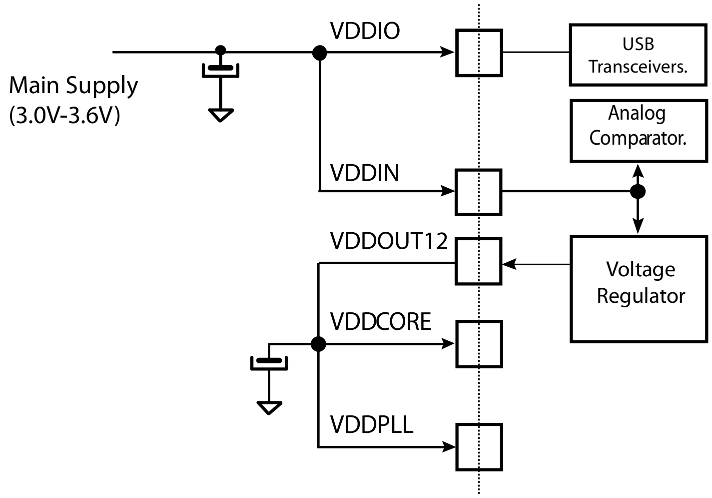
For adequate input and output power supply decoupling/bypassing, refer to the “Voltage Regulator” section in the “Electrical Characteristics” section of the datasheet.

5.3 Typical Powering Schematics

The SAM4SP32A supports a 3.0V-3.6V single supply mode. The internal regulator input is connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

As VDDIN powers the voltage regulator, and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that this is different from Backup mode).

Figure 5-1. Single Supply



Note: Restrictions

For USB, VDDIO needs to be greater than 3.0V.

Figure 5-2. Core Externally Supplied

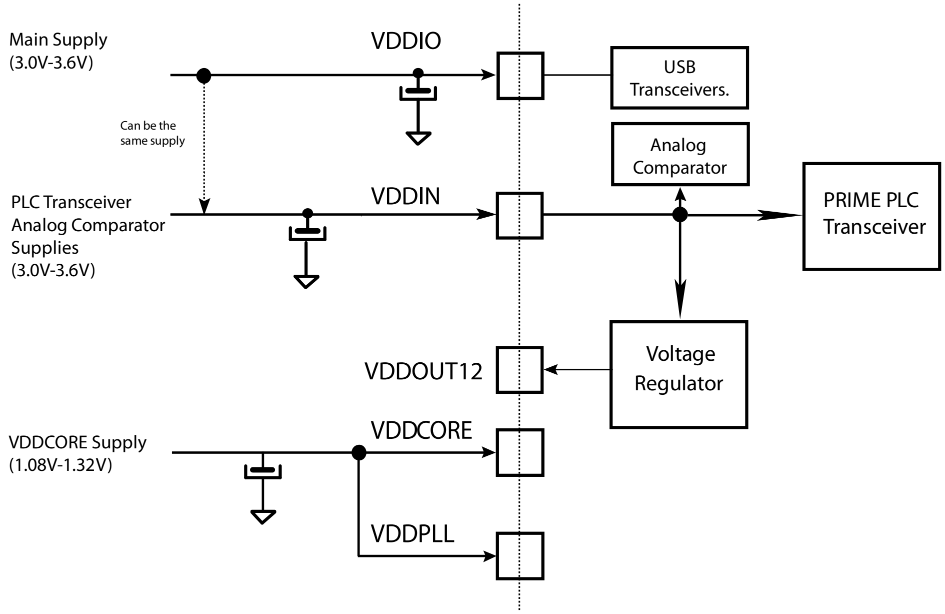
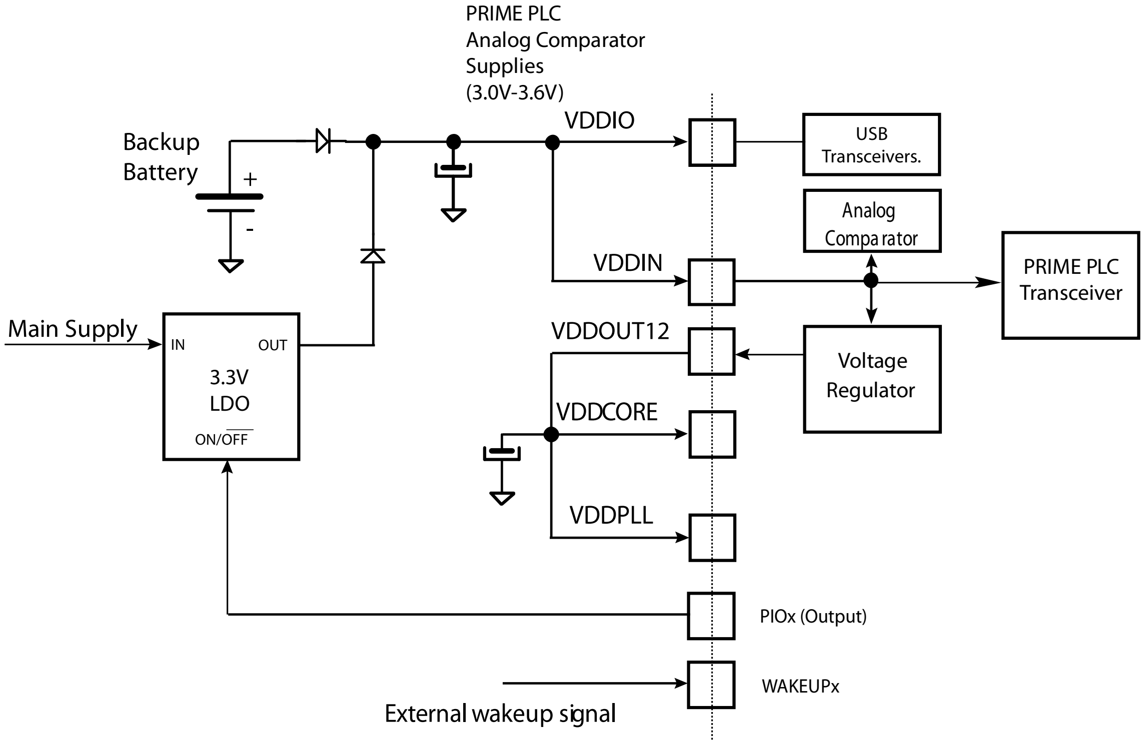


Figure 5-3. Backup Baterry



Note: The two diodes provide a "switchover circuit" (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low-power Modes

In low-power mode, the 3.3 Volts power source must be shut down before running in any low-power mode. The PRIME PLC transceiver peripheral is turned off during a low-power mode configuration.The various low-power modes of the SAM4SP32A are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulators, PRIME PLC transceiver and the core supply are off.

Backup mode is based on the Cortex-M4 deep sleep mode with the voltage regulators disabled.

The SAM4SP32A can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using bit VROFF of Supply Controller (SUPC_CR) and with the SLEEPDEEP bit in the Cortex-M4 System Control Register set to 1.

Entering Backup mode:

- Set the SLEEPDEEP bit of Cortex_M4, set to 1.
- Set the VROFF bit of SUPC_CR at 1

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than few hundred μs. Current Consumption in Wait mode is typically few μA (total current consumption) if the internal voltage regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered except for the PRIME PLC transceiver which remains turned off. From this mode, a fast start up is available.

This mode is entered via WAITMODE =1 (Waitmode bit in CKGR_MOR) and with LPM = 1 (Low Power Mode bit in PMC_FSMR) and with FLPM = 00 or FLPM=01 (Flash Low Power Mode bits in PMC_FSMR).

The Cortex-M4 is able to handle external events or internal events in order to wake-up the core. This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to 0). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU.

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Set the FLPM bitfield in the PMC Fast Startup Mode Register (PMC_FSMR)
- Set Flash Wait State at 0
- Set the WAITMODE bit = 1 in PMC Main Oscillator Register (CKGR_MOR)
- Wait for Master Clock Ready MCKRDY=1 in the PMC Status Register (PMC_SR)

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute unde-sired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) with LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if WFI instruction of the Cortex M4 is used.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low-power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1shows a summary of the configurations of the low-power modes.

Table 5-1. **Low Power Mode Configuration Summary**

Mode	SUPC, 32 kHz Oscillator, RTC, RTT Backup Registers, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption [(2) (3)]	Wake-up Time[(1)]
Backup Mode	ON	OFF	OFF (Not powered)	VROFF = 1 +SLEEPDEEP bit = 1	WUP0-15 pins SM alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	1.5 µA typ[(4)]	< 0.5 ms
Wait Mode	ON	ON	Powered (Not clocked)	Waitmode=1 +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	15 µA/ 25 µA [(5)]	< 10 µs
Sleep Mode	ON	ON	Powered[(1)] (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode =WFI Interrupt Only; Any Enabled Interrupt	Clocked back	Previous state saved	Unchanged	[(6)]	[(6)]

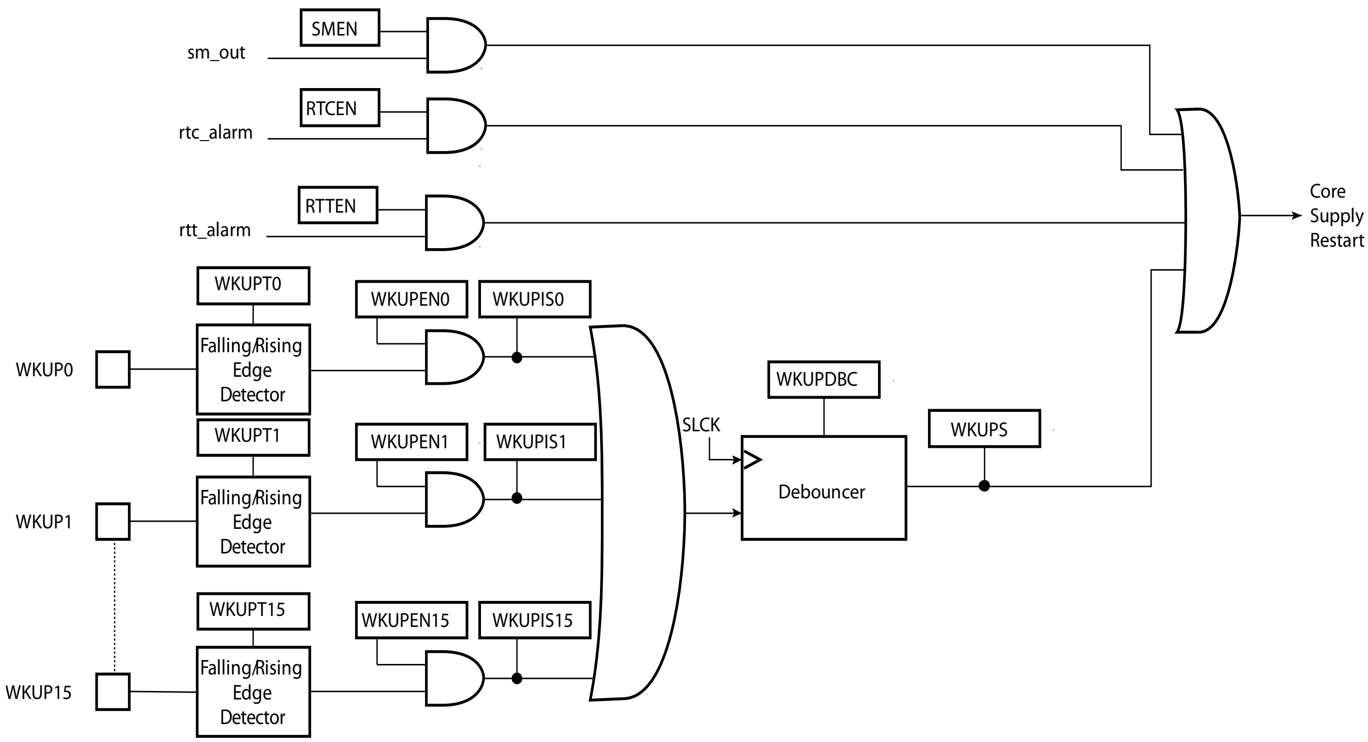
Note:

1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. Supply Monitor current consumption is not included.
4. Total Current consumption.
5. 15 µA on VDDCORE, 25 µA for total current consumption (using internal voltage regulator), 18 µA for total current consump-tion (without using internal voltage regulator).
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically re-enables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Sources

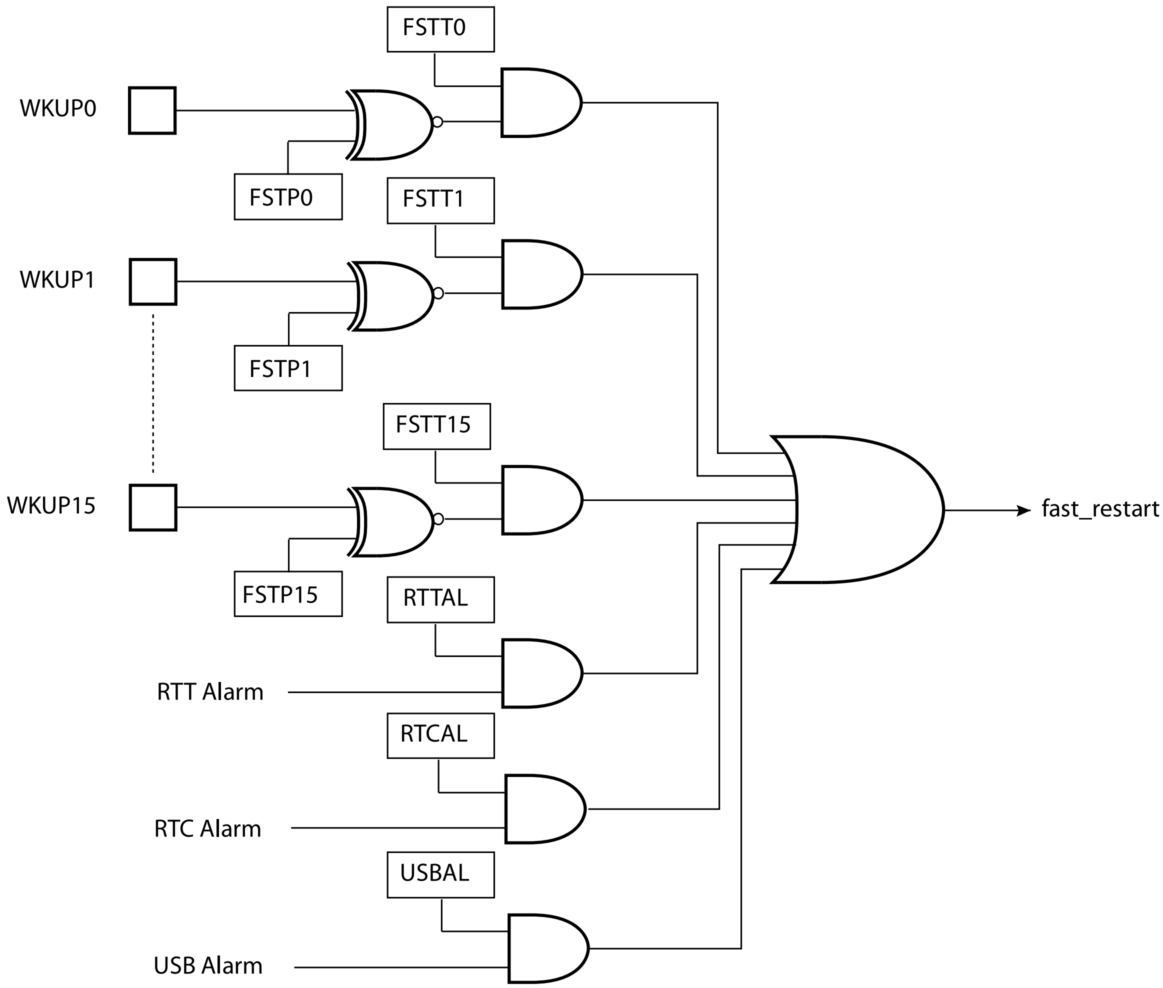


5.7 Fast Startup

The SAM4SP32A allows the processor to restart in a few microseconds while the processor is in wait mode or in sleep mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz Fast RC oscillator, switches the master clock on this 4 MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6. Input/Output Lines

The SAM4SP32A has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

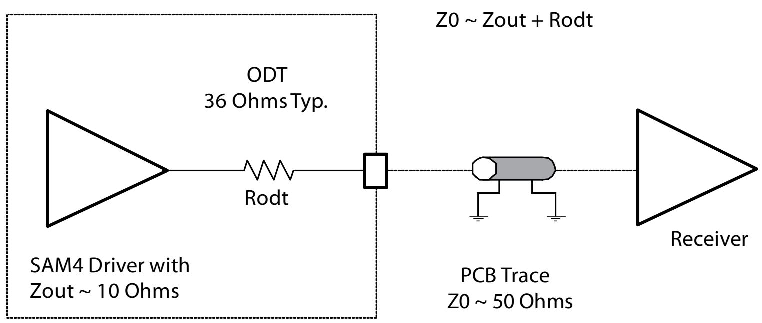
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product “PIO Controller” section.

The input/output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM4SP32A embeds high speed pads able to handle up to 45 MHz for PLC bridge clock lines and 35 MHz on other lines. See AC Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1 below). It consists of an internal series resistor termination scheme for impedance matching between the out-put (SAM4SP32A) driver and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset, JTAG, and the like. Described below in Table 6-1 are the SAM4SP32A system I/O lines shared with PIO lines.

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

Table 6-1. **System I/O Configuration Pin List**

SYSTEM_IO bit number	Default function after reset	Other Functions	Constraints for normal start	Configuration
12	ERASE	PB12	Low level at startup(1)	In Matrix User Interface Registers (Refer to the System I/O Configuration Register in the “Bus Matrix” section of the datasheet.)
10	DMM	PB10	-	
11	DPP	PB11	-	
7	TCK/SWCLK	PB7	-	
6	TMS/SWDIO	PB6	-	
5	TDO/TRACEESWO	PB5	-	
4	TDI	PB4	-	
-	PA7	XIN32	-	See footnote (2) below
-	PA8	XOUT32	-	
-	PB9	XIN	-	See footnote (3) below
-	PB8	XOUT	-	

Note:

1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode,
2. In the product Datasheet Refer to: “Slow Clock Generator” of the “Supply Controller” section.
3. In the product Datasheet Refer to: “3 to 20 MHZ Crystal Oscillator” information in the “PMC” section

6.2.2 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage refer-ence and reset state, refer to Table 3-1.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the “Debug and Test” Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchro-nous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the “Debug and Test” Section.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM4SP32A series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ. By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Refer to Peripheral Signal Multiplexing on I/O Lines Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M4 Processor

- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB Bridge

The SAM4SP32A embeds One Peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Master

The Bus Matrix of the SAM4SP32A manages 4 masters, which means that each master shall perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. **List of Bus Matrix Masters**

Master 0	Cortex-M4 Instruction/Data
Master 1	Cortex-M4 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	CRC Calculation Unit

7.4 Matrix Slaves

The Bus Matrix of the SAM4SP32A manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. **List of Bus Matrix Slaves**

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	External Bus Interface
Slave 4	Peripheral Bridge

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the Cortex-43 S Bus to the Internal ROM. Thus, these paths are forbidden or simply not wired, and shown as "-" in the following table.

Table 7-3. **SAM4SP32A Master to Slave Access**

Slaves	Masters	0	1	2	3
		Cortex-M4 I/D Bus	Cortex-M4 S Bus	PDC	CRCCU
0	Internal SRAM	-	X	X	X
1	Internal ROM	X	-	X	X
2	Internal Flash	X	-	-	X
3	External Bus Interface	-	X	X	X
4	Peripherical Bridge	-	X	X	-

7.6 Peripherical DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-4. **Peripherical DMA Controller**

Instance name	Channel T/R
PWM	Transmit
TWI1	Transmit
TWI0	Transmit
UART1	Transmit
UART0	Transmit
USART1	Transmit
USART0	Transmit
PLC bridge	Transmit
SSC	Transmit

Table 7-5. **Peripherical DMA Controller**

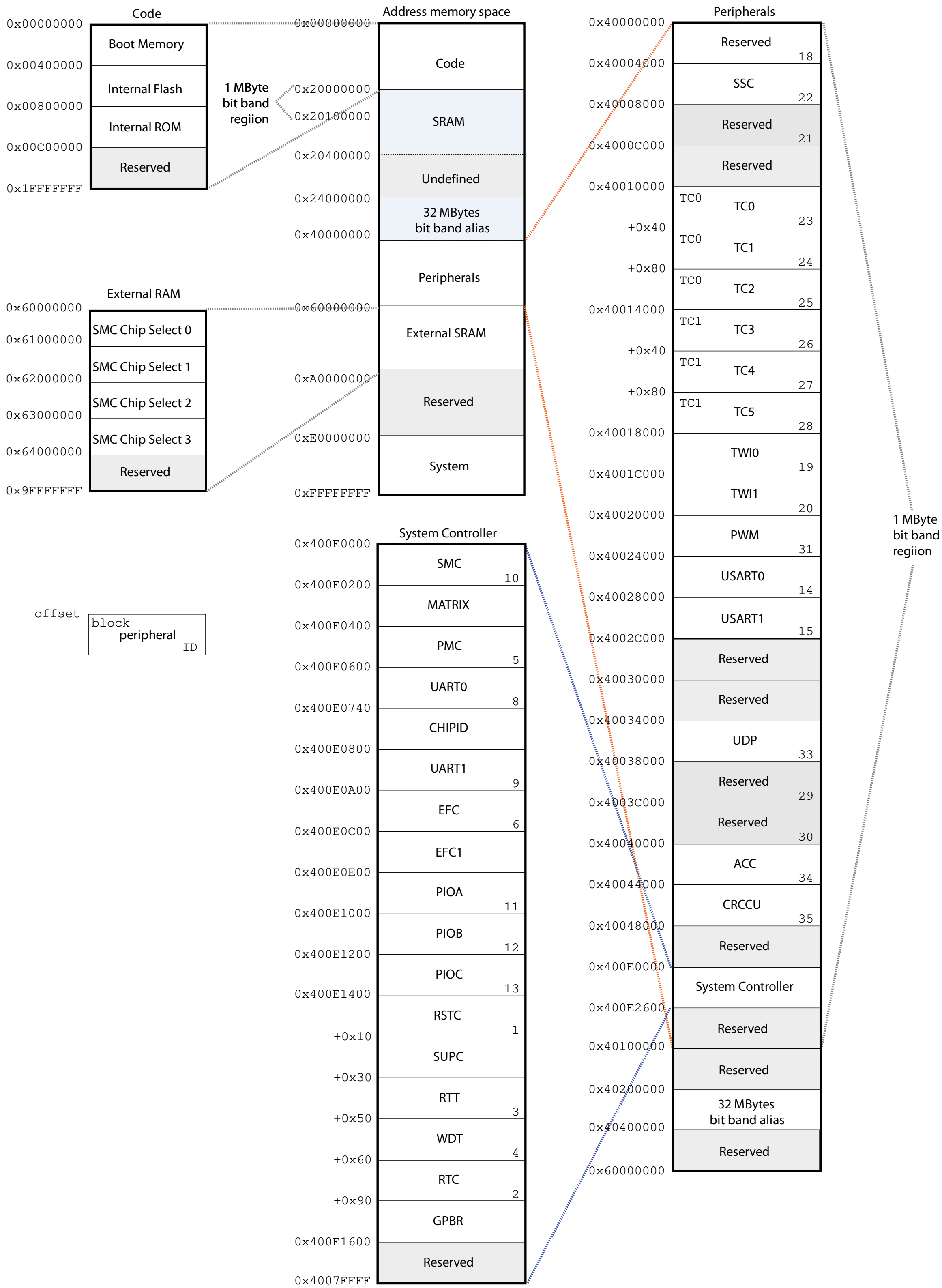
Instance name	Channel T/R
PIOA	Receive
TWI1	Receive
TWI0	Receive
UART1	Receive
UART0	Receive
USART1	Receive
USART0	Receive
PLC bridge	Receive
SSC	Receive

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M4 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watch points, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE®1149.1 JTAG Boundary scan on All Digital Pins

8. SAM4SP32A Product Mapping

Figure 8-1. SAM4SP32A Product Mapping



9. Memories

9.1 Embedded Memories

9.1.1 Internal SRAM

The SAM4SP32A device embeds a total of 160-Kbytes high-speed SRAM.

The SRAM is accessible over System Cortex-M4 bus at address 0x2000 0000. The SRAM is in the bit band region. The bit band alias region is from 0x2200 0000 to 0x23FF FFFF.

9.1.2 Internal ROM

The SAM4SP32A embeds an Internal ROM, which contains the SAM Boot Assistant (SAM-BA®), In Application Programming routines (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

9.1.3 Embedded Flash

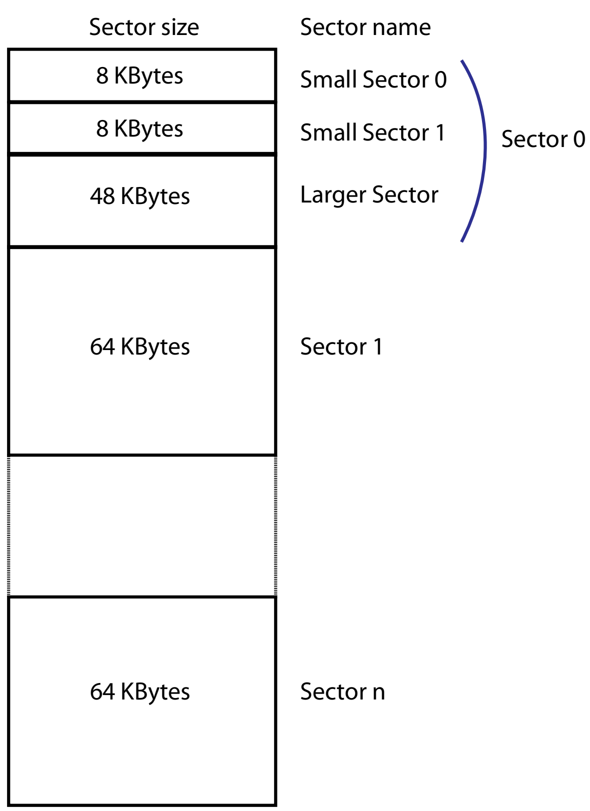
9.1.3.1 Flash Overview

Flash size is 2x1024 Kbytes.

The memory is organized in sectors. Each sector has a size of 64 KBytes. The first sector of 64 Kbytes is divided into 3 smaller sectors.

The three smaller sectors are organized to consist of 2 sectors of 8 KBytes and 1 sector of 48 KBytes. Refer to 41 below.

Figure 9-1. Global Flash Organization



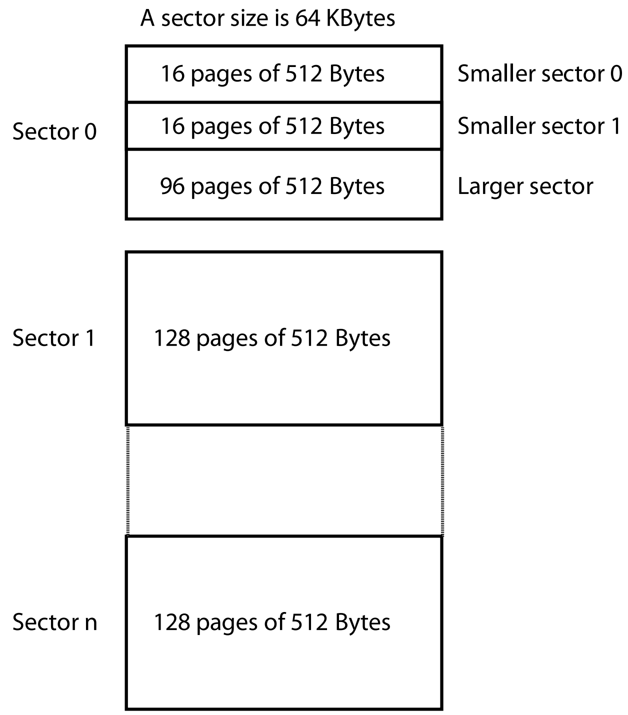
Each Sector is organized in pages of 512 Bytes. For sector 0:

- The smaller sector 0 has 16 pages of 512Bytes
- The smaller sector 1 has 16 pages of 512 Bytes
- The larger sector has 96 pages of 512 Bytes

From Sector 1 to n:

The rest of the array is composed of 64 KBytes sector of each 128 pages of 512bytes. Refer to Figure 9-2 below.

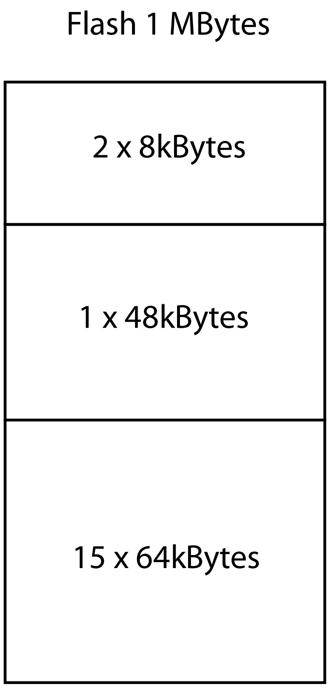
Figure 9-2. Flash Sector Organization



- SAM4SP32A: the Flash size is 2 x 1024 KBytes
  - Internal Flash0 address is 0x0040_0000
  - Internal Flash1 address is 0x0050_0000

Refer to Figure 9-3 below for the organization of the Flash following its size.

Figure 9-3. Flash Size



Erasing the memory can be performed as follows:

- on a 512-byte page inside a sector, of 8K Bytes (1)

Note: EWP and EWPL commands can be only used in 8 KBytes sectors.

- on a 4-Kbyte Block inside a sector of 8 KBytes/48 Kbytes/64 Kbytes
- on a sector of 8 KBytes/48 KBytes/64 KBytes
- on chip

The memory has one additional reprogrammable page that can be used as page signature by the user. It is accessible through specific modes, for erase, write and read operations. Erase pin assertion will not erase the User Signature page.

Erase memory by page is possible only in Sector of 8 Kbytes.

(1) EWP and EWPL commands can be only used in sector 8KBytes sectors.

9.1.3.2 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (HEFC4) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block.

It manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the sys-tem about the Flash organization, thus making the software generic.

9.1.3.3 Flash Speed

The user needs to set the number of wait states depending on the frequency used:

For more details, refer to the “AC Characteristics” sub-section of the product “Electrical Characteristics”.

9.1.3.4 Lock Regions

Several lock bits are used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. **Lock bit number**

Product	Number of lock bits	Lock region size
SAM4SP32A	256 (128 + 128)	8 Kbytes

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.5 Security Bit Feature

The SAM4SP32A features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.6 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.7 Unique Identifier

SAM4SP32A device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.8 User Signature

Each part contains a User Signature of 512 bytes. It can be used by the user to store user information such as trimming, keys, etc., that the customer does not want to be erased by asserting the ERASE pin or by software ERASE command. Read, write and erase of this area are allowed.

9.1.3.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST and PA0 and PA1are tied low.

9.1.3.10 SAM-BA Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

9.1.3.11 GPNVM Bits

The GPNVM bits of the SAM4SP32A are only available on FLash0. There is no GPNVM bit on Flash1. The GPNVM0 is the security bit. The GPNVM1 is used to select the boot mode (boot always at 0x00) on ROM or FLASH. The SAM4SP32A embeds an additional GPNVM bit : GPNVM2. This GPNVM bit is used only to swap the Flash0 and Flash1. If GPNVM bit 2 is:

ENABLE: If the Flash1 is mapped at address 0x0040_0000 (Flash1 and Flash0 are continuous).

DISABLE: If the Flash0 is mapped at address 0x0040_0000 (Flash0 and Flash1 are continuous).

Table 9-2. **General Purpose Non volatile Memory Bits**

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection
2	Flash selection (Flash 0 or Flash 1)

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

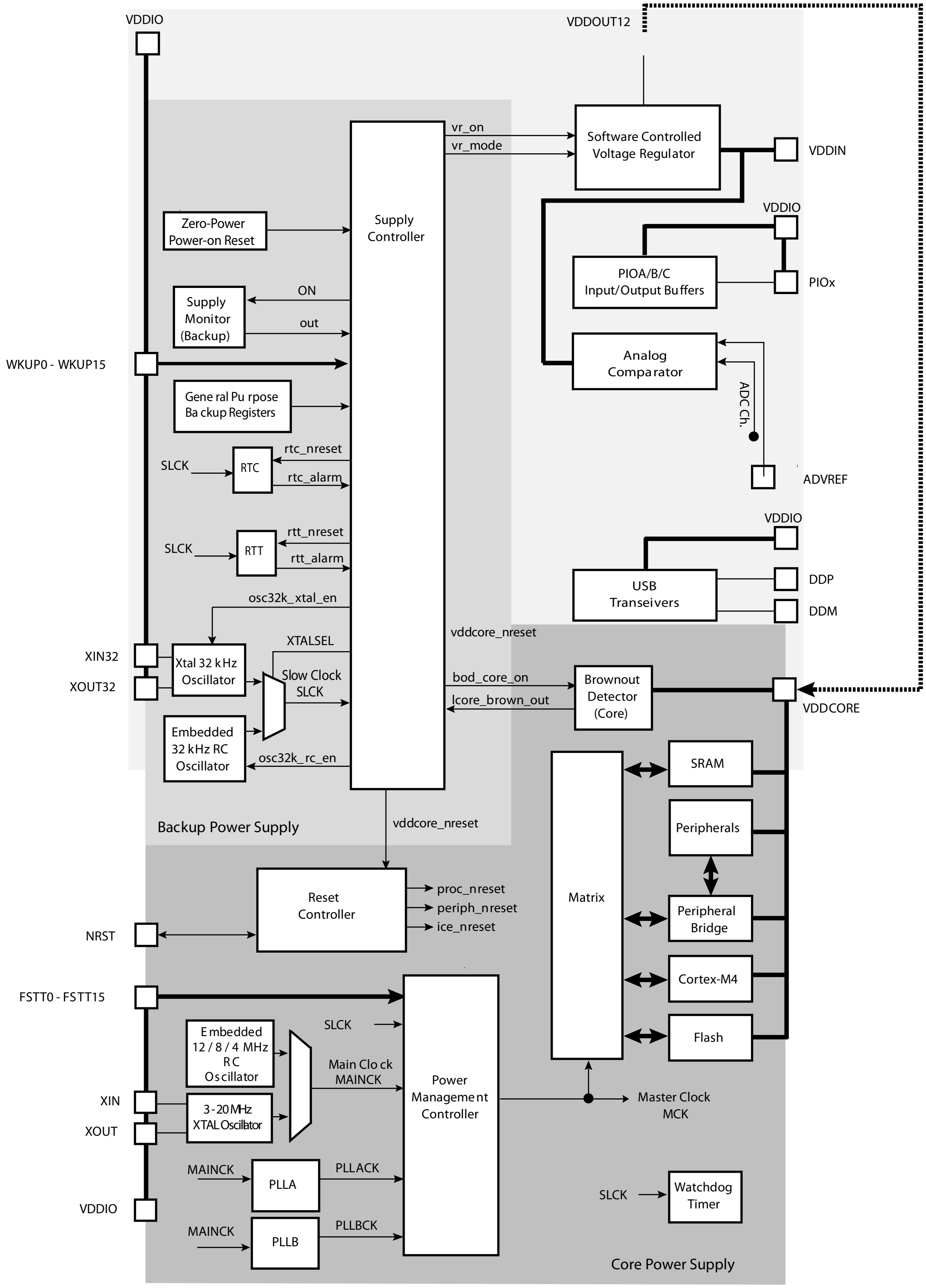
Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

Setting the GPNVM Bit 2 selects bank 1, clearing it selects the boot from bank 0. Asserting ERASE clears the GPNVM Bit 2 and thus selects the boot from bank 0 by default.

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup sources, generated by WKUP0 - WKUP15 pins, but are not physical pins.

10.1 System Controller and Peripherals Mapping

Please refer to SAM4SP32A Product Mapping.

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM4SP32A embeds three features to monitor, warn and/or reset the chip:

- Power-on-Reset on VDDIO
- Brownout Detector on VDDCORE
- Supply Monitor on VDDIO

10.2.1 Power-On-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 3.0 V to 3.6 V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows dividing the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE. The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset. The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset. The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control).

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow Clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the soft-ware-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

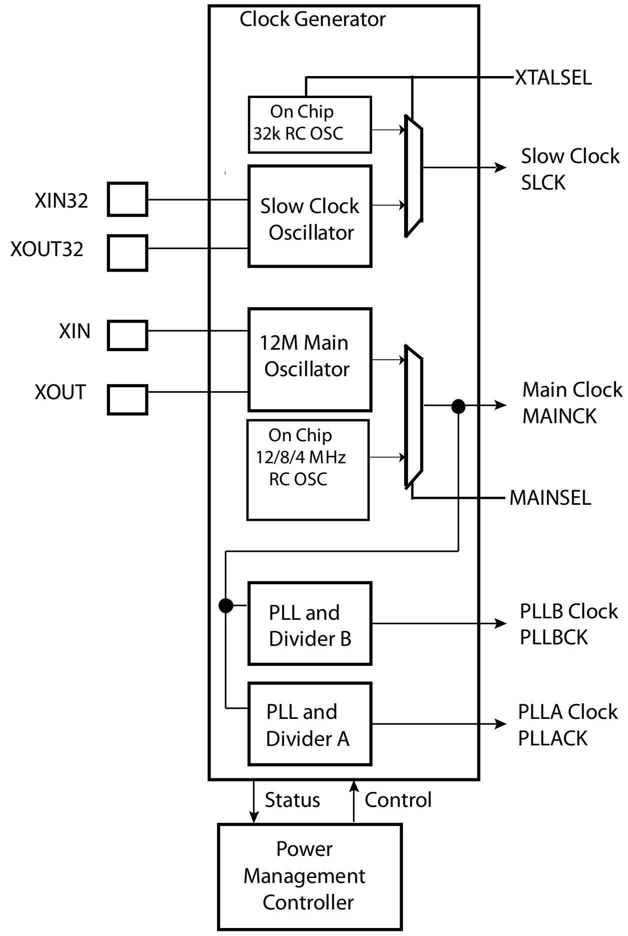
It also enables to set the system in different low-power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low-power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-power RC Oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC Oscillator, factory programmed. Three output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 80 to 240 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller
- One 80 to 240 MHz programmable PLL (PLLA), provides the clock, MCK to the processor and peripherals. The PLLA input frequency is from 3 MHz to 32 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

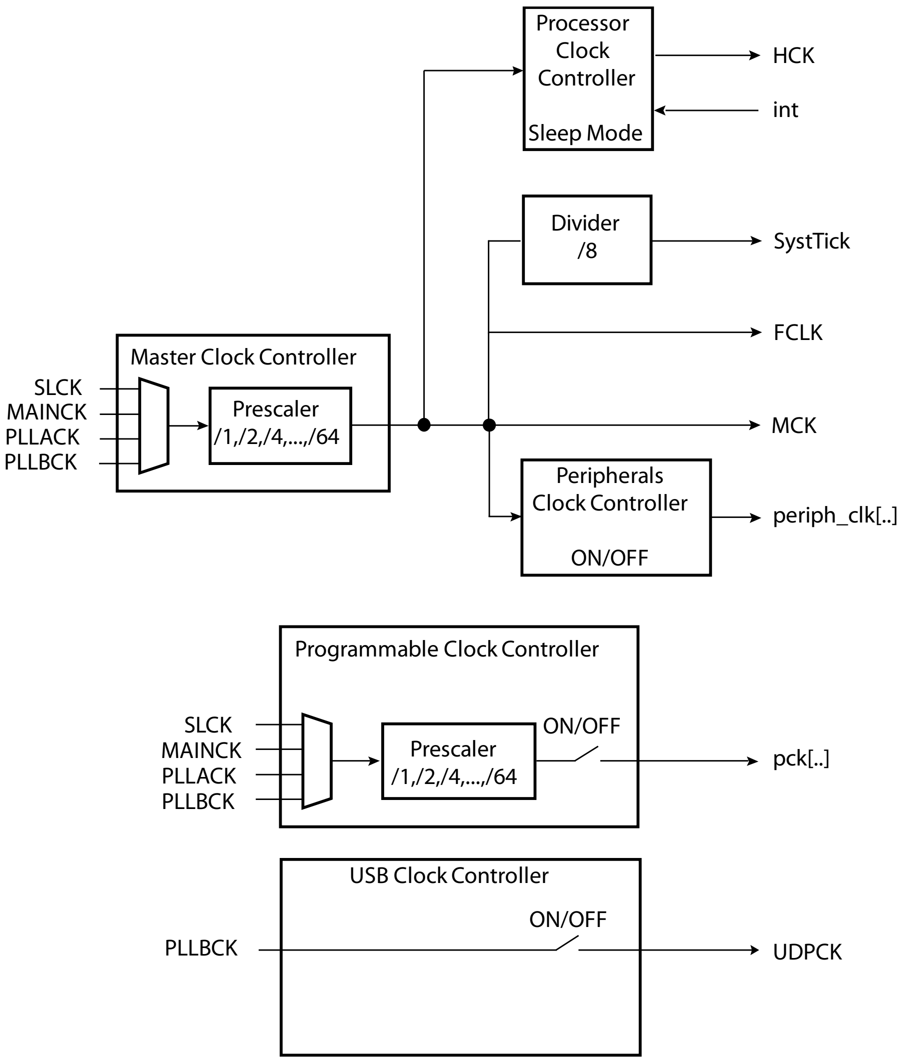
- the Processor Clock, HCLK
- the Free running processor clock, FCLK
- the Cortex SysTick external clock
- the Master Clock, MCK, in particular to the Matrix and the memory interfaces
- the USB Clock, UDPCK
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator and the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4 MHz.

The user can trim the 8 and 12 MHz RC Oscillator frequency by software.

Figure 10-3. Power Management Controller Block Diagram



The SysTick calibration value is fixed at 12500, which allows the generation of a time base of 1 ms with SysTick clock at 12.5 MHz (max HCLK/8 = 100 MHz/8 = 12500, so STCALIB = 0x30D4).

10.7 Watchdog Timer

- 16-bit key-protected only-once Programmable Counter
- Windowed, prevents the processor to be in a deadlock on the watchdog access

10.8 SysTick Timer

- 24-bit down counter
- Self-reload capability
- Flexible System timer

10.9 Real Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running backup Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year Gregorian and Persian calendar
- Programmable Periodic Interrupt
- Trimmable 32.7682 kHz crystal oscillator clock source
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In
- Waveform output capability on GPIO pins in low power modes

10.11 General-Purpose Backup Registers

- Eight 32-bit backup general-purpose registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable external interrupts
- Sixteen priority levels
- Processor state automatically saved on interrupt entry, and restored on
- Dynamic reprioritizing of interrupts
- Priority grouping.
  - selection of pre-empting interrupt levels and non pre-empting interrupt levels.
- Support for tail-chaining and late arrival of interrupts.
  - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. **SAM4SP32A Chip ID´s Register**

Chip Name	Flash Size (KBytes)	RAM Size (KBytes)	Pin Count	CHIPID_CIDR	CHIPID_EXID
SAM4SP32A	2*1024	160	128	0X29A7_0EE8	-
JTAG ID: 05B3_203F					

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC controlling a maximum of 37 I/O Lines
- Each PIO Controller controls up to 22 programmable I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. **PIO available on SAM4SP32A**

Version	Pins
PIOA	22
PIOB	12
PIOC	3

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Programmable Glitch filter
  - Programmable debouncing filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
  - Additional interrupt modes on a programmable event: rising edge, falling edge, low level or high level
  - Lock of the configuration by the connected peripheral
- Synchronous output, provides set and clear of several I/O lines in a single write
- Write Protect Registers
- Programmable Schmitt trigger inputs
- Parallel capture mode

- Can be used to interface a CMOS digital image sensor, etc....
- One clock, 8-bit parallel data and two data enable on I/O lines
- Data can be sampled one time out of two (for chrominance sampling only)
- Supports connection of one Peripheral DMA Controller channel (PDC) which offers buffer reception without processor intervention

10.16 Peripheral Identifiers

Table 10-3 defines the Peripheral Identifiers of the SAM4SP32A. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and control of the peripheral clock with the Power Management Controller.

Table 10-3. **Peripherical Identifiers**

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EFC0	X		Enhanced Embedded Flash Controller 0
7	EFC1	X		Enhanced Embedded Flash Controller 1
8	UART0	X	X	UART 0
9	UART1	X	X	UART 1
10	SMC	X	X	Static Memory Controller
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	USART 0
15	USART1	X	X	USART 1
16	-	-	-	Reserved
17	-	-	-	Reserved
18	-	X	X	Reserved
19	TWI0	X	X	Two Wire Interface 0
20	TWI1	X	X	Two Wire Interface 1
21	-	-	-	Reserved
22	SSC	X	X	Synchronous Serial Controller
23	TC0	X	X	Timer/Counter 0
24	TC1	X	X	Timer/Counter 1
25	-	-	-	Reserved
26	-	-	-	Reserved
27	-	-	-	Reserved
28	-	-	-	Reserved
29	-			Reserved
30	-			Reserved
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

10.17 Peripheral Signal Multiplexing on I/O Lines

The SAM4SP32A features 3 PIO controllers (PIOA, PIOB and PIOC), that multiplex the I/O lines of the peripheral set.

The SAM4SP32A controls up to 22 lines. Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

10.17.1 PIO Controller A Multiplexing

Table 10-4. **Multiplexing on PIO Controller A (PIOA)**

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comment
PA0	PWMH0	TIOA0	A17	WKUP0		
PA1	PWMH1	TIOB0	A18	WKUP1		
PA2	PWMH2	SCK0	DATRG	WKUP2		
PA3	TWD0	NPCS3				
PA4	TWCK0	TCLK0		WKUP3		
PA5	RXD0	NPCS3		WKUP4		
PA6	TXD0	PCK0				
PA7	RTS0	PWMH3			XIN32	
PA8	CTS0	ADTRG		WKUP5	XOUT32	
PA9	URXD0	NPCS1	PWMFI0	WKUP6		
PA10	UTXD0	NPCS2				
PA15	TF	TIOA1	PWML3	WKUP14/PIODCEN1		
PA16	TK	TIOB1	PWML2	WKUP15/PIODCEN2		
PA17	TD	PCK1	PWMH3	AC0		
PA18	RD	PCK2	A14	AC1		
PA19	RK	PWML0	A15	AC2/WKUP9		
PA20	RF	PWML1	A16	AC3/WKUP10		
PA21	RXD1	PCK1				
PA22	TXD1	NPCS3	NCS2			
PA23	SCK1	PWMH0	A19	PIODCCLK		
PA24	RTS1	PWMH1	A20	PIODC0		
PA25	CTS1	PWMH2	A23	PIODC1		

10.17.2 **PIO Controller B Multiplexing**

Table 10-5. **Multiplexing on PIO Controller B (PIOB)**

I/O Line	Peripherical A	Peripherical B	Peripherical C	Extra Function	System Function	Comment
PB0	PWMH0			AC4/RTCOUT0		
PB1	PWMH1			AC5/RTCOUT1		
PB2	URXD1	NPCS2		AC6/WKUP12		
PB3	UTXD1	PCK2		AC7		
PB4	TWD1	PWMH2			TDI	
PB5	TWCK1	PWML0		WKUP13	TDO/TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10					DMM	
PB11					DPP	
PB12	PWML1				ERASE	

10.17.3 **PIO Controller C Multiplexing**

Table 10-6. **Multiplexing on PIO Controller C (PIOC)**

I/O Line	Peripherical A	Peripherical B	Peripherical C	Extra Function	System Function	Comment
PC0	D0	PWML0				
PC5	D5					
PC26	A8	TIOA4				

11. Embedded Peripherals Overview

11.1 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I2C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

11.2 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

11.3 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
  - Full modem line support on USART1 (DCD-DSR-DTR-RI)
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- SPI Mode
  - Master or Slave
  - Serial Clock programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation

- Communication at up to 115.2 Kbps
- Test Modes
    - Remote Loopback, Local Loopback, Automatic Echo

11.4 Synchronous Serial Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader)
- Contains an independent receiver and transmitter and a common clock divider
- Offers configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

11.5 Timer Counter (TC)

- Two 16-bit Timer Counter Channels
- Wide range of functions including:
    - Frequency Measurement
    - Event Counting
    - Interval Measurement
    - Pulse Generation
    - Delay Timing
    - Pulse Width Modulation
    - Up/down Capabilities
- Each channel is user-configurable and contains:
    - One external clock input
    - Five internal clock inputs
    - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
    - Advanced line filtering
    - Position / revolution / speed
- 2-bit Gray Up/Down Counter for Stepper Motor

11.6 Pulse Width Modulation Controller (PWM)

- One Four-channel 16-bit PWM Controller, 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
    - A Modulo n counter providing eleven clocks
    - Two independent Linear Dividers working on modulo n counter outputs
    - High Frequency Asynchronous clocking mode
- Independent channel programming
    - Independent Enable Disable Commands
    - Independent Clock Selection
    - Independent Period and Duty Cycle, with Double Buffering
    - Programmable selection of the output waveform polarity

- Programmable center or left aligned output waveform
- Independent Output Override for each channel
- Independent complementary Outputs with 12-bit dead time generator for each channel
- Independent Enable Disable Commands
- Independent Clock Selection
- Independent Period and Duty Cycle, with Double Buffering

- Synchronous Channel mode
  - Synchronous Channels share the same counter
  - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
  - Provides Buffer transfer without processor intervention, to update duty cycle of synchronous channels
- One programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

11.7 USB Device Port (UDP)

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
  - Endpoint 0: 64bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

11.8 Analog Comparator

- One analog comparator
- High speed option vs. low-power option
  - 170 µA/xx ns active current consumption/propagation delay
  - 20 µA/xx ns active current consumption/propagation delay
- Selectable input hysteresis
  - 0, 15 mV, 30mV (Typ)
- Minus input selection:
  - Temperature Sensor
  - ADVREF
- Plus input selection:
  - All analog inputs
- output selection:
  - Internal signal

- external pin
- selectable inverter

- window function
- Interrupt on:
  - Rising edge, Falling edge, toggle
  - Signal above/below window, signal inside/outside window

11.9 Cyclic Redundancy Check Calculation Unit (CRCCU)

- 32-bit cyclic redundancy check automatic calculation
- CRC calculation between two addresses of the memory

11.10 PLC Brigde

- Six I/O lines to connect to PRIME PLC Transceiver for external configurations

12. PRIME PLC Transceiver

The SAM4SP32A MCU embeds a Certified PRIME Power line communication transceiver with a featured Class D power amplifier and a set of hardware accelerators blocks to execute the heavy tasks of the PRIME protocol without the interruption of the Cortex-M4 CPU.

The PRIME PLC Transceiver peripheral integrates:

- Power Line Carrier Modem for 50 and 60 Hz mains
- 97-carrier OFDM PRIME compliant
- Baud rate Selectable: 21400 to 128600 bps
- Differential BPSK, QPSK, 8-PSK modulations
- Automatic Gain Control and signal amplitude tracking
- Embedded on-chip DMAs
- Media Access Control
- Viterbi decoding and CRC PRIME compliant
- 128-bit AES encryption
- Channel sensing and collision pre-detection

12.1 SAM4SP32A PRIME PHY Layer

12.1.1 SAM4SP32A PHY Layer

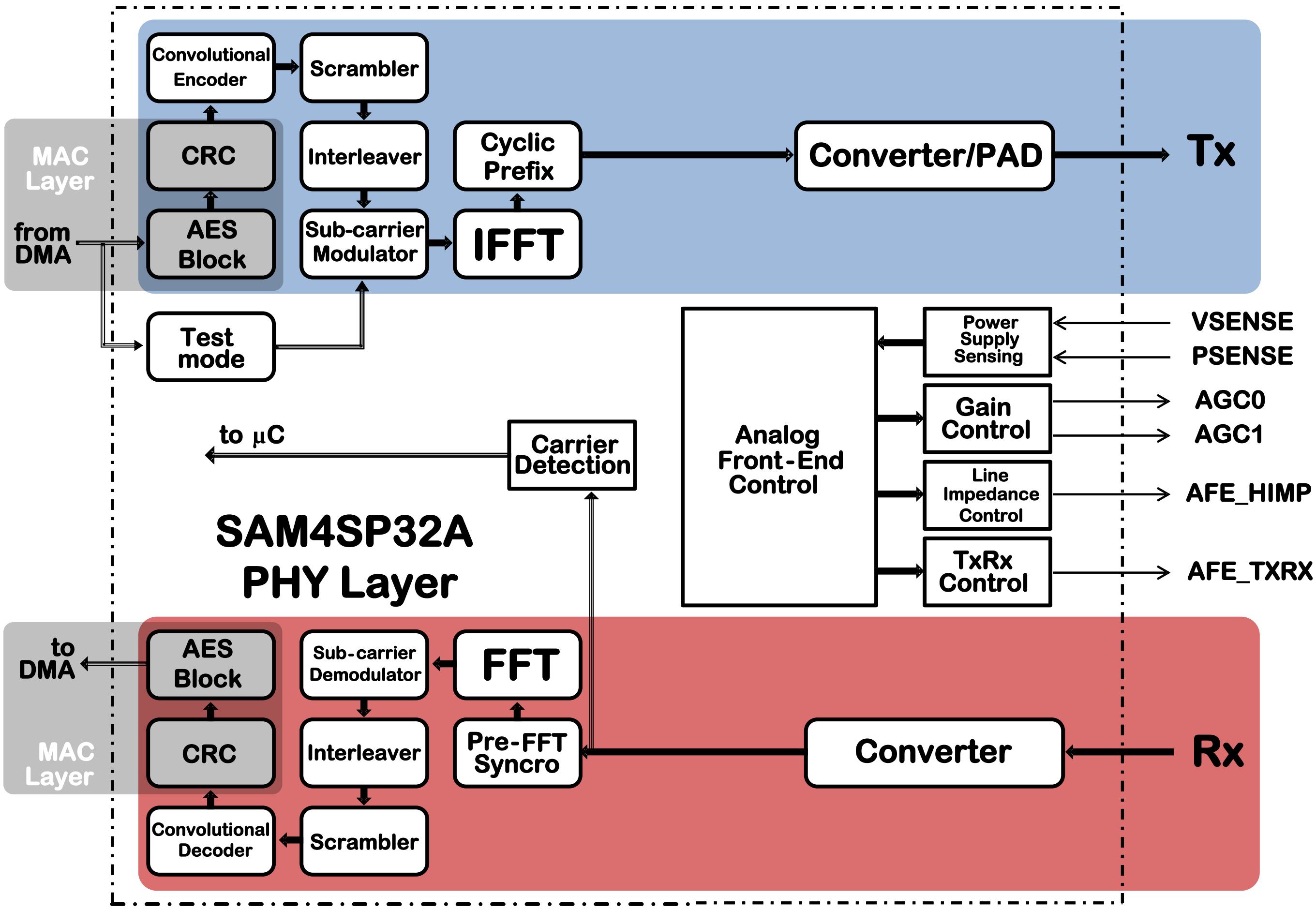
The physical layer of SAM4SP32A consists of a hardware implementation of the PRIME Physical Layer Entity, which is an Orthogonal Frequency Division Multiplexing (OFDM) system in the CENELEC A-band. This PHY layer transmits and receives MPDUs (MAC Protocol Data Unit) between neighbor nodes.

From the transmission point of view, the PHY layer receives its inputs from the MAC (Medium Access Control) layer, via DMA. At the end of transmission branch, data is output to the physical channel.

On the reception side, the PHY layer receives its inputs from the physical channel, and at the end of reception branch, the data flows to the MAC layer, via DMA.

A PHY layer block diagram is shown below:

Figure 12-1. SAM4SP32A PHY Layer Block Diagram



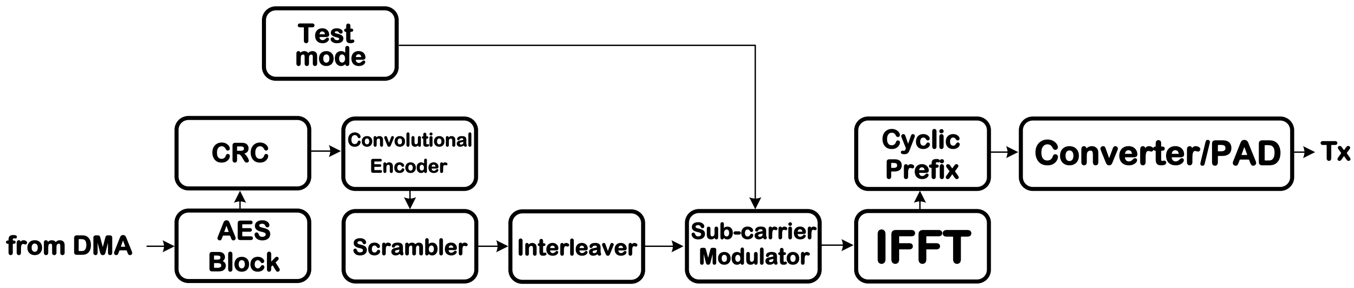
The diagram can be divided in four sub-blocks: Transmission branch, Emission branch, Analog Front End control and Carrier Detection.

12.1.1.2 Transmission and Reception branches

Phy layer takes data to be sent from dedicated DMA channel (PHY_TX). 128-bit AES encryption is done "on the fly", and the Clyclic Redundancy Check (CRC) fields are hardware-generated in real time. These CRCs are properly appended to the transmission data. The rest of the chain is hardware-wired, and performs automatically all the tasks needed to send data according to PRIME specifications.

In Figure 12-2, the block diagram of the transmission brach Is shown.

Figure 12-2. Transmission branch



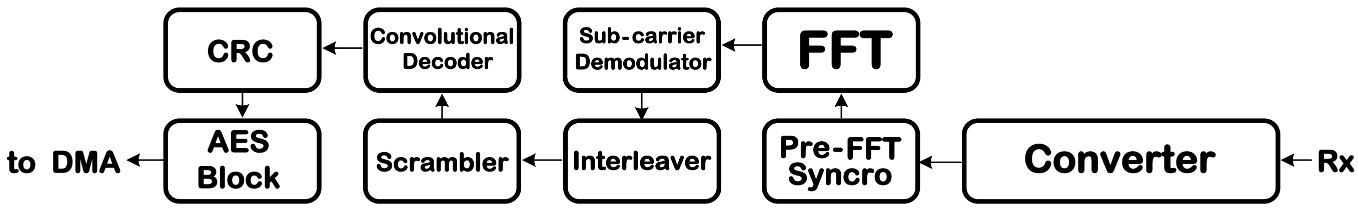
The output is differentially modulated using a BPSK/DQPSK/D8PSK scheme. After modulation, IFFT (Inverse Fourier Transform) block and cyclic prefix block allows to implement an OFDM scheme.

A Converter and a Power Amplifier Driver is the last block in the transmission branch. This block is responsible for adjusting the signal to reach the best transmission efficiency, thus reducing consumption and power dissipation.

Test mode: *When selected, test mode injects data directly to Sub-carrier modulation block. When in test mode, data can be injected continuously to the line using only a set of selected frequencies, in order to test channel behavior.*

The reception branch performs automatically all the tasks needed to process received data. Phy layer delivers data to MAC layer through the dedicated DMA channel (PHY_RX).

Figure 12-3. Reception branch



12.1.1.3 Carrier Detection

Looking for an easy detection of incoming messages, PRIME specification defines a chirp signal located at the beginning of the PRIME frames devised to ease synchronization in the receptor. By means of detection techniques, the receiver can know accurately when the chirp has been completely received and then the correct instant when the frame begins.

Before starting a transmission, it is also necessary to use carrier detection in order to check if another device is already emitting, thus avoiding collisions. If any device is emitting, the carrier detection triggers a microcontroller interruption and sets an internal flag, thus the transmission will be stopped.

The main drawback of this process is that chirp signal length (2.4 milliseconds) is not short enough to guarantee very low collision ratio.

To improve this drawback, the OFDM PLC Modem implements two different algorithms to detect the carrier as soon as possible, aiming to reduce collisions and improving the medium access behavior. By these early detection techniques, the system achieves low collision ratio, and the communication throughput increases significantly.

12.1.1.4 Analog Front End control

The Phy layer controls the Analog Front End by means of four sub-blocks:

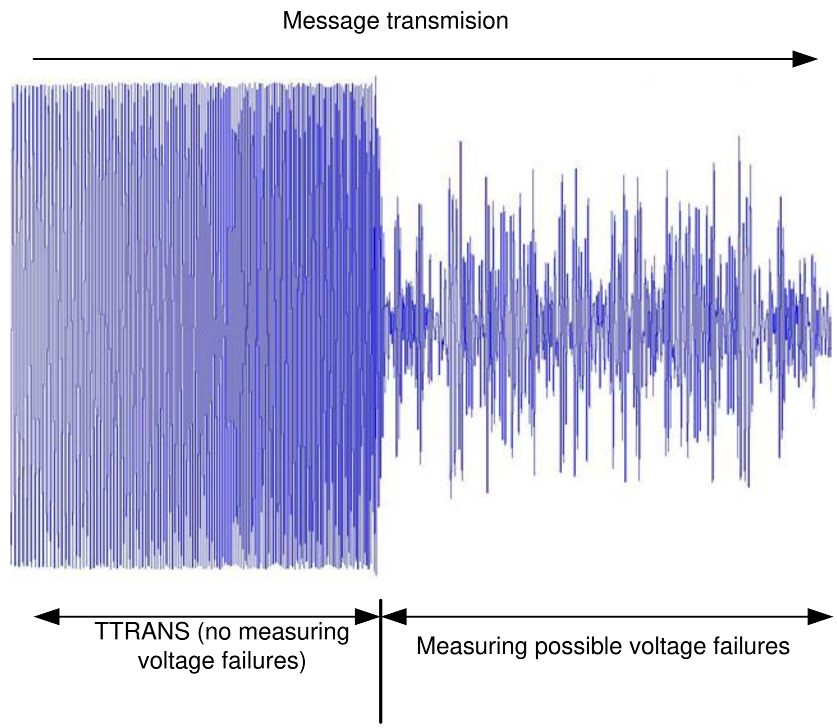
- Power Supply sensing
- Gain control
- Line Impedance control
- TxRx control

12.1.1.5 Power Supply Sensing: VSENSE and PSENSE

The power supply is continuously monitored to avoid power supply failures that could damage the supply device. This block senses the power channel using two different inputs:

- **VSENSE:** VSENSE detects whether voltage falls below 3.3v during a number of cycles while a message is being transmitted. This measurement is done after a transitory guard time (TTRANS in figure below). If a Voltage failure occurs, the transmission is shut down and sending messages again will be not possible if an internal flag (VFAILURE) is not previously cleared.

Figure 12-4. Transitory guard time in message transmission

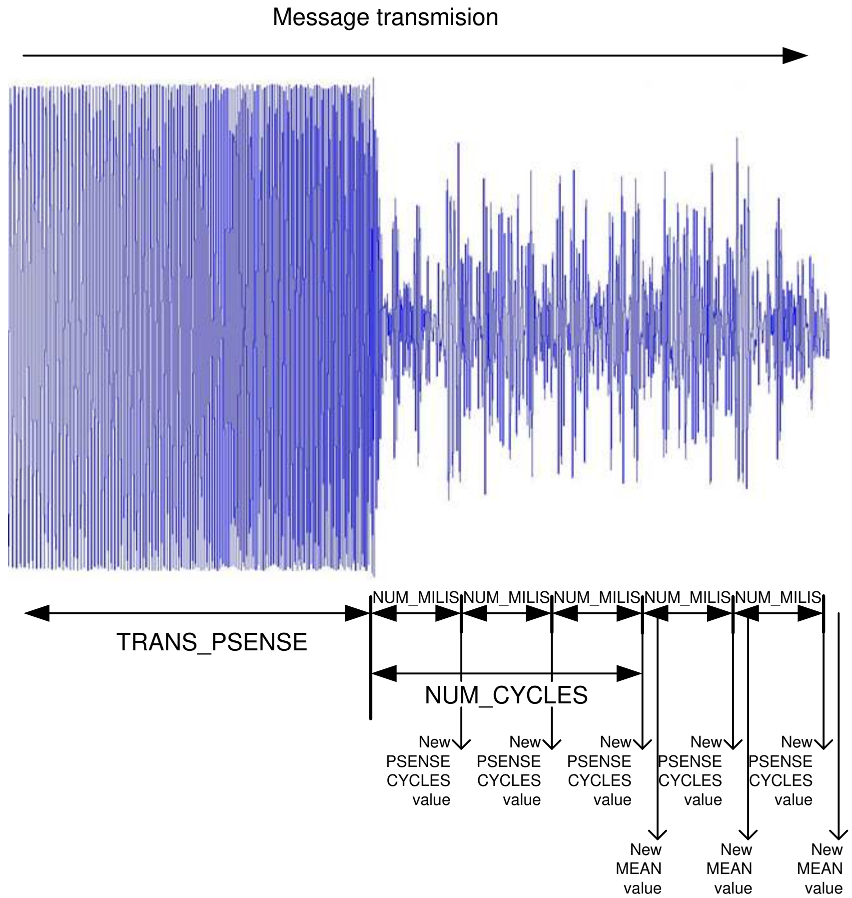


- **PSENSE:** PSENSE measures the power source current consumption, shutting down the transmission if the consumption exceeds a defined threshold (stored in MAXPOT phy layer registers, see 12.1.5.34). This measurement is done after a transitory guard time. As the current measurement varies over time, an averaging is done taking into account an average parameter (Alpha), a configurable number of cycles (NUMCYCLES, see 12.1.5.35) and a configurable length of each cycle (A_NUMMILIS, see 12.1.5.36).

If a power failure occurs, the transmission is shut down and sending messages again will be not possible if an internal flag (PFAILURE, see 12.1.5.22) is not previously cleared.

The system considers that a power failure has occurs when the value read from MEAN registers (see 12.1.5.30) is above the user-definable value stored in MAXPOT registers.

Figure 12-5. PSENSE parameters



Psense and Vsense configurations parameters are automatically set by the Phy layer.

See related peripheral registers for more information about Psense and Vsense.

12.1.1.6 Gain Control

This block implements two Automatic Gain Control outputs to adjust the received signal level to a suitable range. Both of them are set to '1' when the received signal is above two system thresholds in order to activate external attenuators placed in the external analog front end.

The value of these outputs is set during the beginning of a received message and is hold until the end of the message.

AGC0 and AGC1 follow different algorithms, thus using both of them ensures a more accurate gain control.

See AGC_CONFIG register in for information about AGC configuration.

12.1.1.7 Line Impedance Control

This block modifies the configuration of the Analog Front End by means of AFE-HIMP output. When working with a suitable external configuration, the system can change the filter conditions in order to adjust its behavior to the line impedance values. See last SAM4SP32A reference design for further information about Line Impedance topologies.

12.1.1.8 TxRx Control

This block modifies the configuration of the Analog Front End by means of AFE-TXRX output. Thus is possible to change filter conditions between transmission/reception.

See reference design for further information about TxRx control.

12.1.2 PHY parameters

As described below, the PHY layer is specified by certain main parameters, which are fixed for each specific constellation/coding combination. These parameters have to be identical in a network in order to achieve compatibility.

Table 12-1. **PRIME Phy main parameters**

PRIME Phy parameter	Value
Base Band Clock (Hz)	250000
Subcarrier spacing (Hz)	488,28125
Number of data subcarriers	84 (header), 96 (payload)
Number of pilot subcarriers	13 (header), 1 (payload)
FFT interval (samples)	512
FFT interval (μs)	2048
Cyclic Prefix (samples)	48
Cyclic Prefix (μs)	192
Symbol interval (samples)	560
Symbol interval (μs)	2240
Preamble period (μs)	2048

Table 12-2 shows the PHY data rate during payload transmission, and maximum MSDU length for various modulation and coding combinations

Table 12-2. **Phy parameters depending on the modulation**

	DBPSK		DQPSK		D8PSK	
Convolutional Code (1/2)	**On**	**Off**	**On**	**Off**	**On**	**Off**
Information bits per subcarrier	0,5	1	1	2	1,5	3
Information bits per OFDM symbol	48	96	96	192	144	288
Raw data rate (kbps approx)	21,4	42,9	42,9	85,7	64,3	128,6
MAX MSDU length with 63 symbols (bits)	3016	6048	6040	12096	9064	18144

Table 12-3 shows the modulation and coding scheme and the size of the header portion of the PHY frame

Table 12-3. **Header parameters**

	DBPSK
Convolutional Code (1/2)	On
Information bits per subcarrier	0,5
Information bits per OFDM symbol	42

All the parameters of the physical layer such as the base band clock, subcarrier spacing, number of subcarriers...; are defined in PRIME Specification, and have to be identical in a network in order to achieve compatibility.

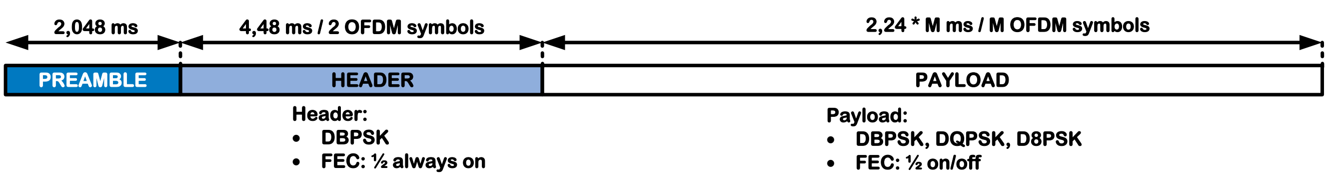
12.1.3 PHY Protocal Data Unit (PPDU) Format

Figure 12-6 shows how OFDM symbols are transmitted in a PPDU (Physical layer Protocol Data Unit). The preamble is used at the beginning of every PPDU for synchronization purposes.

Figure 12-6. PHY layer transmitter block diagram

Phy layer adaptively modifies attenuation values applied to the whole signal. Also, additional attenuations are applied to the chirp section of the signal (preamble) and to the rest of the signal itself (header+payload), to smoothly adapt amplitude values and transitions.

Figure 12-7. PPDU OFDM symbols and duration



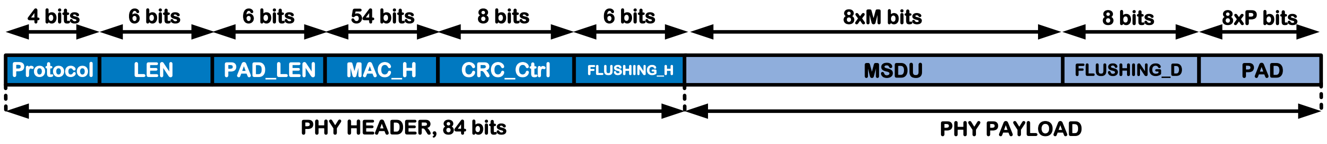
12.1.4 PHY Service Specification

There is an interface specified in PRIME for the PHY layer, with several primitives relative to both data and control planes.

PHY layer has a single 20-bit free-running clock measured in 10µs steps. Time measured by this clock is the one to be used in some PHY primitives to indicate a specific instant in time.

SAM4SP32A includes a hardware implementation of this clock, which consists of a 20-bit register. This register is read-only and it can be accessed as a 32-bit variable by the ADD8051C3A microcontroller.

Figure 12-8. Header and payload structure



Prime specifies a complete set of primitives to manage the PHY Layer, and the PHY-SAP (PHY Service Access Point) from MAC layer. Atmel PRIME stack integrates all this functions, making them transparent to the final user and simplifying the management.

12.1.5 PHY Layer registers

Relative addresses in the PLC modem intenrnal memory map given.

12.1.5.1 PHY_SFR Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
PHY_SFR	BCH_ERR	CD	UMD	--	--	TXRX	--	INT_PHY

Name: PHY_SFR

Address: 0xFE2A

Access: Read/write

Reset: 0x87

- **--:** Reserved bit
- **BCH_ERR:** Busy Channel Error Flag.

  This bit is set to ‘0’ by hardware to indicate the presence of an OFDM signal at the transmission instant. Otherwise, this field value is ‘1’.

  This bit is used for returning a result of “Busy Channel” in the PHY_DATA.confirm primitive (see PRIME specification).
- **CD:** Carrier Detect bit.

  This bit is set to ‘1’ by hardware when an OFDM signal is detected, and it is active during the whole reception.

  This bit is used in channel access (CSMA-CA algorithm) for performing channel-sensing.
- **UMD:** Unsupported Modulation Scheme flag.

  This flag is set to ‘1’ by hardware every time a header with correct CRC is received, but the PROTOCOL field in this header indicates a modulation scheme not supported by the system.
- **TXRX:** Transmission order.

  When data to transmit is ready at ADDR_PHY_INI_TX in data memory, the Time value is set at TX_TIME register and then the emission level is specified at ATTENUATION register, then TXRX bit has to be set to '0' in order to init transmission.

  If this bit is read, only returns '0' when physical transmission has started. Otherwise, it returns '1'.

  The transmission will begin when TIMER_BEACON_REF is equal to TX_TIME.
- **INT_PHY:** Physical Layer interruption

  This bit is internally connected to the external microcontroller interrupt /EXT_INT.

  It is low-level active. It is set to '0' by physical layer and is cleared by writing '1' in the bit PHY_SFR(0).

12.1.5.2 SYS_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
SYS_CONFIG		--		CONV_PD	PHY_PD	PHY_ERR_EN	PHY_ERR	PHY_RST

Name: SYS_CONFIG

Address: 0xFE2C

Access: Read/write

Reset: 0x04

- **--:** Reserved bits
- **CONV_PD:** Converter Power Down

  The SAM4SP32A microcontroller can activate internal converter power down mode by setting this bit. When internal converter is in power down mode, the system is unable to receive.

  This bit is high-level active.
- **PHY_PD:** PHY Power Down

  This bit shuts down Physical Layer clock. When in PHY power down mode, all the system blocks involved in communication remain inactive. Thus, the system will be unable to transmit or receive. The next sequence must be respected to ensure proper power down:

  Setting PHY power down mode

  1-Set Physical Layer reset (SYS_CONFIG(0)), PHY_RST='1'

  2-Set CONV_PD and PHY_PD fields

  Exiting PHY power down mode

  1-Clear CONV_PD and PHY_PD fields

  2-Clear Physical Layer reset (SYS_CONFIG(0)), PHY_RST='0'

  This bit is high-level active.
- **PHY_ERR_EN:** Physical Layer Watchdog enable

  This bit enables or disables Physical layer watchdog. Physical layer watchdog is enabled by default.

  This bit is high-level active.
- **PHY_EN:** Physical Layer Error Flag

  This flag indicates if a Physical layer error has occurred. Physical layer watchdog has a 200milliseconds sampling period. When Physical layer detects an error, it activates the Physical layer interrupt and this flag is set.

  To restore situation, microcontroller must reset Physical layer by means of PHY_RST bit (SYS_CONFIG(0)).
- **PHY_RST:** Physical Layer Reset

  This bit resets the Physical layer. To perform a Physical layer reset cycle, microcontroller must set this bit to '1' and then must clear it to '0'.

12.1.5.3 PHY_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
PHY_CONFIG	--		**CINR_MODE**	**PAD_LEN_AC**	**AES_EN**	**CD_MOD1_EN**	**CD_MOD2_DET**	**MAC_EN**

Name: PHY_CONFIG

Address: 0xFE68

Access: Read/write

Reset: 0x1F

- **--:** Reserved bits
- **CINR_MODE:** Carrier to Interference + Noise Ratio mode

  This bit enables/disables CINR mode when set to ‘1’.
  - ‘0’: CINR mode disabled.
  - ‘1’: CINR mode enabled.
- **PAD_LEN_AC:** This field allows the system to work with two different representations of the Phy header PAD_LEN field (PAD_LEN represented before coding or PAD_LEN represented after coding).
  - ‘0’: PAD_LEN field in PHY header is represented before coding. This is the suitable value to fulfill PRIME specification.
  - ‘1’: PAD_LEN field in PHY header is represented after coding.
- **AES_EN:** This field enables/disables “on the fly” AES encryption and decryption by hardware.
  - ‘0’: “on the fly” AES encryption/decryption disabled.
  - ‘1’: “on the fly” AES encryption/decryption enabled.
- **CD_MOD1_EN:** This field enables/disables Carrier Detection mode 1.
  - ‘0’: Carrier Detection mode 1 disabled.
  - ‘1’: Carrier Detection mode 1 enabled.
- **CD_MOD2_DET:** This field enables/disables Carrier Detection mode 2.
  - ‘0’: Carrier Detection mode 2 disabled.
  - ‘1’: Carrier Detection mode 2 enabled.
- **MAC_EN**: This field enables/disables CRC processing by hardware.
  - ‘0’: CRC processing disabled.
  - ‘1’: CRC processing enabled.

12.1.5.4 ATTENUATION Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ATTENUATION	ATTENUATION(7:0)							

Name: ATTENUATION

Address: 0xFE24

Access: Read/write

Reset: 0xFF

- **ATTENUATION:** Global attenuation for the transmitted signal (chirp+signal). The 16-bit signal level is multiplied by this 8-bit value and the result is truncated to 16 bits.

  Attenuation value = 0xFF → the transmitted signal amplitude is not attenuated.

  Attenuation value = 0x00 → the transmitted signal amplitude is nullified.

12.1.5.5 ATT_CHIRP Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ATT_CHIRP	ATT_CHIRP(7:0)							

Name: ATT_CHIRP

Address: 0xFE9B

Access: Read/write

Reset: 0xFF

- **ATT_CHIRP:** This register stores the attenuation value for the chirp. The 16-bit chirp data is multiplied with this 8-bit value and the 24-bit result is truncated to 16 bits.

  Attenuation value = 0xFF → the chirp amplitude is not attenuated

  Attenuation value = 0x00 → the chirp amplitude is nullified

12.1.5.6 ATT_SIGNAL Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ATT_SIGNAL	ATT_SIGNAL(7:0)							

Name: ATT_SIGNAL

Address: 0xFE9C

Access: Read/write

Reset: 0xFF

- **ATT_SIGNAL:** This register stores the attenuation value for the signal without the chirp section. The 16-bit chirp data is multiplied with this 8-bit value and the 24-bit result is truncated to 16 bits.

  Attenuation value = 0xFF → the signal amplitude is not attenuated

  Attenuation value = 0x00 → the signal amplitude is nullified

12.1.5.7 TX_TIME Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
TX_TIME	TX_TIME(19:12)								@0xFE26
	TX_TIME(11:4)								@0xFE27
	TX_TIME(3:0)				"0000"				@0xFE28
	"00000000"								@0xFE29

Name: TX_TIME

Address: 0xFE26 – 0xFE29

Access: Read/write

Reset: 0x00, …, 0x00;

- **TX_TIME:** This 20-bit value sets the time instant when the MPDU (MAC Protocol Data Unit) has to be transmitted. The time is expressed in 10µs steps.

  When writing a new value to TX_TIME register, a specific writing order must be taken, always from the most significant byte (TX_TIME(19:12) at address 0xFE26) to the least significant byte (TX_TIME(3:0) at address 0xFE28), and it is required to write the 3 bytes to avoid wrong time comparisons in transmission.

  The 20-bit TX_TIME value is managed by the microcontroller as a 4-byte variable. The TX_TIME value is aligned to the 20 most significant bits, being the 12 least significant bits padded with zeros.

  This register is used by the physical layer for being in accordance with PRIME specifications about transmission time (see PRIME spec.)

  Note: TXRX bit (PHY_SFR(2)) has to be cleared to '0' in order to init transmission. Once this bit has been cleared, the transmission will start when TIMER_BEACON_REF value is equal to TX_TIME.

12.1.5.8 TIMER_FRAME Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
TIMER_FRAME	TIMER_FRAME(19:12)								@0xFE2D
	TIMER_FRAME(11:4)								@0xFE2E
	TIMER_FRAME(3:0)				"0000"				@0xFE2F
	"00000000"								@0xFE30

Name: TIMER_FRAME

Address: 0xFE2D – 0xFE30

Access: Read only

Reset: 0x00, …, 0x00;

- **TIMER FRAME:** Time of receipt of the preamble associated with the PSDU (PHY Service Data Unit). It is expressed in 10µs steps and is taken from the physical layer timer TIMER_BEACON_REF.

  It is set by hardware and is a read-only register.

  This register is used by the physical layer for being in accordance with PRIME specification about reception time (see PRIME specification).

  The 20-bit TIMER_FRAME value is managed by the microcontroller as a 4-byte variable. The TIMER_FRAME value is aligned to the 20 most significant bits, being the 12 least significant bits padded with zeros. This simplifies arithmetic calculations with time values.

12.1.5.9 TIMER_BEACON_REF Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
TIMER_BEACON_REF	TIMER_BEACON_REF(19:12)								@0xFE47
	TIMER_BEACON_REF (11:4)								@0xFE48
	TIMER_BEACON_REF (3:0)				"0000"				@0xFE49
	"00000000"								@0xFE4A

Name: TIMER_BEACON_REF

Address: 0xFE47 – 0xFE4A

Access: Read only

Reset: 0x00, …, 0x00;

- **TIMER_BEACON_REF:** Timer for the physical layer, which consists of a single 20-bit free-running clock measured in 10µs steps.

  It indefinitely increases a unit each 10 microseconds from 0 to 1048575, overflowing back to 0.

  It is set by hardware and is a read-only register.

  This register is used by the physical layer for being in accordance with PRIME specification. It is reserved 32-bit in data memory to be able to declare as 32-bit variable. The 20-bit register MSB is aligned to the 32-bit variable MSB, in order to simplify arithmetic calculations with time values.

12.1.5.10 RX_LEVEL Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
RX_LEVEL	RX_LEVEL(15:8)								@0xFE31
	RX_LEVEL(7:0)								@0xFE32

Name: TABLE_ELEMENT_INIT

Address: 0xFE31 – 0xFE32

Access: Read only

Reset: 0x00; 0x00

- **RX_LEVEL:** These registers store the autocorrelation level of the chirp signal.
  When the reception process has started, these registers are set by hardware.

12.1.5.11 RSSI_MIN Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RSSI_MIN	RSSI_MIN(7:0)							

Name: RSSI_MIN

Address: 0xFE33

Access: Read only

Reset: 0xFF

- **RSSI_MIN:** Received Signal Strength Indication Min

  This register stores the minimum RSSI value measured in the last message received.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps

12.1.5.12 RSSI_AVG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RSSI_AVG	RSSI_AVG(7:0)							

Name: RSSI_AVG

Address: 0xFE34

Access: Read only

Reset: 0x00

- **RSSI_AVG:** Received Signal Strength Indication Average

  This register stores the average RSSI value measured in the last message received.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps

12.1.5.13 RSSI_MAX Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RSSI_MAX	RSSI_MAX(7:0)							

Name: RSSI_MAX

Address: 0xFE35

Access: Read only

Reset: 0x00

- **RSSI_MAX:** Received Signal Strength Indication Max

  This register stores the maximum RSSI value measured in the last message received.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps

12.1.5.14 CINR_MIN Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
CINR_MIN	CINR_MIN(7:0)							

Name: CINR_MIN

Address: 0xFE38

Access: Read only

Reset: 0xFF

- **CINR_MIN:** Carrier to Interference + Noise ratio Min

  This register stores the minimum CINR value measured in the last message received.

  In order to calculate CINR properly, the algorithm takes beacon-type messages as a reference, since this message type allows knowing its content beforehand.

  The system uses a table that must be loaded with the beacon data to be received, so CINR mode must be activated (see PHY_CONFIG register) and the same procedure used to send beacons must be followed. As CINR mode is activated, physical layer will load the message in the table instead of sending it (table load time is in the order of microseconds, and is much shorter than the one used to send the message).

  Once the table is loaded, CINR must be disabled, and next messages CINR will be calculated taken the beacon loaded in the table as reference.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps.

12.1.5.15 CINR_AVG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
CINR_AVG	CINR_AVG(7:0)							

Name: CINR_AVG

Address: 0xFE39

Access: Read only

Reset: 0x00

- **CINR_AVG:** Carrier to Interference + Noise ratio Average

  This register stores the average CINR measured in the last message received.

  In order to calculate CINR properly, the algorithm takes beacon-type messages as a reference, since this message type allows knowing its content beforehand.

  The system uses a table that must be loaded with the beacon data to be received, so CINR mode must be activated (see PHY_CONFIG register) and the same procedure used to send beacons must be followed. As CINR mode is activated, physical layer will load the message in the table instead of sending it (table load time is in the order of microseconds, and is much shorter than the one used to send the message).

  Once the table is loaded, CINR must be disabled, and next messages CINR will be calculated taken the beacon loaded in the table as reference

  The measurement is done at symbol level.

  The value is stored in ¼dB steps.

12.1.5.16 CINR_MAX Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
CINR_MAX	CINR_MAX(7:0)							

Name: CINR_MAX

Address: 0xFE3A

Access: Read only

Reset: 0x00

- **CINR_MAX:** Carrier to Interference + Noise ratio Max

  This register stores the maximum CINR value measured in the last message received.

  In order to calculate CINR properly, the algorithm takes beacon-type messages as a reference, since this message type allows knowing its content beforehand.

  The system uses a table that must be loaded with the beacon data to be received, so CINR mode must be activated (see PHY_CONFIG register) and the same procedure used to send beacons must be followed. As CINR mode is activated, physical layer will load the message in the table instead of sending it (table load time is in the order of microseconds, and is much shorter than the one used to send the message).

  Once the table is loaded, CINR must be disabled, and next messages CINR will be calculated taken the beacon loaded in the table as reference

  The measurement is done at symbol level.

  The value is stored in ¼dB steps.

12.1.5.17 EVM_HEADER Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_HEADER	EVM_HEADER(15:8)								@0xFE3B
	EVM_HEADER (7:0)								@0xFE3C

Name: EVM_HEADER

Address: 0xFE3B – 0xFE3C

Access: Read only

Reset: 0x00; 0x00

- **EVM_HEADER:** Header Error Vector Magnitude-

  These registers store in a 16-bit value the maximum error vector magnitude measured in the reception of a message header.

  The 7 MSB (EVM_HEADER(15:9)) represent the integer part in %, being the EVM_HEADER(8:0) bits the fractional part if more precision were required.

  This register is used by the physical layer for being in accordance with PRIME specification. It is reserved 32-bit in data memory to be able to declare as 32-bit variable. The 20-bit register MSB is aligned to the 32-bit variable MSB, in order to simplify arithmetic calculations with time values.

12.1.5.18 EVM_PAYLOAD Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_PAYLOAD	EVM_PAYLOAD(15:8)								@0xFE3D
	EVM_PAYLOAD(7:0)								@0xFE3E

Name: EVM_PAYLOAD

Address: 0xFE3D – 0xFE3E

Access: Read only

Reset: 0x00; 0x00

- **EVM_PAYLOAD:** Payload Error Vector Magnitude-

  These registers store in a 16-bit value the maximum error vector magnitude measured in the reception of a message payload.

  The 7 MSB (EVM_PAYLOAD(15:9)) represent the integer part in %, being the EVM_PAYLOAD(8:0) bits the fractional part if more precision were required.

12.1.5.19 EVM_HEADER_ACUM Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_HEADER_ACUM	EVM_HEADER_ACUM(19:12)								@0xFE3F
	EVM_HEADER_ACUM (11:4)								@0xFE40
	EVM_HEADER_ACUM (3:0)				"0000"				@0xFE41
	"00000000"								@0xFE42

Name: EVM_HEADER_ACUM

Address: 0xFE3F – 0xFE42

Access: Read only

Reset: 0x00, …, 0x00;

- **EVM_HEADER_ACUM:** Header Total Error Vector Magnitude Accumulator

  When receiving an OFDM symbol, the summation of all its individual carriers EVMs is calculated in order to further calculate the average EVM value. These registers store the maximum summation between the two OFDM symbols received in a message header.

12.1.5.20 EVM_PAYLOAD_ACUM Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_PAYLOAD_ACUM	EVM_PAYLOAD_ACUM(19:12)								@0xFE43
	EVM_PAYLOAD_ACUM(11:4)								@0xFE44
	EVM_PAYLOAD_ACUM(3:0)				“0000”				@0xFE45
	“00000000”								@0xFE46

Name: EVM_PAYLOAD_ACUM

Address: 0xFE43 – 0xFE46

Access: Read only

Reset: 0x00, …, 0x00;

- **EVM_PAYLOAD_ACUM:** Payload Total Error Vector Magnitude Accumulator

  When receiving an OFDM symbol, the summation of all its individual carriers EVMs is calculated in order to further calculate the average EVM value. These registers store the maximum summation between all the OFDM symbols received in a message payload.

12.1.5.21 RMS_CALC Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RMS_CALC	RMS_CALC(7:0)							

Name: RMS_CALC

Address: 0xFE58

Access: Read only

Reset: 0x00

- **RMS_CALC:** This register stores an 8-bit value which magnitude is proportional to the emitted signal amplitude.

  By measuring the amplitude of the emitted signal, the hardware can estimate the power line input impedance. Thus hardware can adjust emission configuration appropriately.

12.1.5.22 VSENSE_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VSENSE_CONFIG	--				PFAILURE	PSENSE_SOFT	VFAILURE	VSENSE_EN

Name: VSENSE_CONFIG

Address: 0xFE59

Access: Read only

Reset: 0x00

- **PFAILURE:** Power Failure Flag

  This flag is set to 1 when a power failure occurs. The transmission is stopped and a new transmission is not possible if this flag is not cleared previously.

  When a power failure occurs, a consideration about decreasing voltage amplitude in the source should be taken.

  This flag must be cleared by software.
- **PSENSE_SOFT:** Current measurement is done every time a transmission takes place. With PSENSE_SOFT the system can force a continuous current measurement, including both idle and transmission states.
  - '0': Current consumption is measured every time a transmission begins (after a guard time defined by TRANS_PSENSE). NUMMILIS, NUMCYCLES and TRANS_PSENSE values must be taken into account to accurate PSENSE measurements. This is the default mode and it is the expected one when SAM4SP32A is working.
  - '1': Current consumption is measured both in idle and transmission states. This mode is useful for design purposes, in order to find suitable values for the current threshold (MAXPOT registers) depending on the external net requirements.
- **VFAILURE:** Voltage Failure Flag

  This flag is set to 1 when a voltage failure occurs. The transmission is stopped and a new transmission is not possible if this flag is not cleared previously.

  When a voltage failure occurs, a consideration about decreasing voltage amplitude in the source should be taken.

  This flag must be cleared by software.
- **VSENSE_EN:**VSENSE enable

  This bit enables VSENSE.
  - '0': VSENSE disabled (default).
  - '1': VSENSE enabled.

12.1.5.23 NUM_FAILS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
NUM_FAILS	NUM_FAILS(7:0)							

Name: NUM_FAILS

Address: 0xFE5A

Access: Read/write

Reset: 0x02

- **NUM_FAILS:** This register stores the number of 50 ns cycles (clk=20MHz) during which a voltage failure must be detected before shutting off the transmission and setting VFAILURE flag.

  This detection shall be done after a guard period set by TTRANS from the beginning of the transmission.

  Default value: 0x02 → 2 * 50 = 100ns

12.1.5.24 TTRANS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
TTRANS	TTRANS(7:0)							

Name: TTRANS

Address: 0xFE5B

Access: Read/write

Reset: 0x2D

- **TTRANS:** This register stores the number of 50 µs cycles (clk=20MHz) to wait from the beginning of the transmission before looking for a possible voltage failure.

  Default value: 0x2D → 45 * 50 = 2.25ms (Thus, voltage failures are not expected until the end of chirp signal period)

12.1.5.25 AGC0_KRSSI Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC0_KRSSI	AGC0_KRSSI(7:0)							

Name: AGC0_KRSSI

Address: 0xFE5C

Access: Read/write

Reset: 0x00

- **AGC0_KRSSI:** This register is used to correct RSSI (Received Signal Strength Indication) computation when Automatic Gain Control 0 (AGC0) is active.

12.1.5.26 AGC1 KRSSI Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC1_KRSSI	AGC1_KRSSI(7:0)							

Name: AGC1_KRSSI

Address: 0xFE5D

Access: Read/write

Reset: 0x00

- **AGC1_KRSSI:** This register is used to correct RSSI (Received Signal Strength Indication) computation when Automatic Gain Control 1 (AGC1) is active.

12.1.5.27 ZERO_CROSS_TIME Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ZERO_CROSS_TIME	ZERO_CROSS_TIME(19:12)								@0xFE69
	ZERO_CROSS_TIME (11:4)								@0xFE6A
	ZERO_CROSS_TIME (3:0)				"0000"				@0xFE6B
	"00000000"								@0xFE6C

Name: ZERO_CROSS_TIME

Address: 0xFE69 – 0xFE6C

Access: Read only

Reset: 0x00, …, 0x00;

- **ZERO_CROSS_TIME:** Instant in time at which the last zero-cross event took place. It is expressed in 10µs steps and may take values from 0 to 1e6 (20-bit effective).

  It is set by hardware and is a read-only register.

  This register is used by the physical layer for being in accordance with PRIME specification. It is reserved 32-bit in data memory to be able to declare as 32-bit variable. The 20-bit register MSB is aligned to the 32-bit variable MSB, in order to simplify arithmetic calculations with time values.

12.1.5.28 ZERO_CROSS_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ZERO_CROSS_CONFIG	--					VEZC	REZC	FEZC

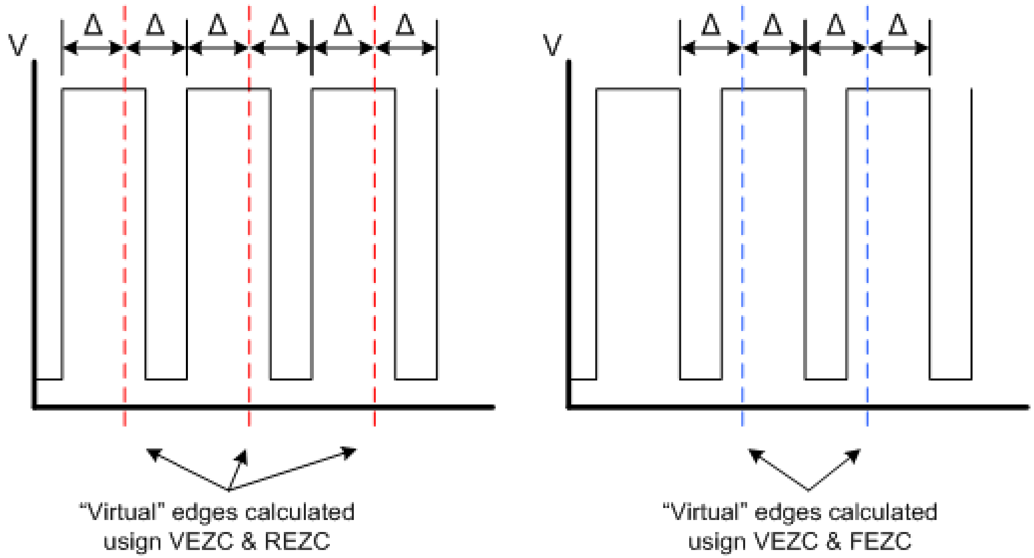
Name: ZERO_CROSS_CONFIG

Address: 0xFE6D

Access: Read/write

Reset: 0x06

- **--:** Reserved bits
- **VEZC:** Virtual Edge for Zero Crossing
  In this bit is equal to one, the hardware calculates the middle point between two VNR edges to calculate de zero crossing.
  This mode is used when the VNR signal duty cycle is different from 50%:



  VECZ can be used simultaneously with RECZ or FECZ.
  Using the three of them at a time is not recommended.
- **REZC**: Rising Edge for Zero Crossing
  If this bit is set to '1', the hardware uses the VNR rising edges to calculate zero-crossing.
  FEZC and REZC can be used simultaneously.
- **FEZC:** Falling Edge for Zero Crossing
  If this bit is set to '1', the hardware uses the VNR falling edges to calculate zero-crossing.
  FEZC and REZC can be used simultaneously.

12.1.5.29 PSENSECYCLES Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
PSENSECYCLES	--				FLAG_PSENSE	D(18:16)			@0xFE7D
	D(15:8)								@0xFE7E
	D(7:0)								@0xFE7F

Name: PSENSECYCLES

Address: 0xFE7D – 0xFE7F

Access: Read/write

Reset: 0x00, …, 0x00;

- **--:** Reserved bits
- **FLAG_SENSE:** Whenever a new power value is written in PSENSECYCLES, FLAG_PSENSE is set 1.

  This flag must be cleared by software
- **D(17:0):** Power supply consumption measurement

  The power supply line is sampled (f_{clk}=20MHz), and the number of logic ‘1’ detected during NUMMILIS milliseconds is stored in this field in order to calculate power consumption.

  Note: The first valid value is written after NUMMILIS, and then a new valid value is written every NUMMILIS milliseconds.

  Note: Measurement is only active when a message transmission begins or PSENSE_SOFT bit is active (see Name:12.1.5.22)

12.1.5.30 MEAN Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
MEAN	--				FLAG_MEAN	D(18:16)			@0xFE80
	D(15:8)								@0xFE81
	D(7:0)								@0xFE82

Name: PSENSECYCLES

Address: 0xFE80 – 0xFE82

Access: Read/write

Reset: 0x00, …, 0x00;

- **--:** Reserved bits
- **FLAG_MEAN:** Whenever a new value is written in MEAN, FLAG_MEAN is set to ‘1’

  This flag must be cleared by software
- **D(17:0):** This value stores the average power consumption calculated from the value in PSENSECYCLES and having into account the convergence factor “A” (see A_NUMMILIS register in 12.1.5.36).

  Note: The first valid value is written after NUMCYCLES*NUMMILIS, and then a new valid value is written every NUMMILIS milliseconds

12.1.5.31 PMAX Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
PMAX	--				FLAG_PMAX	D(18:16)			@0xFE83
	D(15:8)								@0xFE84
	D(7:0)								@0xFE85

Name: PMAX

Address: 0xFE83 – 0xFE85

Access: Read/write

Reset: 0x00, …, 0x00;

- **--:** Reserved bits
- **FLAG_PMAX:** Whenever a new value is written in PMAX, FLAG_PMAX is set to '1'.

  This flag must be cleared by software
- **D(17:0):** As described in MAXPOT register (see 12.1.5.34), every time the average power consumption exceeds a user defined threshold value, the current transmission is cancelled.

  PMAX register stores the average power consumption value that has risen above MAXPOT threshold.

12.1.5.32 TRANS_PSENSE Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
TRANS_PSENSE	TRANS_PSENSE(7:0)							

Name: TRANS_PSENSE

Address: 0xFE86

Access: Read/write

Reset: 0x2B

- **TRANS_PSENSE:** This register stores the number of 50 µs cycles to wait from the beginning of a transmission before looking for a possible power failure. This guard time is taken to avoid transient period where the measurement would be inaccurate

  Default value: 0x2B → 43 * 50 = 2.15ms

12.1.5.33 P_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
P_TH	--					P_TH(18:16)			@0xFE87
	P_TH(15:8)								@0xFE88
	P_TH(7:0)								@0xFE89

Name: P_TH

Address: 0xFE87 – 0xFE89

Access: Read/write

Reset: 0x07, 0xFF, 0xFF.

- **--:** Reserved bits
- **P_TH:** These registers contain a user defined power threshold. When the threshold value is exceeded, a low power consumption mode is automatically activated. In this low power consumption mode, the power dissipated in the transistors decreases at the expense of distortion increasing.

12.1.5.34 MAXPOT Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
MAXPOT	--					MAXPOT(18:16)			@0xFE8A
	MAXPOT (15:8)								@0xFE8B
	MAXPOT (7:0)								@0xFE8C

Name: MAXPOT

Address: 0xFE8A – 0xFE8C

Access: Read/write

Reset: 0x07, 0xFF, 0xFF.

- **--:** Reserved bits
- **MAXPOT:** These registers contain a user defined power consumption threshold. When this threshold is exceeded, current transmission is cancelled.

  When the threshold is exceeded, two flags are activated:

  - POTFAILURE flag (see VSENSE_CONFIG in 12.1.5.22). This flag indicates that a power failure has occurred.
  - FLAG_PMAX flag (see PMAX in 12.1.5.31). This flag indicates that, after a power failure, the last mean power value measured has been stored in PMAX register.

  To reset both flags is enough to reset either of them, the other will be automatically reset. This will enable to start new transmissions.

12.1.5.35 NUMCYCLES Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
NUMCYCLES	NUMCYCLES(7:0)							

Name: NUMCYCLES

Address: 0xFE8D

Access: Read/write

Reset: 0x05

- **NUMCYCLES:** Number of cycles of measuring power before obtaining a mean value that can be taken as valid.

  Example1: If NUMCYCLES=5(cycles) and NUMMILIS=1(milliseconds), 5 power measurements will be taken during 1 millisecond each one .The first valid power measurement value will be output in the fifth millisecond.

  Example2: If NUMCYCLES=3(cycles) and NUMMILIS=20(milliseconds), 3 power measurements will be taken during 20 milliseconds each one. The first valid power measurement value will be output after 60 milliseconds.

12.1.5.36 A_NUMMILIS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
NUMMILIS	--	A(1:0)		NUMMILIS(4:0)				

Name: A_NUMMILIS

Address: 0xFE8E

Access: Read/write

Reset: 0x21

- **--:** Reserved bits
- **A(1:0):** Convergence Factor

  Averaging factor that sets the convergence speed of the mean calculation algorithm.

  A=00 sets quicker convergence, while A=11 sets the slowest one. A=01,10 are intermediate values.

  Note: Power supply presents high dispersion values, so NUMMILIS value must be take into account in order to select a suitable value for A. If NUMMILIS is high, the mean value can be calculated slowly, because the averaging in being calculated over a long period of time. When NUMMILIS is low, the mean value must be calculated quickly in order to obtain more accurate values.
- **NUMMILIS(4:0):** Measurement acquisition time in milliseconds

  Stores the measurement acquisition time in milliseconds.

  Example1: If NUMCYCLES=5(cycles) and NUMMILIS=1(milliseconds), 5 power measurements will be taken during 1 millisecond each one .The first valid power measurement value will be output in the fifth millisecond.

  Example2: If NUMCYCLES=3(cycles) and NUMMILIS=20(milliseconds), 3 power measurements will be taken during 20 milliseconds each one. The first valid power measurement value will be output after 60 milliseconds.

12.1.5.37 EMIT_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
EMIT_CONFIG	--						TR_EMIT	TWO_H_BRIDGES

Name: EMIT_CONFIG

Address: 0xFE8F

Access: Read/write

Reset: 0x03

- **TR_EMIT:** Emission mode
  This bit selects the emission mode (Internal Drive or External transistors bridge).
  - ‘0’: Emission is done by means of internal SAM4SP32A driver.
  - ‘1’: Emission is done by means of external transistors (Default).
- **TWO_H_BRIDGES:** This bit selects the number of semi-H-bridges in the external interface.
  - ‘0’: There is only one semi-H-bridge in the external interface.
  - ‘1’: There are two semi-H-bridges in the external interface and the field HIMP (AFE_CTL register) determines which one is active (Default).

  Semi-H-Bridges must be connected following the table below

	TWO_H_BRIDGES=’0’	TWO_H_BRIDGES=’1’
EMIT1	P	N1
EMIT2	P	N1
EMIT3	P	N1
EMIT4	N	P2
EMIT5	N	P2
EMIT6	N	P2

12.1.5.38 AFE_CTL Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AFE_CTL	--			HIMP	HIMP_INV	TXRX	TXRX_HARD	TXRX_INV

Name: AFE_CTL

Address: 0xFE90

Access: Read/write

Reset: 0x10

- **--:** Reserved bits
- **HIMP:** Analog Front End Impedance control bit-

  This bit selects which branch is active when working with a two half-H-bridge branches analog front end.

  - ‘0’: “Low impedance” half-H-bridge is active (P2-N2).
  - ‘1’: “High impedance” half-H-bridge is active (P1-N1).
- **HIMP_INV:** HIMP pin polarity control

  This field inverts the polarity of the HIMP pin output.

  Note: This field only affect to the polarity of the external pin HIMP output, the value taken from HIMP bit (AFE_CTL(4)) remains unchanged
- **TXRX:** The value stored in this bit is taken by the microcontroller in order to set the TXRX pin level.
  - ‘0’: TXRX pin output = ‘0’.
  - ‘1’: TXRX pin output = ‘1’.
- **TXRX_HARD:** TXRX pin control

  This field selects if the TXRX pin is software/hardware controlled.

  - ‘0’: TXRX pin is software controlled. TXRX value is set by TXRX bit field (AFE_CTL(2)).
  - ‘1’: TXRX pin is hardware controlled.
- **TXRX_INV:** TXRX pin polarity control

  This field inverts the polarity of the TXRX pin output

12.1.5.39 R Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
R1	R1(7:0)								0xFE9F
R2	R2(7:0)								0xFEA0
R3	R3(7:0)								0xFEA1
R4	R4(7:0)								0xFEA2
R5	R5(7:0)								0xFEA3
R6	R6(7:0)								0xFEA4
R7	R7(7:0)								0xFEA5
R8	R8(7:0)								0xFEA6

Name: R1 – R8

Address: 0xFE9F – 0xFEA6

Access: Read/write

Reset: 0x60; 0x60; 0x60; 0x60; 0xFF; 0xFF; 0xFF; 0xFF.

- **R:** The value in these registers strongly depends on the external circuit configuration.

  Atmel provides values to be used according with the design recommended in SAM4SP32A kits

  Please contact Atmel Power Line if different external configurations are going to be used

  Recommended values (according to the configuration recommended in SAM4SP32A kits)

  R1(7:0): 0x21

  R2(7:0): 0x20

  R3(7:0): 0x12

  R4(7:0): 0x02

  R5(7:0): 0x37

  R6(7:0): 0x77

  R7(7:0): 0x37

  R8(7:0): 0x77

  Order of precedence: In the event of a conflict between the Ri(7:0) values above and Ri(7:0) values specified in the latest documentation in an SAM4SP32A kit, the values in the kit documentation shall take precedence.

12.1.5.40 PHY_ERRORS Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
PHY_ERRORS	--			PHY_ERRORS(4:0)				

Name: PHY_ERRORS

Address: 0xFE94

Access: Read/write

Reset: 0x00

- **--:** Reserved bits
- **PHY_ERRORS:** Physical Layer Error Counter

  The system stores in these bits the number of times that a Physical layer error has occurred. Microcontroller can clear this counter to zero.

  The value stored in this register is cleared every time the register is read.

12.1.5.41 FFT_MODE Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
FFT_MODE	NSYM(5:0)						CONTINUOUS	TEST_MODE_EN

Name: FFT_MODE

Address: 0xFEB0

Access: Read/write

Reset: 0x00

- **NSYM:** Number of symbols to transmit

  When in continuous transmission mode, symbol data acts as a free-running buffer, increasing from 0 to NSYM-1 and overflowing back to symbol 0.
- **CONTINUOUS:** This field enables/disables continuous transmission mode.
  - '0': Continuous transmission mode disabled.
  - '1': Continuous transmission mode enabled.
- **TEST_MODE_EN:** This field enables/disables test mode
  - '0': Test mode disabled.
  - '1': Test mode enabled.

Configuration for test mode. This register is used by the physical layer to fulfill with PRIME specification (PLME_TESTMODE.request primitive and PLME_TESTMODE.confirm primitive, see PRIME specification). In this mode data provided to FFT is written in data memory at ADDR_PHY_INI_TX, codifying each value with 4 bits according to DPSK modulation mapping. The msb of the value is to indicate an input of zero when set to '1'. Each byte in data memory contains 2 input values for FFT, with the first value located at high bits. There are 97 input values for FFT, so many as the number of subcarriers, so there are 48 bytes and a half of the next byte used for codifying them. The other half of this byte (low bits) will be used for the next symbol data.

12.1.5.42 AGC_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC_CONFIG	--		AGC0_POL	AGC0_VALUE	AGC0_MODE	AGC1_POL	AGC1_VALUE	AGC1_MODE

Name: AGC_CONFIG

Address: 0xFEB1

Access: Read/write

Reset: 0x24

SAM4SP32A has implemented two Automatic Gain Control outputs in order to adjust the received signal level to a suitable range. When in "automatic" mode, both of them are set to '1' when the received signal is above 16-bit-user-definable thresholds (AGC1_TH and AGC0_TH) in order to activate external attenuators placed in the external analog front end.

The value of these outputs is set during the beginning of a received message and is hold until the end of the message.

AGC0 and AGC1 follow different algorithms, thus using both of them ensures more accurate gain control

- --: Reserved bits
- **AGC0_POL:** AGC0 polarity

  This bit sets the polarity of the AGC0 output.

  - '0': Polarity is inverted.
  - '1': Polarity is not inverted (default).
- **AGC0_VALUE:** AGC0 output value-

  This bit stores the value wrote by the user to be the AGC0 output.

  This bit is only taken into account when AGC0 "forced" mode is active (AGC0_MODE='1').

  AGC0_POL field can invert this value.
- **AGC0_MODE:** AGC0 mode

  This bit selects which AGC0 mode is being used

  - '0': "Automatic" Mode. AGC0 output will be managed by the MAC, depending on saturation detected in received signal. If saturation is detected, AGC0 output will be '1'. Else, AGC0 output will be '0'. AGC0_POL field can invert this value.

    (See SAT_TH registers in 12.1.5.43)
  - '1': "Forced" Mode. AGC0 output will be managed by the user, according to the value wrote in AGC0_VALUE field (AGC_CONFIG(4)).
- **AGC1_POL:** AGC1 polarity

  This bit sets the polarity of the AGC1 output.

  - '0': Polarity is inverted.
  - '1': Polarity is not inverted (default).
- **AGC1_VALUE:** AGC1 output value-

  This bit stores the value wrote by the user to be the AGC1 output.

  This bit is only taken into account when AGC1 "forced" mode is active (AGC1_MODE='1').

  AGC1_POL field can invert this value.

- **AGC1_MODE:** AGC1 mode

  This bit selects which AGC1 mode is being used

  - '0': "Automatic" Mode. AGC1 output will be managed by the MAC, depending on saturation detected in received signal. If saturation is detected, AGC1 output will be '1'. Else, AGC1 output will be '0'. AGC1_POL field can invert this value.

    (See SAT_TH registers in 12.1.5.43)
  - '1': "Forced" Mode. AGC1 output will be managed by the user, according to the value wrote in AGC1_VALUE field (AGC_CONFIG(4)).

12.1.5.43 SAT_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
SAT_TH	SAT_TH(15:8)								@0xFEB7
	SAT_TH(7:0)								@0xFEB8

Name: SAT_TH

Address: 0xFEB7 – 0xFEB8

Access: Read/write

Reset: 0x40; 0x00

- **SAT_TH:** These registers store a threshold for the PLC input-signal amplitude.

  If this threshold is exceeded, AGC thresholds (AGC0_TH and AGC1_TH) will be taken into account.

  If this threshold is not exceeded, AGC0_TH and AGC1_TH thresholds will be ignored, thus the AGC algorithm will be never triggered.

  Recommended value for Atmel reference design = 0x37AA.

12.1.5.44 AGC1_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AGC1_TH	AGC1_TH(15:8)								@0xFE5F
	AGC1_TH(7:0)								@0xFE60

Name: AGC1_TH

Address: 0xFE5F – 0xFE60

Access: Read/write

Reset: 0x40; 0x00

- **AGC1_TH:** AGC1 Threshold

  These registers store the 16-bit upper threshold used by the AGC1 algorithm to determine that the input signal must be attenuated.

  This threshold is only taken into account in AGC1 “automatic” mode (AGC_CONFIG.AGC1_MODE=’0’).

  This threshold is only taken into account if SAT_TH value is exceeded.

  Recommended value for Atmel reference design = 0x4A00.

12.1.5.45 AGC0_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AGC0_TH	AGC0_TH(15:8)								@0xFEB2
	AGC0_TH(7:0)								@0xFEB3

Name: AGC0_TH

Address: 0xFEB2 – 0xFEB3

Access: Read/write

Reset: 0x10; 0x00

- **AGC0_TH:** AGC0 Threshold

  These registers store the 16-bit upper threshold used by the AGC0 algorithm to determine that the input signal must be attenuated.

  This threshold is only taken into account in AGC0 "automatic" mode (AGC_CONFIG.AGC0_MODE='0').

  This threshold is only taken into account if SAT_TH value is exceeded.

  Recommended value for Atmel reference design = 0x1000.

12.1.5.46 AGC_PADS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC_PADS	--						P46_MODE	SWITCH_AGC

Name: AGC_PADS

Address: 0xFE61

Access: Read/write

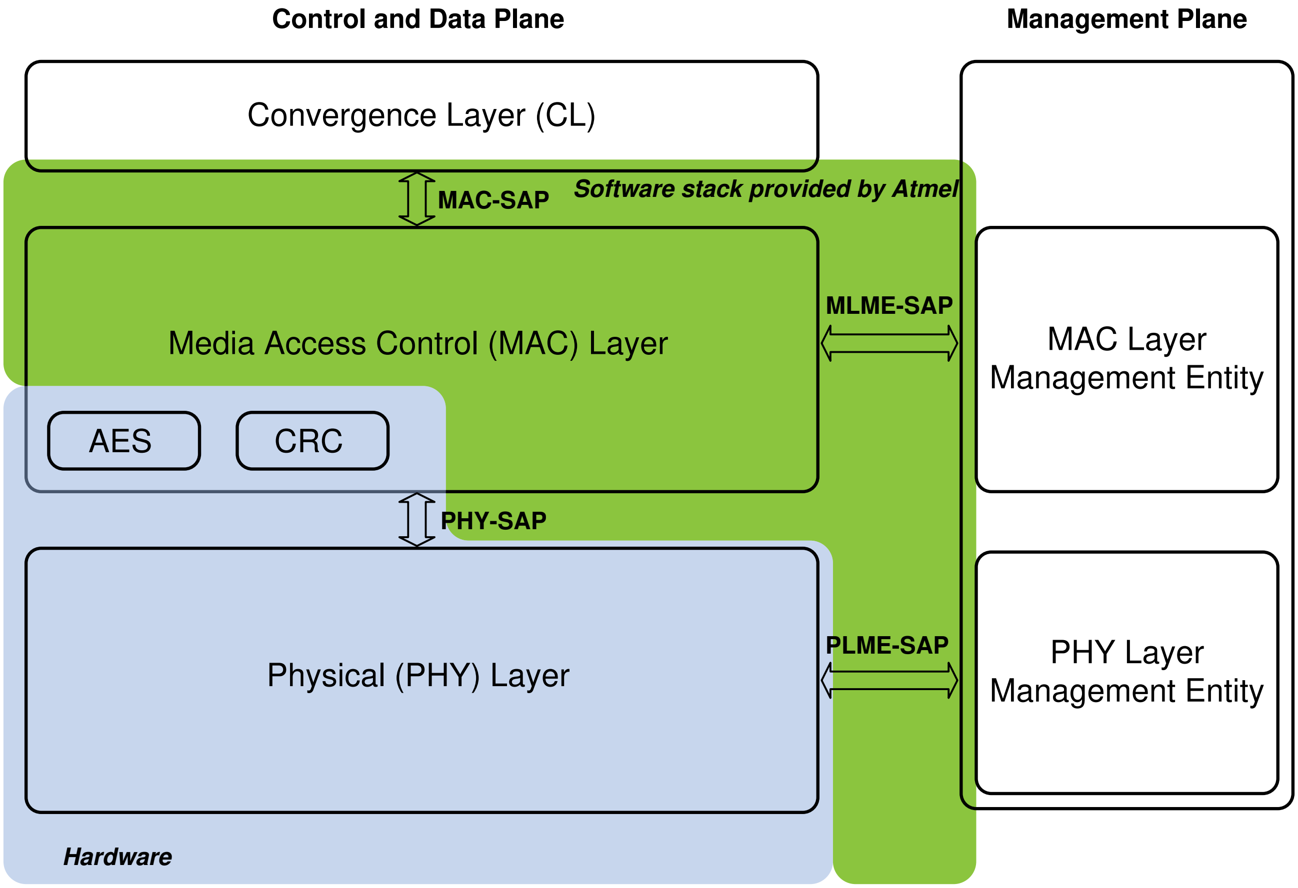
Reset: 0x00

- --: Reserved bits
- **P46_MODE:** This field controls the P4.6/T2/AGC1 output pin (pin no.94).
  - ‘0’: Pin no.94 works as P4.6/T2 output pin.
  - ‘1’: Pin no.94 works as AGC1 output pin.
- **SWITCH_AGC:** This bit switches the AGC0 and AGC1 outputs.
  - ‘0’: Not switched AGC outputs.
  - ‘1’: Switched AGC outputs.

12.2 SAM4SP32A MAC Layer

The SAM4SP32A hardware MAC layer consists of a hardware implementation of some functionalities of the MAC Layer Entity specified in PRIME specification. These features are CRC calculation and AES128 block.

Figure 12-9. SAM4SP32A Software Stack Diagram



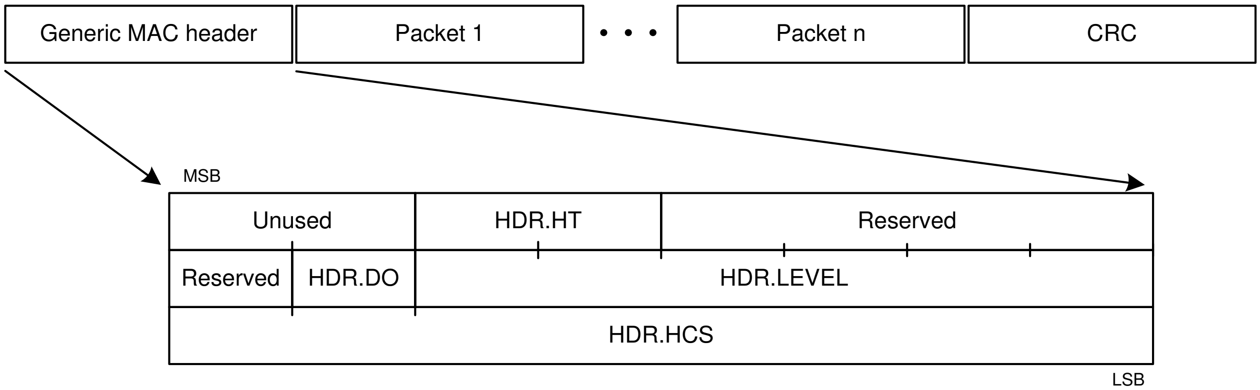
Atmel PRIME stack implements by software the rest of the MAC layer requirements and capabilities. Furthermore, the software package allows the communication with the Management Plane by means of the two Access points described by PRIME (PHY Layer Management Entity SAP and MAC Layer Management Entity SAP) and the interface to communicate MAC layer with the upper layer (Convergence Layer).

Please check the “Atmel PRIME Stack User Manual” for software package detailed description and functionality.

12.2.1 Cyclic Redundancy Check (CRC)

There are three types of MAC PDUs (generic, promotion and beacon) for different purposes, and each one has its own specific CRC. In SAM4SP32A there is a hardware implementation of every CRC type calculated by the MAC layer. This CRC hardware-calculation is enabled by default. Note that the CRC included at the physical layer is also a hardware implementation available in SAM4SP32A and it is also enabled by default.

Figure 12-10. Generic MAC PDU format and generic MAC header detail



In transmission all CRC bytes are real-time calculated and the last bytes of the MAC PDU are overwritten with these values, (provided that the field HT in the first byte of the MAC header in transmission data is equal to the corresponding MAC PDU type).

In reception the CRC bytes are also real-time calculated and these bytes are checked with the last bytes of the MAC PDU. If the CRC is not correct, then an error flag is activated, the complete frame is discarded, and the corresponding error counter is increased. These counters allow the MAC layer to take decisions according to error ratio.

For the Generic MAC PDU, there is an 8-bit CRC in the Generic MAC header, which corresponds to PRIME HDR.HCS. In reception if this CRC doesn't check successfully, the current frame is discarded and no interruption is generated.

This works in the same way as CRC for the PHY layer (CRC Ctrl, located in the PHY header, see PRIME specification for further information).

There is another CRC for the Generic MAC PDU which is the last field of the GPDU. It is 32 bits long and it is used to detect transmission errors. The CRC shall cover the concatenation of the SNA with the GPDU except for the CRC field itself. In reception, if the CRC is not successful then an internal flag is set and the error counter is increased.

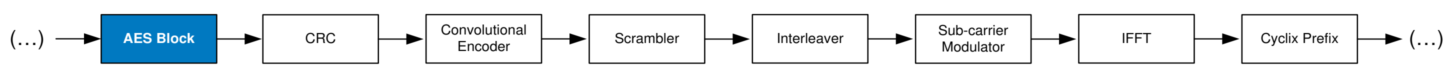
For the Promotion Needed PDU there is an 8-bit CRC, calculated with the first 13 bytes of the header. In reception, if this CRC is not correct, then an internal flag is set and the corresponding error counter is increased.

For the Beacon PDU there is a 32-bit CRC calculated with the same algorithm as the one defined for the CRC of the Generic MAC PDU. This CRC shall be calculated over the complete BPDU except for the CRC field itself. In reception, if this CRC is not successful, then an internal flag is set and the same error counter as for GPDU is increased. The hardware used for this CRC is the same as the one used for GPDU.

12.2.2 Advanced Encryption Standard (AES)

One of the security functionalities in PRIME is the 128-bit AES encryption of data and its associated CRC. SAM4SP32A includes a hardware implementation of this block, and it is used by the physical layer in real-time transmission/reception. It is possible to use this block externally as a peripheral unit, by accessing the specific registers designed to control it. Therefore there are some configurable parameters and input/output buffers to the block.

Figure 12-11. PHY Layer transmitter block diagram



There are two basic operation ways in SAM4SP32A when using PRIME Security Profile 1. The first one is real-time encryption and the second one is independent encryption from the PHY layer.

Real-Time Encryption: the AES128 core is integrated in the physical chain, and data is encrypted and decrypted in real-time when needed. In transmission, data is transferred to the emission buffer by means of the DMA TX channel. Then the 128 bits located in the buffer are encrypted before starting transmission (Note that Beacon PDU, Promotion PDU and Generic MAC header, as well as several control packets, are not encrypted). Data is extracted when required from this buffer until it is empty, and then a new DMA transfer is requested to fill the 16 bytes and a new encryption is executed. The key used for encryption must be set at the corresponding register, and it can vary from a packet to another.

In reception, data is obtained from the PHY layer and it is passed to the AES128 block. When the reception buffer is full with incoming data, the 128 bits are decrypted and transferred to external memory through DMA RX channel. Then the reception buffer is available again to fill with processed data.

The header is always real-time analyzed in order to know if encryption process must be applied.

Independent Encryption: the AES128 core is used as a peripheral unit, accessible with several registers mapped in external memory. In this mode, when in transmission, data must be encrypted previously to the use of the PHY_DATA.request primitive (see PRIME specification), in an independent way. In reception, data passed by the PHY layer is already encrypted and must be decrypted in a subsequent process.

When working with AES block as a peripheral unit, automatic CRC calculation by hardware is disabled.

12.2.3 **MAC Layer Registers**

12.2.3.1 SNA Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
SNA	SNA(47:40)								@FE62
	…							…	
	SNA(7: 0)								@FE67

Name: SNA

Address: 0xFE62 – 0xFE67

Access: Read/write

Reset: 0x00, …, 0x00

- **SNA:** Sub Network Address

  These registers store the 48-bit Sub Network Address. When the system Sub Network Address is available, the SAM4SP32A microcontroller must write it down so the Phy layer will be able to correctly calculate the CRC's, which depend on this parameter.

12.2.3.2 VITERBI_BER_HARD Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VITERBI_BER_HARD	VITERBI_BER_HARD(7:0)							

Name: VITERBI_BER_HARD

Address: 0xFE36

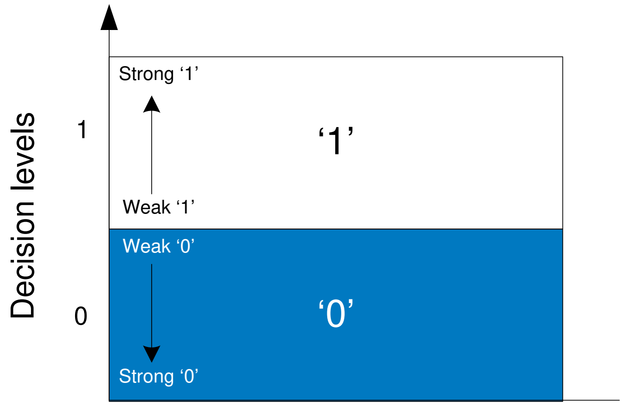
Access: Read only

Reset: 0x00

- **VITERBI_BER_HARD:** This register stores the number of errors accumulated in a message reception using Viterbi hard* decision. The value is cleared by hardware each time a new message is received.

  **Hard Decision: in "hard" detection there are only two decision levels. If the received value is different than the corrected one, the error value taken is "1". Otherwise, the error value taken is "0".*

Figure 12-12. Viterbi Hard detection decision levels



From the value in VITERBI_BER_HARD register it is possible to calculate de Bit Error Rate according to the following formula:

$$BER = \frac{10^{\frac{VTB\_BER\_HARD}{40}} - 1}{100}$$

12.2.3.3 VITERBI_BER_SOFT Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VITERBI_BER_SOFT	VITERBI_BER_SOFT(7:0)							

Name: VITERBI_BER_SOFT

Address: 0xFE37

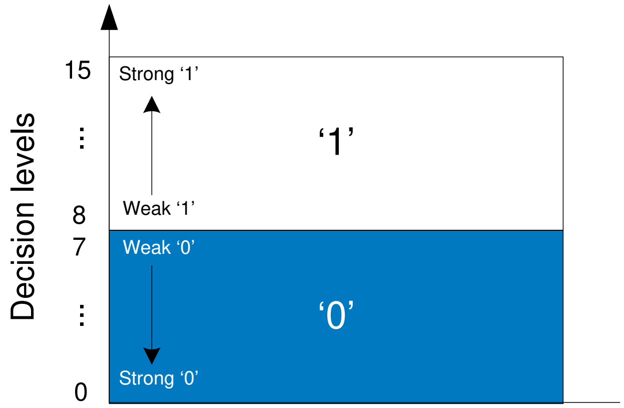
Access: Read only

Reset: 0x00

- **VITERBI_BER_SOFT:** This register stores a value proportional to the number of errors accumulated in a message reception using Viterbi soft* decision. The value is cleared by hardware each time a new message is received.

  **Soft Decision: in "soft" decision there are fifteen decision levels. A strong '0' is represented by a value of "0", while a strong '1' is represented by a value of "15". The rest of values are intermediate, so "7" is used to represent a weak '0' and "8" represents a weak '1'. Soft decision calculates the error in one bit received as the distance in decision levels between the value received (a value in the range 0 to 15) and the corrected one (0 or 15).*

Figure 12-13. Viterbi Hard detection decision levels



12.2.3.4 ERR_CRC32_MAC Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC32_MAC	ERR_CRC32_MAC(15:8)								@0xFEBA
	ERR_CRC32_MAC(7:0)								@0xFEBB

Name: ERR_CRC32_MAC

Address: 0xFEBA – 0xFEBB

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC32_MAC:** 16-bit value that stores the number of received messages that have been discarded by an error in the MAC layer CRC32.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller.

12.2.3.5 ERR_CRC8_MAC Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_MAC	ERR_CRC8_MAC(15:8)								@0xFEBC
	ERR_CRC8_MAC(7:0)								@0xFEBD

Name: ERR_CRC8_MAC

Address: 0xFEBC – 0xFEBD

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_MAC:** 16-bit value that stores the number of received messages that have been discarded by an error in the payload MAC layer CRC8.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller.

12.2.3.6 ERR_CRC8_AES Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_AES	ERR_CRC8_AES(15:8)								@0xFEBE
	ERR_CRC8_AES(7:0)								@0xFEBF

Name: ERR_CRC8_AES

Address: 0xFEBE – 0xFEBF

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_AES:** 16-bit value that stores the number of received messages that have been discarded by an error in the payload AES CRC8.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller.

12.2.3.7 ERR_CRC8_MAC_HD Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_MAC_HD	ERR_CRC8_MAC_HD(15:8)								@0xFEC0
	ERR_CRC8_MAC_HD(7:0)								@0xFEC1

Name: ERR_CRC8_MAC_HD

Address: 0xFEC0 – 0xFEC1

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_MAC_HD:** 16-bit value that stores the number of received messages that have been discarded by an error in the header MAC layer.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller.

12.2.3.8 ERR_CRC8_PHY Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_PHY	ERR_CRC8_PHY(15:8)								@0xFEC2
	ERR_CRC8_PHY(7:0)								@0xFEC3

Name: ERR_CRC8_AES

Address: 0xFEC2 – 0xFEC3

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_PHY:** 16-bit value that stores the number of received messages that have been discarded by an error in the PHY layer CRC8.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller.

12.2.3.9 FALSE_DET_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
FALSE_DET _CONFIG	--		ERR_CRC8 _MAC	INVALID _PROTOCOL	ERROR _LEN	ERROR_PAD _LEN	UNKNOWN _PDU	UNKNOWN _SP

Name: FALSE_DET_CONFIG

Address: 0xFEC4

Access: Read/write

Reset: 0x10

- **--:** Reserved bits
- **ERR_CRC8_MAC:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the MAC layer CRC8 present in its header is wrong.
- **INVALID_PROTOCOL:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the PROTOCOL field indicates a modulation not supported by the system.
- **ERROR_LEN:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the LEN field indicates a not valid message length.
- **ERROR_PAD_LEN:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the PAD_LEN field indicates a not valid message padding length.
- **UNKNOWN_PDU:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the HT field indicates a header type different from BEACON, PROMOTION or GENERIC.
- **UNKNOWN_SP:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the SECURITY_PROTOCOL field is wrong.

12.2.3.10 FALSE_DET Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
FALSE_DET	FALSE_DET(15:8)								@0xFEC5
	FALSE_DET(7:0)								@0xFEC6

Name: FALSE_DET

Address: 0xFEC5 – 0xFEC6

Access: Read/write

Reset: 0x00, 0x00

- **FALSE_DET:** Erroneous non-discarded messages.

  16-bit value that stores the number of received messages that have not been discarded since its PHY layer CRC8 is correct, but in which there are other incorrect fields. The fields that shall be taken into account to increase the counter in case they were wrong can be selected by FALSE_DET_CONFIG register.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller

12.2.3.11 MAX_LEN_DBPSK Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DBPSK	--		MAX_LEN_DBPSK(5:0)					

Name: MAX_LEN_DBPSK

Address: 0xFEC8

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with DBPSK modulation and no Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DBPSK value, the message will be discarded.

12.2.3.12 MAX_LEN_DBPSK_VTB Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DBPSK_VTB	--		MAX_LEN_DBPSK_VTB(5:0)					

Name: MAX_LEN_DBPSK_VTB

Address: 0xFEC9

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK_VTB:** This register sets the maximum length, measured in OFDM symbols that the system allows to receive when working with DBPSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DBPSK_VTB value, the message will be discarded.

12.2.3.13 MAX_LEN_DQPSK Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DQPSK	--		MAX_LEN_DQPSK(5:0)					

Name: MAX_LEN_DQPSK

Address: 0xFECA

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with DQPSK modulation and no Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DQPSK value, the message will be discarded.

12.2.3.14 MAX_LEN_DQPSK_VTB Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DQPSK_VTB	--		MAX_LEN_DQPSK_VTB(5:0)					

Name: MAX_LEN_DQPSK_VTB

Address: 0xFECB

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DQPSK_VTB:** This register sets the maximum length, measured in OFDM symbols that the system allows to receive when working with DQPSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DQPSK_VTB value, the message will be discarded.

12.2.3.15 MAX_LEN_D8PSK Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_D8PSK	--		MAX_LEN_D8PSK(5:0)					

Name: MAX_LEN_D8PSK

Address: 0xFECC

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_D8PSK:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with D8PSK modulation and no Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_D8PSK value, the message will be discarded.

12.2.3.16 MAX_LEN_D8PSK_VTB Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_D8PSK_VTB	--		MAX_LEN_D8PSK_VTB(5:0)					

Name: MAX_LEN_D8PSK_VTB

Address: 0xFECD

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_D8PSK_VTB:** This register sets the maximum length, measured in OFDM symbols that the system allows to receive when working with D8PSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_D8PSK_VTB value, the message will be discarded.

12.2.3.17 AES_PAD_LEN Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AES_PAD_LEN	--				AES_PAD_LEN(3:0)			

Name: AES_PAD_LEN

Address: 0xFE25

Access: Read/write

Reset: 0x00

- **--:** Reserved bits
- **AES_PAD_LEN:** AES protocol works over 16-bytes-lenght blocks. When a block is not 16-bytes long, this register indicates the number of padding bytes to append.

  This register takes values between 0 and 15.

  In transmission, if encryption is being used, microcontroller must write the AES padding length in this register.

  In no-encrypted transmission and in reception, the value in this register is not used.

12.2.3.18 AES_DATA_IN Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AES_DATA_IN	AES_DATA_IN(127:120)								@FFA0
	…							…	
	AES_DATA_IN(7: 0)								@FFAF

Name: AES_DATA_IN

Address: 0xFFA0 – 0xFFAF

Access: Read/write

Reset: 0x00, …, 0x00

- **AES_DATA_IN:** Input buffer for AES128 block.

  This buffer can be written to be encrypted/decrypted by the key in KEY_PERIPH (see 12.2.3.20) register.

  The resulting data could be read at AES_DATA_OUT (see 12.2.3.19) registers.

12.2.3.19 AES_DATA_OUT Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AES_DATA_OUT	AES_DATA_OUT(127:120)								@FFB0
	…								
								…	
	AES_DATA_OUT(7: 0)								@FFBF

Name: AES_DATA_OUT

Address: 0xFFB0 – 0xFFBF

Access: Read only

Reset: 0x00, …, 0x00

- **AES_DATA_OUT:** Output buffer for AES128 block.

  This buffer stores the result of the encryption/decryption processing of data in AES_DATA_IN (see 12.2.3.18) register with the key in KEY_PERIPH (see 12.2.3.20) register.

12.2.3.20 KEY_PERIPH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
KEY_PERIPH	KEY_PERIPH(127:120)								@FFC0
	…								
								…	
	KEY_PERIPH (7: 0)								@FFCF

Name: KEY_PERIPH

Address: 0xFFC0 – 0xFFCF

Access: Read/write

Reset:

KEY_PERIPH(127:120) :	0x00;	KEY_PERIPH(119:112) :	0x01;	KEY_PERIPH(111:104) :	0x02;
KEY_PERIPH(103:96) :	0x03;	KEY_PERIPH(95:88) :	0x04;	KEY_PERIPH(87:80) :	0x05;
KEY_PERIPH(79:72) :	0x06;	KEY_PERIPH(71:64) :	0x07;	KEY_PERIPH(63:56) :	0x08;
KEY_PERIPH(55:48) :	0x09;	KEY_PERIPH(47:40) :	0x0A;	KEY_PERIPH(39:32) :	0x0B;
KEY_PERIPH(31:24) :	0x0C;	KEY_PERIPH(23:16) :	0x0D;	KEY_PERIPH(15:8) :	0x0E;
KEY_PERIPH(7:0) :	0x0F;				

- **KEY_PERIPH:** Key for AES128 block when used as peripheral part.
  This key is used for encrypting/decrypting data in AES_DATA_IN registers.

12.2.3.21 KEY_PHY Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
KEY_PHY	KEY_PHY(127:120)								@FFD0
	…							…	
	KEY_PHY(7: 0)								@FFDF

Name: KEY_PHY

Address: 0xFFD0 – 0xFFDF

Access: Read/write

Reset:

KEY_PHY(127:120):	0x00;	KEY_PHY(119:112) :	0x01;	KEY_PHY(111:104) :	0x02;
KEY_PHY(103:96) :	0x03;	KEY_PHY(95:88) :	0x04;	KEY_PHY(87:80) :	0x05;
KEY_PHY(79:72) :	0x06;	KEY_PHY(71:64) :	0x07;	KEY_PHY(63:56) :	0x08;
KEY_PHY(55:48) :	0x09;	KEY_PHY(47:40) :	0x0A;	KEY_PHY(39:32) :	0x0B;
KEY_PHY(31:24) :	0x0C;	KEY_PHY(23:16) :	0x0D;	KEY_PHY(15:8) :	0x0E;
KEY_PHY(7:0) :	0x0F;				

- **KEY_PHY:** Key for AES128 block when used by the physical layer

  This key is used in real time encryption/decryption for Security Profile 1. When any of the DMA channels of the physical layer accesses to the memory, then this key and the input data are multiplexed to the AES128-core. Also output data is multiplexed in order to provide encrypted/decrypted data to the physical buffer.

12.2.3.22 AES_SFR Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AES_SFR	--					READY	START	CIPHER

Name: AES_SFR

Address: 0xFFE0

Access: Read/write

Reset: 0x00

- --: Reserved bits.
- **READY:** Flag to indicate encryption/decryption process completion.
  When the encryption/decryption has been completed, this flag is set to ‘1’.
  This flag is automatically cleared when an encryption/decryption process begins.
- **START:** When this bit is set to ‘1’, the encryption/decryption process is triggered.
  If encryption/decryption starts successfully, then this bit is automatically cleared to ‘0’.
- **CIPHER:** This field indicates if data must be encrypted or decrypted.
  - ‘0’ - Decryption mode
  - ‘1’ - Encryption mode

13. Electrical Characteristics

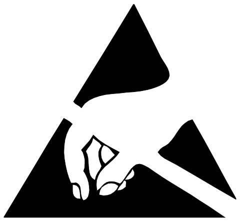
13.1 Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

Table 13-1. **SAM4SP32A Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Operating Temperature (Industrial)	OT	-40 to +85	ºC
Storage Temperature	TST	-55 to 125	ºC
Voltage on Input Pins With Respect to Ground	--	-0.3 to +4.0	V
Maximum Operating Voltage (VDDCORE)	VDDCORE max	1.32	V
Maximum Operating Voltage (VDDIO)	VDDIO max	4.0	V
Junction Temperature	TJ	-40 to 125	ºC
Total DC Output Current On all I/O lines	IO	300	mA

ATTENTION observe EDS precautions



Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection

13.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to +85°C, unless otherwise specified.

Table 13-2. **SAM4SP32A DC Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{VDDCORE}$	DC Supply Core		1.08	1.20	1.32	V
V_{VDDIO}	DC Supply I/Os	[1] [2]	3.00	3.30	3.60	
V_{VDDPLL}	PLLA, PLLB and Main Oscillator Suplly		1.08	--	1.32	
A_{VDD}	PLC Analog Converter Power Supply		3.00	3.30	3.60	
V_{IL}	Input Low-level Voltage	PA0-PA25, PB0-PB12, PC0, PC5, PC26	-0.3		MIN[0.8V:0.3 x V_{VDDIO}]	
V_{IH}	Input High-level Voltage	PA0-PA25, PB0 PB12, PC0, PC5, PC26	MIN[2.0V:0.7 x V_{VDDIO}]		V_{VDDIO} + 0.3V	
V_{OH}	Output High-level Voltage	PA0-PA25, PB0-PB12, PC0, PC5, PC26 I_{OL} = 4.0 mA	V_{VDDIO} -0.4V			
		VDDIO [3.0V : 3.60V] PB0-PB12	V_{VDDIO} -0.15V			
V_{OL}	Output Low-level Voltage	PA0-PA25, PB0 PB12, PC0, PC5, PC26 I_{OL} = 4.0 mA			0.4	
		VDDIO [3.0V : 3.60V] PB0-PB12			0.15	
V_{Hys}	Hysteresis Voltage	PA0-PA25, PB0-PB9, PB12, PC0,PC5,PC26 (Hysteresis mode enabled)	150			mV
I_{OH}	I_{OH} (or I_{SOURCE})	VDDIO [3V : 3.60V] ;V_{OH} = V_{VDDIO} - 0.4V - PA14 (SPCK) - PA[12-13], - PA[0-3] - Other pins [1] VDDIO [3.0V : 3.60V] - PB[10-11] -EMIT[1:6] -Other PLC pins			 -4 -4 -2 -2 -30 -20 -10	mA
		VDDIO [3V : 3.60V] ; V_{OH} = V_{VDDIO} - 0.4V - NRST			-2	

Table 13-2. **SAM4SP32A DC Characteristics (Continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OL}	I_{OL} (or I_{SINK})	VDDIO [3V : 3.60V] ;V_{OH} = V_{VDDIO} - 0.4V - PA14 (SPCK) - PA[12-13], - PA[0-3] - Other pins [1] VDDIO [3.0V : 3.60V] - PB[10-11] -EMIT[1:6] -Other PLC pins			4 4 2 2 30 20 10	
		VDDIO [3V : 3.60V] ; V_{OH} = V_{VDDIO} - 0.4V - NRST			2	
I_{IL}	Input Low	Pull_up OFF	-1		1	µA
		Pull_up ON	10		50	
I_{IH}	Input High	Pull_up OFF	-1		1	
		Pull_up ON	10		50	
R_{PULLUP}	Internal Pull-up Resistor	PA0-PA25, PB0- PB12, PC0, PC5, PC26, NRST	70	100	130	kΩ
$R_{PULLDOWN}$	Internal Pull-down Resistor	PA0-PA25, PB0-PB12, PC0, PC5, PC26, NRST	70	100	130	
PLC_{RPU}	PLC Internal Pull-up Resistor	3.3v I/O	10	33	80	
PLC_{RPD}	PLC Internal Pull-down Resistor	3.3v I/O	10	33	80	

Note:

1. At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V
2. VDDIO voltage needs to be equal or below to (VDDIN voltage +0.5V)

Table 13-3. **1.2V Voltage Regulator Characteristics (VDDOUT12)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	DC Input Voltage Range	(4)(5)	1.6	3.3	3.6	V
V_{VDDOUT}	DC Output Voltage	Normal Mode Standby Mode		1.2 0		V
$V_{ACCURACY}$	Output Voltage Accuracy	I_{Load} = 0.8mA to 80 mA (after trimming)	-3		3	%
I_{LOAD}	Maximum DC Output Current	V_{VDDIN} > 1.8V V_{VDDIN} ≤ 1.8V			80 40	mA
$I_{LOAD-START}$	Maximum Peak Current during startup	See Note(3)			400	mA
$D_{DROPOUT}$	Dropout Voltage	V_{VDDIN} = 1.6V, I_{Load} = Max		400		mV
V_{LINE} $V_{LINE-TR}$	Line Regulation Transient Line regulation	V_{VDDIN} from 2.7V to 3.6V; I_{Load} MAX V_{VDDIN} from 2.7V to 3.6V; tr = tf = 5µs; I_{Load} Max		10 50	30 150	mV
V_{LOAD} $V_{LOAD-TR}$	Load Regulation Transient Load Regulation	V_{VDDIN} ≥ 1.8V; I_{Load} = 10% to 90% MAX V_{VDDIN} ≥ 1.8V; I_{Load} = 10% to 90% MAX tr = tf = 5 µs		20 50	40 150	mV
I_Q	Quiescent Current	Normal Mode; @ I_{Load} = 0 mA @ I_{Load} = 80 mA Standby Mode;		5 500	1	µA
CD_{IN}	Input Decoupling Capacitor	Cf. External Capacitor Requirements (1)		4.7		µF
CD_{OUT}	Output Decoupling Capacitor	Cf. External Capacitor Requirements (2) ESR	1.85 0.1	2.2	5.9 10	µF Ω
T_{ON}	Turn on Time	CD_{OUT}= 2.2µF, V_{VDDOUT} reaches 1.2V (+/-3%)		300		µs
T_{OFF}	Turn off Time	CD_{OUT}= 2.2µF			40	ms

Note:

1. A 10µF or higher ceramic capacitor must be connected between VDDIN and the closest GND pin of the device. This large decoupling capacitor is mandatory to reduce startup current, improving transient response and noise rejection.
2. To ensure stability, an external 2.2µF output capacitor, CDOUT must be connected between the VDDOUT and the closest GND pin of the device. The ESR (Equivalent Series Resistance) of the capacitor must be in the range 0.1 to 10 ohms. Solid tantalum and multilayer ceramic capacitors are all suitable as output capacitor. A 100nF bypass capacitor between VDDOUT and the closest GND pin of the device helps decreasing output noise and improves the load transient response.
3. Defined as the current needed to charge external bypass/decoupling capacitor network.
4. At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V
5. VDDIO voltage needs to be equal or below to (VDDIN voltage +0.5V)

Table 13-4. **Core Power Supply Brownout Detector Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Falling Threshold[1]	V_{TH-}		0.98	1.0	1.04	V
Hysteresis	V_{HYST}				110	mV
Supply Rising Threshold	V_{TH+}		0.8	1.0	1.08	V
Current Consumption on VDDCOARE	I_{DDON}	Brownout Detector enabled			24	µA
	I_{DDOFF}	Brownout Detector disable			2	
Current Consumption on VDDIO	I_{DD33ON}	Brownout Detector enabled			24	
	$I_{DD33OFF}$	Brownout Detector disable			2	
V_{TH-} detection propagation time	Td-	[-40/+85°C]	-2.5		+2.5	%
Start Time	T_{START}	From disable state to enable state			320	µs

Note:

1. The product is guaranteed to be functional at V_{TH-}

Figure 13-1. Core Brownout Output Waveform

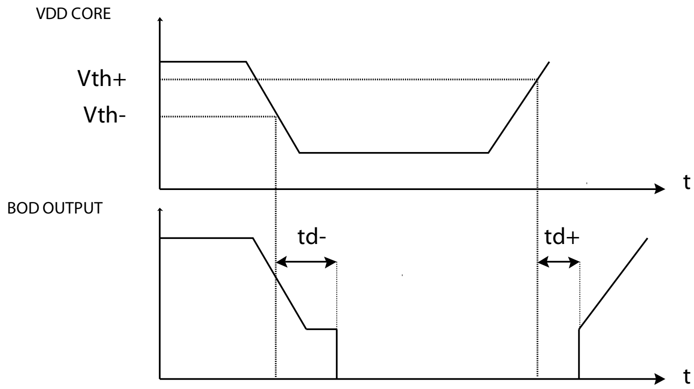


Table 13-5. **VDDIO Supply Monitor**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Monitor Threshold	V_{TH}	16 selectable steps	1.6		3.34	V
Threshold Level Accuracy	$T_{ACCURACY}$	[-40/+85°C]	-2.5		+2.5	%
Hysteresis	V_{HYST}			20	30	mV
Current Consumption on VDDCOARE	I_{DDON}	Enabled			40	µA
	I_{DDOFF}	Disable			10	
Start Time	T_{START}	From disable state to enable state			320	µs

Table 13-6. **Threshold Selection**

Digital Code	Threshold min (V)	Threshold typ (V)	Threshold max (V)
0000	1.58	1.6	1.62
0001	1.7	1.72	1.74
0010	1.82	1.84	1.86
0011	1.94	1.96	1.98
0100	2.05	2.08	2.11
0101	2.17	2.2	2.23
0110	2.29	2.32	2.35
0111	2.41	2.44	2.47
1000	2.53	2.56	2.59
1001	2.65	2.68	2.71
1010	2.77	2.8	2.83
1011	2.8	2.92	2.95
1100	3.0	3.04	3.07
1101	3.12	3.16	3.2
1110	3.24	3.28	3.32
1111	3.36	3.4	3.44

Figure 13-2. VDDIO Supply Monitor

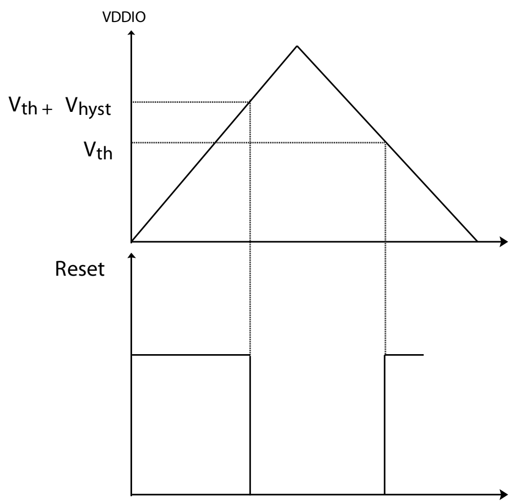


Table 13-7. **Zero-Power-on Reset Characteristics**

Parameter	Symbol	Coditions	Min	Typ	Max	Units
Threshold voltage rising	V_{TH+}	At Startup	1.45	1.53	1.59	V
Threshold voltage falling	V_{TH-}		1.35	1.45	1.55	V
Reset Time-out Period	Tres		100	240	500	µs

Figure 13-3. Zero-Power-on Reset Characteristics

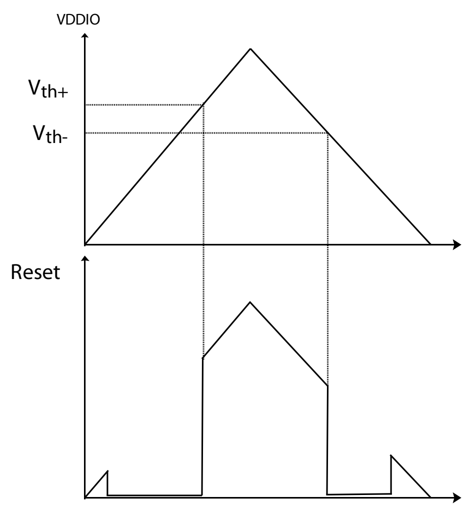


Table 13-8. **DC Flash Characteristics**

Parameter	Symbol	Coditions	Typ	Max	Units
Active current	I_{CC}	Random 144-bit Read: Maximum Read Frequency onto VDDCORE = 1.2 @ 25°C	16	25	mA
		Random 72-bit Read: Maximum Read Frequency onto VDDCORE = 1.2 @ 25°C	10	18	
		Program onto VDDCORE = 1.2V @ 25°C	3	5	

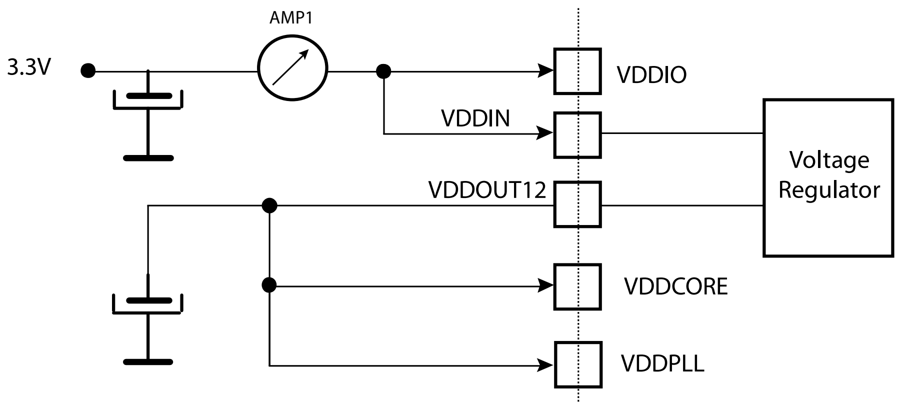
13.3 Power Consumption

- Power consumption of the device according to the different Low Power Mode Capabilities (Backup, Wait, Sleep) and Active Mode.
- Power consumption on power supply in different modes: Backup, Wait, Sleep and Active.
- Power consumption by peripheral: calculated as the difference in current measurement after having enabled then disabled the corresponding clock.

13.3.1 Backup Mode Current Consuption

The Backup Mode configuration and measurements are defined as follows.

Figure 13-4. Measurement Setup



13.3.1.1 Configuration A

- Supply Monitor on VDDIO is disabled
- RTT and RTC not used
- Embedded slow clock RC Oscillator used
- One WKUPx enabled
- Current measurement on AMP1 (See Figure 13-4)

13.3.1.2 Configuration B

- Supply Monitor on VDDIO is disabled
- RTT used
- One WKUPx enabled
- Current measurement on AMP1 (See Figure 13-4)
- 32 KHz Crystal Oscillator used

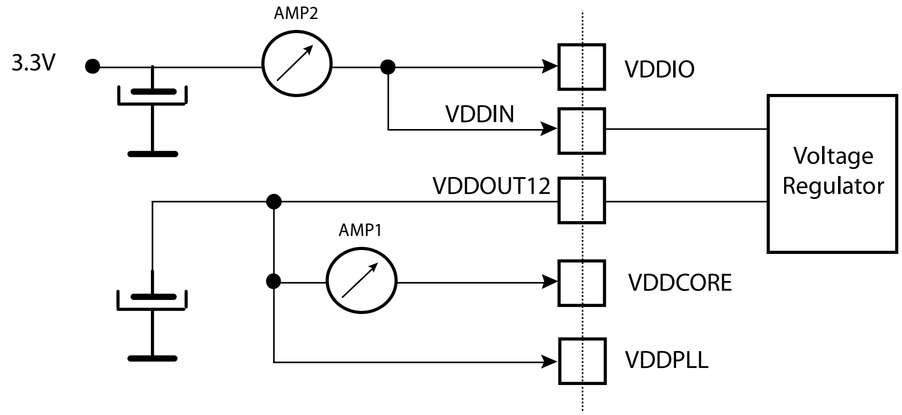
Table 13-9. **Power Consumption for Backup Mode Configuration A and B**

Conditions	Total Consumption (AMP1) Configuration A	Total Consumption (AMP1) Configuration B	Unit
VDDIO = 3.3V @25°C VDDIO = 3.0V @25°C VDDIO = 2.5V @25°C VDDIO = 1.8V @25°C	1.98 1.79 1.51 1	1.85 1.66 1.37 0.95	µA
VDDIO = 3.3V @85°C VDDIO = 3.0V @85°C VDDIO = 2.5V @85°C VDDIO = 1.8V @85°C	13.0 12.0 10.5 8.78	12.42 11.42 10.05 8.42	µA

13.3.2 Sleep and Wait Mode Current Consumption

The Wait Mode and Sleep Mode configuration and measurements are defined below.

Figure 13-5. Measurement Setup for Sleep Mode



13.3.2.1 Sleep Mode

- Core Clock OFF
- Master Clock (MCK) running at various frequencies with PLLA or the fast RC oscillator.
- Fast start-up through WKUP0-15 pins
- Current measurement as shown in figure Figure 13-6
- All peripheral clocks deactivated

Table 13-10 below gives current consumption in typical conditions.

Table 13-10. **Typical Current Consumption for Sleep Mode**

Conditions	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	Unit
Figure 13-6 @25°C MCK = 48 MHz There is no activity on the I/Os of the device.	2.52	3.04	mA

Figure 13-6. Current Consumption in Sleep Mode (AMP1) versus Master Clock ranges (Condition from Table 13-10)

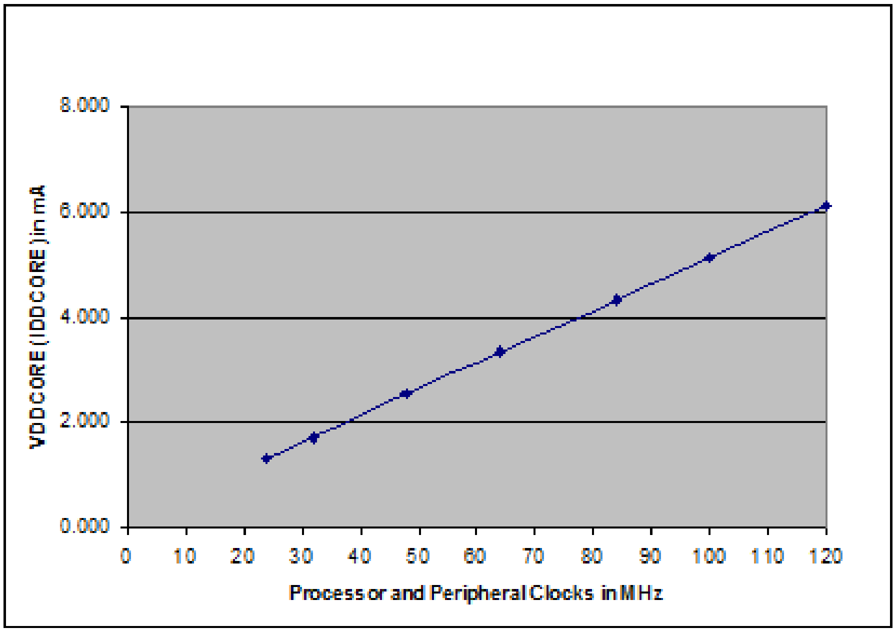
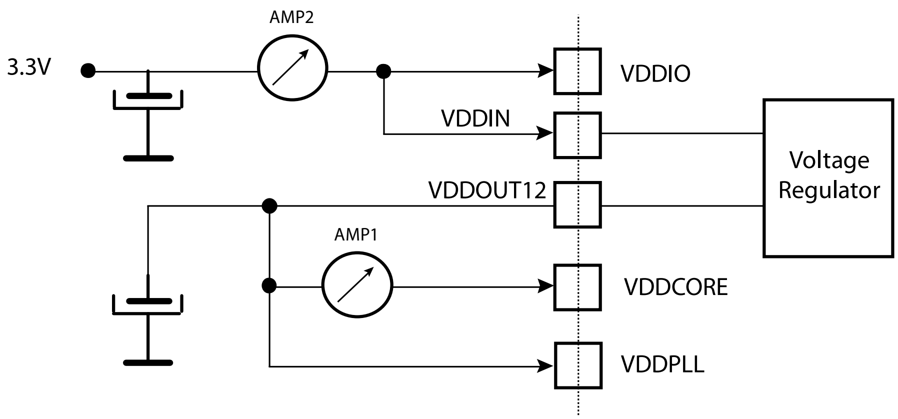


Table 13-11. **Sleep mode Current consumptionversus Master Clock (MCK) variation with PLLA**

Core Clock/MCK (MHz)	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	Unit
120	8.1	9.9	mA
100	6.7	8.3	mA
84	5.7	7.1	mA
64	4.5	6.4	mA
48	3.4	4.8	mA
32	2.3	3.38	mA
24	1.8	3.31	mA

13.3.2.2 Wait Mode

Figure 13-7. Measurement Setup for Wait Mode



- Core Clock and Master Clock Stopped
- Current measurement as shown in the above figure
- All Peripheral clocks deactivated

Table 13-12 gives current consumption in typical conditions.

Table 13-12. **Typical Current Consumption in Wait Mode**

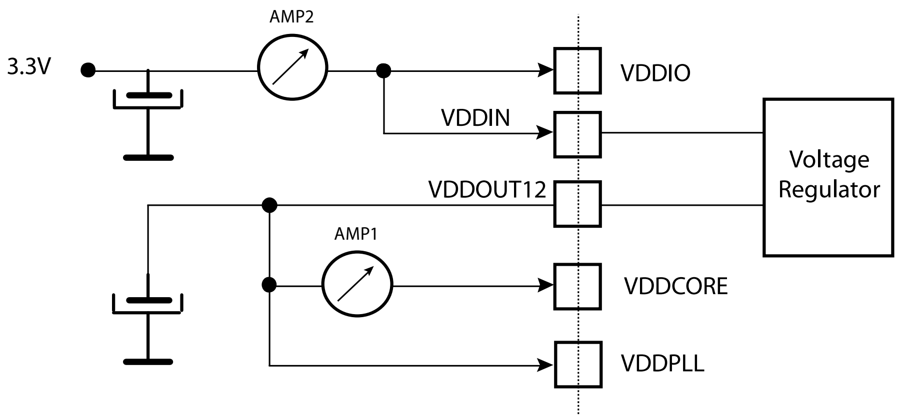
Conditions	VDDOUT Consumption (AMP1)	Total Consumption (AMP2)	Unit
See Figure 13-7 @25°C There is no activity on the I/Os of the device. With the Flash in Standby Mode	20.4	32.2	µA
See Figure 13-7 @25°C There is no activity on the I/Os of the device. With the Flash in Deep Power Down Mode	20.5	27.6	µA

13.3.3 Active Mode Power Consumption

The Active Mode configuration and measurements are defined as follows:

- VDDIO = VDDIN = 3.3V
- VDDCORE = 1.2V (Internal Voltage regulator used)
- T_A = 25°C
- Application Running from Flash Memory with128-bit access Mode
- All Peripheral clocks are deactivated.
- Master Clock (MCK) running at various frequencies with PLLA or the fast RC oscillator.
- Current measurement on AMP1 (VDDCORE) and total current on AMP2

Figure 13-8. Active Mode Measurement Setup



Tables below give Active Mode Current Consumption in typical conditions.

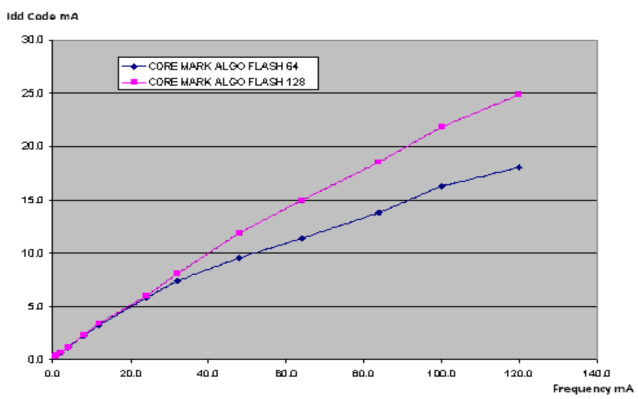
- VDDCORE at 1.2V
- Temperature = 25°C

Table 13-13. **Active Power Consumption with VDDCORE @ 1.2V (VDDOUT12) running from Flash Memory or SRAM**

Core Clock (MHz)	CoreMark				Unit
	128-bit Flash access[(1)]		64-bit Flash access[(1)]		
	AMP1	**AMP2**	**AMP1**	**AMP2**	mA
120	24.9	28.8	18	21.4	
100	21.9	25.4	16.3	19.5	
84	18.5	21.4	13.8	16.6	
64	15.0	17.6	11.4	13.9	
48	11.9	14.3	9.6	11.8	
32	8.1	9.9	7.4	9.3	
24	6.0	7.7	5.8	7.5	
12	3.4	6.1	3.2	6.0	
8	2.3	4.5	2.2	4.5	
4	1.2	2.6	1.2	2.9	
2	0.7	1.9	0.7	2.0	
1	0.4	1.3	0.4	1.6	
0.5	0.3	1.1	0.3	1.3	

Note:

1. Flash Wait State (FWS) in EEFC_FMR adjusted versus Core Frequency



13.3.4 Peripheral Power Consumption in Active Mode

Table 13-14. **Power Consumption on $V_{VDDCORE}$[(1)] (when PRIME PLC Transceiver is turned off)**

Peripheral	Consumption (Typ)	Unit
PIO Controller A (PIOA)	5.6	µA/MHz
PIO Controller B (PIOB)	7.5	
PIO Controller C (PIOC)	5.9	
UART	3.8	
USART	7.7	
PWM	10.5	
TWI	5.8	
PLC_Bridge	6.9	
Timer Counter (TCx)	4.7	
ACC	1.3	
CRCCU	1.4	
SMC	3.6	
SSC	6.1	
UDP	5	

Table 13-15. **PRIME PLC Transceiver Peripheral Power Consumption**

Parameter	Condition	Symbol	Rating			Unit
			Min.	Typ.	Max.	
Power Consumption	[2]	P_{25}	--	260	--	mW
Power Consumption (worst case)	[3]	P_{85}	--	--	355	--

Note:

1. VDDIO = 3.3V, $V_{VDDCORE}$ = 1.08V, T_A = 25°C
2. VDDIO = 3.3V, $V_{VDDCORE}$ = 1.08V, T_A = 25°C
3. VDDIO = 3.3V, $V_{VDDCORE}$ = 1.08V, T_A = 25°C

13.4 Oscillator Characteristics

13.4.1 32 kHz RC Oscillator Characteristics

Table 13-16. **32 kHz RC Oscillator Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	RC Oscillator Frequency		20	32	44	kHz
	Frequency Supply Dependency		-3		3	%/V
	Frequency Temperature Dependency	Over temperature range (-40°C/ +85°C) versus 25°C	-7		7	%
Duty	Duty Cycle		45	50	55	%
T_{ON}	Startup Time				100	µs
I_{DDON}	Current Consumption	After Startup Time Temp. Range = -40°C to +125°C Typical Consumption at 2.2V supply and Temp = 25°C		540	860	nA

13.4.2 4/8/12 MHz RC Oscillators Characteristics

Table 13-17. **4/8/12 MHz RC Oscillators Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{Range}	RC Oscillator Frequency Range	[1]	4		12	MHz
ACC_4	4 MHz Total Accuracy	-40°C<Temp<+85°C 4 MHz output selected [1][2]			±30	%
ACC_8	8 MHz Total Accuracy	-40°C<Temp<+85°C 8 MHz output selected [1][2]			±30	%
		-40°C<Temp<+85°C 8 MHz output selected [1][3]			±5	
ACC_{12}	12 MHz Total Accuracy	-40°C<Temp<+85°C 12 MHz output selected [1][2]			±30	%
		-40°C<Temp<+85°C 12 MHz output selected [1][3]			±5	
	Frequency deviation versus trimming code	8 MHz 12 MHz		47 64		kHz/trimming code
Duty	Duty Cycle		45	50	55	%
T_{ON}	Startup Time				10	µs
I_{DDON}	Active Current Consumption[2]	4MHz 8MHz 12MHz		50 65 82	75 95 118	µA

Note:

1. Frequency range can be configured in the Supply Controller Registers
2. Not trimmed from factory
3. After Trimming from factory

The 4/8/12 MHz Fast RC oscillator is calibrated in production. This calibration can be read through the Get CALIB Bit command (see EEFC section) and the frequency can be trimmed by software through the PMC.

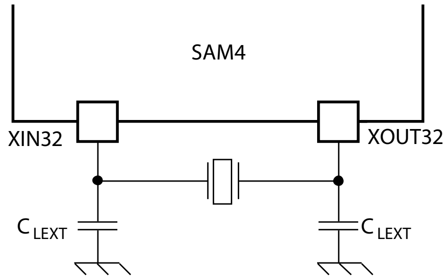
13.4.3 32.768 kHz Crystal Oscillator Characteristics

Table 13-18. **32.768 kHz Crystal Oscillator Characteristics**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{req}	Operating Frequency	Normal mode with crystal				32.768	KHz
	Supply Ripple Voltage (on VDDIO)	Rms value, 10 KHz to 10 MHz				30	mV
	Duty Cycle			40	50	60	%
	Startup Time	Rs < 50KΩ Rs < 100KΩ (1)	$C_{crystal}$ = 12.5pF $C_{crystal}$ = 6pF $C_{crystal}$ = 12.5pF $C_{crystal}$ = 6pF			900 300 1200 500	ms
Iddon	Current consumption	Rs < 50KΩ Rs < 100KΩ (1)	$C_{crystal}$ = 12.5pF $C_{crystal}$ = 6pF $C_{crystal}$ = 12.5pF $C_{crystal}$ = 6pF		550 380 820 530	1150 980 1600 1350	nA
P_{ON}	Drive level					0.1	µW
R_f	Internal resistor	between XIN32 and XOUT32			10		MΩ
C_{LEXT}	Maximum external capacitor on XIN32 and XOUT32					20	pF
C_{para}	Internal Parasitic Capacitance			0.6	0.7	0.8	pF

Note:

1. R_S is the series resitor



$C_{LEXT} = 2x(C_{CRYSTAL} - C_{para} - C_{PCB})$.

Where C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the SAM4 pin.

13.4.4 32.768 kHz Crystal Characteristics

Table 13-19. **Crystal Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor (R_{S})	Crystal @ 32.768 KHz		50	100	KΩ
C_M	Motional capacitance	Crystal @ 32.768 KHz	0.6		3	fF
C_{SHUNT}	Shunt capacitance	Crystal @ 32.768 KHz	0.6		2	pF

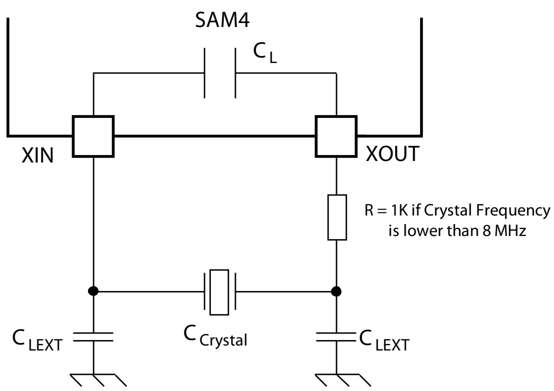
13.4.5 3 to 20 MHz Crystal Oscillator Characteristics

Table 13-20. **3 to 20 MHz Crystal Oscillator Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{req}	Operating Frequency	Normal mode with crystal	3	16	20	MHz
	Supply Ripple Voltage (on VDDPLL)	Rms value, 10 KHz to 10 MHz			30	mV
	Duty Cycle		40	50	60	%
T_{ON}	Startup Time	3 MHz, C_{SHUNT} = 3pF 8 MHz, C_{SHUNT} = 7pF 16 MHz, C_{SHUNT} = 7pF with Cm = 8fF 16 MHz, C_{SHUNT} = 7pF with Cm = 1.6fF 20 MHz, C_{SHUNT} = 7pF			14.5 4 1.4 2.5 1	ms
I_{DD_ON}	Current consumption (on VDDIO)	3 MHz [(2)] 8 MHz[(3)] 16 MHz[(4)] 20 MHz[(5)]		230 300 390 450	350 400 470 560	µA
P_{ON}	Drive level	3 MHz 8 MHz 16 MHz, 20 MHz			15 30 50	µW
R_f	Internal resistor	between XIN and XOUT		0.5		MΩ
C_{LEXT}	Maximum external capacitor on XIN and XOUT		12.5		17.5	pF
C_L	Internal Equivalent Load Capacitance	Integrated Load Capacitance (XIN and XOUT in series)	7.5	9.5	10.5	pF

Note:

1. R_S = 100-200 Ohms; Cs = 2.0 - 2.5pF; Cm = 2 – 1.5 fF(typ, worst case) using 1 K<Symbol>W serial resistor on XOUT.
2. R_S = 50-100 Ohms; Cs = 2.0 - 2.5pF; Cm = 4 - 3 fF(typ, worst case).
3. R_S = 25-50 Ohms; Cs = 2.5 - 3.0pF; Cm = 7 - 5 fF (typ, worst case).
4. R_S = 20-50 Ohms; Cs = 3.2 - 4.0pF; Cm = 10 - 8 fF(typ, worst case).



$C_{LEXT} = 2x(C_{CRYSTAL} – C_L – C_{PCB})$.

Where C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the SAM4 pin

13.4.6 3 to 20 MHz Crystal Characteristics

Table 13-21. **3 to 20 MHz Crystal Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor (Rs)	Fundamental @ 3 MHz Fundamental @ 8 MHz Fundamental @ 12 MHz Fundamental @ 16 MHz Fundamental @ 20 MHz			200 100 80 80 50	Ω
C_M	Motional capacitance				8	fF
C_{SHUNT}	Shunt capacitance				7	pF

13.4.7 Crystal Oscillator Design Considerations Information

13.4.7.1 Choosing a Crystal

When choosing a crystal for the 32768 Hz Slow Clock Oscillator or for the 3-20 MHz Oscillator, several parameters must be taken into account. Important parameters between crystal and SAM4S specifications are as follows:

- Load Capacitance
  - $C_{crystal}$ is the equivalent capacitor value the oscillator must "show" to the crystal in order to oscillate at the target frequency. The crystal must be chosen according to the internal load capacitance (C_L) of the on-chip oscillator. Having a mismatch for the load capacitance will result in a frequency drift.
- Drive Level
  - Crystal drive level >= Oscillator Drive Level. Having a crystal drive level number lower than the oscillator specification may damage the crystal.
- Equivalent Series Resistor (ESR)
  - Crystal ESR <= Oscillator ESR Max. Having a crystal with ESR value higher than the oscillator may cause the oscillator to not start.
- Shunt Capacitance
  - Max. crystal Shunt capacitance <= Oscillator Shunt Capacitance (C_{SHUNT}). Having a crystal with ESR value higher than the oscillator may cause the oscillator to not start.

13.4.7.2 Printed Circuit Board (PCB)

SAM4SP32A Oscillators are low power oscillators requiring particular attention when designing PCB systems.

13.5 PLLA, PLLB Characteristics

Table 13-22. **Supply Voltage Phase Lock Loop Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDPLL	Supply Voltage Range		1.08	1.2	1.32	V
	Allowable Voltage Ripple	RMS Value 10 kHz to 10 MHz RMS Value > 10 MHz			20 10	mV

Table 13-23. **PLLA and PLLB Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{IN}	Input Frequency		3		32	MHz
F_{OUT}	Output Frequency		80		240	MHz
I_{PLL}	Current Consumption	Active mode @ 80 MHz @1.2V Active mode @ 96 MHz @1.2V Active mode @ 160 MHz @1.2V Active Mode @240 MHz @1.2V		0.94 1.2 2.1 3.34	1.2 1.5 2.5 4	mA
T_{START}	Settling Time			60	150	µS

13.6 USB Transceiver Characteristics

13.6.1 Typical Connections

For typical connection please refer to the USB Device Section.

13.6.2 Electrical Characteristics

Table 13-24. **Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Input Levels				
V_{IL}	Low Level				0.8	V
V_{IH}	High Level		2.0			V
V_{DI}	Differential Input Sensitivity	|(D+) - (D-)|	0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
C_{IN}	Transceiver capacitance	Capacitance to ground on each line			9.18	pF
I	Hi-Z State Data Line Leakage	0V < V_{IN} < 3.3V	-10		+10	µA
R_{EXT}	Recommended External USB Series Resistor	In series with each USB pin with ±5%		27		Ω
		Output Levels				
V_{OL}	Low Level Output	Measured with R_L of 1.425 kΩ tied to 3.6V	0.0		0.3	V
V_{OH}	High Level Output	Measured with R_L of 14.25 kΩ tied to GND	2.8		3.6	V
V_{CRS}	Output Signal Crossover Voltage	Measure conditions described in Figure 13-9	1.3		2.0	V
		Consumption				
I_{VDDIO}	Current Consumption	Transceiver enabled in input mode DDP = 1 and DDM = 0		105	200	µA
$I_{VDDCORE}$	Current Consumption			80	150	µA

Table 13-23. **Electrical Characteristics (Continued)**

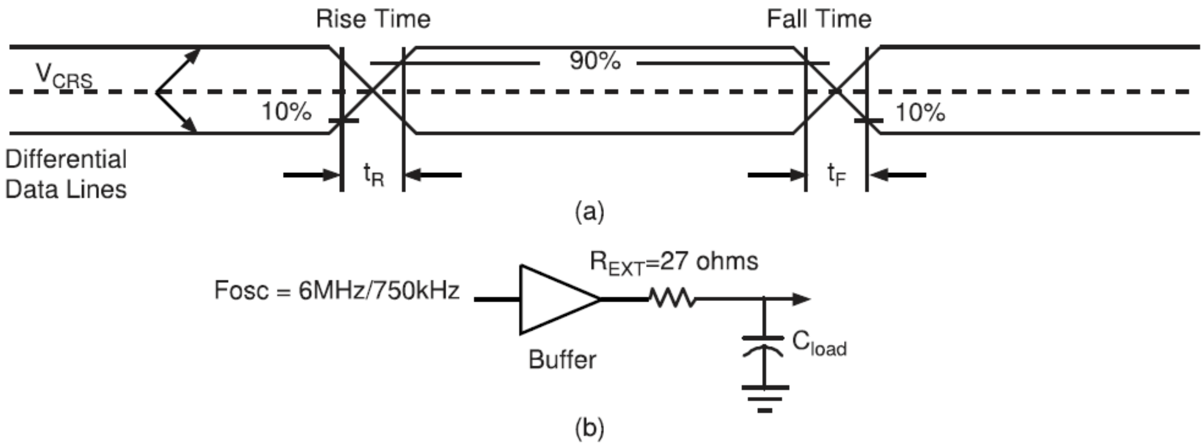
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pull-up Resistor						
R_{PUI}	Bus Pull-up Resistor on Upstream Port (idle bus)		0.900		1.575	kΩ
R_{PUA}	Bus Pull-up Resistor on Upstream Port (upstream port receiving)		1.425		3.090	kΩ

13.6.3 Switching Characteristics

Table 13-24. **In Full Speed**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FR}	Transition Rise Time	C_{LOAD} = 50 pF	4		20	ns
t_{FE}	Transition Fall Time	C_{LOAD} = 50 pF	4		20	ns
t_{FRFM}	Rise/Fall time Matching		90		111.11	%

Figure 13-9. USB Data Signal Rise and Fall Times



13.7 Analog Comparator Characteristics

Table 13-25. **Analog Comparator Characteristics**

Parameter	Conditions	Min	Typ	Max	Units
Voltage Range	The Analog Comparator is supplied by VDDIN	1.62	3.3	3.6	V
Input Voltage Range		GND + 0.2		VDDIN - 0.2	V
Input Offset Voltage				20	mV
Current Consumption	On VDDIN Low Power Option (ISEL = 0) High Speed Option (ISEL = 1)			 25 170	µA
Hysteresis	HYST = 0x01 or 0x10 HYST = 0x11		15 30	50 90	mV
Settling Time	Given for overdrive > 100 mV Low Power Option High Speed Option			 1 0.1	µs

13.8 Temperature Sensor

The temperature sensor is connected to Channel 15 of the ADC.

The temperature sensor provides an output voltage (V_T) that is proportional to absolute temperature (PTAT). The V_T output voltage linearly varies with a temperature slope dV_T/dT = 4.72 mV/°C.

The V_T voltage equals 1.44V at 27°C, with a ±50mV accuracy. The V_T slope versus temperature dV_T/dT = 4.72 mV/°C only shows a ±8% slight variation over process, mismatch and supply voltage.

The user needs to calibrate it (offset calibration) at ambient temperature in order to get rid of the VT spread at ambient temperature (+/-15%).

Table 13-26. **Temperature Sensor Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_T	Output Voltage	T° = 27° C		1.44		V
<Symbol> DV_T	Output Voltage Accuracy	T° = 27° C	-50		+50	mV
dV_T/dT	Temperature Sensitivity (slope voltage versus temperature)			4.72		mV/°C
	Slope accuracy	Over temperature range [-40°C / +85°C]	-8		+8	%
	Temperature accuracy	After offset calibration Over temperature range [-40°C / +85°C]	-5		+5	°C
		After offset calibration Over temperature range [0°C / +80°C]	-3		+3	°C
$T_{START-UP}$	Startup Time	After TSON = 1		5	10	µs
$I_{VDDCORE}$	Current Consumption		50	70	80	µA

13.9 AC Characteristics

13.9.1 Master Clock Characteristics

Table 13-27. **Master Clock Waveform Parameters**

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPMCK})$	Master Clock Frequency	VDDCORE @ 1.20V		120	MHz
$1/(t_{CPMCK})$	Master Clock Frequency	VDDCORE @ 1.08V		100	MHz

13.9.2 I/O Characteristics

Criteria used to define the maximum frequency of the I/Os:

- Output duty cycle (40%-60%)
- Minimum output swing: 100 mV to VDDIO - 100 mV
- Minimum output swing: 100 mV to VDDIO - 100 mV
- Addition of rising and falling time inferior to 75% of the period

Table 13-28. **I/O Characteristics**

Symbol	Parameter	Conditions		Min	Max	Units
FreqMax1	Pin Group 1 [(1)] Maximum output frequency	10 pF	V_{DDIO} = 1.62V		70	MHz
		30 pF	V_{DDIO} = 1.62V		45	
$PulseminH_1$	Pin Group 1 [(1)] High Level Pulse Width	10 pF	V_{DDIO} = 1.62V	7.2		ns
		30 pF	V_{DDIO} = 1.62V	11		
$PulseminL_1$	Pin Group 1 [(1)] Low Level Pulse Width	10 pF	V_{DDIO} = 1.62V	7.2		ns
		30 pF	V_{DDIO} = 1.62V	11		
FreqMax2	Pin Group 2 [(2)] Maximum output frequency	10 pF	V_{DDIO} = 1.62V		46	MHz
		25 pF	V_{DDIO} = 1.62V		23	
$PulseminH_2$	Pin Group 2 [(2)] High Level Pulse Width	10 pF	V_{DDIO} = 1.62V	11		ns
		25pF	V_{DDIO} = 1.62V	21.8		
$PulseminL_2$	Pin Group 2 [(2)] Low Level Pulse Width	10 pF	V_{DDIO} = 1.62V	11		ns
		25 pF	V_{DDIO} = 1.62V	21.8		
FreqMax3	Pin Group3[(3)] Maximum output frequency	10 pF	V_{DDIO} = 1.62V		70	MHz
		25 pF	V_{DDIO} = 1.62V		35	
$PulseminH_3$	Pin Group 3 [(3)] High Level Pulse Width	10 pF	V_{DDIO} = 1.62V	7.2		ns
		25 pF	V_{DDIO} = 1.62V	14.2		
$PulseminL_3$	Pin Group 3 [(3)] Low Level Pulse Width	10 pF	V_{DDIO} = 1.62V	7.2		ns
		25 pF	V_{DDIO} = 1.62V	14.2		

Table 13-28. **I/O Characteristics**

Symbol	Parameter	Conditions		Min	Max	Units
FreqMax4	Pin Group 4[4] Maximum output frequency	10 pF	V_{DDIO} = 1.62V		58	MHz
		25 pF	V_{DDIO} = 1.62V		29	
PulseminH4	Pin Group 4[4] High Level Pulse Width	10 pF	V_{DDIO} = 1.62V	8.6		ns
		25pF	V_{DDIO} = 1.62V	17.2		
PulseminL4	Pin Group 4[4] Low Level Pulse Width	10 pF	V_{DDIO} = 1.62V	8.6		ns
		25 pF	V_{DDIO} = 1.62V	17.2		
FreqMax5	Pin Group 5[5] Maximum output frequency	25 pF	V_{DDIO} = 1.62V		25	MHz

Note:

1. Pin Group 1 = PA14, PA29
2. Pin Group 2 = PA[4-11], PA[15-25], PA[30-31], PB[0-9], PB[12-14], PC[0-31]
3. Pin Group 3 = PA[12-13], PA[26-28], PA[30-31]
4. PIn Group 4 = PA[0-3]
5. PIn Group 5 = PB[10-11]

13.9.3 SSC Timings

Timings are given in the following domain:

1.8V domain: VDDIO from 1.65V to 1.95V, maximum external capacitor = 20 pF

3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 30 pF.

Figure 13-10. SSC Transmitter, TK and TF as output

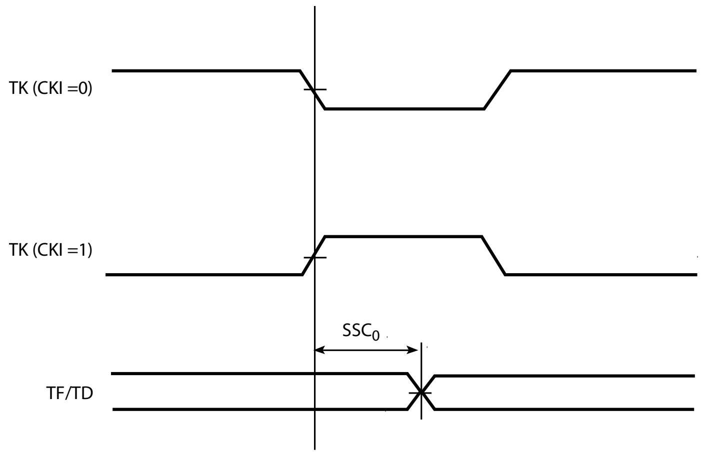


Figure 13-11. SSC Transmitter, TK as input and TF as output

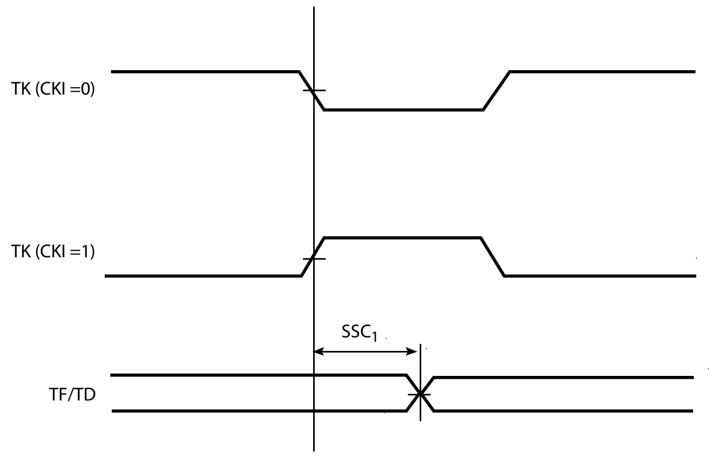


Figure 13-12. SSC Transmitter, TK as output and TF as input

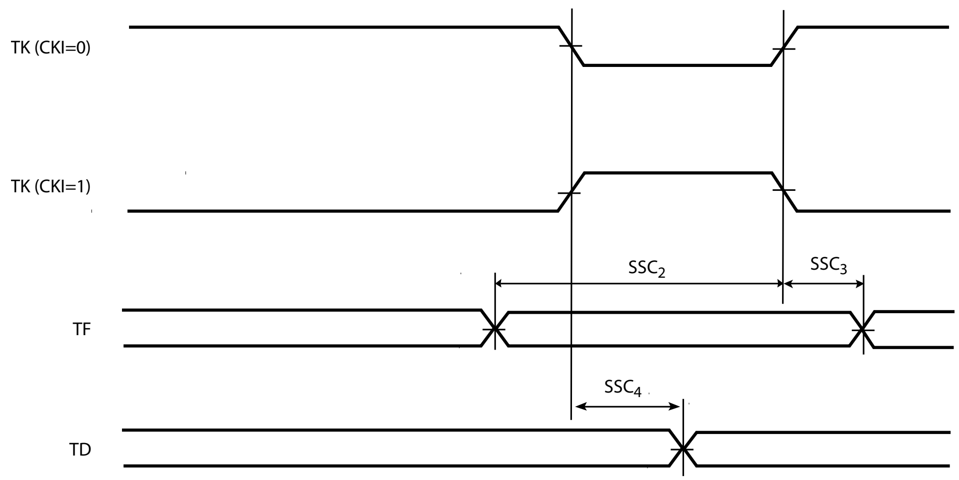


Figure 13-13. SSC Transmitter, TK and TF as input

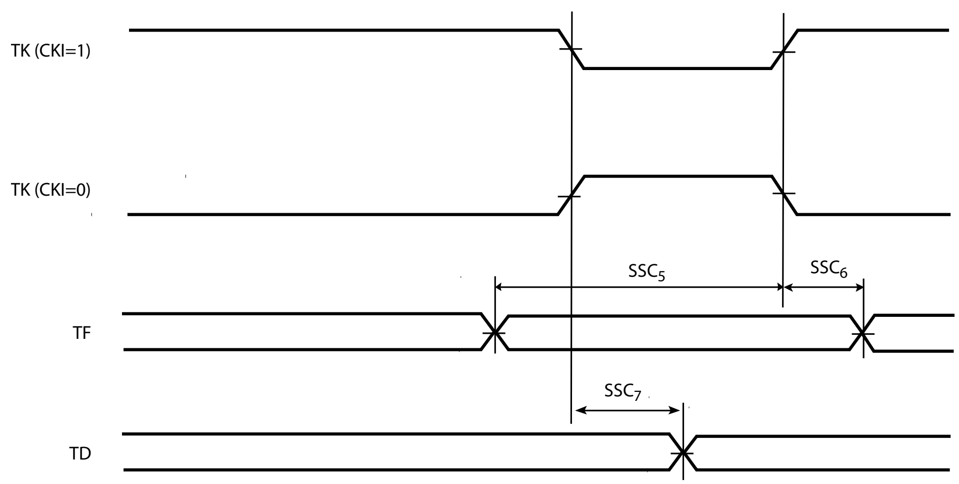


Figure 13-14. SSC Receiver RK and RF as input

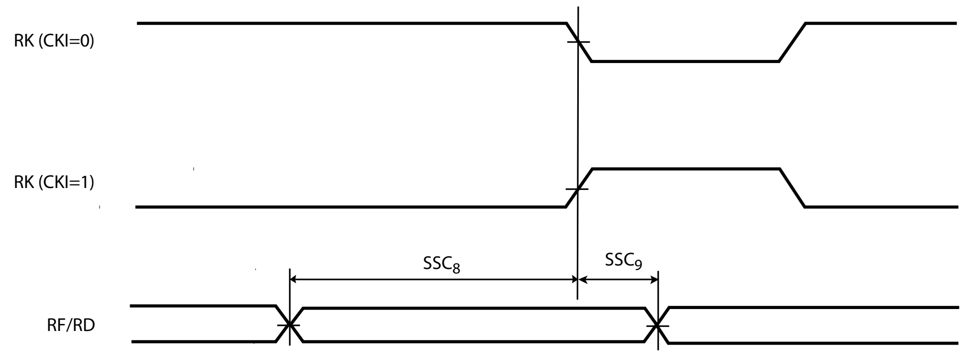


Figure 13-15. SSC Receiver, RK as input and RF as output

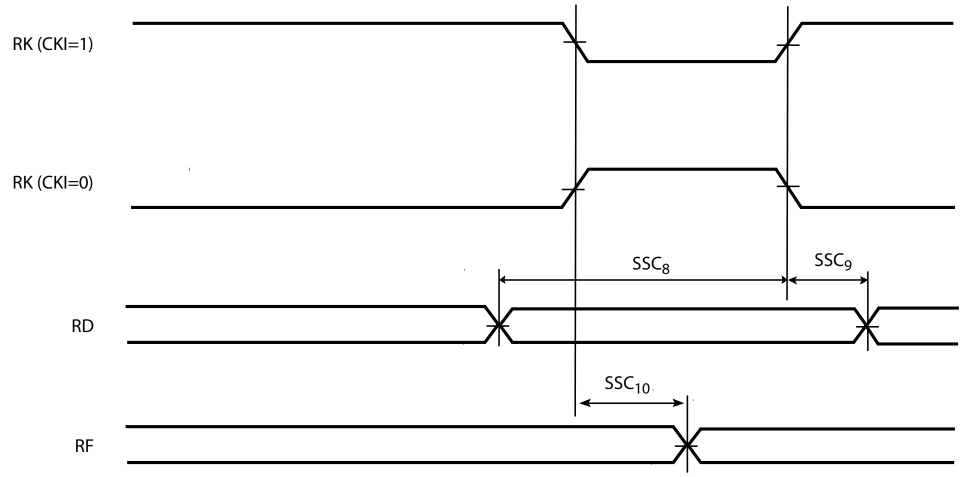


Figure 13-16. SSC Receiver, RK and RF as output

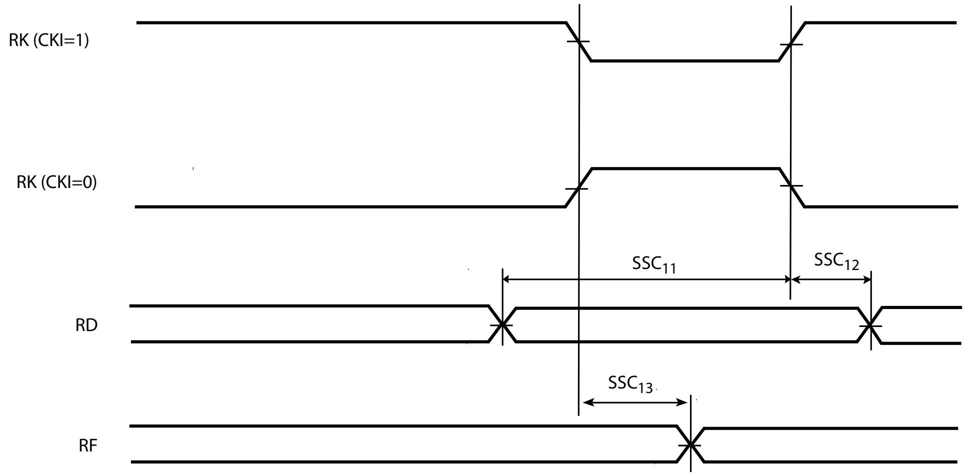
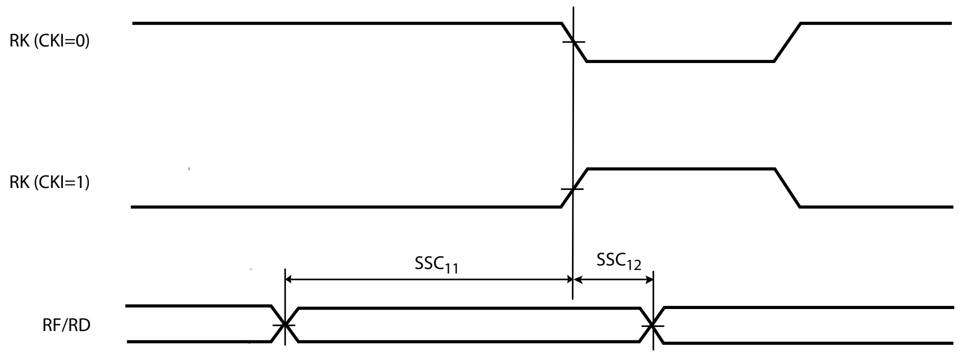


Figure 13-17. SSC Receiver, RK as output and RF as input



13.9.3.2 SSC Timings

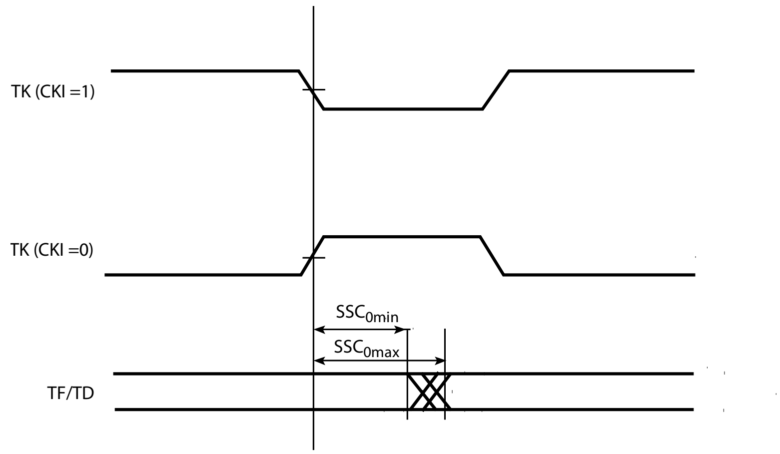
Table 13-29. **SSC Timings**

Symbol	Parameter	Condition	Min	Max	Units
	Transmitter				
SSC_0	TK edge to TF/TD (TK output, TF output)	1.8v domain[3] 3.3v domain[4]	-3 -2.6	5.4 5.0	ns
SSC_1	TK edge to TF/TD (TK input, TF output)	1.8v domain[3] 3.3v domain[4]	4.5 3.8	16.3 13.3	ns
SSC_2	TF setup time before TK edge (TK output)	1.8v domain[3] 3.3v domain[4]	14.8 12.0		ns
SSC_3	TF hold time after TK edge (TK output)	1.8v domain[3] 3.3v domain[4]	0		ns
SSC_4[1]	TK edge to TF/TD (TK output, TF input)	1.8v domain[3] 3.3v domain[4]	2.6(+2*t_{CPMCK}) [1][4] 2.3(+2*t_{CPMCK}) [1][4]	5.4(+2*t_{CPMCK}) [1][4] 5.0(+2*t_{CPMCK}) [1][4]	ns
SSC_5	TF setup time before TK edge (TK input)	1.8v domain[3] 3.3v domain[4]	0		ns
SSC_6	TF hold time after TK edge (TK input)	1.8v domain[3] 3.3v domain[4]	t_{CPMCK}		ns
SSC_7[1]	TK edge to TF/TD (TK input, TF input)	1.8v domain[3] 3.3v domain[4]	4.5(+3*t_{CPMCK}) [1][4] 3.8(+3*t_{CPMCK}) [1][4]	16.3(+3*t_{CPMCK}) [1][4] 13.3(+3*t_{CPMCK}) [1][4]	ns
	Receiver				
SSC_8	RF/RD setup time before RK edge (RK input)	1.8v domain[3] 3.3v domain[4]	0		ns
SSC_9	RF/RD hold time after RK edge (RK input)	1.8v domain[3] 3.3v domain[4]	t_{CPMCK}		ns
SSC_{10}	RK edge to RF (RK input)	1.8v domain[3] 3.3v domain[4]	4.7 4	16.1 12.8	ns
SSC_{11}	RF/RD setup time before RK edge (RK output)	1.8v domain[3] 3.3v domain[4]	15.8 - t_{CPMCK} 12.5- t_{CPMCK}		ns
SSC_{12}	RF/RD hold time after RK edge (RK output)	1.8v domain[3] 3.3v domain[4]	t_{CPMCK} - 4.3 t_{CPMCK} - 3.6		ns
SSC_{13}	RK edge to RF (RK output)	1.8v domain[3] 3.3v domain[4]	-3 -2.6	4.3 3.8	ns

Note:

1. Timings SSC4 and SSC7 depend on the start condition. When STTDLY = 0 (Receive start delay) and START = 4, or 5 or 7(Receive Start Selection), two Periods of the MCK must be added to timings.
2. For output signals (TF, TD, RF), Min and Max access times are defined. The Min access time is the time between the TK (or RK) edge and the signal change. The Max access timing is the time between the TK edge and the signal stabilization. Figure 13-18 illustrates Min and Max accesses for SSC0. The same applies for SSC1, SSC4, and SSC7, SSC10 and SSC13.
3. 1.8V domain: V_{VDDIO} from 1.65V to 1.95V, maximum external capacitor = 20 pF.
4. 3.3V domain: V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 30 pF..

Figure 13-18. Min and Max Access Time of Output Signals



13.9.4 SMC Timings

Timings are given in the following domain:

1.8V domain: VDDIO from 1.65V to 1.95V, maximum external capacitor = 30 pF

3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 50 pF.

Timings are given assuming a capacitance load on data, control and address pads:

In the following tables t_{CPMCK} is MCK period. Timing extraction

13.9.4.1 Read Timings

Table 13-30. **SMC Read Signals - NRD Controlled (READ_MODE = 1)**

Symbol	Parameter	Min		Max		Units
	VDDIO Supply	**1.8V**[2]	**3.3V**[3]	**1.8V**[2]	**3.3V**[3]	
NO HOLD SETTINGS (nrd hold = 0)						
SMC_1	Data Setup before NRD High	19.9	17.9			ns
SMC_2	Data Hold after NRD High	0	0			ns
HOLD SETTINGS (nrd hold <Symbol>1 0)						
SMC_3	Data Setup before NRD High	16.0	14.0			ns
SMC_4	Data Hold after NRD High	0	0			ns
HOLD or NO HOLD SETTINGS (nrd hold <Symbol>1 0, nrd hold = 0)						
SMC_5	A0 - A22 Valid before NRD High	(nrd setup + nrd pulse) * t_{CPMCK} - 6.5	(nrd setup + nrd pulse)* t_{CPMCK} - 6.3			ns
SMC_6	NCS low before NRD High	(nrd setup + nrd pulse - ncs rd setup) * t_{CPMCK} - 4.6	(nrd setup + nrd pulse - ncs rd setup) * t_{CPMCK} - 5.1			ns
SMC_7	NRD Pulse Width	nrd pulse * t_{CPMCK} - 7.2	nrd pulse * t_{CPMCK} - 6.2			ns

Table 13-31. **SMC Read Signals - NCS Controlled (READ_MODE= 0)**

Symbol	Parameter	Min		Max		Units
	VDDIO supply	1.8V[(2)]	3.3V[(3)]	1.8V[(2)]	3.3V[(3)]	
NO HOLD SETTINGS (ncs rd hold = 0)						
SMC$_8$	Data Setup before NCS High	20.7	18.4			ns
SMC$_9$	Data Hold after NCS High	0	0			ns
HOLD SETTINGS (ncs rd hold <Symbol>[1] 0)						
SMC$_{10}$	Data Setup before NCS High	16.8	14.5			ns
SMC$_{11}$	Data Hold after NCS High	0	0			ns
HOLD or NO HOLD SETTINGS (ncs rd hold <Symbol>[1] 0, ncs rd hold = 0)						
SMC$_{12}$	A0 - A22 valid before NCS High	(ncs rd setup + ncs rd pulse)* t$_{CPMCK}$ - 6.5	(ncs rd setup + ncs rd pulse)* t$_{CPMCK}$ - 6.3			ns
SMC$_{13}$	NRD low before NCS High	(ncs rd setup + ncs rd pulse - nrd setup)* t$_{CPMCK}$ - 5.6	(ncs rd setup + ncs rd pulse - nrd setup)* t$_{CPMCK}$- 5.4			ns
SMC$_{14}$	NCS Pulse Width	ncs rd pulse length * t$_{CPMCK}$ -7.7	ncs rd pulse length * t$_{CPMCK}$ - 6.7			ns

13.9.4.2 Write Timings

Table 13-32. **SMC Write Signals - NWE Controlled (WRITE_MODE = 1)**

Symbol	Parameter	Min		Max		Units
		1.8V[2]	3.3V[3]	1.8V[2]	3.3V[3]	
HOLD or NO HOLD SETTINGS (nwe hold <Symbol>1 0, nwe hold = 0)						
SMC_{15}	Data Out Valid before NWE High	nwe pulse * t_{CPMCK} - 6.9	nwe pulse * t_{CPMCK} - 6.7			ns
SMC_{16}	NWE Pulse Width	nwe pulse * t_{CPMCK} - 7.3	nwe pulse * t_{CPMCK} - 6.3			ns
SMC_{17}	A0 - A22 valid before NWE low	nwe setup * t_{CPMCK} - 7.2	nwe setup * t_{CPMCK} - 7.0			ns
SMC_{18}	NCS low before NWE high	(nwe setup - ncs rd setup + nwe pulse) * t_{CPMCK} -7.1	(nwe setup - ncs rd setup + nwe pulse) * t_{CPMCK} - 6.8			ns
HOLD SETTINGS (nwe hold <Symbol>1 0)						
SMC_{19}	NWE High to Data OUT, NBS0/A0 NBS1, NBS2/A1, NBS3, A2 - A25 change	nwe hold * t_{CPMCK} - 8.8	nwe hold * t_{CPMCK} - 6.9			ns
SMC_{20}	NWE High to NCS Inactive [1]	(nwe hold - ncs wr hold)* t_{CPMCK} - 5.2	(nwe hold - ncs wr hold)* t_{CPMCK} - 5.0			ns
NO HOLD SETTINGS (nwe hold = 0)						
SMC_{21}	NWE High to Data OUT, NBS0/A0 NBS1, NBS2/A1, NBS3, A2 - A25, NCS change[1]	3.0	2.8			ns

Table 13-33. **SMC Write NCS Controlled (WRITE_MODE = 0)**

Symbol	Parameter	Min		Max		Units
		1.8V(2)	3.3V(3)	1.8V(2)	3.3V(3)	
SMC_{22}	Data Out Valid before NCS High	ncs wr pulse * t_{CPMCK} - 6.3	ncs wr pulse * t_{CPMCK} - 6.2			ns
SMC_{23}	NCS Pulse Width	ncs wr pulse * t_{CPMCK} - 7.7	ncs wr pulse * t_{CPMCK} - 6.7			ns
SMC_{24}	A0 - A22 valid before NCS low	ncs wr setup * t_{CPMCK} - 6.5	ncs wr setup * t_{CPMCK} - 6.3			ns
SMC_{25}	NWE low before NCS high	(ncs wr setup - nwe setup + ncs pulse)* t_{CPMCK} - 5.1	(ncs wr setup - nwe setup + ncs pulse)* t_{CPMCK} - 4.9			ns
SMC_{26}	NCS High to Data Out,A0 - A25, change	ncs wr hold * t_{CPMCK} - 10.2	ncs wr hold * t_{CPMCK} - 8.4			ns
SMC_{27}	NCS High to NWE Inactive	(ncs wr hold - nwe hold)* t_{CPMCK} - 7.4	(ncs wr hold - nwe hold)* t_{CPMCK} - 7.1			ns

Note:

1. Hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs wr hold length” or “NWE hold length”.
2. 1.8V domain: VDDIO from 1.65 V to 1.95V, maximum external capacitor = 30pF
3. 3.3V domain: VDDIO from2.85V to 3.6V, maximum external capacitor = 50pF.

Figure 13-19. SMC Timings - NCS Controlled Read and Write

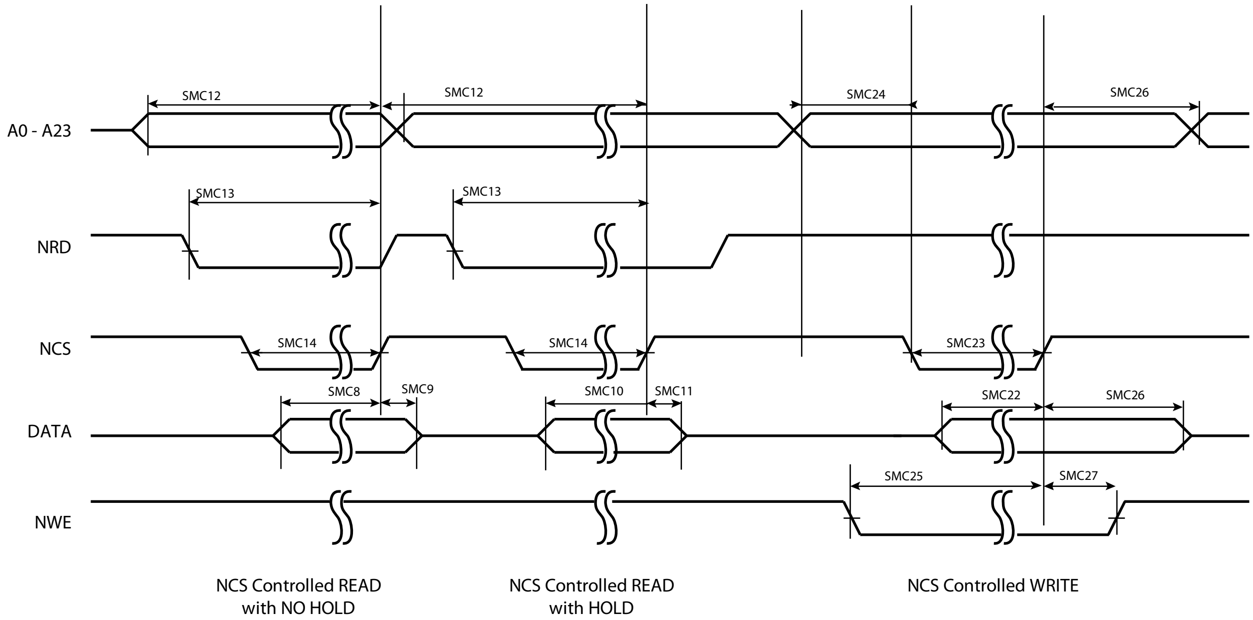
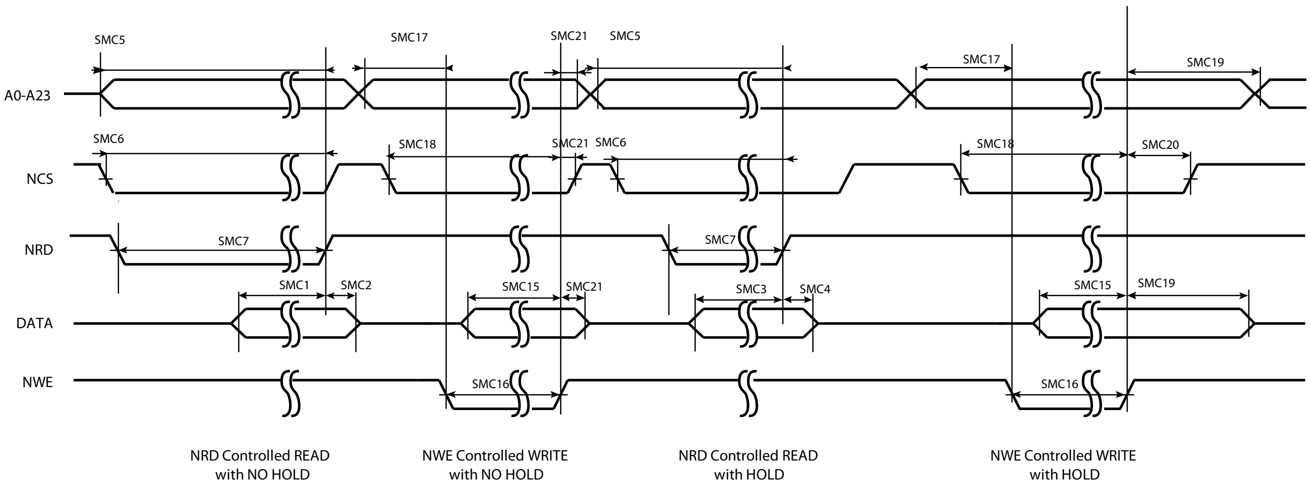


Figure 13-20. SMC Timings - NRD Controlled Read and NWE Controlled Write



13.9.5 USART in SPI Mode Timings

Timings are given in the following domain:

1.8V domain: VDDIO from 1.65V to 1.95V, maximum external capacitor = 20 pF

3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF.

Figure 13-21. USART SPI Master Mode

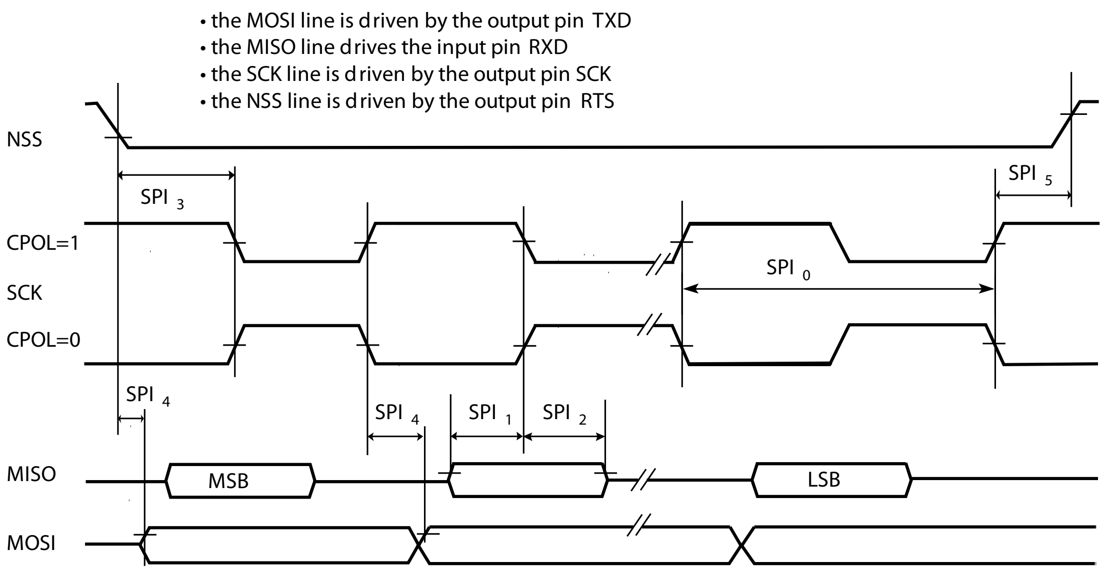


Figure 13-22. USART SPI Slave Mode: (Mode 1 or 2)

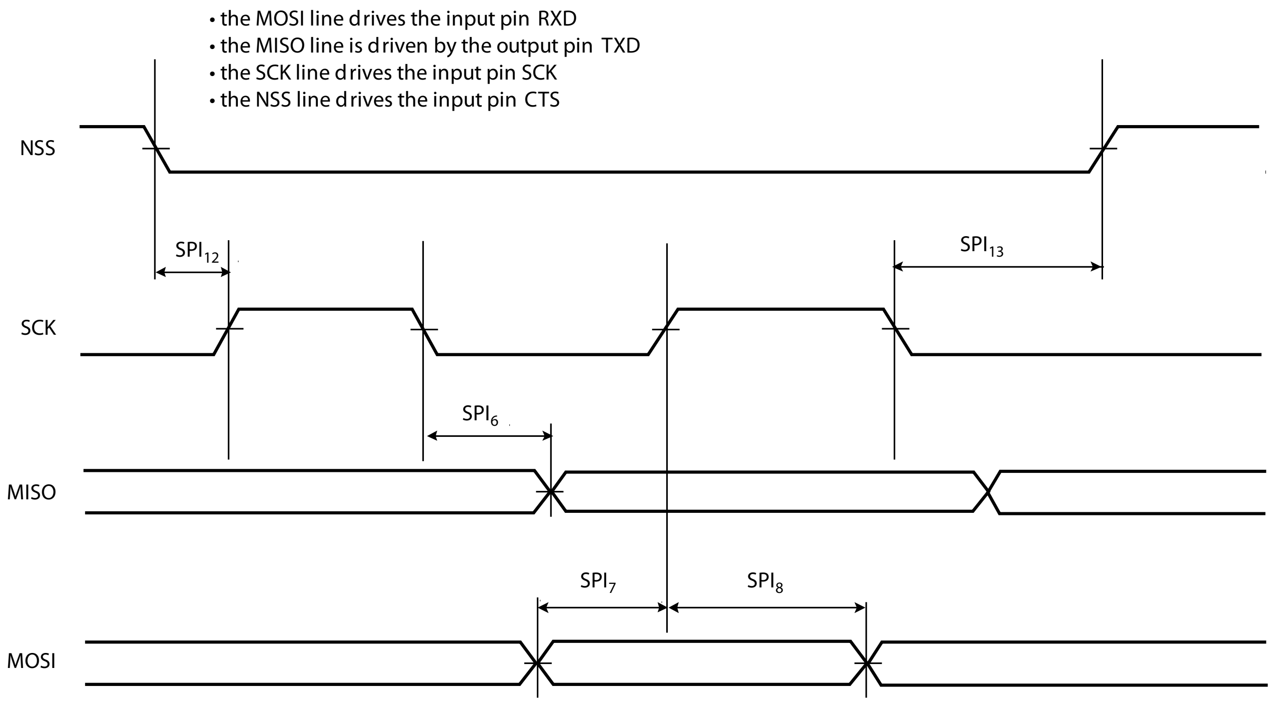
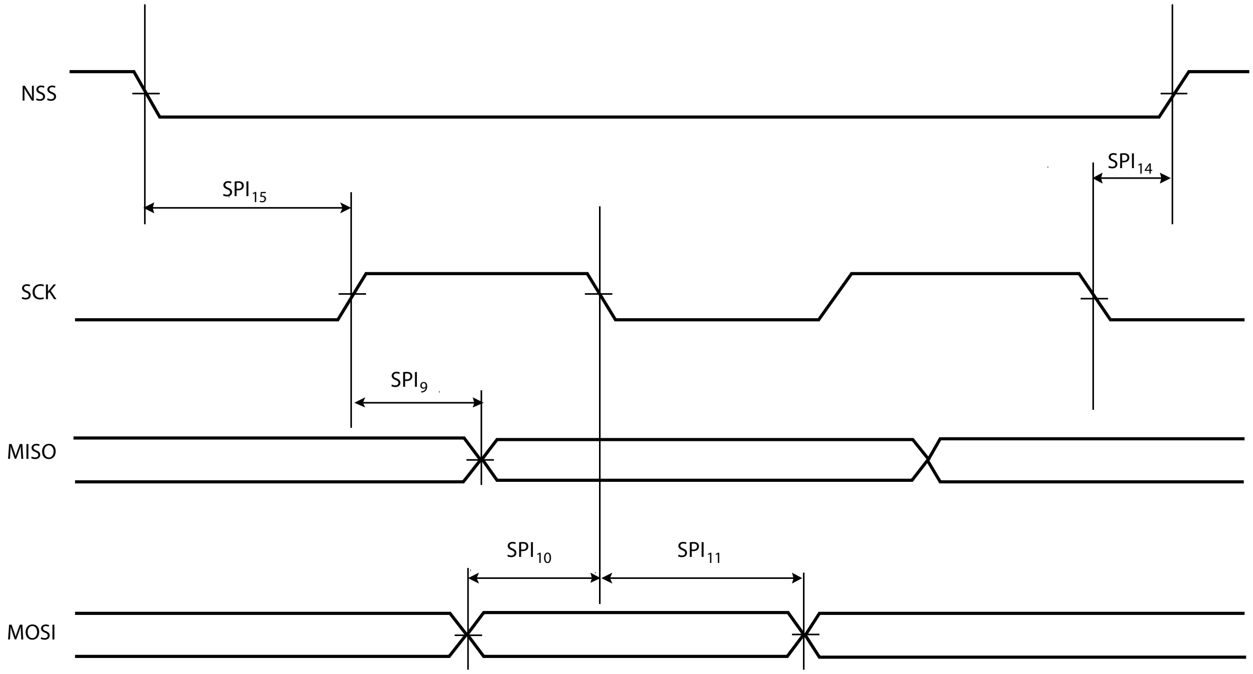


Figure 13-23. USART SPI Slave mode: (Mode 0 or 3)



13.9.5.2 USART SPI TImings

Table 13-34. **USART SPI TImings**

Symbol	Parameter	Conditions	Min	Max	Units
		Master Mode			
SPI_0	SCK Period	1.8v domain 3.3v domain	MCK/6		ns
SPI_1	Input Data Setup Time	1.8v domain 3.3v domain	0.5 * MCK + 0.8 0.5 * MCK + 1.0		ns
SPI_2	Input Data Hold Time	1.8v domain 3.3v domain	1.5 * MCK + 0.3 1.5 * MCK + 0.1		ns
SPI_3	Chip Select Active to Serial Clock	1.8v domain 3.3v domain	1.5 * SPCK - 1.5 1.5 * SPCK - 2.1		ns
SPI_4	Output Data Setup Time	1.8v domain 3.3v domain	- 7.9 - 7.2	9.9 10.7	ns
SPI_5	Serial Clock to Chip Select Inactive	1.8v domain 3.3v domain	1 * SPCK - 4.1 1 * SPCK - 4.8		ns
		Slave Mode			
SPI_6	SCK falling to MISO	1.8V domain 3.3V domain	4.7 4	17.3 15.2	ns
SPI_7	MOSI Setup time before SCK rises	1.8V domain 3.3V domain	2 * MCK + 0.7 2 * MCK		ns
SPI_8	MOSI Hold time after SCK rises	1.8v domain 3.3v domain	0 0.1		ns
SPI_9	SCK rising to MISO	1.8v domain 3.3v domain	4.7 4.1	17.1 15.5	ns
SPI_{10}	MOSI Setup time before SCK falls	1.8v domain 3.3v domain	2 * MCK + 0.7 2 * MCK + 0.6		ns
SPI_{11}	MOSI Hold time after SCK falls	1.8v domain 3.3v domain	0.2 0.1		ns

Table 13-34. **USART SPI Timings (Continued)**

Symbol	Parameter	Conditions	Min	Max	Units
SPI_{12}	NPCS0 setup to SCK rising	1.8v domain 3.3v domain	2,5 * MCK + 0.5 2,5 * MCK		ns
SPI_{13}	NPCS0 hold after SCK falling	1.8v domain 3.3v domain	1,5 * MCK + 0.2 1,5 * MCK		ns
SPI_{14}	NPCS0 setup to SCK falling	1.8v domain 3.3v domain	2,5 * MCK + 0.5 2,5 * MCK + 0.3		ns
SPI_{15}	NPCS0 hold after SCK rising	1.8v domain 3.3v domain	1,5 * MCK 1,5 * MCK		ns

Note:

1. 1.8V domain: VDDIO from 1.65V to 1.95V, maximum external capacitor = 20 pF
2. 3.3V domain: VDDIO from2.85V to 3.6V, maximum external capacitor = 40 pF.

13.9.6 Two-wire Serial Interface Characteristics

Following table describes the requirements for devices connected to the Two-wire Serial Bus. For timing symbols refer to Figure 13-24

Table 13-35. **Two-wire Serial Bus Requirements**

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.3	0.3 V_{VDDIO}	V
V_{IH}	Input High-voltage		0.7xV_{VDDIO}	V_{CC} + 0.3	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.150	–	V
V_{OL}	Output Low-voltage	3 mA sink current	-	0.4	V
t_R	Rise Time for both TWD and TWCK		20 + 0.1C_b(1)(2)	300	ns
t_{OF}	Output Fall Time from V_{IHmin} to V_{ILmax}	10 pF < C_b < 400 pF Figure 13-24	20 + 0.1C_b(1)(2)	250	ns
C_i(1)	Capacitance for each I/O Pin		–	10	pF
f_{TWCK}	TWCK Clock Frequency		0	400	kHz
Rp	Value of Pull-up resistor	f_{TWCK} ≤100 kHz			Ω
		f_{TWCK} > 100 kHz			Ω

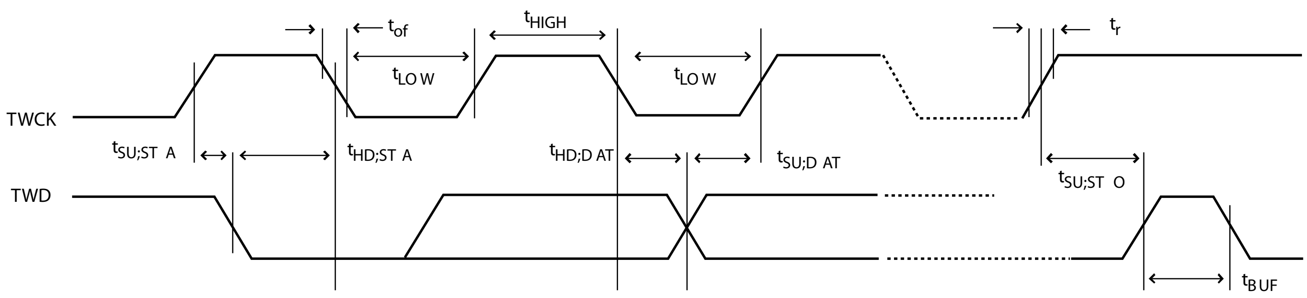
Table 13-35. **Two-wire Serial Bus Requirements (Continued)**

Symbol	Parameter	Condition	Min	Max	Units
t_{LOW}	Low Period of the TWCK clock	$f_{TWCK} \leq 100$ kHz	[3]	–	µs
		$f_{TWCK} > 100$ kHz	[3]	–	µs
t_{HIGH}	High period of the TWCK clock	$f_{TWCK} \leq 100$ kHz	[4]	–	µs
		$f_{TWCK} > 100$ kHz	[4]	–	µs
$t_{HD;STA}$	Hold Time (repeated) START Condition	$f_{TWCK} \leq 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{TWCK} \leq 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs
$t_{HD;DAT}$	Data hold time	$f_{TWCK} \leq 100$ kHz	0	$3 \times T_{CP\_MCK}$[5]	µs
		$f_{TWCK} > 100$ kHz	0	$3 \times T_{CP\_MCK}$[5]	µs
$t_{SU;DAT}$	Data setup time	$f_{TWCK} \leq 100$ kHz	$t_{LOW} - 3 \times t_{CP\_MCK}$[5]	–	ns
		$f_{TWCK} > 100$ kHz	$t_{LOW} - 3 \times t_{CP\_MCK}$[5]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	$f_{TWCK} \leq 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs
$t_{HD;STA}$	Hold Time (repeated) START Condition	$f_{TWCK} \leq 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs

Note:

1. Required only for $f_{TWCK} > 100$ kHz.
2. C_B = capacitance of one bus line in pF. Per I2C Standard, C_b Max = 400pF
3. The TWCK low Period is defined as follows: $T_{low} = ((CLDIV \times 2^{CKDIV}) + 4) \times T_{MCK}$
4. The TWCK high period is defined as follows: $T_{High} = ((CHDIV \times 2^{CKDIV}) + 4) \times T_{MCK}$
5. t_{CP_MCK} = MCK Bus Period.

Figure 13-24. Two-wire Serial Bus Timing



13.9.7 Embedded Flash Characteristics

The maximum operating frequency is given in Table 13-36 to Table 13-39 below but is limited by the Embedded Flash access time when the processor is fetching code out of it. The tables below give the device maximum operating frequency depending on the field FWS of the MC_FMR register. This field defines the number of wait states required to access the Embedded Flash Memory.

The embedded flash is fully tested during production test, the flash contents are not set to a known state prior to shipment. Therefore, the flash contents should be erased prior to programming an application.

Table 13-36. **Embedded Flash Wait State VDDCORE set at 1.08V and VDDIO 1.62V to 3.6V @85C**

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	16
1	2 cycles	33
2	3 cycles	50
3	4 cycles	67
4	5 cycles	84
5	6 cycles	100

Table 13-37. **Embedded Flash Wait State VDDCORE set at 1.08V and VDDIO 2.7V to 3.6V @85C**

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	20
1	2 cycles	40
2	3 cycles	60
3	4 cycles	80
4	5 cycles	100

Table 13-38. **Embedded Flash Wait State VDDCORE set at 1.2V and VDDIO 1.62V to 3.6V @ 85C**

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	17
1	2 cycles	34
2	3 cycles	52
3	4 cycles	69
4	5 cycles	87
5	6 cycles	104
6	7 cycles	121

Table 13-39. **Embedded Flash Wait State VDDCORE set at 1.20V and VDDIO 2.7V to 3.6V @ 85C**

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	21
1	2 cycles	42
2	3 cycles	63
3	4 cycles	84
4	5 cycles	105
5	6 cycles	123

Table 13-40. **AC Flash Characteristics**

Parameter	Conditions	Min	Typ	Max	Units
Program Cycle Time	Erase page mode		10	50	ms
	Erase block mode (by 4Kbytes)		50	200	ms
	Erase sector mode		400	950	ms
Full Chip Erase	1 MBytes 512 KBytes		9 5.5	18 11	s
Data Retention	Not Powered or Powered		20		Years
Endurance	Write/Erase cycles per page, block or sector @ 25°C Write/Erase cycles per page, block or sector @ 85°C	 10K	100K 		cycles

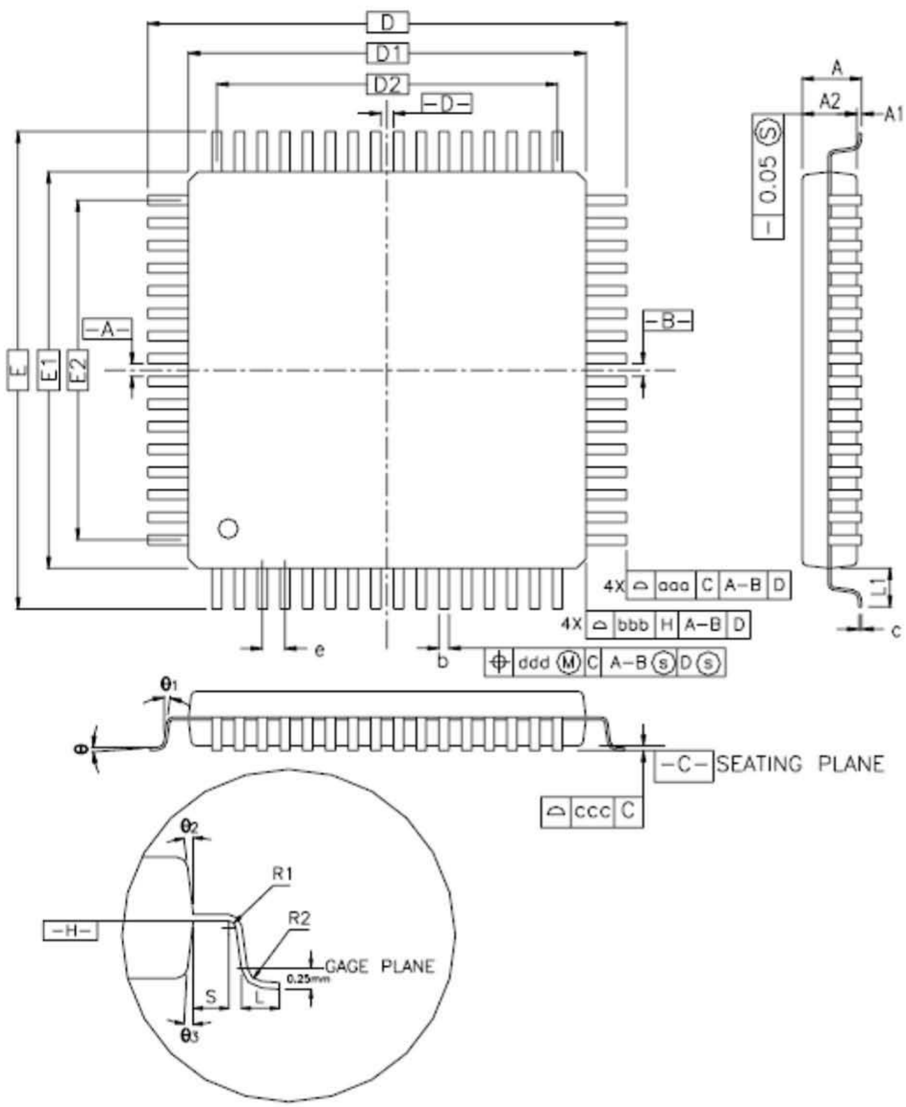
13.10 Recommended Operating Conditions

Table 13-41. **SAM4SP32A Recommended Operating Conditions**

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	$V_{VDDCORE}$	1.08	1.20	1.32	V
	V_{VDDIN}	3.00	3.30	3.60	
	V_{VDDIO}	3.00	3.30	3.60	
	V_{VDDPLL}	1.08	--	1.32	
	A_{VDD}	3.00	3.30	3.60	
Junction Temperature	TJ	-40	25	+125	ºC
Ambient Temperature	TA	-40	--	+85	

14. Mechanical Characteristics

Figure 14-1. 128-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

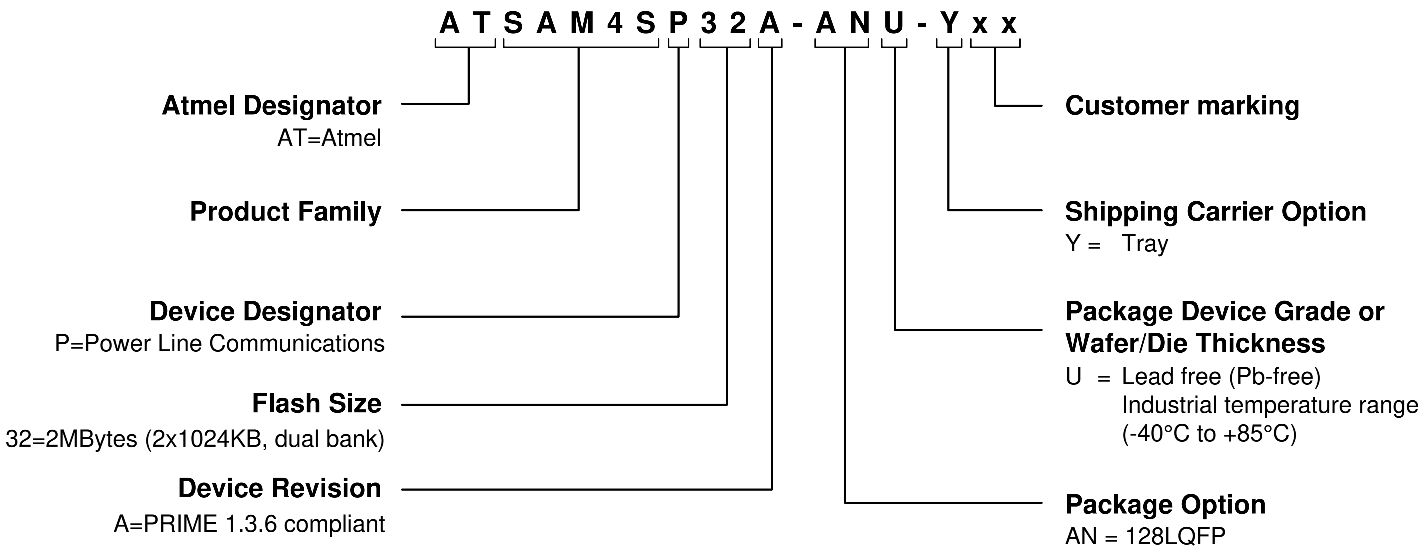
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

15. Ordering Information

Table 15-1. **Atmel SAM4SP32A Ordering Codes**

Atmel Ordering Code	Package	Package Type	Temperature Range
ATSAM4SP32A-ANU-Y	128 LQFP	Pb-Free	Industrial (-40ºC to 85º)



16. Revision History

Doc. Rev.	Date	Comments
A	10/2012	Initial release

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