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# FXMA2104

## Dual-Supply, 4-Bit Voltage Translator / Buffer / Repeater / Isolator for Open-Drain Applications

### Features

- Bi-Directional Interface between Any Two Levels: 1.65V to 5.5V
- Direction Control not Needed
- System GPIO Resources Not Required when OE Tied to  $V_{CCA}$
- I<sup>2</sup>C 400pF Buffer / Repeater
- I<sup>2</sup>C-Bus® Isolation
- A/B Port  $V_{OL} = 175\text{mV}$  (Typical),  $V_{IL} = 150\text{mV}$ ,  $I_{OL} = 6\text{mA}$
- Open-Drain Inputs / Outputs
- Accommodates Standard-Mode and Fast-Mode I<sup>2</sup>C-Bus Devices
- Supports I<sup>2</sup>C Clock Stretching & Multi-Master
- Fully Configurable: Inputs and Outputs Track  $V_{CC}$
- Non-Preferential Power-Up; Either  $V_{CC}$  May Be Powered-Up First
- Outputs Switch to 3-State if Either  $V_{CC}$  is at GND
- Tolerant Output Enable: 5V
- Packaged in 12-Lead Ultrathin MLP (1.8mm x 1.8mm)
- ESD Protection Exceeds:
  - 5kV HBM ESD (per JESD22-A114)
  - 2kV CDM (per JESD22-C101)

### Description

The FXMA2104 is a 4-bit high-performance, configurable dual-voltage supply, open-drain translator for bi-directional voltage translation over a wide range of input and output voltages levels.

Intended for use as a voltage translator in applications using the I<sup>2</sup>C-Bus® interface, the input and output voltage levels are compatible with I<sup>2</sup>C device specification voltage levels. External pull-up resistors are required.

The device is designed so that the A port tracks the  $V_{CCA}$  level and the B port tracks the  $V_{CCB}$  level. This allows for bi-directional A/B port voltage translation between any two levels from 1.65V to 5.5V.  $V_{CCA}$  can equal  $V_{CCB}$  from 1.65V to 5.5V.

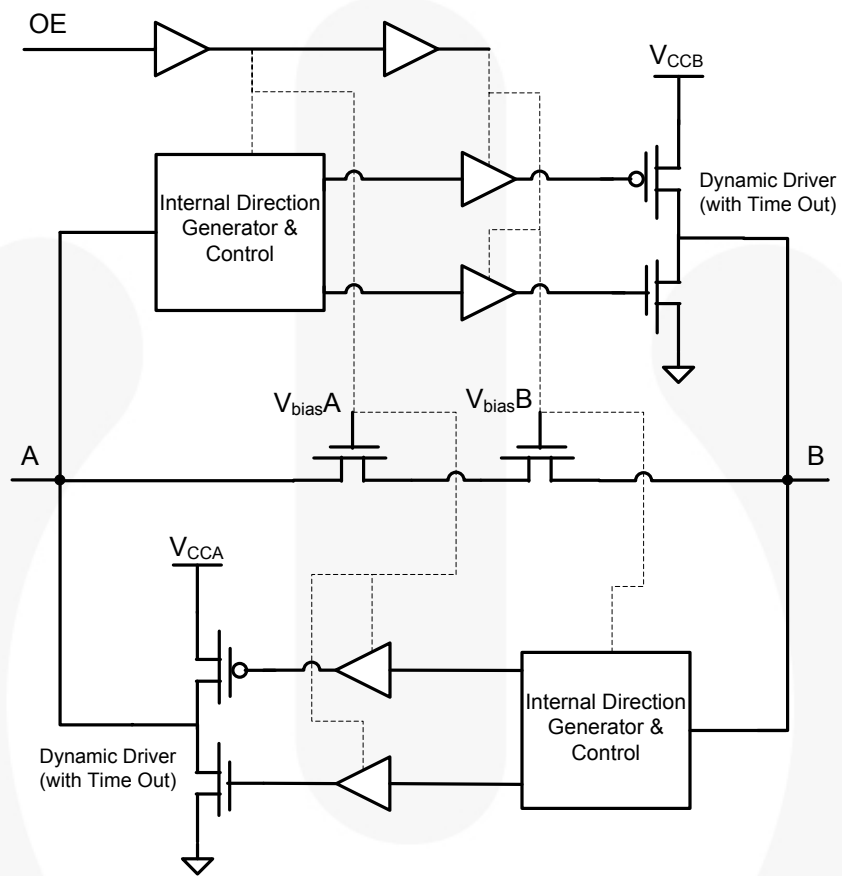
Non-preferential power-up means either  $V_{CC}$  can be powered-up first. Internal power-down control circuits place the device in 3-state if either  $V_{CC}$  is removed.

The two ports of the device have automatic direction-sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

### Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FXMA2104UMX	-40 to +85°C	BX	12-Lead, Ultrathin, MLP, 1.8mm x 1.8mm	5000 Units on Tape and Reel

**Block Diagram**



**Figure 1. Block Diagram, 1 of 4 Channels**

## Pin Configuration

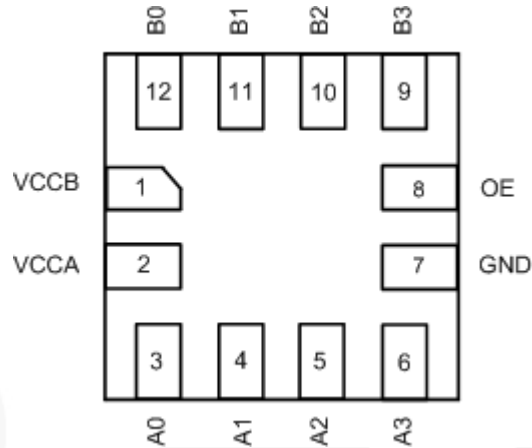


Figure 2. UMLP (Top-Through View)

## Pin Definitions

Pin #	Name	Description
1	V <sub>CCB</sub>	B-Side Power Supply
2	V <sub>CCA</sub>	A-Side Power Supply
3, 4, 5, 6	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub>	A-Side Inputs or 3-State Outputs
7	GND	Ground
8	OE	Output Enable Input
9, 10, 11, 12	B <sub>3</sub> , B <sub>2</sub> , B <sub>1</sub> , B <sub>0</sub>	B-Side Inputs or 3-State Outputs

## Truth Table

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

### Note:

1. If the OE pin is driven LOW, the FXMA2104 is disabled and the A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>, B<sub>0</sub>, B<sub>1</sub>, B<sub>2</sub> and B<sub>3</sub> pins (including dynamic drivers) are forced into 3-state.

## Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
$V_{CCA}, V_{CCB}$	Supply Voltage		-0.5	7.0	V
$V_{IN}$	DC Input Voltage	A Port	-0.5	7.0	
		B Port	-0.5	7.0	
		Control Input (OE)	-0.5	7.0	
$V_O$	Output Voltage <sup>(2)</sup>	$A_n$ Outputs 3-State	-0.5	7.0	V
		$B_n$ Outputs 3-State	-0.5	7.0	
		$A_n$ Outputs Active	-0.5	$V_{CCA} + 0.5V$	
		$B_n$ Outputs Active	-0.5	$V_{CCB} + 0.5V$	
$I_{IK}$	DC Input Diode Current	At $V_{IN} < 0V$		-50	mA
$I_{OK}$	DC Output Diode Current	At $V_O < 0V$		-50	mA
		At $V_O > V_{CC}$		+50	
$I_{OH} / I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin			±100	mA
$P_D$	Power Dissipation	At 400KHz		0.129	mW
$T_{STG}$	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5	kV
		Charged Device Mode, JESD22-C101		2	

**Note:**

- $I_O$  absolute maximum rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Units
$V_{CCA}, V_{CCB}$	Power Supply Operating		1.65	5.50	V
$V_{IN}$	Input Voltage	A Port	0	5.5	V
		B Port	0	5.5	
		Control Input (OE)	0	$V_{CCA}$	
$\Theta_{JA}$	Thermal Resistance			301.5	C°/W
$T_A$	Free Air Operating Temperature		-40	+85	°C

**Note:**

- All unused inputs and I/O pins must be held at  $V_{CCI}$  or GND,  $V_{CCI}$  is the  $V_{CC}$  associated with the input side.

## Functional Description

### Power-Up/Power-Down Sequencing

FXM translators offer an advantage in that either  $V_{CC}$  may be powered up first. This benefit derives from the chip design. When either  $V_{CC}$  is at 0V, outputs are in a high-impedance state. The control input (OE) is designed to track the  $V_{CCA}$  supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is:

1. Apply power to the first  $V_{CC}$ .
2. Apply power to the second  $V_{CC}$ .
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either  $V_{CC}$ .
3. Remove power from other  $V_{CC}$ .

#### Note:

4. Alternatively, the OE pin can be hardwired to  $V_{CCA}$  to save GPIO pins. If OE is hardwired to  $V_{CCA}$ , either  $V_{CC}$  can be powered up or down first.

### Application Circuit

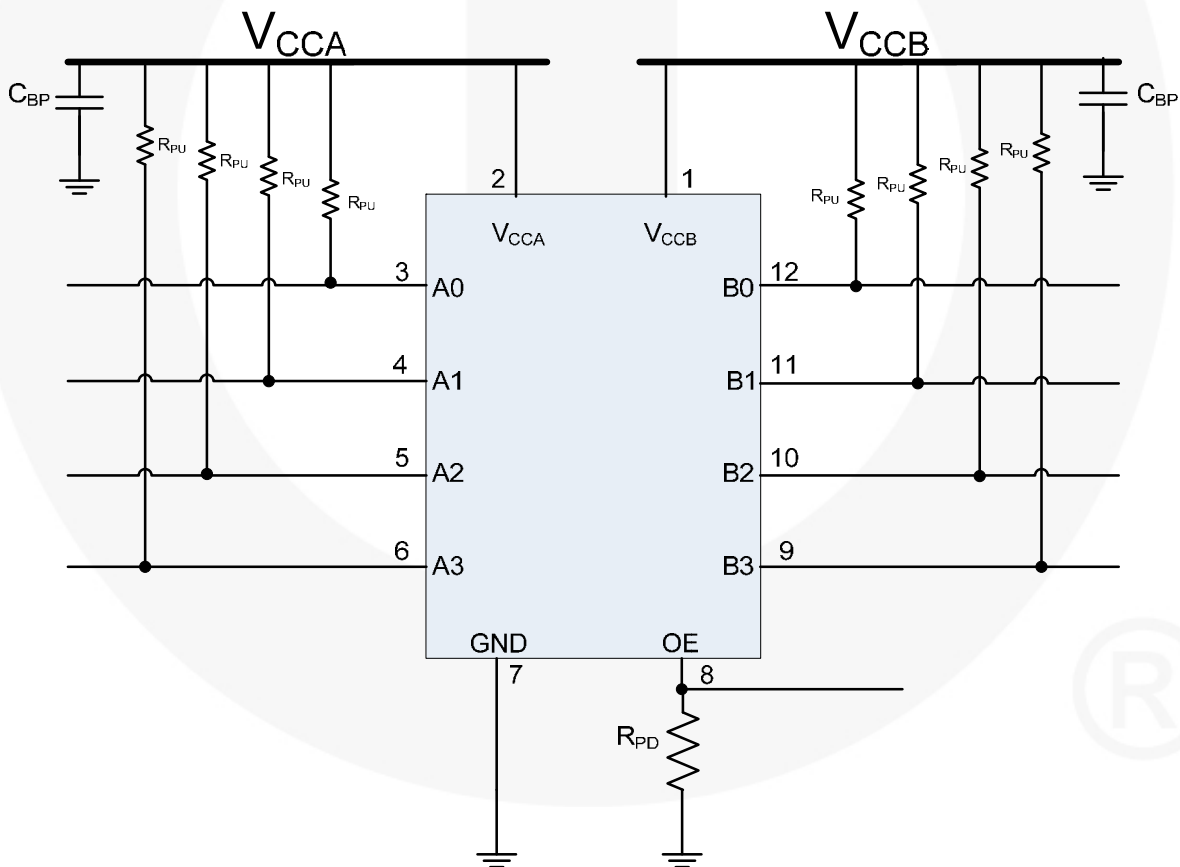


Figure 3. Application Circuit

## Application Information

The FXMA2104 has open-drain I/Os and requires external pull-up resistors on the eight data I/O pins, as shown in Figure 3. If a pair of data I/O pins ( $A_n/B_n$ ) is not used, both pins should be tied to GND (or both to  $V_{CC}$ ). In this case, pull-down or pull-up resistors are not required. The recommended values for the pull-up resistors (RPU) are 1K $\Omega$  to 10K, depending on the total bus capacitance, the user is free to vary the pull-up resistor value to meet the maximum I<sup>2</sup>C edge rate per the I<sup>2</sup>C specification (UM10204 rev. 03, June 19, 2007). For example, the maximum edge rate (30% - 70%) during Fast Mode (400kbit/s) is 300ns. If bus capacitance is approaching the maximum 400pF, lower the RPU value to keep the rise time below 300ns (Fast Mode). Section 7.1 of the I<sup>2</sup>C specification provides an excellent guideline for pull-up resistor sizing.

## Theory of Operation

The FXMA2104 is designed for high-performance level shifting and buffer / repeating in an I<sup>2</sup>C application. Figure 1 shows that each bi-directional channel contains two series-Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I<sup>2</sup>C application where auto-direction is a necessity.

For example, during the following three I<sup>2</sup>C protocol events:

- Clock Stretching
- Slave's ACK Bit (9<sup>th</sup> bit = 0) following a Master's Write Bit (8<sup>th</sup> bit = 0)
- Clock Synchronization and Multi Master Arbitration

the bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I<sup>2</sup>C translator between the master and slave in these examples, the I<sup>2</sup>C translator must change direction when both A and B ports are LOW. The Npassgates can accomplish this task very efficiently because, when both A and B ports are LOW, the Npassgates act as a low resistive short between the two (A and B) ports.

Due to I<sup>2</sup>C's open-drain topology, I<sup>2</sup>C masters and slaves are not push-pull drivers. Logic LOWs are "pulled down" ( $I_{sink}$ ), while logic HIGHs are "let go" (3-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where  $R = R_{PU}$  and  $C =$  the bus capacitance. If the FXMA2104 is attached to the master [on the A port] and there is a slave on the B port, the Npassgates act as a low resistive short

between the ports until either of the port's  $V_{CC}/2$  thresholds are reached. After the RC time constant has reached the  $V_{CC}/2$  threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot in Figure 4. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports because both the Npassgates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that device's driver pulls down ( $I_{sink}$ ) SCL or SDA until the edge reaches the A or B port  $V_{CC}/2$  threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

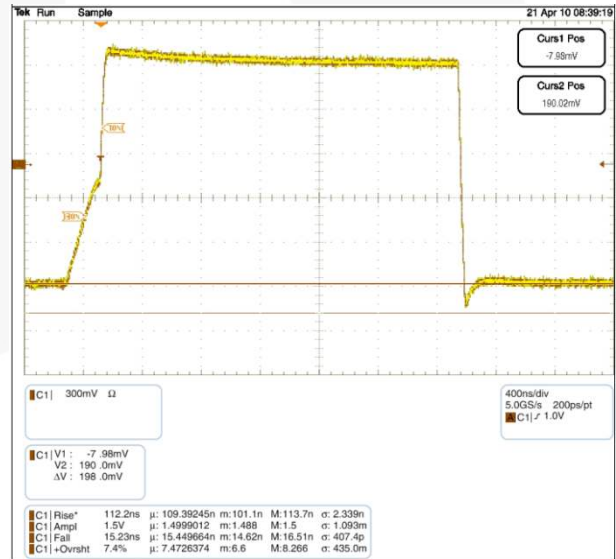


Figure 4. Waveform C: 600pF, Total  $R_{PU}$ : 2.2K $\Omega$

### Buffer / Repeater Performance

The FXMA2104 dynamic drivers have enough current-sourcing capability to drive a 400pF capacitive bus. This is beneficial when an I<sup>2</sup>C buffer / repeater is required. The I<sup>2</sup>C specification stipulates a maximum bus capacitance of 400pF. If an I<sup>2</sup>C segment exceeds 400pF, an I<sup>2</sup>C buffer / repeater is required to split the segment into two segments, each of which is less than 400pF. Figure 4 is a scope shot of an FXMA2104 driving a lumped load of 600pF. Notice the (30% - 70%) rise time is only 112ns (total R<sub>PU</sub> = 2.2K · ). This is well below the maximum edge rate of 300ns. Not only does the FXMA2104 drive 400pF; it also provides excellent headroom below the I<sup>2</sup>C specification maximum edge rate of 300ns.

### V<sub>OL</sub> vs. I<sub>OL</sub>

The I<sup>2</sup>C specification mandates a maximum V<sub>IL</sub> (I<sub>OL</sub> of 3mA) of V<sub>CC</sub> · 0.3 and a maximum V<sub>OL</sub> of 0.4V. If there is a master on the A port of an I<sup>2</sup>C translator with a V<sub>CC</sub> of 1.65V and a slave on the I<sup>2</sup>C translator B port with a V<sub>CC</sub> of 3.3V, the maximum V<sub>IL</sub> of the master is (1.65V x 0.3) 495mV. The slave could legally transmit a valid logic LOW of 0.4V to the master.

If the I<sup>2</sup>C translator's channel resistance is too high, the voltage drop across the translator could present a V<sub>IL</sub> to the master greater than 495mV. To complicate matters, the I<sup>2</sup>C specification states that 6mA of I<sub>OL</sub> is recommended for bus capacitances approaching 400pF. More I<sub>OL</sub> increases the voltage drop across the I<sup>2</sup>C translator. The I<sup>2</sup>C application benefits when I<sup>2</sup>C translators exhibit low V<sub>OL</sub> performance. Figure 5 depicts typical FXMA2104 V<sub>OL</sub> performance vs. a competitor, given a 0.4V V<sub>IL</sub>.

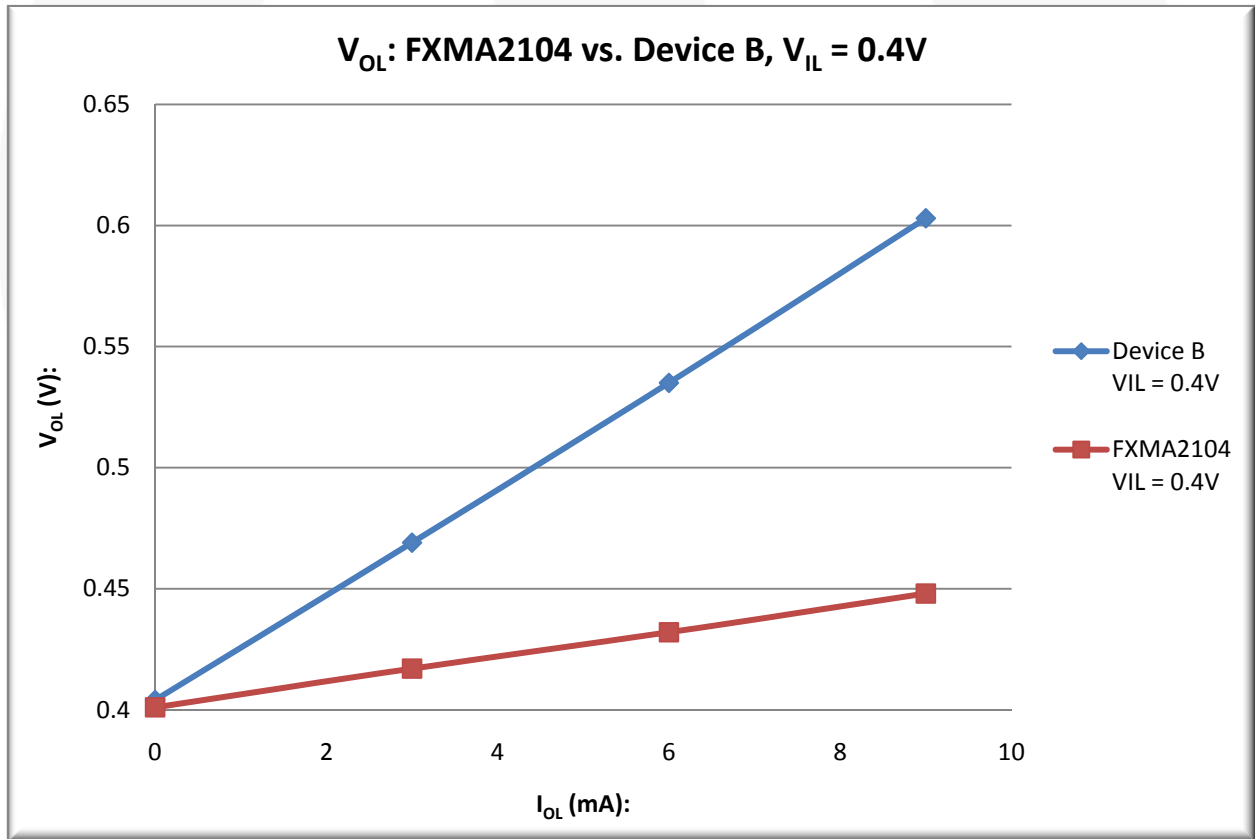


Figure 5. V<sub>OL</sub> vs. I<sub>OL</sub>



## I<sup>2</sup>C Bus Isolation

The FXMA2104 supports I<sup>2</sup>C-Bus<sup>®</sup> isolation for the following conditions:

- Bus isolation if bus clear
- Bus isolation if either V<sub>CC</sub> goes to ground

### Bus Clear

Because the I<sup>2</sup>C specification defines the minimum SCL frequency of DC, the SCL signal can be held LOW forever; however, this condition shuts down the I<sup>2</sup>C bus. The I<sup>2</sup>C specification refers to this condition as Bus Clear. In Figure 6, if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the FXMA2104 passes the SCL stuck-LOW

condition from slave #2 to slave #1 as well as the master. However, if the OE pin is pulled LOW (disabled), both ports (A and B) are 3-stated. This results in the FXMA2104 isolating slave #2 from the master and slave #1, allowing full communication between the master and slave #1.

### Either V<sub>CC</sub> to GND

If slave #2 is a camera that is suddenly removed from the I<sup>2</sup>C bus, resulting in V<sub>CCB</sub> transitioning from a valid V<sub>CC</sub> (1.65V – 5.5V) to 0V; the FXMA2104 automatically forces all I/Os on both its A and B ports into 3-state. Once V<sub>CCB</sub> has reached 0V, full I<sup>2</sup>C communication between the master and slave #1 remains undisturbed.

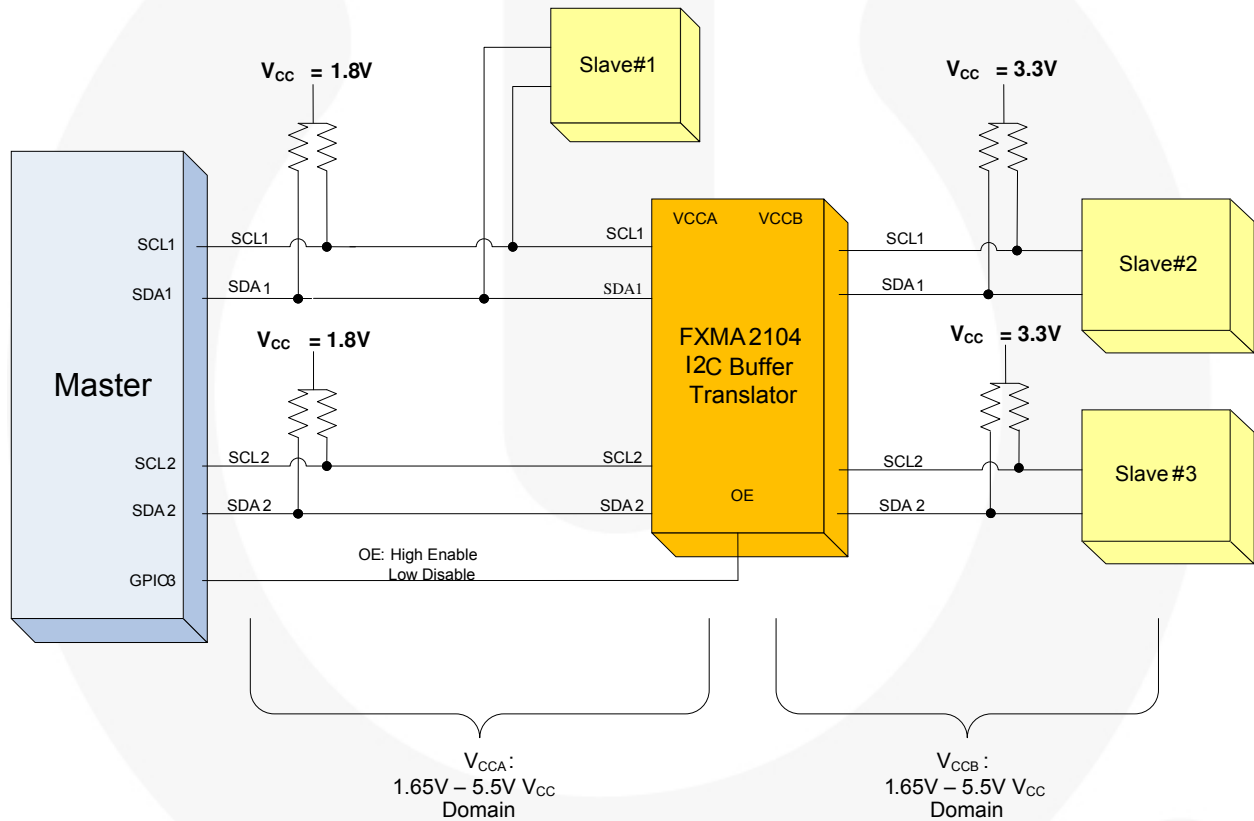


Figure 6. Bus Isolation

## DC Electrical Characteristics

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Symbol	Parameter	Condition	$V_{CCA}$ (V)	$V_{CCB}$ (V)	Min.	Max.	Unit
$V_{IHA}$	High Level Input Voltage A	Data Inputs $A_n$	1.65–5.50	1.65–5.50	$V_{CCA} - 0.4$		V
		Control Input OE	1.65–5.50	1.65–5.50	$0.7 \times V_{CCA}$		
$V_{IHB}$	High Level Input Voltage B	Data Inputs $B_n$	1.65–5.50	1.65–5.50	$V_{CCB} - 0.4$		V
$V_{ILA}$	Low Level Input Voltage A	Data Inputs $A_n$	1.65–5.50	1.65–5.50		0.4	V
		Control Input OE	1.65–5.50	1.65–5.50		$0.3 \times V_{CCA}$	
$V_{ILB}$	Low Level Input Voltage B	Data Inputs $B_n$	1.65–5.50	1.65–5.50		0.4	V
$V_{OL}$	Low Level Output Voltage	$V_{IL} = 0.15\text{V}$	1.65–5.50	1.65–5.50		0.4	V
		$I_{OL} = 6\text{mA}$					
$I_L$	Input Leakage Current	Control Input OE, $V_{IN} = V_{CCA}$ or GND	1.65–5.50	1.65–5.50		$\pm 1$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$A_n$ $V_{IN}$ or $V_O = 0\text{V}$ to 5.5V	0	5.50		$\pm 2$	$\mu\text{A}$
		$B_n$ $V_{IN}$ or $V_O = 0\text{V}$ to 5.5V	5.50	0		$\pm 2$	
$I_{OZ}$	3-State Output Leakage <sup>(6)</sup>	$A_n, B_n$ $V_O = 0\text{V}$ to 5.5V, OE = $V_{IL}$	5.50	5.50		$\pm 2$	$\mu\text{A}$
		$A_n$ $V_O = 0\text{V}$ to 5.5V, OE = Don't Care	5.50	0		$\pm 2$	
		$B_n$ $V_O = 0\text{V}$ to 5.5V, OE = Don't Care	0	5.50		$\pm 2$	
$I_{CCA/B}$	Quiescent Supply Current <sup>(7,8)</sup>	$V_{IN} = V_{CCI}$ or GND, $I_O = 0$	1.65–5.50	1.65–5.50		5	$\mu\text{A}$
$I_{CCZ}$	Quiescent Supply Current <sup>(7)</sup>	$V_{IN} = V_{CCI}$ or GND, $I_O = 0$ , OE = $V_{IL}$	1.65–5.50	1.65–5.50		5	$\mu\text{A}$
$I_{CCA}$	Quiescent Supply Current <sup>(6)</sup>	$V_{IN} = 5.5\text{V}$ or GND, $I_O = 0$ , OE = Don't Care, $B_n$ to $A_n$	0	1.65–5.50		-2	$\mu\text{A}$
			1.65–5.50	0		2	
$I_{CCB}$	Quiescent Supply Current <sup>(6)</sup>	$V_{IN} = 5.5\text{V}$ or GND, $I_O = 0$ , OE = Don't Care, $A_n$ to $B_n$	1.65–5.50	0		-2	$\mu\text{A}$
			0	1.65–5.50		2	

### Notes:

- This table contains the output voltage for static conditions. Dynamic drive specifications are given in Dynamic Output Electrical Characteristics.
- "Don't Care" indicates any valid logic level.
- $V_{CCI}$  is the  $V_{CC}$  associated with the input side.
- Reflects current per supply,  $V_{CCA}$  or  $V_{CCB}$ .

## Dynamic Output Electrical Characteristics

### Output Rise / Fall Time

Output load:  $C_L = 50\text{pF}$ ,  $R_{PU} = 2.2\text{k}\Omega$ , push / pull driver, and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	$V_{CCO}^{(10)}$				Unit
		4.5 to 5.5V	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V	
		Typical				
$t_{rise}$	Output Rise Time; A Port, B Port <sup>(11)</sup>	3	4	5	7	ns
$t_{fall}$	Output Fall Time; A Port, B Port <sup>(12)</sup>	11	8	6	4	ns

#### Notes:

9. Output rise and fall times guaranteed by design simulation and characterization; not production tested.

10.  $V_{CCO}$  is the  $V_{CC}$  associated with the output side.

11. See Figure 11.

12. See Figure 12.

### Maximum Data Rate<sup>(13)</sup>

Output load:  $C_L = 50\text{pF}$ ,  $R_{PU} = 2.2\text{k}\Omega$ , push-pull driver, and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

$V_{CCA}$	Direction	$V_{CCB}$				Unit
		4.5 to 5.5V	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V	
		Minimum				
4.5V to 5.5V	A to B	26	20	16	9	MHz
	B to A	26	20	16	9	
3.0V to 3.6V	A to B	26	20	16	9	MHz
	B to A	26	20	16	9	
2.3V to 2.7V	A to B	26	20	16	9	MHz
	B to A	26	20	16	9	
1.65V to 1.95V	A to B	26	20	16	9	MHz
	B to A	26	20	16	9	

#### Note:

13. F-toggle guaranteed by design simulation; not production tested.

## AC Characteristics<sup>(17)</sup>

Output Load:  $C_L = 50\text{pF}$ ,  $R_{PU} = 2.2\text{k}\Omega$ , and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	$V_{CCB}$								Units
		4.5 to 5.5V		3.0 to 3.6V		2.3 to 2.7V		1.65 to 1.95V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
<b><math>V_{CCA} = 4.5</math> to <math>5.5\text{V}</math></b>										
$t_{PLH}$	A to B	1	3	1	3	1	3	1	3	ns
	B to A	1	3	2	4	3	5	4	7	
$t_{PHL}$	A to B	2	4	3	5	4	6	6	7	ns
	B to A	2	4	2	5	2	6	5	7	
$t_{PZL}$	OE to A	4	5	6	10	5	9	7	15	ns
	OE to B	3	5	4	7	5	8	10	15	
$t_{PLZ}$	OE to A	65	100	65	105	65	105	65	105	ns
	OE to B	5	9	6	10	7	12	9	16	
$t_{skew}$	A Port, B Port <sup>(14)</sup>	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
<b><math>V_{CCA} = 3.0</math> to <math>3.6\text{V}</math></b>										
$t_{PLH}$	A to B	2.0	5.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	B to A	1.5	3.0	1.5	4.0	2.0	6.0	3.0	9.0	
$t_{PHL}$	A to B	2	4	2	4	2	5	6	7	ns
	B to A	2	4	2	4	2	5	3	5	
$t_{PZL}$	OE to A	4	8	5	9	6	11	7	15	ns
	OE to B	4	8	6	9	8	11	10	14	
$t_{PLZ}$	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	5	10	4	8	5	10	9	15	
$t_{skew}$	A Port, B Port <sup>(14)</sup>	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
<b><math>V_{CCA} = 2.3</math> to <math>2.7\text{V}</math></b>										
$t_{PLH}$	A to B	2.5	5.0	2.5	5.0	2.0	4.0	1.0	3.0	ns
	B to A	1.5	3.0	2.0	4.0	3.0	6.0	5.0	10.0	
$t_{PHL}$	A to B	2	5	2	5	2	5	5	6	ns
	B to A	2	5	2	5	2	5	3	6	
$t_{PZL}$	OE to A	5	10	5	10	6	12	9.0	18.0	ns
	OE to B	4.0	8.0	4.5	9.0	5.0	10.0	9.0	18.0	
$t_{PLZ}$	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	65	110	65	110	65	115	12	25	
$t_{skew}$	A Port, B Port <sup>(14)</sup>	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
<b><math>V_{CCA} = 1.65</math> to <math>1.95\text{V}</math></b>										
$t_{PLH}$	A to B	4.0	7.0	4.0	7.0	5.0	8.0	5.0	10.0	ns
	B to A	1.0	2.0	1.0	2.0	1.5	3.0	5.0	10.0	
$t_{PHL}$	A to B	5	8	3	7	3	7	8	9	ns
	B to A	4	8	3	7	3	7	3	7	
$t_{PZL}$	OE to A	11	15	11	14	14	28	14	23	ns
	OE to B	6	14	6	14	6	14	9	19	
$t_{PLZ}$	OE to A	75	115	75	115	75	115	75	115	ns
	OE to B	75	115	75	115	75	115	75	115	
$t_{skew}$	A Port, B Port <sup>(14)</sup>	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

**Note:**

14. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port ( $A_n$  or  $B_n$ ) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 14). Skew is guaranteed, but not tested.

15. AC Characteristic is guaranteed by Design and Characterization.

## Capacitance

$T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance Control Pin (OE)	$V_{CCA} = V_{CCB} = \text{GND}$	2.2	pF
$C_{I/O}$	Input / Output Capacitance, $A_n, B_n$	$V_{CCA} = V_{CCB} = 5.0\text{V}$ , $\text{OE} = \text{GND}$	13.0	pF
$C_{pd}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 5.0\text{V}$ , $V_{IN} = 0\text{V}$ or $V_{CC}$ , $f = 400\text{KHz}$	13.5	pF

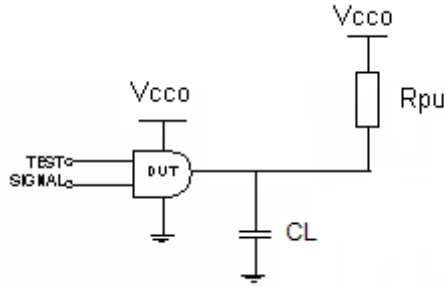


Figure 7. AC Test Circuit

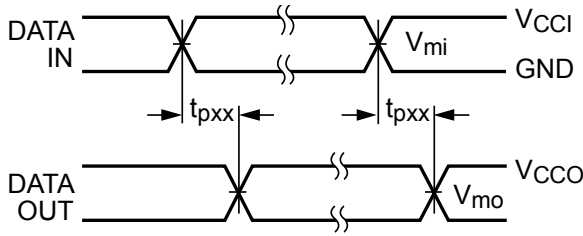
Table 1. Propagation Delay Table<sup>(17)</sup>

Test	Input Signal	Output Enable Control
$t_{PLH}$ , $t_{PHL}$	Data Pulses	$V_{CCA}$
$t_{PZL}$ (OE to $A_n, B_n$ )	0V	LOW to HIGH Switch
$t_{PLZ}$ (OE to $A_n, B_n$ )	0V	HIGH to LOW Switch

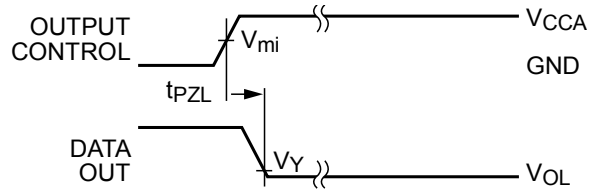
Table 2. AC Load Table

$V_{cco}$	$C_L$	$R_L$
$1.8 \pm 0.15\text{V}$	50pF	2.2k $\Omega$
$2.5 \pm 0.2\text{V}$	50pF	2.2k $\Omega$
$3.3 \pm 0.3\text{V}$	50pF	2.2k $\Omega$
$5.0 \pm 0.5\text{V}$	50pF	2.2k $\Omega$

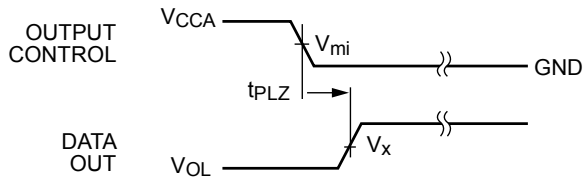
## Timing Diagrams



**Figure 8. Waveform for Inverting and Non-Inverting Functions<sup>(16)</sup>**

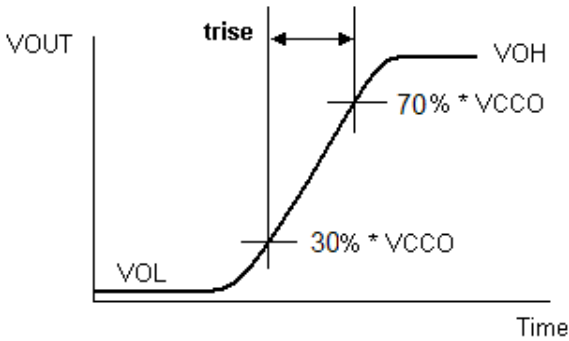


**Figure 9. 3-STATE Output Low Enable Time<sup>(16)</sup>**

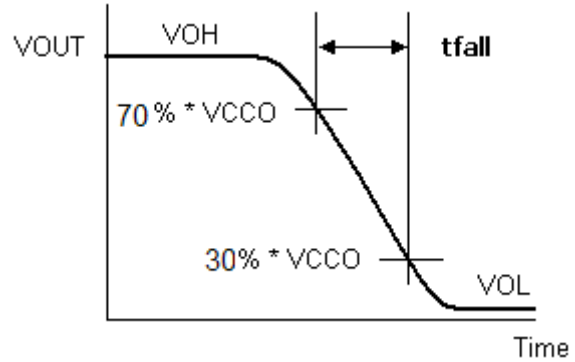


**Figure 10. 3-STATE Output High Enable Time<sup>(16)</sup>**

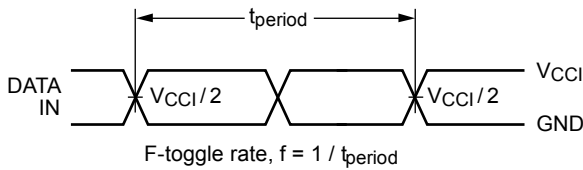
Symbol	V <sub>CC</sub>
V <sub>mi</sub>	V <sub>CCI</sub> / 2
V <sub>mo</sub>	V <sub>CCO</sub> / 2
V <sub>X</sub>	0.5 x V <sub>CCO</sub>
V <sub>Y</sub>	0.1 x V <sub>CCO</sub>



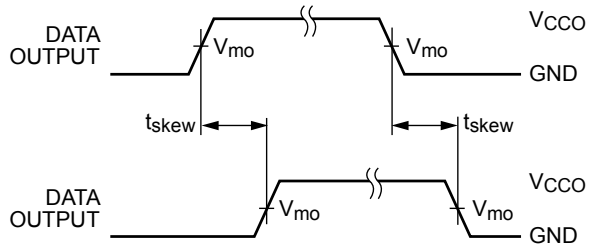
**Figure 11. Active Output Rise Time**



**Figure 12. Active Output Fall Time**



**Figure 13. F-Toggle Rate**

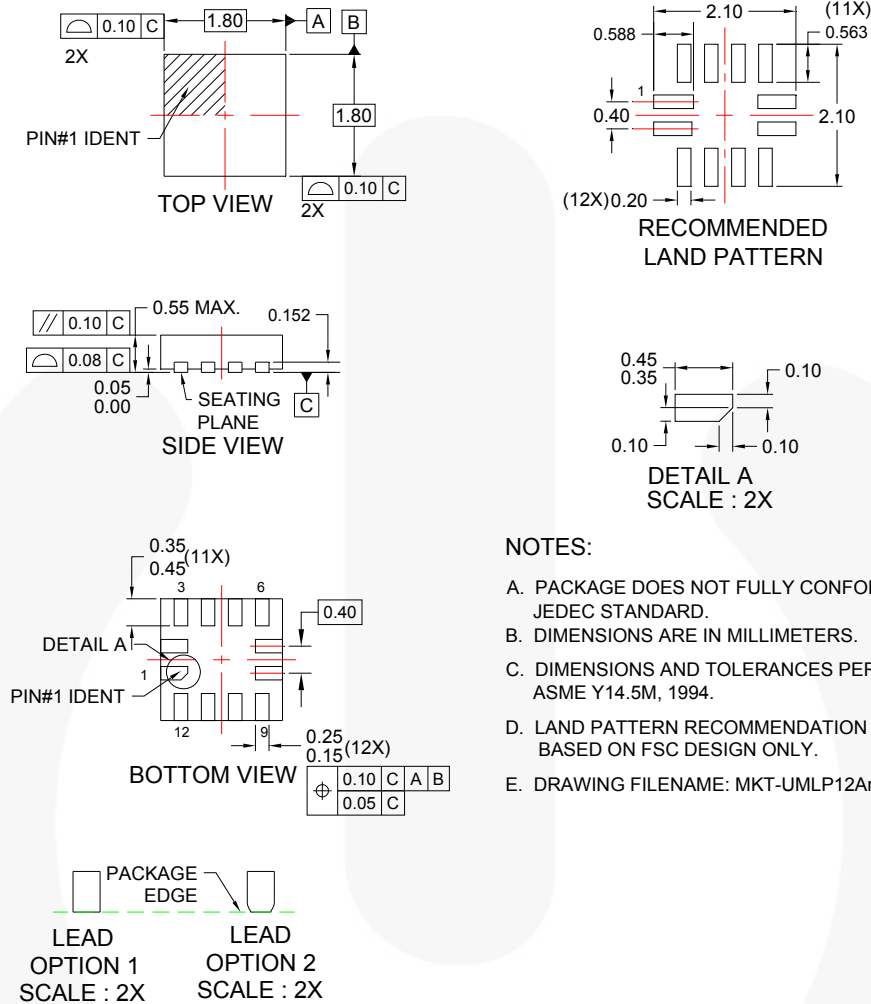


**Figure 14. Output Skew Time**

### Notes:

16. Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% at  $V_{IN} = 1.65\text{V}$  to  $1.95\text{V}$ ;  
 Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% at  $V_{IN} = 2.3$  to  $2.7\text{V}$ ;  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, at  $V_{IN} = 3.0\text{V}$  to  $3.6\text{V}$  only;  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, at  $V_{IN} = 4.5\text{V}$  to  $5.5$  only.
17.  $V_{CCI} = V_{CCA}$  for control pin OE or  $V_{mi} = (V_{CCA} / 2)$ .

## Physical Dimensions



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**Figure 15. 12-Lead Ultrathin MLP, 1.8mm x 1.8mm**





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