High-Efficiency, Quad Output, Main Power-Supply Controllers for Notebook Computers

General Description

The RT8203 dual step-down, Switch Mode Power Supply (SMPS) controllers generate logic-supply voltages in battery-powered systems. The RT8203 include two pulse-width modulation (PWM) controllers, adjustable from 2V to 5.5V or fixed at 5V and 3.3V. These devices feature two linear regulators providing 5V and 3.3V always-on outputs. Each linear regulator provides up to 100mA output current with automatic linear regulator bootstrapping to the main SMPS outputs. The RT8203 include on-board power-up sequencing, a power good (PGOOD) output, internal soft-start, and soft-shutdown output discharge that prevents negative voltages on shutdown. Richtek's proprietary Mach-PWM™ "instant-on" response, constant on-time PWM control scheme operates without sense resistors and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The unique ultrasonic mode maintains the switching frequency above 25kHz, which eliminates noise in audio applications. Other features include diode-emulation, which maximizes efficiency in light-load applications, and fixed-frequency PWM mode, which reduces RF interference in sensitive applications. The RT8203 provides a pin-selectable switching frequency, allowing either 200kHz/300kHz or 400kHz/500kHz operation of the 5V/3.3V SMPSs, respectively. The RT8203 is available in SSOP-28 package.

Ordering Information

RT8203□ □

- Package Type
  - A : SSOP-28
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **No Current Sense Resistor Needed**
- **1.5% Output Voltage Accuracy**
- **3.3V and 5V 100mA Bootstrapped Linear Regulators**
- **Internal Soft-Start and Soft-Shutdown Output Discharge**
- **Mach-PWM with 100ns Load Step Response**
- **3.3V and 5V Fixed or Adjustable Outputs**
- **7V to 24V Input Voltage Range**
- **Ultrasonic Mode Operation 25kHz (min.)**
- **Power Good (PGOOD) Signal**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Notebook and Subnotebook Computers
- PDAs and Mobile Communication Devices
- 3- and 4-Cell Li+ Battery-Powered Devices

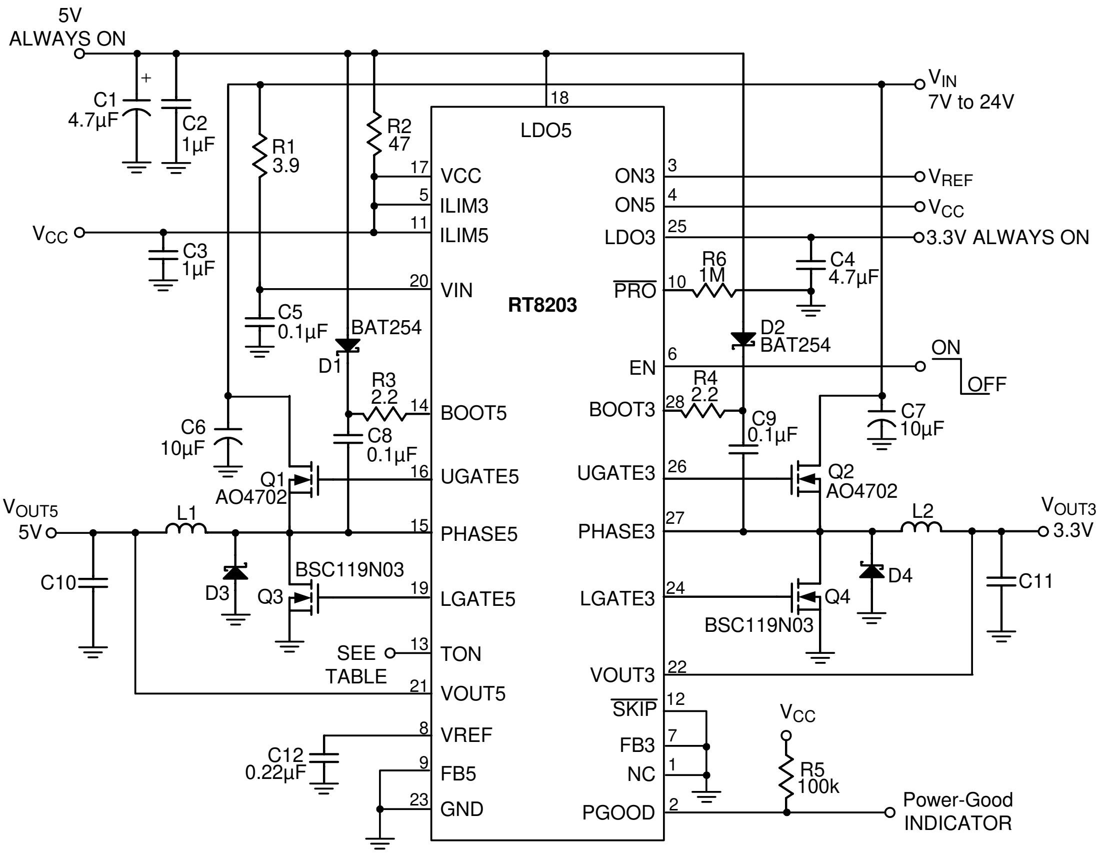
Pin Configurations

(TOP VIEW)

Pin Name	Pin	Pin	Pin Name
NC	1	28	BOOT3
PGOOD	2	27	PHASE3
ON3	3	26	UGATE3
ON5	4	25	LDO3
ILIM3	5	24	LGATE3
EN	6	23	GND
FB3	7	22	VOUT3
VREF	8	21	VOUT5
FB5	9	20	VIN
$\overline{\text{PRO}}$	10	19	LGATE5
ILIM5	11	18	LDO5
$\overline{\text{SKIP}}$	12	17	VCC
TON	13	16	UGATE5
BOOT5	14	15	PHASE5

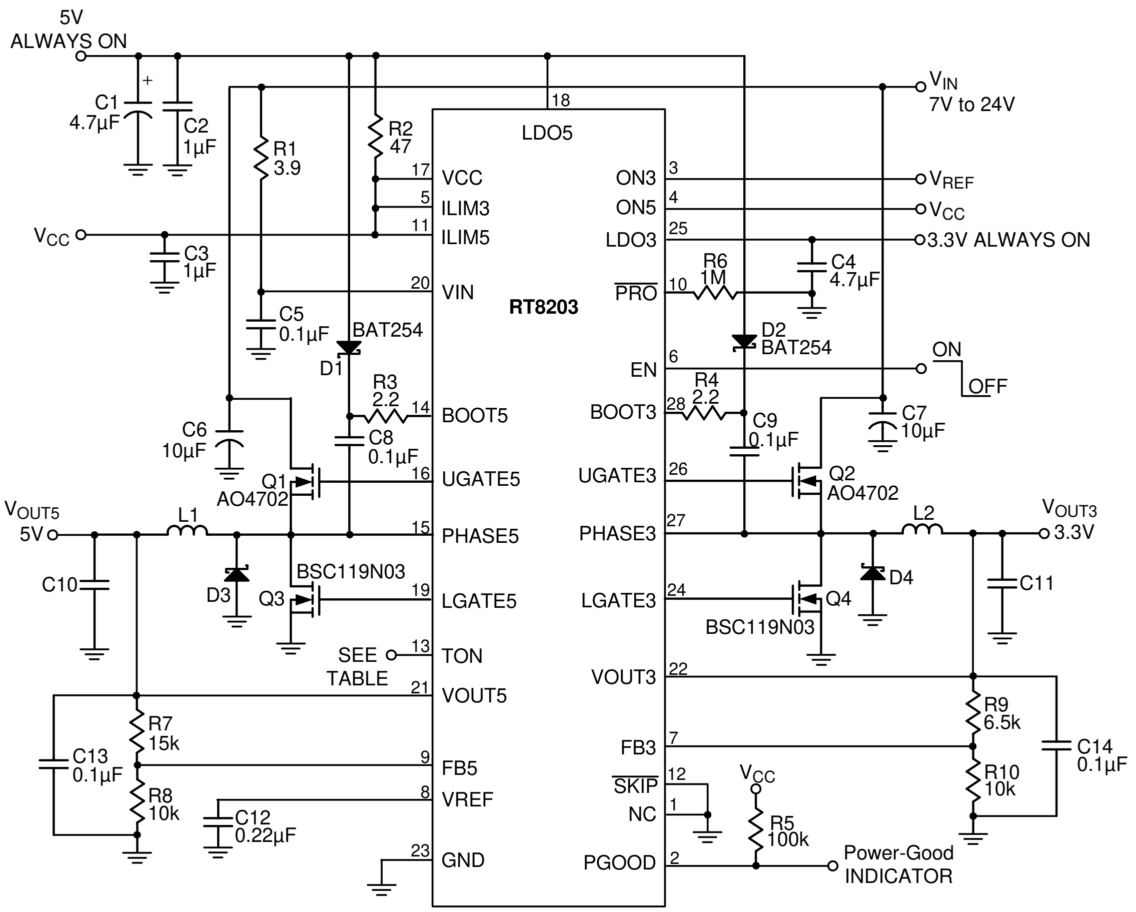
SSOP-28

Typical Application Circuit



Frequency-dependent Components			
VOUT5		VOUT3	
TON = VCC	TON = GND	TON = VCC	TON = GND
f = 200kHz	f = 400kHz	f = 300kHz	f = 500kHz
L1 = 7.6µH	L1 = 5.6µH	L2 = 4.7µH	L2 = 3µH
C10 = 330µF	C10 = 150µF	C11 = 470µF	C11 = 220µF

Figure 1. Fixed Voltage Regulator



Frequency-dependent Components			
VOUT5		**VOUT3**	
TON = VCC	TON = GND	TON = VCC	TON = GND
f = 200kHz	f = 400kHz	f = 300kHz	f = 500kHz
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C10 = 330μF	C10 = 150μF	C11 = 470μF	C11 = 220μF

Figure 2. Adjustable Voltage Regulator

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	NC	Connect to GND.
2	PGOOD	Power Good Open Drain Output. PGOOD is pulled low if either output is disable or is more than 8.75% below its normal value.
3	ON3	VOUT3 Enable Input. The 3.3V SMPS is enable if ON3 is greater than the on level and disable if ON3 is less than the off level. If ON3 is connected to V_{REF}, the 3.3V SMPS starts after the 5V SMPS reached regulation(delay start). Force ON3 below the clear fault level to reset the fault latched.
4	ON5	VOUT5 Enable Input. The 5V SMPS is enable if ON5 is greater than the on level and disable if ON5 is less than the off level. If ON5 is connected to VREF, the 5V SMPS starts after the 3.3V SMPS reached regulation(delay start). Force ON5 below the clear fault level to reset the fault latched.
5	ILIM3	VOUT3 Current Limit Adjustment. The GND-PHASE3 current limit threshold defaults to 100mV if ILIM3 is tied to VCC. In adjustable mode, the current limit threshold is 1/10 the voltage seen at ILIM3 over 0.5V to 3V range. The logic threshold for switch over to 100mV default value is approximately VCC − 1V.
6	EN	Enable Control Input. The device enters its 15μA supply current shutdown mode if EN is less than the EN input falling edge trip level and does not restart until EN is greater than the EN input rising edge trip level. Connect EN to VIN for automatically startup. EN can be connected to VIN through a resistive voltage divider to implement a programmable undervoltage lockout.
7	FB3	VOUT3 Feedback Input. Connect FB3 to GND for fixed 3.3V operation. Connect FB3 to a resistive voltage divider from VOUT3 to GND to adjust the output from 2V to 5.5V.
8	VREF	2V Reference Output. Bypass to GND with a $0.22\mu F_{(MIN)}$ capacitor. VREF can source up to 100μA for external loads. Loading VREF degrades FBx and VOUTx accuracy according to the VREF load regulation error.
9	FB5	VOUT5 Feedback Input. Connect FB5 to GND for fixed 5V operation. Connect FB5 to a resistive voltage divider from VOUT5 to GND to adjust the output from 2V to 5.5V.
10	$\overline{PRO}$	Over Voltage and Under Voltage Fault Protection Enable/Disable. Connect $\overline{PRO}$ to VCC to disable Over Voltage and Under Voltage protection. Connect PRO to GND to enable Over Voltage and Under Voltage protection.
11	ILIM5	VOUT5 Current Limit Adjustment. The GND − PHASE5 current limit threshold defaults to 100mV if ILIM5 is tied to VCC. In adjustable mode, the current limit threshold is 1/10 the voltage seen at ILIM5 over 0.5V to 3V range. The logic threshold for switch over to 100mV default value is approximately VCC − 1V.
12	$\overline{SKIP}$	Operation Mode Input Control. Connect $\overline{SKIP}$ to GND for diode-emulation mode (DEM) or to VCC for CCM mode(fixed frequency). Connect to VREF or floating for ultrasonic mode.
13	TON	Frequency Select Input. Connect to VCC for 200kHz/300kHz operation and to GND for 400kHz/500kHz operation (VOUT5/VOUT3 switching frequency respectively).
14	BOOT5	Boost Capacitor Connection for 5V SMPS. Connect an external ceramic capacitor to PHASE5 and an external diode to LDO5.

To be continued

Pin No.	Pin Name	Pin Function
15	PHASE5	Inductor Connection for 5V SMPS. PHASE5 is the internal lower supply rail for the UGATE5 high side gate driver, and the current sense input for the 5V SMPS.
16	UGATE5	High Side N-MOSFET Floating Gate-Driver Output for VOUT5. Swings between PHASE5 and BOOT5.
17	VCC	Analog Supply Voltage Input for the internal analog integrated circuit. Bypass to GND with a 1μF ceramic capacitor.
18	LDO5	5V Linear Regulator Output. LDO5 is the gate driver supply for the external MOSFETs. LDO5 can provide a total of 100mA, including the MOSFET gate-driver requirements and external loads. If VOUT5 is greater than the LDO5 switchover threshold, the LDO5 regulator shuts down and LDO5 pin connects to VOUT5 through a 1.4Ω switch. Bypass a 4.7μF ceramic capacitor to GND.
19	LGATE5	Low side N-MOSFET Gate-Drive Output for VOUT5. Swings between GND and LDO5.
20	VIN	Power-Supply Input. VIN powers the LDO5/LDO3 linear regulators and is also used for PWM control circuits. Connect VIN to the battery input or the AC adapter output.
21	VOUT5	VOUT5 Sense Input. Connect to the 5V output. VOUT5 is an input to the PWM control circuit. It also serves as the 5V feedback input in fixed-voltage mode. If VOUT5 is greater than the LDO5 switchover threshold, the LDO5 shuts down and LDO5 connects to VOUT5 through 1.4Ω switch.
22	VOUT3	VOUT3 Sense Input. Connect to the 3.3V output. VOUT3 is an input to the PWM control circuit. It also serves as the 3.3V feedback input in fixed voltage mode. If VOUT3 is greater than the LDO3 switchover threshold, the LDO3 shuts down and LDO3 connects to VOUT3 through 1.5Ω switch.
23	GND	Analog and Power Ground.
24	LGATE3	Low side N-MOSFET Gate-Drive Output for VOUT3. Swings between GND and LDO5.
25	LDO3	3.3V Linear Regulator Output. LDO3 can provide a total of 100mA to external loads. If VOUT3 is greater than the LDO3 switchover threshold, the LDO3 regulator shuts down and LDO3 pin connects to VOUT3 through a 1.5Ω switch. Bypass a 4.7μF ceramic capacitor to GND.
26	UGATE3	High Side N-MOSFET Floating Gate-Driver Output for VOUT3. Swings between PHASE3 and BOOT3.
27	PHASE3	Inductor Connection for 3.3V SMPS. PHASE3 is the internal lower supply rail for the UGATE3 high side gate driver, and the current sense input for the 3.3V SMPS.
28	BOOT3	Boost Capacitor Connection for 3.3V SMPS. Connect an external ceramic capacitor to PHASE3 and an external diode to LDO5.

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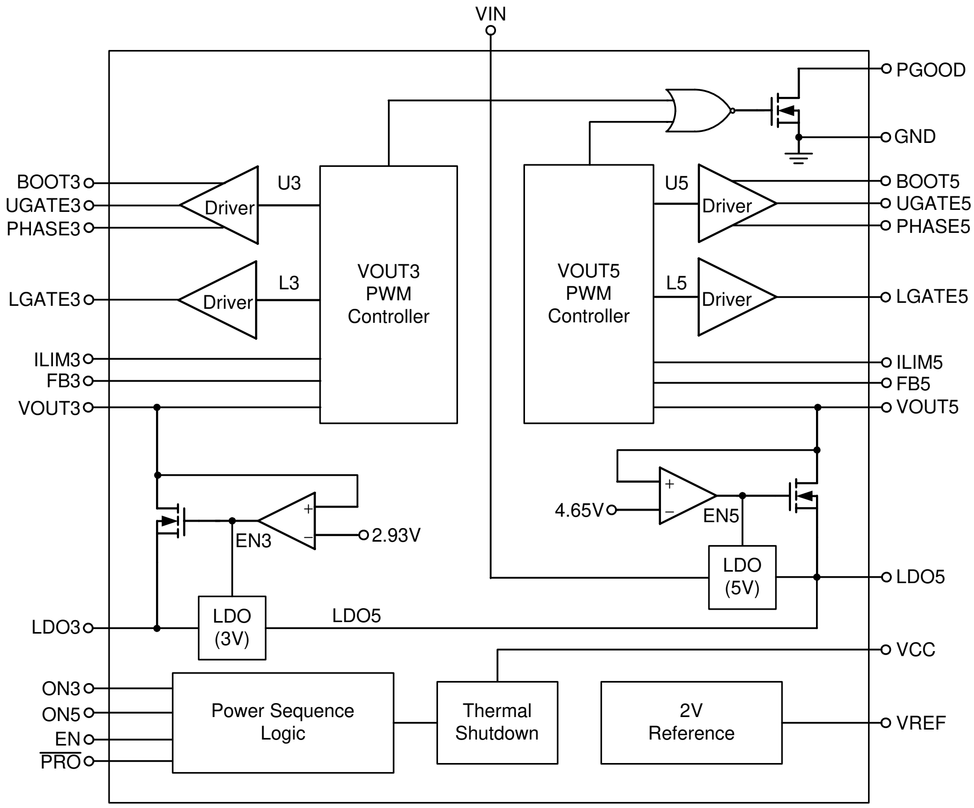
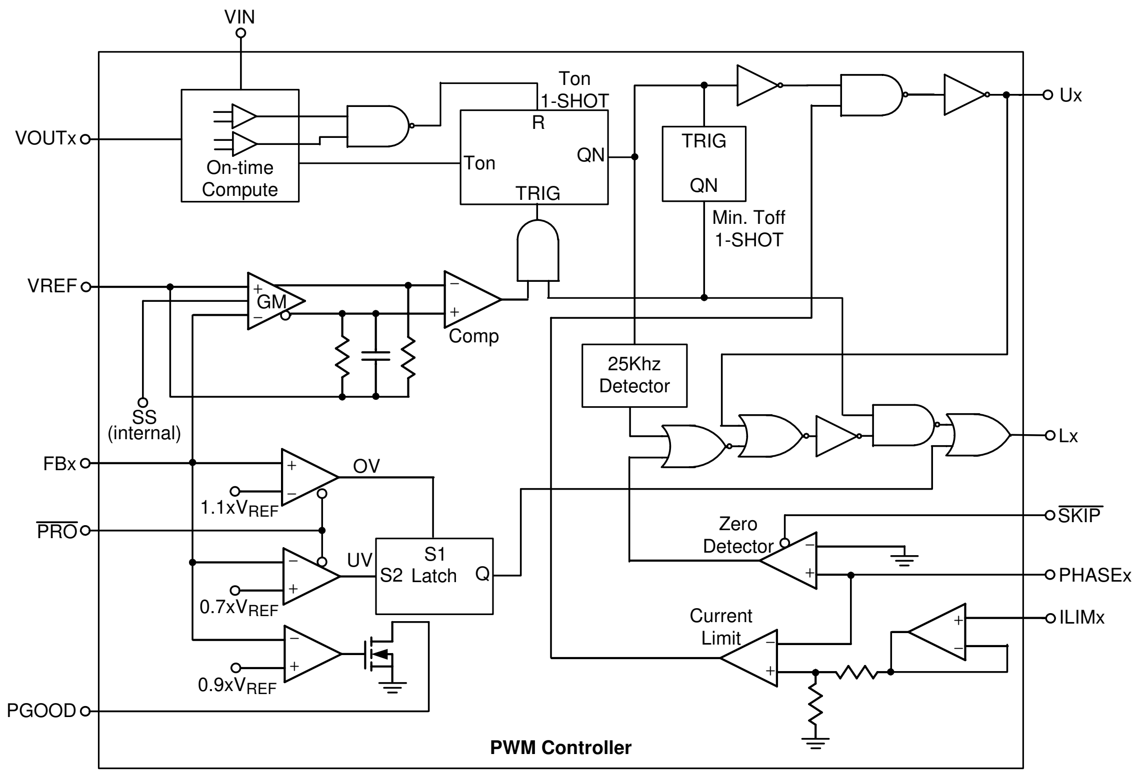
Function Block Diagram





Absolute Maximum Ratings (Note 1)

- Input Voltage, V_{IN}, EN to GND ---------- –0.3V to 25V
- BOOTx to GND ---------- –0.3V to 30V
- PHASEx to BOOTx ---------- –6V to 0.3V
- PHASEx to GND ---------- –1V to 25V
- VCC, LDOx, VOUTx, ONx, VREF, FBx, $\overline{SKIP}$, $\overline{PRO}$, PGOOD to GND ---------- –0.3V to 6V
- UGATEx to PHASEx ---------- –0.3V to (V_{BOOTx} + 0.3V)
- ILIMx to GND ---------- –0.3V to (V_{CC} + 0.3V)
- LGATEx to GND ---------- –0.3V to (V_{LDO5} + 0.3V)
- TON to GND ---------- –0.3V to 6V
- LDOx, VREF Short Circuit to GND ---------- Momentary
- LDOx Circuit (Internal Regulator) Continuous ---------- 100mA
- LDOx Circuit (Switchover to VOUTx) Continuous ---------- 200mA
- Power Dissipation, P_D @ T_A = 25°C
  SSOP-28 ---------- 1.053W
- Package Thermal Resistance (Note 2)
  SSOP-28, θ_{JA} ---------- 95°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 7V to 24V
- Control Voltage, V_{CC} ---------- 5V ± 5%
- Junction Temperature Range ---------- –10°C to 125°C
- Ambient Temperature Range ---------- –10°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, No load on LDOx, VOUTx and VREF, ONx = VCC, V_{EN} = 5V, T_A = 25°C, unless Otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Main SMPS Controllers						
Input Voltage Range	V_{IN}	LDO5 in regulation	7	--	24	V
VOUT3 Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 7V to 24V, FB3 = GND, $V_{\overline{SKIP}}$ = 5V	3.285	3.330	3.375	V
VOUT5 Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 8V to 24V, FB5 = GND, $V_{\overline{SKIP}}$ = 5V	4.975	5.059	5.125	V
Output Voltage in Adjustable Mode		V_{IN} = 7V to 24V, either SMPS	1.975	2.00	2.025	V
Output Voltage Adjust Range		Either SMPS	2	--	5.5	V
FBx Adjustable-Mode Threshold Voltage		Dual-Mode comparator	0.12	--	0.22	V

To be continued

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DC Load Regulation	ΔV_{LOAD}	Either SMPS, $V_{\overline{SKIP}}$ = 5V, 0 to 5A		--	–0.1	--	%
		Either SMPS, $V_{\overline{SKIP}}$ = GND, 0 to 5A		--	–1.5	--	
		Either SMPS, $V_{\overline{SKIP}}$ = 2V, 0 to 5A		--	–1.7	--	
Line Regulation	ΔV_{LINE}	Either SMPS, 7V< V_{IN} <24V		---	0.005	--	%/V
Current-Limit Threshold (Positive, Default)		I_{LIMx} = V_{CC}, GND to PHASEx		90	100	110	mV
Current-Limit Threshold (Positive, Adjustable)		V_{ILIMx} = 0.5V, GND to PHASEx		40	50	60	mV
		V_{ILIMx} = 1V, GND to PHASEx		90	100	110	
		V_{ILIMx} = 2V, GND to PHASEx		185	200	215	
Zero-Current Threshold		$\overline{SKIP}$ = GND, I_{LIMx} = V_{CC}, GND – PHASEx		--	3	--	mV
Soft-Start Ramp Time		Zero to full limit		--	1.5	---	ms
Operating Frequency	f_{OSC}	V_{TON} = 5V, $V_{\overline{SKIP}}$ = V_{CC}	5V SMPS	--	200	--	kHz
			3.3V SMPS	--	300	--	
		V_{TON} = GND $V_{\overline{SKIP}}$ = V_{CC}	5V SMPS	--	400	--	
			3.3V SMPS	--	500	--	
		$\overline{SKIP}$ = V_{REF}		25	--	--	
On-Time Pulse Width		V_{TON} = 5V	V_{OUT5} = 5.05V	1.854	2.060	2.265	μs
			V_{OUT3} = 3.33V	0.821	0.912	1.003	
		V_{TON} = GND	V_{OUT5} = 5.05V	0.876	1.030	1.184	
			V_{OUT3} = 3.33V	0.467	0.546	0.625	
Minimum Off-time	t_{OFF}			300	400	500	ns
Maximum Duty Cycle		V_{TON} = 5V	V_{OUT5} = 5.05V	--	92	--	%
			V_{OUT3} = 3.33V	--	88	--	
		V_{TON} = GND	V_{OUT5} = 5.05V	--	84	--	
			V_{OUT3} = 3.33V	--	80	--	
Internal Regulator And Reference Voltage							
LDO5 Output Voltage		ONx = GND, 7V < V_{IN} < 24V, 0 < I_{LDO5} < 100mA (Note 5)		4.90	5.0	5.10	V
LDO5 Short-Circuit Current		LDO5 = GND		--	350	--	mA
VCC Under-Voltage Lockout Fault Threshold		Falling edge of VCC, hysteresis = 1%		3.95	4.25	4.55	V
LDO5 Bootstrap Switch Threshold		Falling edge of VOUT5, rising edge at VOUT5 regulation point		4.52	4.65	4.78	V
LDO5 Bootstrap Switch Resistance		LDO5 to VOUT5, VOUT5 = 5V		--	1.4	3.2	Ω
LDO3 Output Voltage		ONx = GND, 7V < V_{IN} < 24V, 0 < I_{LDO3} < 100mA (Note 5)		3.28	3.35	3.42	V
LDO3 Short-Circuit Current		LDO3 = GND		--	175	--	mA
LDO3 Bootstrap Switch Threshold		Falling edge of VOUT3, rising edge at VOUT3 regulation point		2.82	2.93	3.04	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO3 Bootstrap Switch Resistance		LDO3 to VOUT3, VOUT3 = 3.2V	--	1.5	3.5	Ω
VREF Output Voltage	V_{REF}	No external load	1.98	2	2.02	V
VREF Load Regulation		$0 < I_{LOAD} < 50\mu A$	--	--	10	mV
VREF Sink Current		VREF in regulation	10	--	--	μA
VIN Standby Supply Current	$I_{Standby}$	V_{IN} = 7V to 24V, both SMPSs off, includes I_{EN}	--	150	250	μA
VIN Shutdown Supply Current	I_{SD}	V_{IN} = 7V to 24V	--	15	25	μA
Quiescent Power Consumption		Both SMPSs on, FBx = $\overline{SKIP}$ = GND, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V (Note 6)	--	3.5	5	mW
Fault Detection						
Over Voltage Trip Threshold		FBx with respect to nominal regulation point	8	11	14	%
Over Voltage Fault Propagation Delay		FBx delay with 50mV overdrive	--	20	--	μs
PGOOD Threshold		FBx with respect to nominal output, falling edge, typical hysteresis = 1%	−11.25	−8.75	−6.25	%
PGOOD Propagation Delay		Falling edge, 50mV overdrive	--	5	--	μs
PGOOD Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
PGOOD Leakage Current		High state, forced to 5.5V	--	--	1	μA
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Output Undervoltage Shutdown Threshold	ΔT_{SD}	FBx with respect to nominal output voltage	65	70	75	%
Output Undervoltage Shutdown Blanking Time		From ONx signal going high	10	22	35	ms
Inputs and Outputs						
Feedback Input Leakage Current		V_{FBx} = 2.2V	−200	40	200	nA
$\overline{PRO}$ Input Threshold Voltage		Low level	--	--	0.6	V
		High level	1.5	--	--	
$\overline{SKIP}$ Input Threshold Voltage		Low level	--	--	0.8	V
		Float level	1	--	2.3	
		High level	2.4	--	--	
T_{ON} Input Threshold Voltage		Low level	--	--	0.8	V
		High level	2.4	--	--	
ON3, ON5 Input Threshold Voltage		Clear fault level/SMPS off level	--	--	0.8	V
		Delay start level	1.3	--	2.3	
		SMPS on level	2.4	--	--	
Input Leakage Current		$V_{\overline{PRO}}$ or V_{TON} = 0 or 5V	−1	--	2	μA
		V_{ONx} = 0 or 5V	−2	--	2	

To be continued

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current		$V_{\overline{SKIP}}$ = 0 or 5V	–1	--	5	μA
		V_{EN} = 0 or 24V	–1	--	3	
		V_{ILIMx} = 0 or 2V	–0.2	--	0.2	
EN Input Trip level		Rising edge	1.2	1.6	2	V
		Falling edge	0.96	1	1.04	
UGATEx Driver Sink/Source Current		UGATEx forced to 2V	--	2	--	A
LGATEx Driver Source Current		LGATEx (source) forced to 2V	--	1.7	--	A
LGATEx Driver Sink Current		LGATEx (sink) forced to 2V	--	3.3	--	A
UGATEx Driver On-Resistance		(BOOTx to PHASEx) forced to 5V	--	1.5	4	Ω
LGATEx Driver On-Resistance		LGATEx, High State (pull up)	--	2.2	5.0	Ω
		LGATEx, Low State (pull down)	--	0.6	1.5	
VOUTx Discharge-Mode On-Resistance			--	17.7	40	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

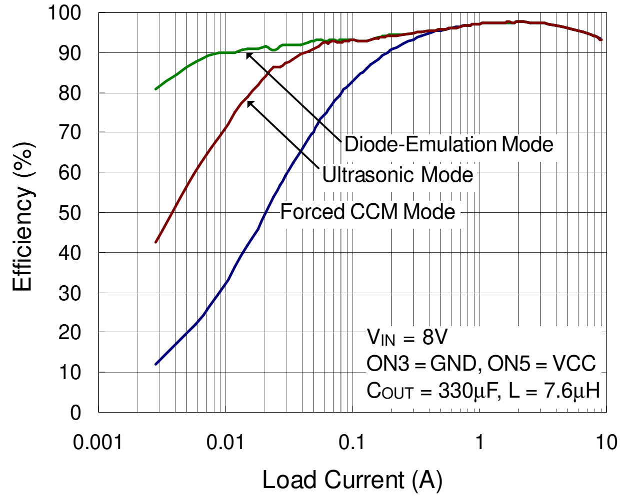
Note 5. $I_{LDO3} + I_{LDO5} < 150mA$

Note 6. $P_{VIN} + P_{VCC}$

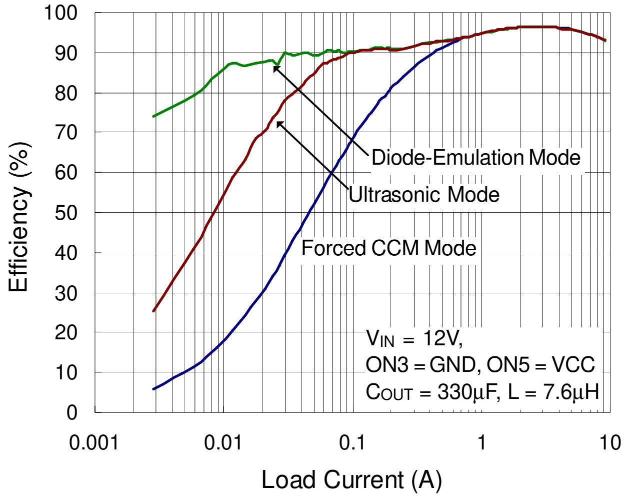
Typical Operating Characteristics

No load on LDO5, LDO3,VOUT5, VOUT3 and REF, T_{ON} = VCC, EN = VIN, T_A = 25°C, unless otherwise specified.

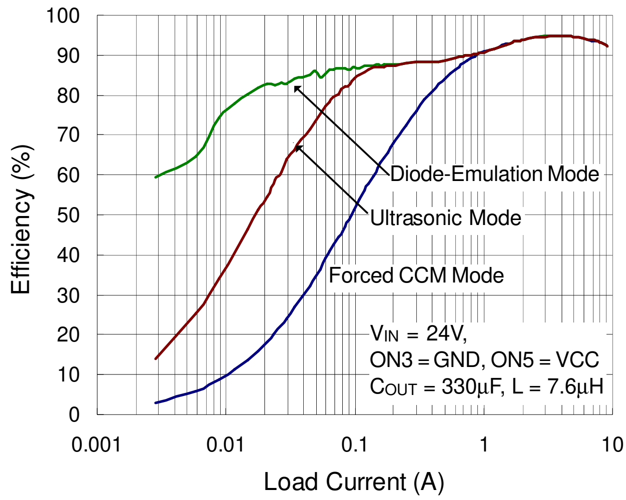
VOUT5 Efficiency vs. Load Current



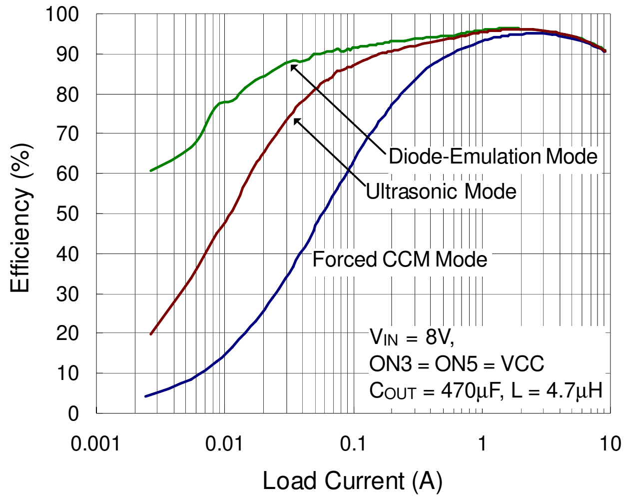
VOUT5 Efficiency vs. Load Current



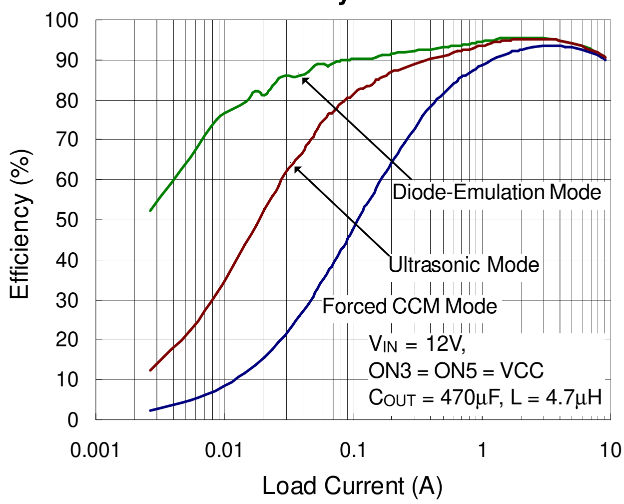
VOUT5 Efficiency vs. Load Current



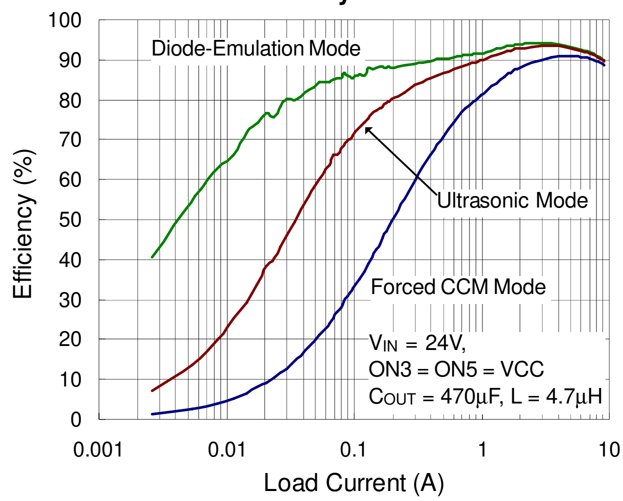
VOUT3 Efficiency vs. Load Current

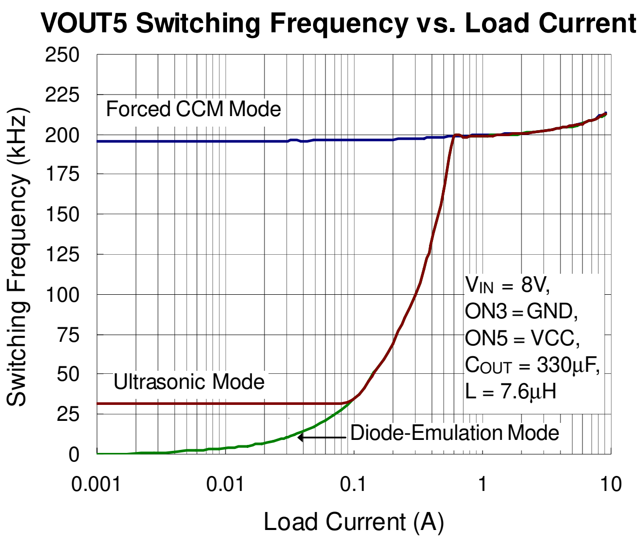


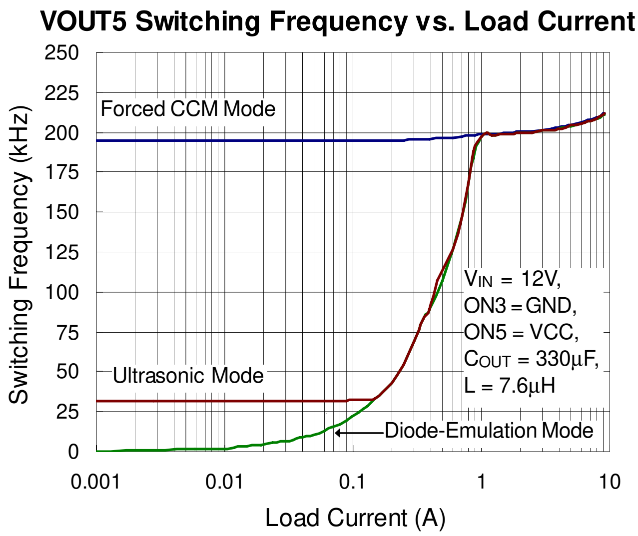
VOUT3 Efficiency vs. Load Current

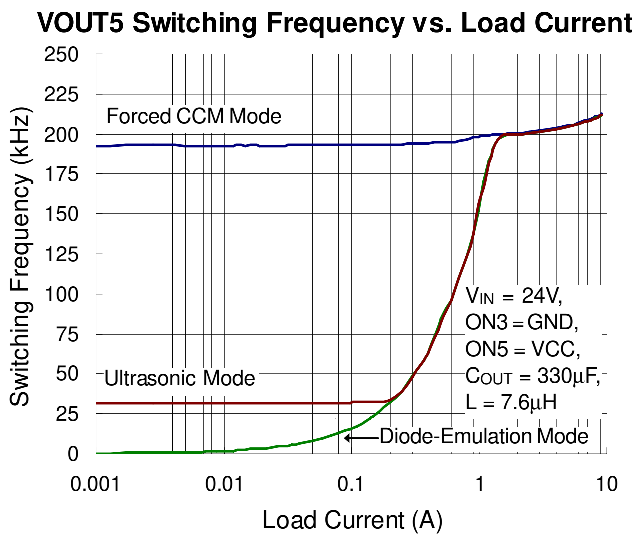


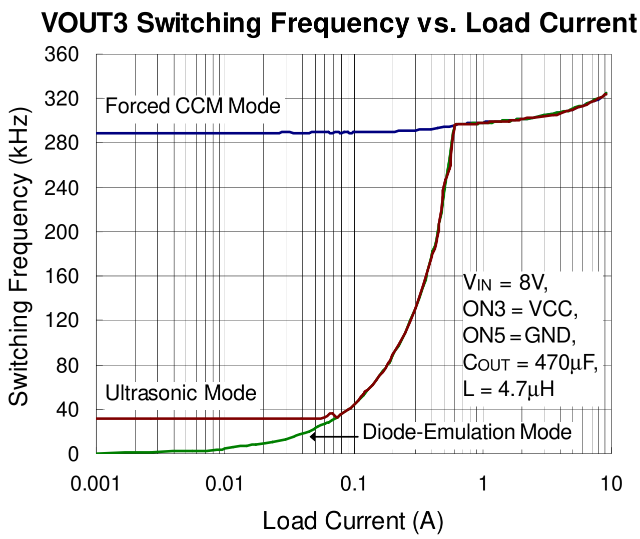
VOUT3 Efficiency vs. Load Current

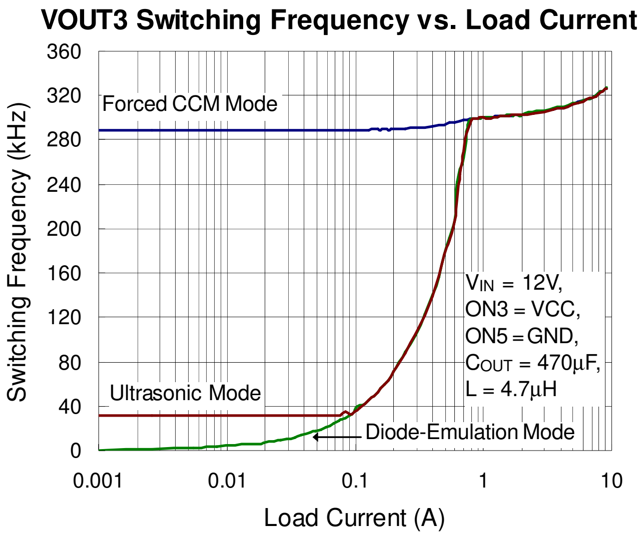


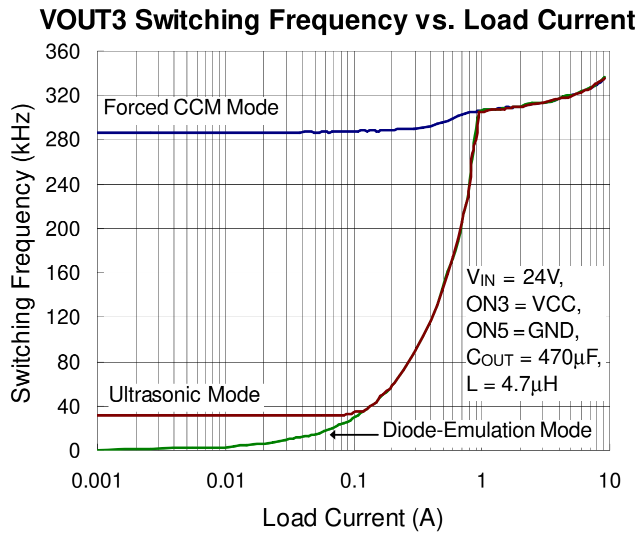

VOUT5 Switching Frequency vs. Load Current
Forced CCM Mode
Ultrasonic Mode
Diode-Emulation Mode
VIN = 8V,
ON3 = GND,
ON5 = VCC,
COUT = 330µF,
L = 7.6µH
Switching Frequency (kHz)
Load Current (A)


VOUT5 Switching Frequency vs. Load Current
Forced CCM Mode
Ultrasonic Mode
Diode-Emulation Mode
VIN = 12V,
ON3 = GND,
ON5 = VCC,
COUT = 330µF,
L = 7.6µH
Switching Frequency (kHz)
Load Current (A)

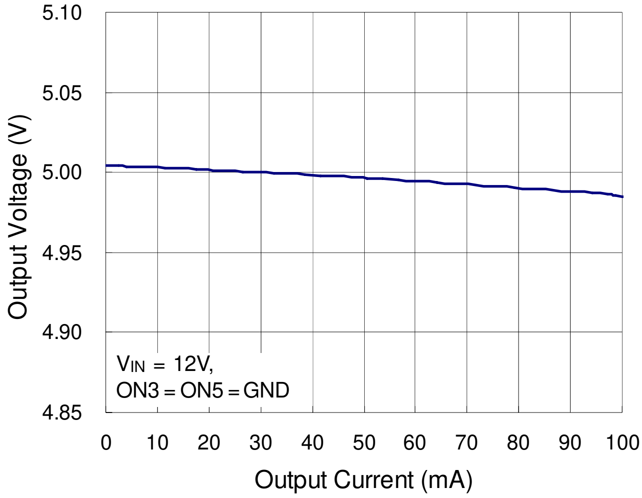

VOUT5 Switching Frequency vs. Load Current
Forced CCM Mode
Ultrasonic Mode
Diode-Emulation Mode
VIN = 24V,
ON3 = GND,
ON5 = VCC,
COUT = 330µF,
L = 7.6µH
Switching Frequency (kHz)
Load Current (A)


VOUT3 Switching Frequency vs. Load Current
Forced CCM Mode
Ultrasonic Mode
Diode-Emulation Mode
VIN = 8V,
ON3 = VCC,
ON5 = GND,
COUT = 470µF,
L = 4.7µH
Switching Frequency (kHz)
Load Current (A)

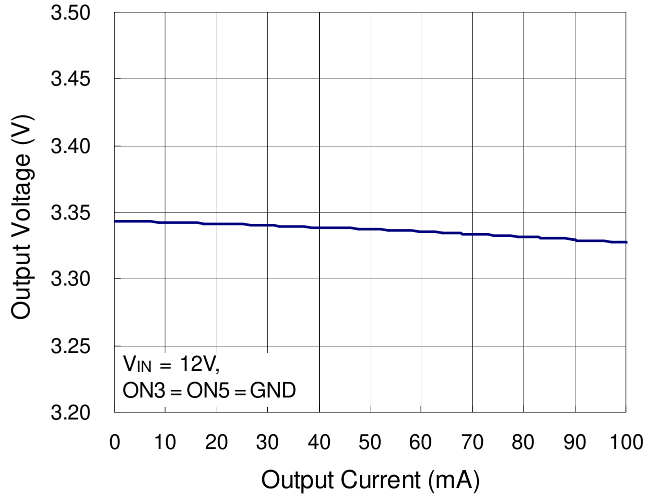

VOUT3 Switching Frequency vs. Load Current
Forced CCM Mode
Ultrasonic Mode
Diode-Emulation Mode
VIN = 12V,
ON3 = VCC,
ON5 = GND,
COUT = 470µF,
L = 4.7µH
Switching Frequency (kHz)
Load Current (A)


VOUT3 Switching Frequency vs. Load Current
Forced CCM Mode
Ultrasonic Mode
Diode-Emulation Mode
VIN = 24V,
ON3 = VCC,
ON5 = GND,
COUT = 470µF,
L = 4.7µH
Switching Frequency (kHz)
Load Current (A)

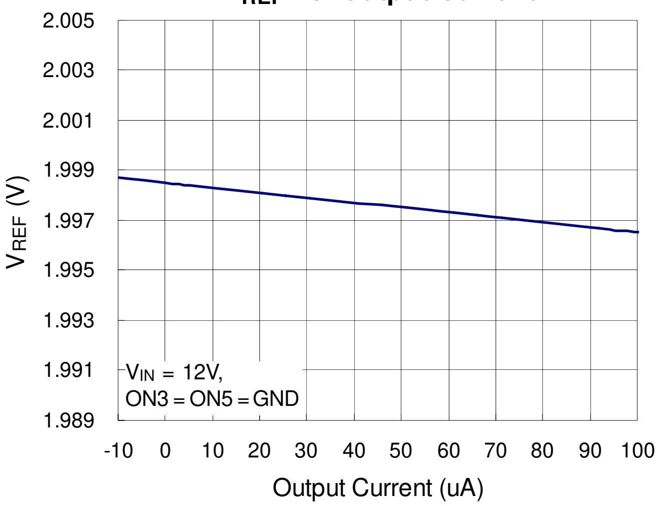
LDO5 Output Voltage vs. Output Current



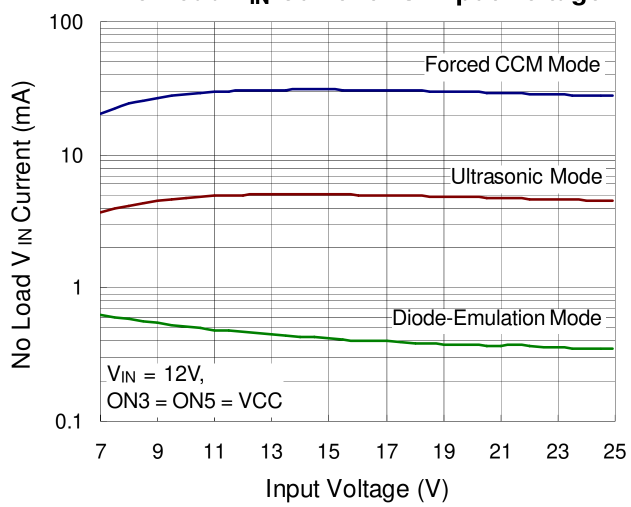
LDO3 Output Voltage vs. Output Current



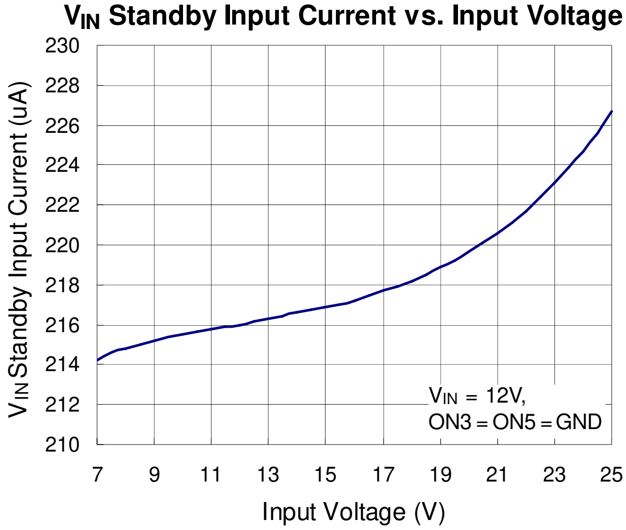
V_{REF} vs. Output Current



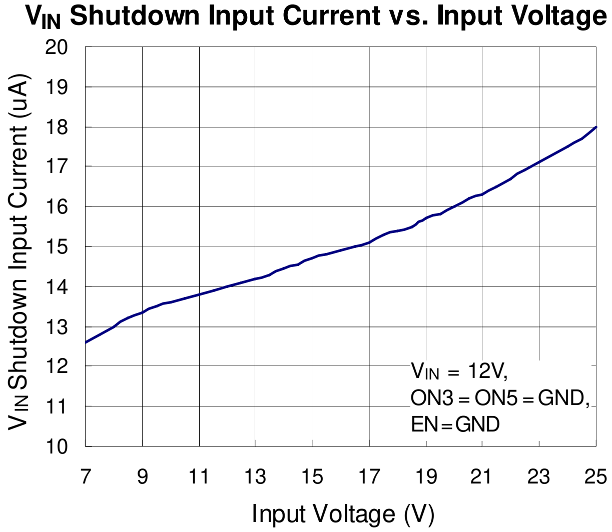
No Load V_{IN} Current vs. Input Voltage



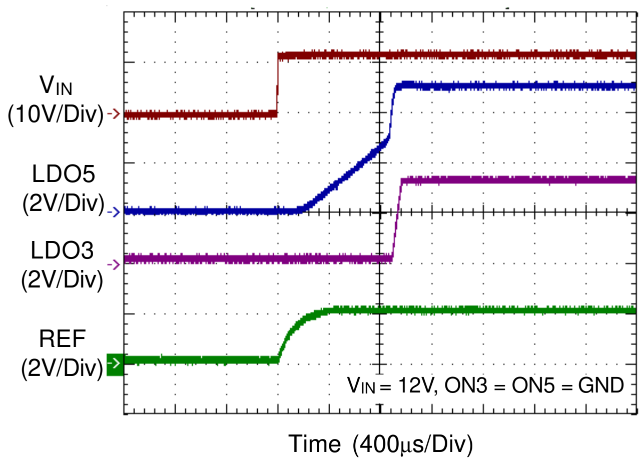
V_{IN} Standby Input Current vs. Input Voltage



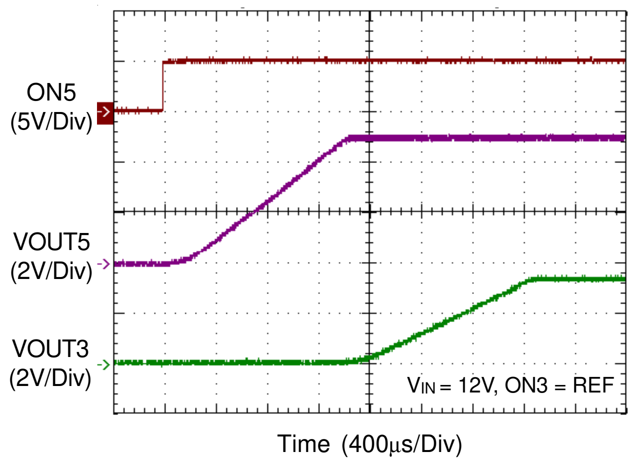
V_{IN} Shutdown Input Current vs. Input Voltage



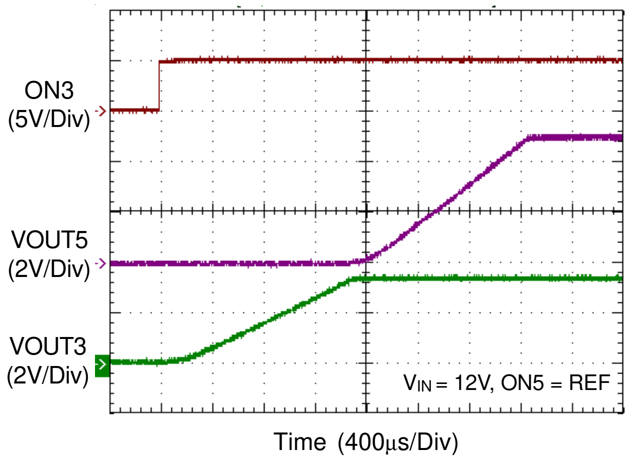
Power Up



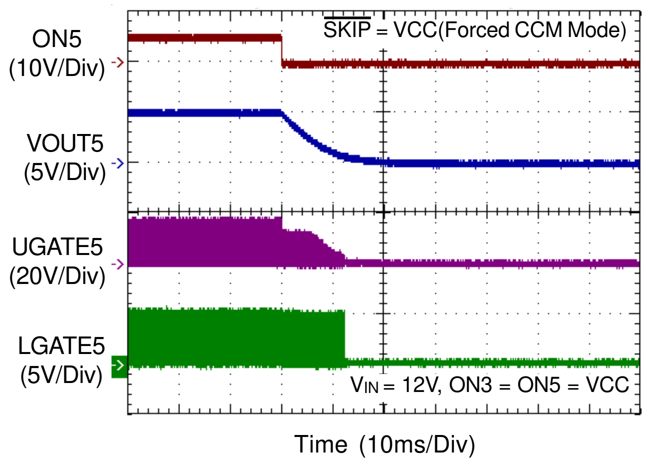
Delayed Start



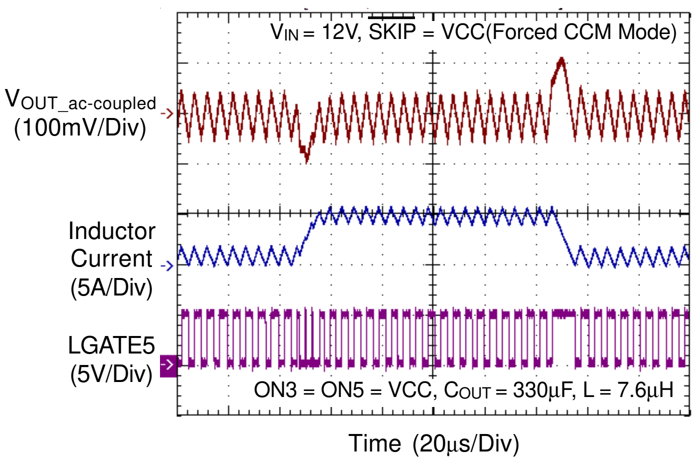
Delayed Start



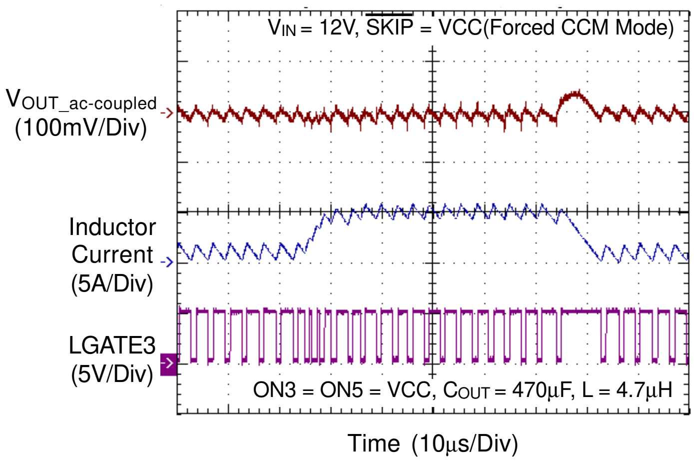
Shutdown Response

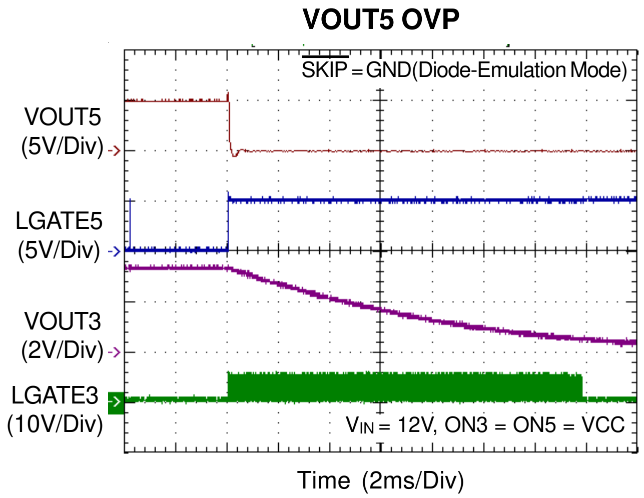


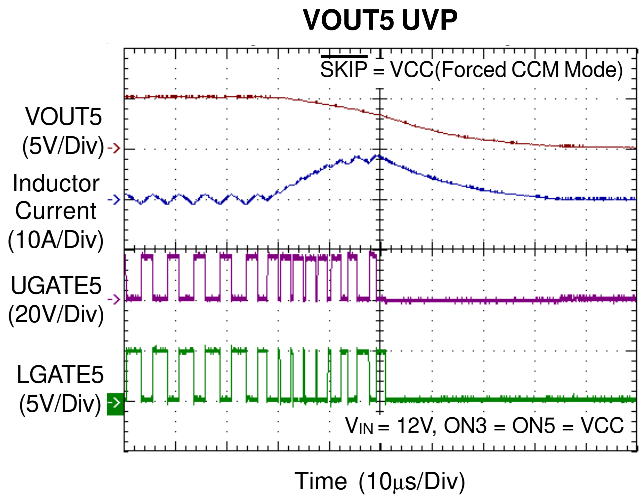
VOUT5 Load Transient Response

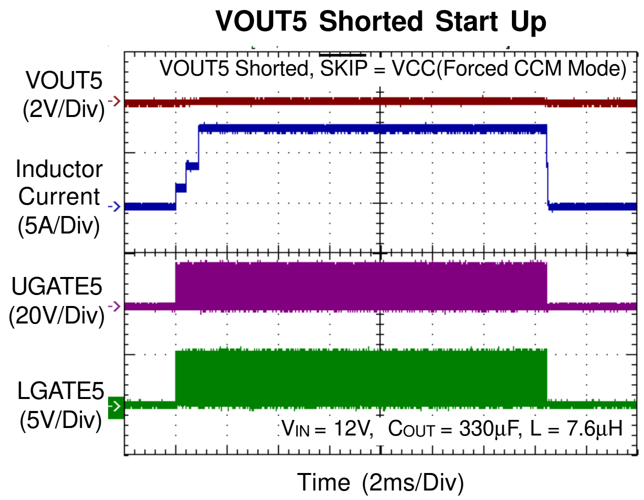


VOUT3 Load Transient Response




VOUT5 OVP
SKIP = GND(Diode-Emulation Mode)
VOUT5 (5V/Div)
LGATE5 (5V/Div)
VOUT3 (2V/Div)
LGATE3 (10V/Div)
VIN = 12V, ON3 = ON5 = VCC
Time (2ms/Div)


VOUT5 UVP
SKIP = VCC(Forced CCM Mode)
VOUT5 (5V/Div)
Inductor Current (10A/Div)
UGATE5 (20V/Div)
LGATE5 (5V/Div)
VIN = 12V, ON3 = ON5 = VCC
Time (10μs/Div)


VOUT5 Shorted Start Up
VOUT5 Shorted, SKIP = VCC(Forced CCM Mode)
VOUT5 (2V/Div)
Inductor Current (5A/Div)
UGATE5 (20V/Div)
LGATE5 (5V/Div)
VIN = 12V, COUT = 330μF, L = 7.6μH
Time (2ms/Div)

Application Information

The RT8203 is a dual, Mach Response^{TM} DRV^{TM} dual ramp valley mode synchronous buck controller. The controller is designed for low voltage power supplies for notebook computers. Richtek's Mach Response^{TM} technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant off-time PWM schemes. The DRV^{TM} mode PWM modulator is specifically designed to have better noise immunity for such a dual output application. The RT8203 includes 5V (LDO5) and 3.3V (LDO3) linear regulators. LDO5 linear regulator can step down the battery voltage to supply both internal circuitry and gate drivers. The synchronous-switch gate drivers are directly powered from LDO5. When VOUT5 voltage is above 4.65V, an automatic circuit turns off the LDO5 linear regulator and powers the device form VOUT5.

PWM Operation

The Mach Response^{TM} DRV^{TM} mode controller relies on the output filter capacitor's effective series resistance (ESR) to act as a current sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the RT8203's function block diagram, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range. Another one shot sets a minimum off-time (400ns typ). The on-time one shot is triggered if the error comparator is high, the low side switch current is below the current limit threshold, and the minimum off-time one shot has timed out.

PWM Frequency and On-Time Control

The Mach Response^{TM} control architecture runs with pseudo-constant frequency by feed forwarding the input and output voltage into the on-time one shot timer. The high side switch on-time is inversely proportional to the input voltage as measured by the V_{IN}, and proportional to the output voltage. There are two benefits of a constant switching frequency. The first is the frequency can be selected to avoid noise sensitive regions such as the 455kHz IF band. The second is the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The frequency for 5V SMPS is set at 100kHz higher than the frequency for 3V SMPS. This is done to prevent audio-frequency "beating" between the two sides, which switch asynchronously for each side. The on-time is given by :

$$\text{On-Time} = K\ (V_{OUT} / V_{IN})$$

where K is set by the TON pin-strap connection (Table 1). The on-times guaranteed in the Electrical Characteristics tables are influenced by switching delays in the external high-side power MOSFET. Two external factors that influence switching frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead time effect increases the effective on-time, reducing the switching frequency as one or both dead times. It occurs only in Forced CCM Mode ($\overline{SKIP}$ = high) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor' s EMF causes PHASEx to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time. For loads above the critical conduction point, the actual switching frequency is :

$$f = \frac{(V_{OUT} + V_{DROP1})}{t_{ON} \times (V_{IN} + V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path; and t_{ON} is the on-time calculated by the RT8203.

Operation Mode Selection ($\overline{SKIP}$)

The RT8203 supports three operation modes: Diode-Emulation Mode, Ultrasonic Mode, and Forced-CCM Mode.

Diode-Emulation Mode ($\overline{SKIP}$ = GND)

In Diode-Emulation mode, RT8203 automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of V_{OUT} ripple or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor free-wheeling current reach negative. As the load current further decreases, it takes longer and longer to discharge the output capacitor to the level that requires the next “ON ” cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation can be calculated as follows (Figure 3) :

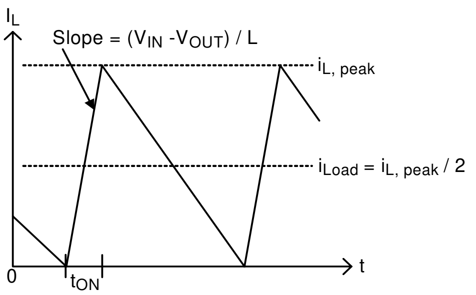


Figure 3. Boundary Condition of CCM/DCM

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where Ton is the On-time.

The switching waveforms may appear noisy and asynchronous when light loading causes Diode-Emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input-voltage levels).

Ultrasonic Mode ($\overline{SKIP}$ = Float)

Leaving $\overline{SKIP}$ unconnected or connecting $\overline{SKIP}$ to VREF activates a unique Diode-Emulation mode with a minimum switching frequency of 25kHz. This ultrasonic mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low-side switch gate-driver signal is OR with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the ultrasonic controller pulls LGATEx high, turning on the low side MOSFET to induce a negative inductor current. After the output voltage across the VREF, the controller turns off the low side MOSFET (LGATEx pulled low) and triggers a constant on-time (UGATEx driven high). When the on-time has expired, the controller re-enables the low-side MOSFET until the controller detects that the inductor current drops below the zero-crossing threshold.

Forced-CCM Mode ($\overline{SKIP}$ = VCC)

The low noise, forced-CCM mode ($\overline{SKIP}$ = VCC) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low side gate-driver waveform to become the complement of the high side gate-driver waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop strives to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost: The no-load battery current can be 10mA to 40mA, depending on the external MOSFETs.

Reference and linear Regulators (VREF, LDOx)

The 2V reference (VREF) is accurate within ± 1% over temperature, making VREF useful as a precision system reference. Bypass VREF to GND with 0.22μF(min) capacitor. VREF can supply up to 100uA for external loads. Loading VREF reduces the VOUTx output voltage slightly because of the reference load-regulation error.

LDO5 regulator supplies total of 100mA for internal and external loads, including MOSFET gate driver and PWM controller. LDO3 regulator supplies up to 100mA for external loads. Bypass LDO5 and LDO3 with a minimum 4.7uF load; use an additional 1μF per 5mA of internal and external load.

When the 5V main output voltage is above the LDO5 switchover threshold, an internal 1.4Ω N-MOSFET switch connects VOUT5 to LDO5 while simultaneously shutting down the LDO5 linear regulator. Similarly, when the 3.3V main output voltage is above the LDO3 switchover threshold, an internal 1.5Ω N-MOSFET switch connects VOUT3 to LDO3 while simultaneously shutting down the LDO3 linear regulator. It can decrease the power dissipation from the same battery, because the converted efficiency of SMPS is better than the converted efficiency of linear regulator.

Current Limit Setting (ILIMx)

The RT8203 has cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery and output voltage.

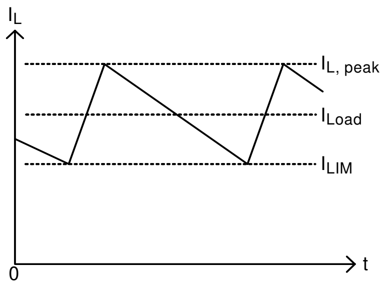


Figure 4. "Valley" Current Limit

The RT8203 uses the on-resistance of the synchronous rectifier as the current sense element. Use the worse-case maximum value for $R_{DS(ON)}$ from the MOSFET data sheet, and add a margin of 0.5%/°C for the rise in $R_{DS(ON)}$ with temperature.

The current limit threshold is adjusted with an external voltage divider at ILIMx. The current limit threshold adjustment range is from 50 mV to 200mV. In the adjustable mode, the current limit threshold voltage is precisely 1/10 the voltage seen at ILIMx. The threshold defaults to 100mV when ILIMx is connected to VCC. The logic threshold for switchover to the 100mV default value is approximately VCC - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal at PHASEx and GND. Mount or place the IC close to the low side MOSFET.

MOSFET Gate Driver (UGATEx, LGATEx)

The high side driver is designed to drive high current, low $R_{DS(on)}$ NMOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from LDO5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5 V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOTx and PHASEx pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on.

The low side driver is designed to drive high current low $R_{DS(on)}$ NMOSFET(s). The internal pull-down transistor that drives LGATEx low is robust, with a 0.6Ω typical on-resistance. A 5V bias voltage is delivered from LDO5 supply.

For high current applications, some combinations of high and low side MOSFETs may cause excessive gate-drain coupling, which can lead to efficiency-killing and EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 5).

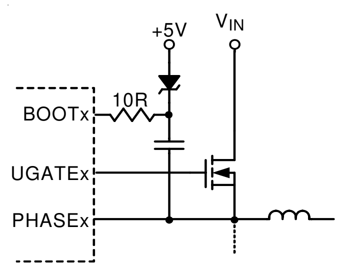


Figure 5. Reducing the UGATEx Rise Time

Soft-Start

A build-in soft-start is used to prevent surge current from power supply input after ONx is enabled. It clamps the ramping of internal reference voltage which is compared with the FBx signal. The typical soft-start duration is 1.5ms period. Furthermore, the maximum allowed current limit is segmented in 3 steps : 20%, 50%, and 100% during the 1.5ms period. The current limit steps can minimize the V_{OUT} folded-back in the soft-start duration when RT8203 is determining fixed or adjustable output.

POR and UVLO

Power On Reset (POR) occurs when V_{IN} rises above approximately 3.5V, resetting the fault latch and preparing the PWM for operation. Below 4.25V(min), the VCC undervoltage lockout (UVLO) circuitry inhibits switching by keeping UGATEx and LGATEx low.

Power Good Output (PGOOD)

The PGOOD is an open-drain type output. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when both outputs voltage above than 91.25% of nominal regulation point. The PGOOD goes low if either output turns of or is 8.75% below its nominal regulation point.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. When over voltage protection is enabled, if the output exceeds the over voltage threshold, over voltage fault protection is triggered and the LGATEx low side gate drivers are forced high. This activates the low side MOSFET switch, which rapidly discharges the output capacitor and reduces the input voltage.

Note that LGATEx latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp. Connect $\overline{\text{PRO}}$ to GND to enable the default over voltage threshold level, which is 11% above the set voltage.

If the over voltage condition is caused by a short in high side switch, turning the low side MOSFET on 100% creates an electrical short between the battery and GND, blowing the fuse and disconnecting the battery from the output.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. When under voltage protection is enabled ($\overline{\text{PRO}}$ = GND), if the output is less than 70% of the error-amplifier trip voltage, under voltage protection is triggered, then both UGATEx and LGATEx gate drivers are forced low. In order to remove the residual charge on the output capacitor during the UV period, if PHASEx is greater than 1V, the LGATEx gate driver is forced high until PHASEx lower than 1V. Connect UVP to GND to disable under voltage protection.

Thermal Protection

The RT8203 have thermal shutdown to prevent the overheat damage. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitry shuts down during thermal shutdown. The RT8203 will trigger thermal shutdown if LDOx is not supplied from VOUTx, while input voltage on VIN and drawing current form LDOx are too high. Even if LDOx is supplied from VOUTx, overloading the LDOx causes large power dissipation on automatic switches, which may result in thermal shutdown.

Discharge Mode

When $\overline{\text{PRO}}$ is low and a transition to standby or shutdown mode occurs, or the output under voltage fault latch is set, the outputs discharge mode is triggered. During discharge mode, there are two paths to discharge the outputs capacitor residual charge during discharge mode. The first is output capacitor discharge to GND through an internal 17Ω switch. The second is output capacitor discharged by forcing the low-side MOSFET turn on/off until PHASEx voltage decrease under 1V.

Shutdown Mode

Drive EN below the precise EN input falling-edge trip level to place the RT8203 in their low-power shutdown state. When shutdown mode activates, the reference turns off, making the threshold to exit shutdown inaccurate. For automatic shutdown and startup, connect EN to VIN. If $\overline{\text{PRO}}$ is low, both SMPS outputs will enter discharge mode before entering true shutdown. The accurate 1V falling-edge threshold on EN can be used to detect a specific analog voltage level and shutdown the device. Once in shutdown, the 1.6V rising-edge threshold activates, providing sufficient hysteresis for most application.

Power-Up Sequencing and On/Off Controls (ONx)

ON3 and ON5 control SMPS power-up sequencing. When RT8203 applies in the single channel mode, ON3 or ON5 enables the respective outputs when ONx voltage rising above 2.4V, and disables the respective outputs when ONx voltage falling below 1.3V.

Connecting one of ONx to VCC and the other one connecting to V_{REF} can force the latter one output starts after the former one regulates.

If both of ONx forced connecting to V_{REF}, both outputs always wait the other one regulating and no one will regulate.

Output Voltage Setting (FBx)

Connect FBx directly to GND to enable the fixed, preset SMPS output voltages (3.3V and 5V). Connect a resistor voltage-divider at FBx between VOUTx and GND to adjust the respective output voltage between 2V and 5.5V (Figure 6). Choose R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUTx} = V_{FBx} \times \left[1+\left(\frac{R1}{R2}\right)\right]$$

where V_{FBx} is 2.0V (typ.).

LDO5 connects to VOUT5 through an internal switch only when VOUT5 above the LDO5 automatic switch threshold (4.65V). LDO3 connects to VOUT3 through an internal switch only when VOUT3 is above the LDO3 automatic switch threshold (2.93V). This is the most effective way when the fixed output voltages are used. Once LDOx is supplied from VOUTx, the internal linear regulator turns off. This reduces internal power dissipation and improves efficiency when LDOx is powered with a high input voltage.

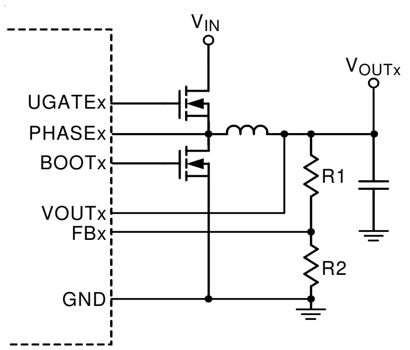


Figure 6. Setting VOUTx with a Resistor-Divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + [(L_{IR} / 2) \times I_{LOAD(MAX)}]$$

This inductor ripple current also impacts transient-response performance, especially at low VIN -VOUTx differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the output transient. The (V_{SAG}) also features a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (K\frac{V_{OUTx}}{V_{IN}} + T_{OFF(MIN)})}{2 \times C_{OUT} \times V_{OUTx}\left[K\left(\frac{V_{IN} - V_{OUTx}}{V_{IN}}\right) - T_{OFF(MIN)}\right]}$$

Where the minimum off-time ($T_{OFF(MIN)}$) = 400ns (typical) and K is from Table 1.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. Moreover, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \le \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak-to-peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

For low input-to-output voltage differentials (VIN / VOUTx < 2), additional output capacitance is required to maintain stability and good efficiency in ultrasonic mode.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} = \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability

The output capacitor stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high-value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VOUTx or the FBx divider close to the inductor.

Unstable operation manifests itself in two related and distinctly different ways : double-pulsing and feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or overshoot.

Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout using the RT8203.

- Connect RC low pass filter from LDO5 to VCC, 1-mF and 10Ω are recommended. Place the filter capacitor close to the IC, within 12mm(0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance. Use 0.65-mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOUTx, FBx, GND, ONx, PGOOD, ILIMx, VCC, and TON should be placed away from high-voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Gather ground terminal of VIN capacitor(s), VOUTx capacitor(s), and source of low side MOSFETs as close as possible. PCB trace defined as PHASEx node, which connects to source of high side MOSFET, drain of low side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Table 1. TON Setting and PWM Frequency Table

T_{ON}	VOUT5 K-Factor (μs)	VOUT5 Frequency (kHz)	VOUT3 K-Factor (μs)	VOUT3 Frequency (kHz)	Approximate K-Factor Error (%)
VCC	4.90	200	3.29	300	± 10
GND	2.45	400	1.97	500	± 10

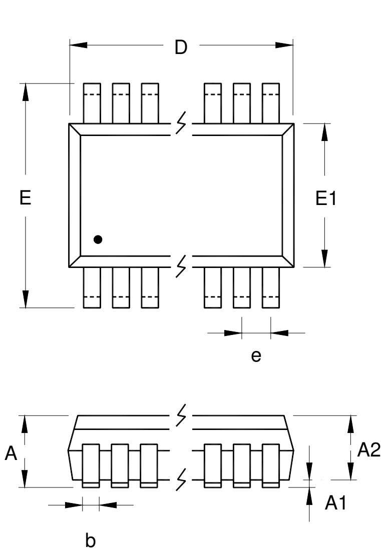
Table 2. Operation Mode Truth Table

Mode	Condition	Comment
Power-UP	LDOx < UVLO threshold	Transitions to discharge mode after a VIN POR and after VREF becomes valid. LDO5, LDO3, and VREF remain active.
RUN	EN = High, ON3 or ON5 enabled	Normal Operation.
Over Voltage Protection	Either output > 111% of nominal level, $\overline{PRO}$ = Low	LGATEx is forced high. LDO3, LDO5 active. Exited by VIN POR or by toggling EN, ON3, or ON5
Under Voltage Protection	Either output < 70% of nominal level after 22ms time-out expires and output is enabled, $\overline{PRO}$ = Low	If $\overline{PRO}$ is low, both UGATEx and LGATEx are forced low until enter discharge mode terminates. LDO3, LDO5 active. Exited by VIN POR or by toggling EN, ON3, or ON5.
Discharge	$\overline{PRO}$ is low and either SMPS output is still high in either standby mode or shutdown mode	During discharge mode, there are two paths to discharge the outputs capacitor residual charge during discharge mode. The first is output capacitor discharge to GND through an internal 17Ω switch. The second is output capacitor discharged by forcing the low-side MOSFET turn on/off until PHASEx voltage decrease under 1V.
Standby	ONx < startup threshold, EN = High.	LGATEx stays low if $\overline{PRO}$ is low. LDO3, LDO5 active.
Shutdown	EN = Low	All circuitry off.
Thermal Shutdown	T_J > 150°C	All circuitry off. Exit by VIN POR or by toggling EN, ON3, or ON5.

Table 3 Power-Up Sequencing

EN (V)	VON5 (V)	VON3 (V)	LDO5	LDO3	5V SMPS	3V SMPS
Low	X	X	Off	Off	Off	Off
" >2.4V " => High	Low	Low	On (after REF powers up)	On (after LDO5 powers up)	Off	Off
" >2.4V " => High	Low	VREF	On (after VREF powers up)	On (after LDO5 powers up)	Off	Off
" >2.4V " => High	Low	High	On (after VREF powers up)	On (after LDO5 powers up)	Off	On
" >2.4V " => High	VREF	Low	On (after VREF powers up)	On (after LDO5 powers up)	Off	Off
" >2.4V " => High	VREF	VREF	On (after VREF powers up)	On (after LDO5 powers up)	Off	Off
" >2.4V " => High	VREF	High	On (after VREF powers up)	On (after LDO5 powers up)	On (after 3V SMPS on)	On
" >2.4V " => High	High	LOW	On (after VREF powers up)	On (after LDO5 powers up)	On	Off
" >2.4V " => High	High	VREF	On (after VREF powers up)	On (after LDO5 powers up)	ON	On (after 5V SMPS on)
" >2.4V " => High	High	High	On (after VREF powers up)	On (after LDO5 powers up)	On	On

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.346	1.753	0.053	0.069
A1	0.100	0.254	0.004	0.010
A2	1.499		0.059	
b	0.203	0.360	0.008	0.014
C	0.178	0.274	0.007	0.011
D	9.800	10.010	0.386	0.394
e	0.635		0.025	
E	5.790	6.200	0.228	0.244
E1	3.810	3.990	0.150	0.157
L	0.380	1.270	0.015	0.050

28-Lead SSOP Plastic Package

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