



PUMD48-Q

NPN/PNP resistor-equipped double transistor; R1 = 47 k Ω , R2 = 47 k Ω and R1 = 2.2 k Ω , R2 = 47 k Ω

25 October 2021

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

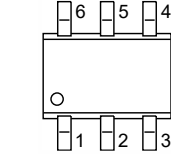
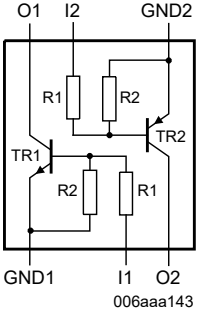
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
Transistor TR1 (NPN)						
R1	bias resistor 1	[1]	33	47	61	k Ω
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	
Transistor TR2 (PNP)						
R1	bias resistor 1	[1]	1.54	2.2	2.86	k Ω
R2/R1	bias resistor ratio	[1]	17	21	26	

[1] See section "Test information" for resistor calculation and test conditions.

NPN/PNP resistor-equipped double transistor; R1 = 47 k Ω , R2 = 47 k Ω and R1 = 2.2 k Ω , R2 = 47 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>TSSOP6 (SOT363)</p>	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD48-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD48-Q	4%8

[1] % = placeholder for manufacturing site code

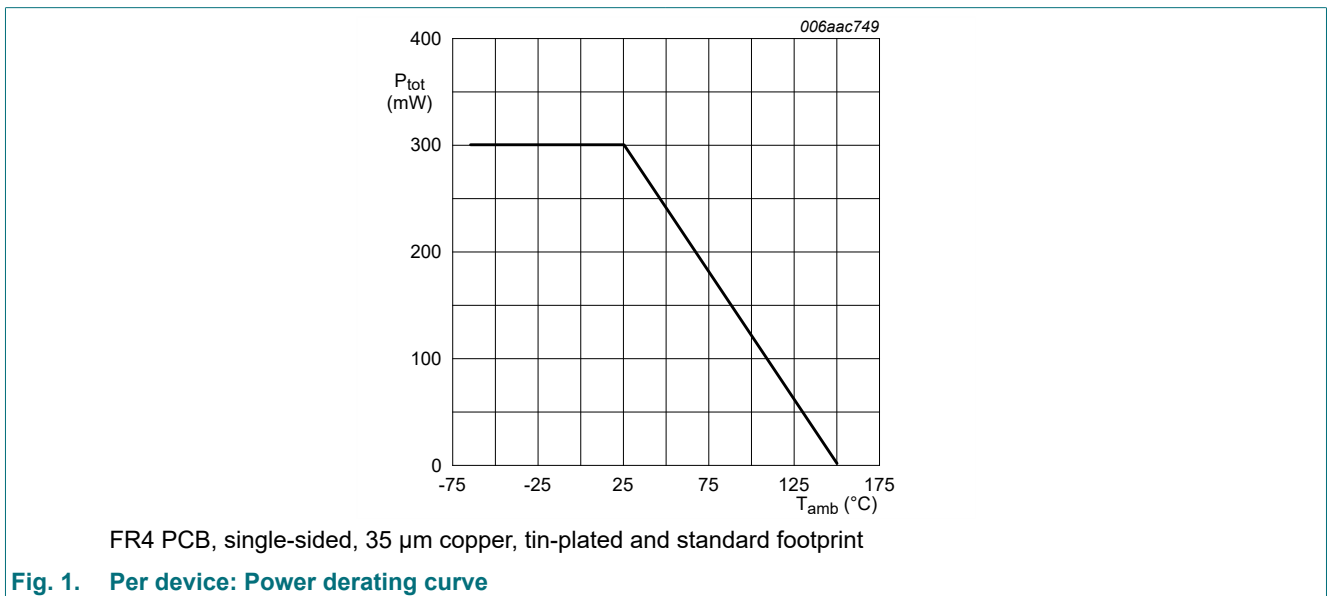
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector TR1 (NPN)		-	10	V
		open collector TR2 (PNP)		-	-5	V
V _I	input voltage	positive (input voltage TR1)		-	40	V
		negative (input voltage TR1)		-	-10	V
		positive (input voltage TR2)		-	5	V
		negative (input voltage TR2)		-	-12	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

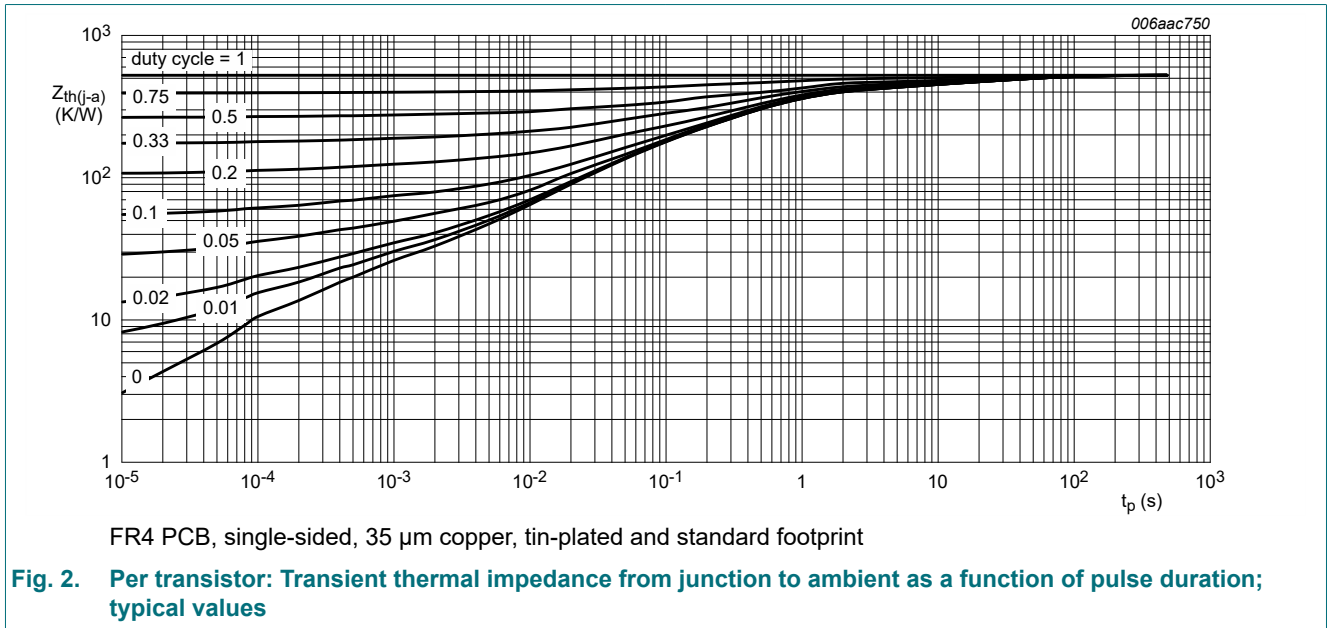


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



NPN/PNP resistor-equipped double transistor; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

10. Characteristics

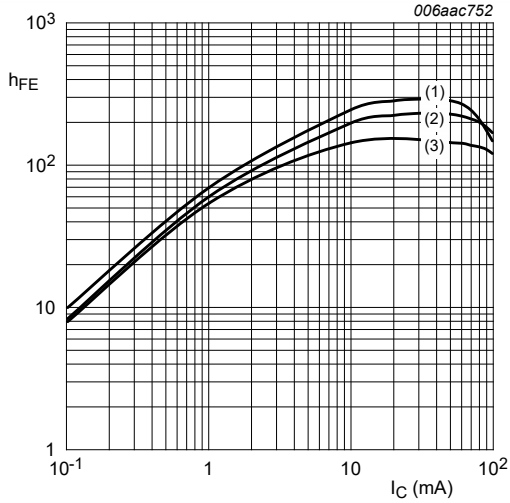
Table 7. Characteristics
 $T_{amb} = 25\text{ °C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor; for the PNP transistor with negative polarity							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\ \mu\text{A}$; $I_E = 0\ \text{A}$	50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\ \text{mA}$; $I_B = 0\ \text{A}$	50	-	-	V	
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\ \text{V}$; $I_E = 0\ \text{A}$	-	-	100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\ \text{V}$; $I_B = 0\ \text{A}$	-	-	1	μA	
		$V_{CE} = 30\ \text{V}$; $I_B = 0\ \text{A}$; $T_J = 150\text{ °C}$	-	-	5	μA	
Transistor TR1 (NPN)							
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\ \text{V}$; $I_C = 0\ \text{A}$	-	-	90	μA	
h_{FE}	DC current gain	$V_{CE} = 5\ \text{V}$; $I_C = 5\ \text{mA}$	80	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\ \text{mA}$; $I_B = 0.5\ \text{mA}$	-	-	100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\ \text{V}$; $I_C = 100\ \mu\text{A}$	-	1.2	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\ \text{V}$; $I_C = 2\ \text{mA}$	3	1.6	-	V	
R1	bias resistor 1		[1]	33	47	61	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\ \text{V}$; $I_E = 0\ \text{A}$; $i_e = 0\ \text{A}$; $f = 1\ \text{MHz}$	-	-	2.5	pF	
f_T	transition frequency	$V_{CE} = 5\ \text{V}$; $I_C = 10\ \text{mA}$; $f = 100\ \text{MHz}$	[2]	-	230	-	MHz
Transistor TR2 (PNP)							
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\ \text{V}$; $I_C = 0\ \text{A}$	-	-	-180	μA	
h_{FE}	DC current gain	$V_{CE} = -5\ \text{V}$; $I_C = -10\ \text{mA}$	100	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -5\ \text{mA}$; $I_B = -0.25\ \text{mA}$	-	-	-100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\ \text{V}$; $I_C = -100\ \mu\text{A}$	-	-0.6	-0.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\ \text{V}$; $I_C = -5\ \text{mA}$	-1.1	-0.75	-	V	
R1	bias resistor 1		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	
C_c	collector capacitance	$V_{CB} = -10\ \text{V}$; $I_E = 0\ \text{A}$; $i_e = 0\ \text{A}$; $f = 1\ \text{MHz}$	-	-	3	pF	
f_T	transition frequency	$V_{CE} = -5\ \text{V}$; $I_C = -10\ \text{mA}$; $f = 100\ \text{MHz}$	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

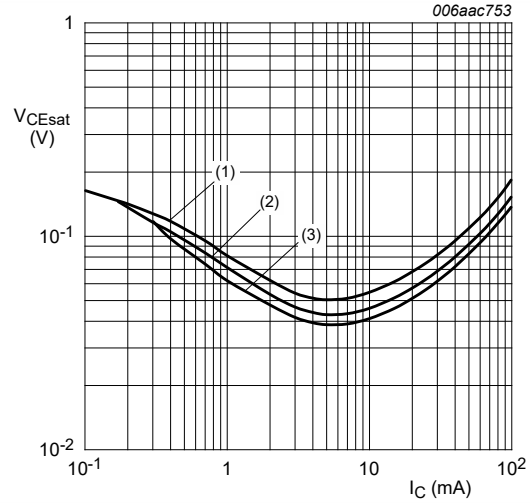
[2] Characteristics of built-in transistor

NPN/PNP resistor-equipped double transistor; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ



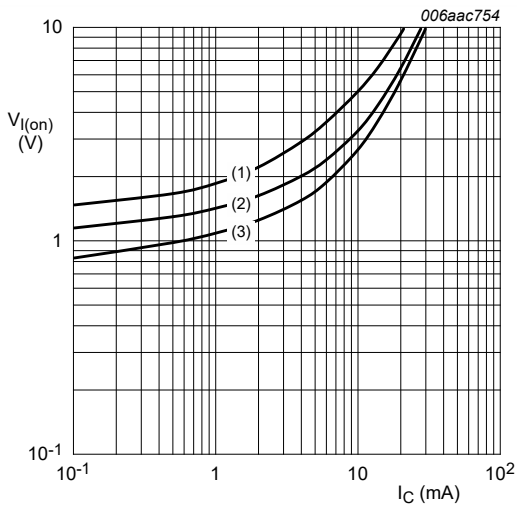
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values



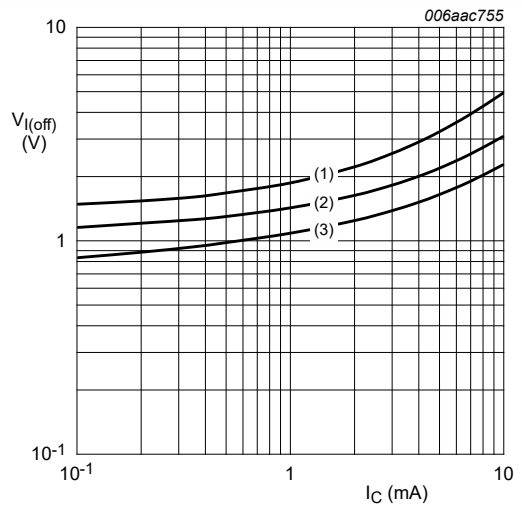
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

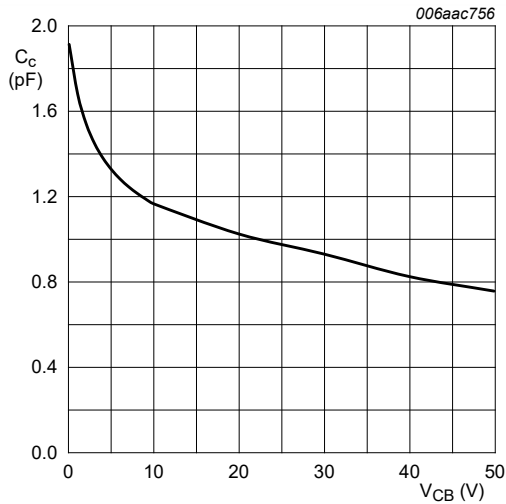
Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values



$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

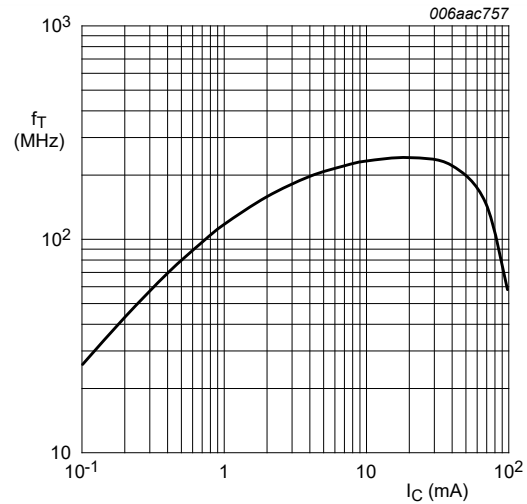
Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

NPN/PNP resistor-equipped double transistor; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ



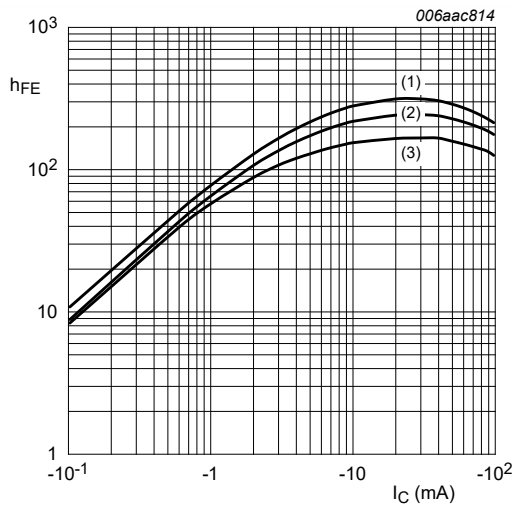
f = 1 MHz
T_{amb} = 25 °C

Fig. 7. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



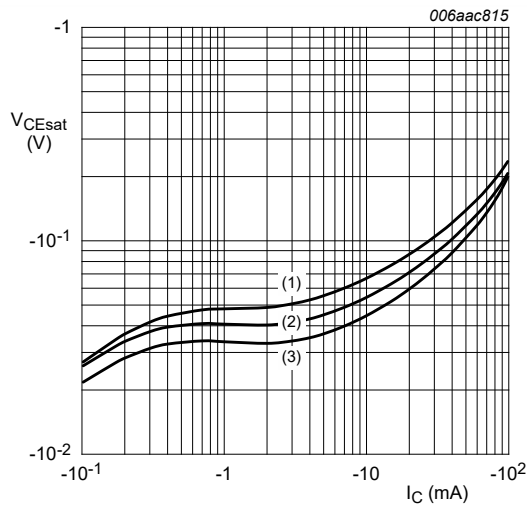
f = 100 MHz
T_{amb} = 25 °C
V_{CE} = 5 V

Fig. 8. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

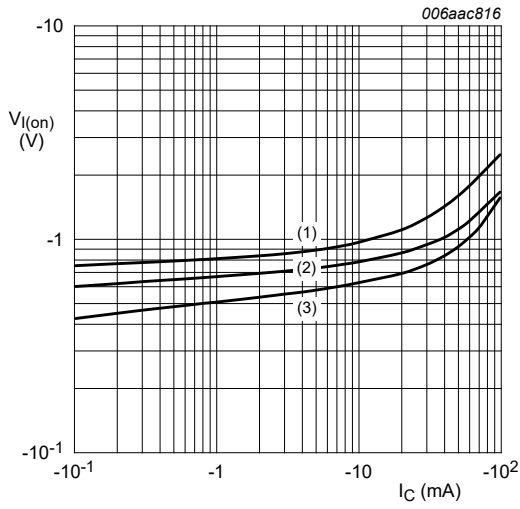
Fig. 9. TR2 (PNP): DC current gain as a function of collector current; typical values



I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

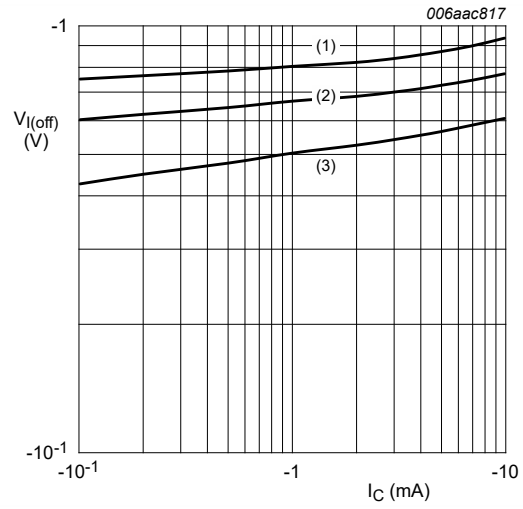
Fig. 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

NPN/PNP resistor-equipped double transistor; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ



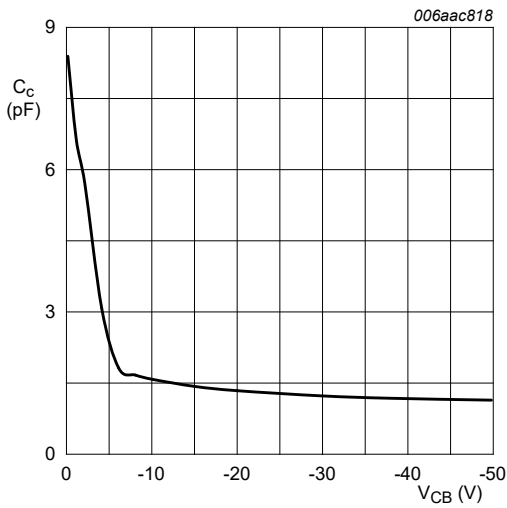
$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values



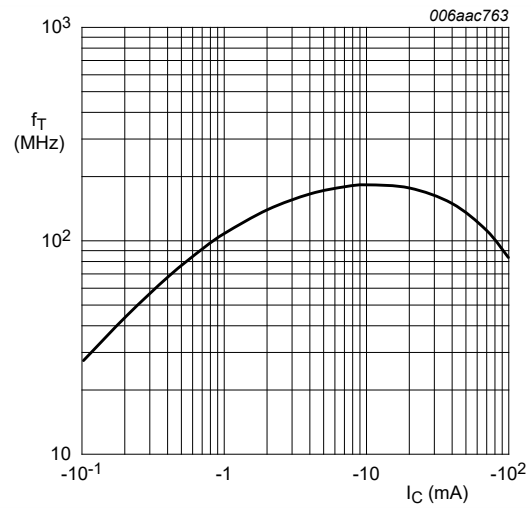
$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 13. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



$f = 100 \text{ MHz}$
 $T_{amb} = 25 \text{ }^\circ\text{C}$
 $V_{CE} = -5 \text{ V}$

Fig. 14. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

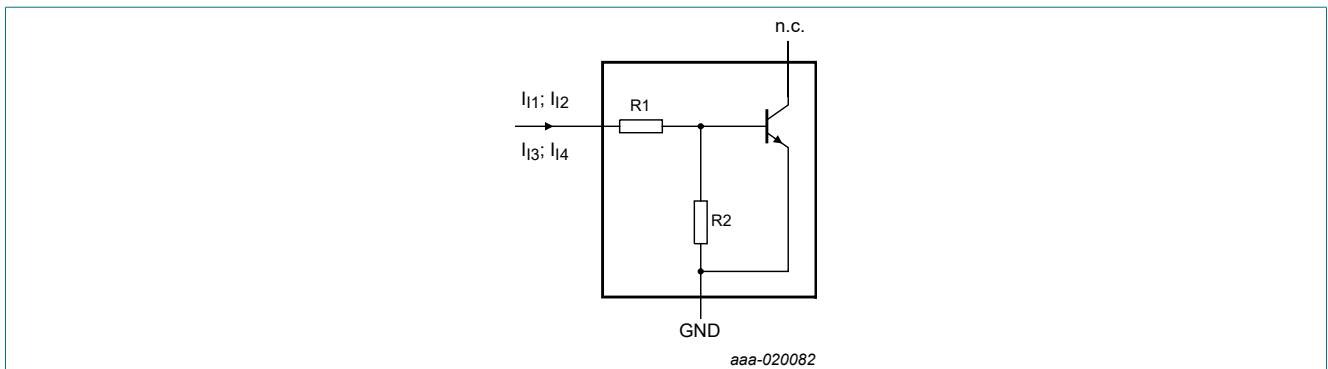


Fig. 15. NPN transistor: Resistor test circuit

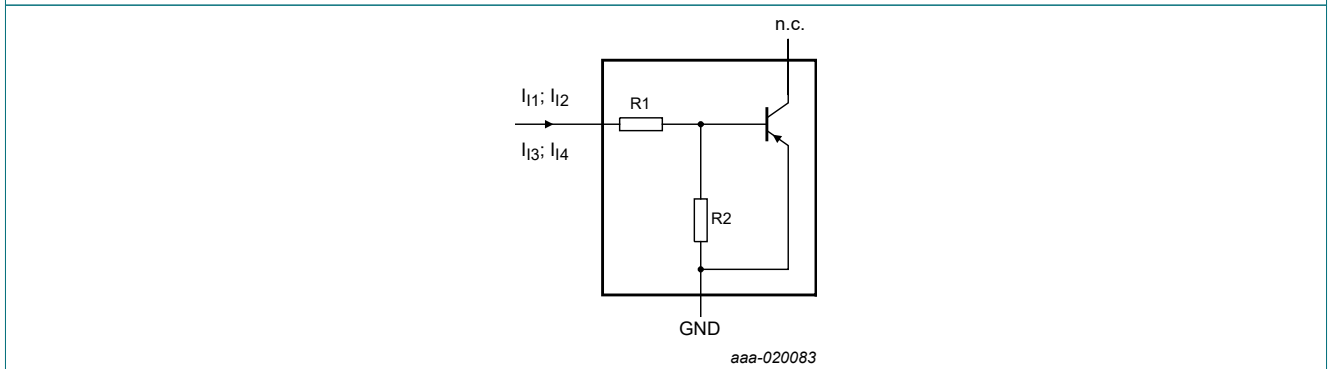


Fig. 16. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	Test conditions			
	I ₁₁	I ₁₂	I ₁₃	I ₁₄
PUMD48-Q	55 μA	105 μA	-55 μA	-105 μA
PUMD48-Q	-90 μA	-140 μA	55 μA	105 μA

NPN/PNP resistor-equipped double transistor; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

12. Package outline

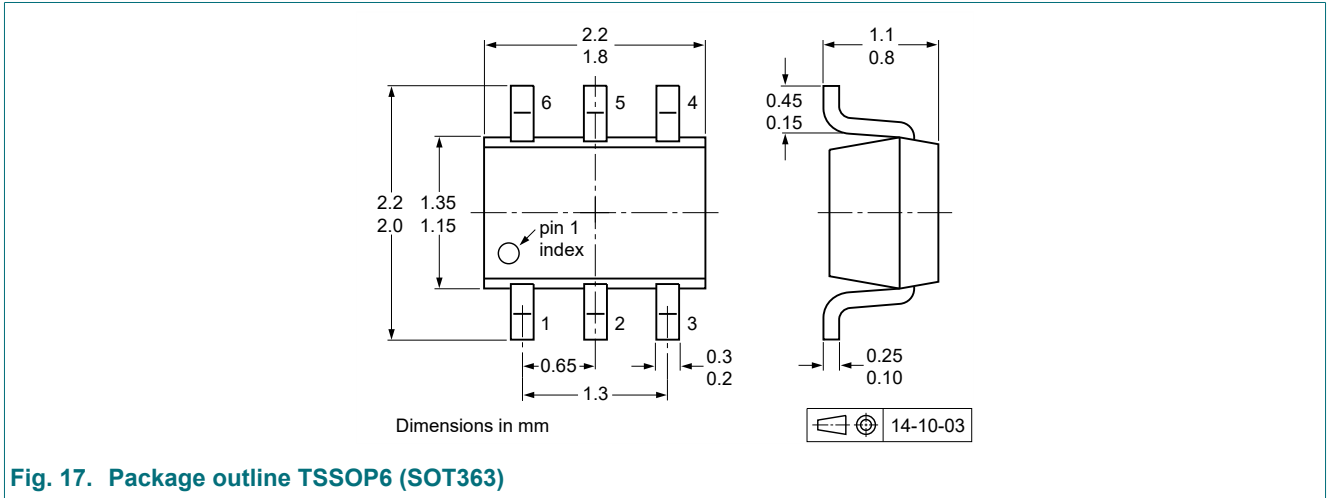


Fig. 17. Package outline TSSOP6 (SOT363)

13. Soldering

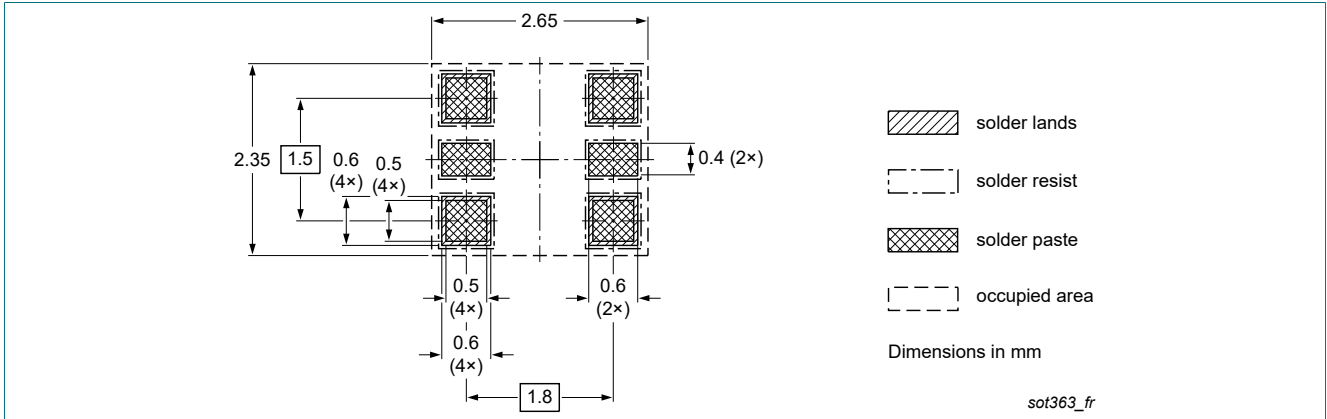


Fig. 18. Reflow soldering footprint for TSSOP6 (SOT363)

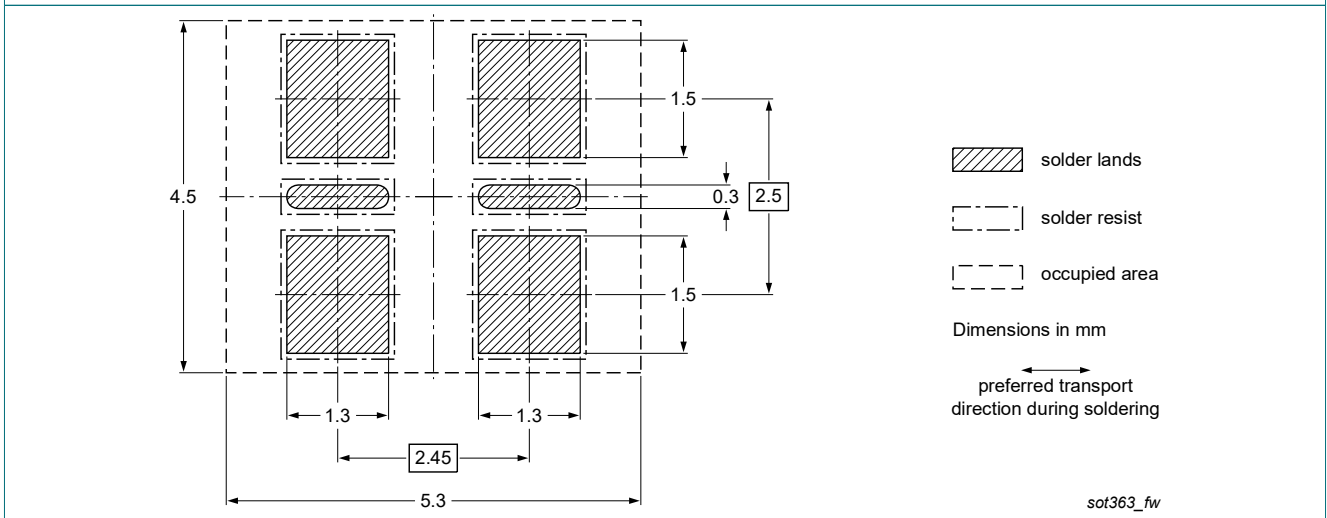


Fig. 19. Wave soldering footprint for TSSOP6 (SOT363)

NPN/PNP resistor-equipped double transistor; R1 = 47 k Ω , R2 = 47 k Ω and R1 = 2.2 k Ω , R2 = 47 k Ω

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD48-Q v.1	20211025	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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