Synchronous Buck Converter with Integrated FET

BD9106FVM BD9107FVM BD9109FVM BD9110NV BD9120HFN

General Description

The BD9106FVM, BD9107FVM, BD9109FVM, BD9110NV, and BD9120HFN are ROHM's high efficiency step-down switching regulators designed to produce a voltage as low as 1V from a supply voltage of 3.3V or 5.0V. It offers high efficiency by using synchronous switches and provides fast transient response to sudden load changes by implementing current mode control.

Features

- Fast Transient Response because of Current Mode Control System
- High Efficiency for All Load Ranges because of Synchronous Switches (Nch and Pch FET) and SLLM™ (Simple Light Load Mode)
- Soft-Start Function
- Thermal Shutdown and ULVO Functions
- Short-Circuit Protection with Time Delay Function
- Shutdown Function

Application

Power Supply for LSI including DSP, Microcomputer and ASIC

Key Specifications

- Input Voltage Range
  - BD9120HFN: 2.7V to 4.5V
  - BD9106FVM, BD9107FVM: 4.0V to 5.5V
  - BD9109FVM, BD9110NV: 4.5V to 5.5V
- Output Voltage Range
  - BD9109FVM: 3.30V ± 2%
  - BD9120HFN: 1.0V to 1.5V
  - BD9107FVM: 1.0V to 1.8V
  - BD9106FVM, BD9110NV: 1.0V to 2.5V
- Output Current
  - BD9106FVM, BD9109FVM, BD9120HFN: 0.8A(Max)
  - BD9107FVM: 1.2A(Max)
  - BD9110NV: 2.0A(Max)
- Switching Frequency: 1MHz(Typ)
- FET ON-Resistance

	Pch(Typ)/Nch(Typ)
BD9110NV:	200mΩ / 150mΩ
BD9106FVM, BD9107FVM:	350mΩ / 250mΩ
BD9120HFN, BD9109FVM:	350mΩ / 250mΩ

- Standby Current: 0μA(Typ)
- Operating Temperature Range
  - BD9110NV: -25°C to +105°C
  - BD9120HFN, BD9106FVM: -25°C to +85°C
  - BD9107FVM, BD9109FVM: -25°C to +85°C

Typical Application Circuit

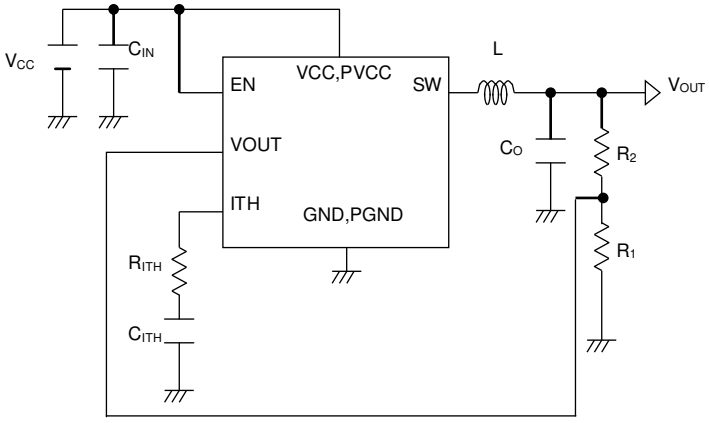


Figure 1. Typical Application Circuit

Packages

W(Typ) x D(Typ) x H(Max)

HSON8
2.90mm x 3.00mm x 0.60mm

MSOP8
2.90mm x 4.00mm x 0.90mm

SON008V5060
5.00mm x 6.00mm x 1.00mm

Pin Configuration

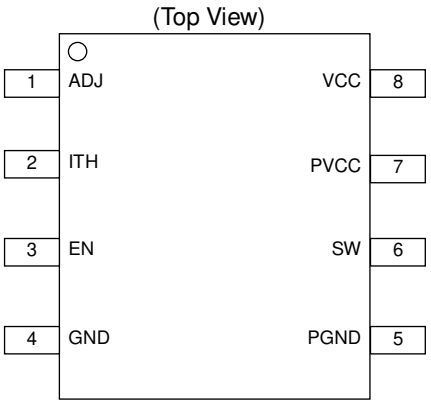


Figure 2. BD9106FVM, BD9107FVM

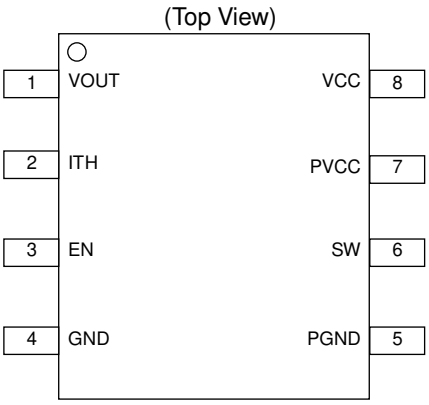


Figure 3. BD9109FVM

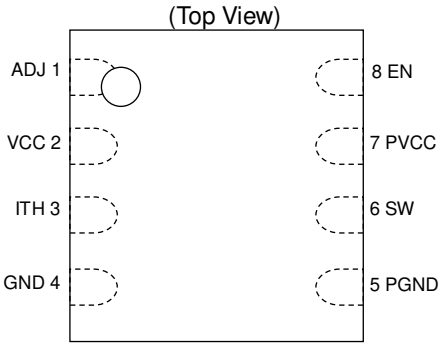


Figure 4. BD9110NV

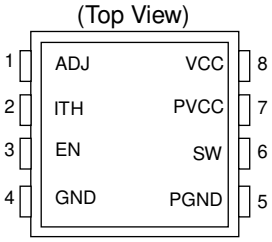


Figure 5. BD9120HFN

Pin Description

[BD9106FVM, BD9107FVM, BD9109FVM]

Pin No.	Pin Name	Function
1	ADJ/VOUT	Output voltage detection pin / ADJ for BD9106FVM·BD9107FVM
2	ITH	GmAmp output pin/connected to phase compensation capacitor
3	EN	Enable pin(active high)
4	GND	Ground pin
5	PGND	Power switch ground pin
6	SW	Power switch node
7	PVCC	Power switch supply pin
8	VCC	Power supply input pin

[BD9110NV]

Pin No.	Pin Name	Function
1	ADJ	Output voltage detection pin
2	VCC	Power supply input pin
3	ITH	GmAmp output pin/connected to phase compensation capacitor
4	GND	Ground pin
5	PGND	Power switch ground pin
6	SW	Power switch node
7	PVCC	Power switch supply pin
8	EN	Enable pin(active high)

[BD9120HFN]

Pin No.	Pin Name	Function
1	ADJ	Output voltage detection pin
2	ITH	GmAmp output pin/connected to phase compensation capacitor
3	EN	Enable pin(active high)
4	GND	Ground pin
5	PGND	Power switch ground pin
6	SW	Power switch node
7	PVCC	Power switch supply pin
8	VCC	Power supply input pin

Lineup

Operating Temperature Range	Input Voltage Range	Output Voltage Range	Output Current (Max)	UVLO Threshold Voltage (Typ)	Package		Available Part Number
-25°C to +85°C	4.0V to 5.5V	Adjustable (1.0V to 2.5V)	0.8A	3.4V	MSOP8	Reel of 3000	BD9106FVM-TR
		Adjustable (1.0V to 1.8V)	1.2A	2.7V	MSOP8	Reel of 3000	BD9107FVM-TR
	4.5V to 5.5V	3.30±2%	0.8A	3.8V	MSOP8	Reel of 3000	BD9109FVM-TR
	2.7V to 4.5V	Adjustable (1.0V to 1.5V)	0.8A	2.5V	HSON8	Reel of 3000	BD9120HFN-TR
-25°C to +105°C	4.5V to 5.5V	Adjustable (1.0V to 2.5V)	2.0A	3.7V	SON008V5060	Reel of 2000	BD9110NV-E2

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit			Unit
		BD910xFVM	BD9110NV	BD9120HFN	
VCC Voltage	V_{CC}	-0.3 to +7 (Note 1)	-0.3 to +7 (Note 1)	-0.3 to +7 (Note 1)	V
PVCC Voltage	PV_{CC}	-0.3 to +7 (Note 1)	-0.3 to +7 (Note 1)	-0.3 to +7 (Note 1)	V
EN Voltage	V_{EN}	-0.3 to +7	-0.3 to +7	-0.3 to +7	V
SW , ITH Voltage	V_{SW},V_{ITH}	-0.3 to +7	-0.3 to +7	-0.3 to +7	V
Power Dissipation 1	Pd1	0.38 (Note 2)	0.64 (Note 4)	0.63 (Note 6)	W
Power Dissipation 2	Pd2	0.58 (Note 3)	5.29 (Note 5)	1.75 (Note 7)	W
Operating Temperature Range	Topr	-25 to +85	-25 to +105	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	+150	+150	°C

(Note 1) Pd should not be exceeded.
(Note 2) IC only
(Note 3) 1-layer. mounted on a 70mm x 70mm x 1.6mm glass-epoxy board
(Note 4) IC only
(Note 5) 4-layer. mounted on a 74.2mm x 74.2mm x 1.6mm glass-epoxy board, area of copper foil in 1st layer : 5505mm^2
(Note 6) 1-layer. mounted on a 74.2mm x 74.2mm x 1.6mm glass-epoxy board, area of copper foil : 0.2%
(Note 7) 1-layer. mounted on a 74.2mm x 74.2mm x 1.6mm glass-epoxy board, area of copper foil : 65%
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	BD9106FVM		BD9107FVM		BD9109FVM		BD9110NV		BD9120HFN		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
VCC Voltage	V_{CC} (Note 8)	4.0	5.5	4.0	5.5	4.5	5.5	4.5	5.5	2.7	4.5	V
PVCC Voltage	PV_{CC} (Note 8)	4.0	5.5	4.0	5.5	4.5	5.5	4.5	5.5	2.7	4.5	V
EN Voltage	V_{EN}	0	V_{CC}	0	V_{CC}	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
SW Average Output Current	I_{SW} (Note 8)	-	0.8	-	1.2	-	0.8	-	2.0	-	0.8	A

(Note 8) Pd should not be exceeded.

Electrical Characteristics

BD9106FVM (Ta=25°C, V_{CC}=5V, V_{EN}=V_{CC}, R_1=20kΩ, R_2=10kΩ unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	250	400	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 9)	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=5V
Nch FET ON-Resistance (Note 9)	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=5V
ADJ Voltage	V_{ADJ}	0.780	0.800	0.820	V	
Output Voltage (Note 9)	V_{OUT}	-	1.200	-	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	ADJ=H
ITH Source Current	I_{THSO}	10	20	-	μA	ADJ=L
UVLO Threshold Voltage	V_{UVLOTh}	3.2	3.4	3.6	V	V_{CC}=H to L
UVLO Hysteresis Voltage	$V_{UVLOHys}$	50	100	200	mV	
Soft Start Time	t_{SS}	1.5	3	6	ms	
Timer Latch Time	t_{LATCH}	0.5	1	2	ms	

(Note 9) Design Guarantee（Outgoing inspection is not done on all products）

BD9107FVM (Ta=25°C, V_{CC}=5V, V_{EN}=V_{CC}, R_1=20kΩ, R_2=10kΩ unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	250	400	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 9)	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=5V
Nch FET ON-Resistance (Note 9)	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=5V
ADJ Voltage	V_{ADJ}	0.780	0.800	0.820	V	
Output Voltage (Note 9)	V_{OUT}	-	1.200	-	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	V_{OUT}=H
ITH Source Current	I_{THSO}	10	20	-	μA	V_{OUT}=L
UVLO Threshold Voltage	V_{UVLOTh}	2.6	2.7	2.8	V	V_{CC}=H to L
UVLO Hysteresis Voltage	$V_{UVLOHys}$	150	300	600	mV	
Soft Start Time	t_{SS}	0.5	1	2	ms	
Timer Latch Time	t_{LATCH}	0.5	1	2	ms	

(Note 9) Design Guarantee（Outgoing inspection is not done on all products）

BD9109FVM (Ta=25°C, V_{CC}=PV_{CC}=5V, V_{EN}= V_{CC} unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	250	400	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 9)	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=5V
Nch FET ON-Resistance (Note 9)	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=5V
Output Voltage (Note 9)	V_{OUT}	3.234	3.300	3.366	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	V_{OUT}=H
ITH Source Current	I_{THSO}	10	20	-	μA	V_{OUT}=L
UVLO Threshold Voltage	V_{UVLO1}	3.6	3.8	4.0	V	V_{CC}=H to L
UVLO Hysteresis Voltage	V_{UVLO2}	3.65	3.9	4.2	V	V_{CC}=L to H
Soft Start Time	t_{SS}	0.5	1	2	ms	
Timer Latch Time	t_{LATCH}	1	2	3	ms	SCP/TSD operated
Output Short Circuit Threshold Voltage	V_{SCP}	-	2	2.7	V	V_{OUT}=H to L

(Note 9) Design Guarantee（Outgoing inspection is not done on all products）

Electrical Characteristics – continued

BD9110NV (Ta=25°C, V_{CC}=PV_{CC}=5V, V_{EN}=V_{CC}, R_1=10kΩ,R_2=5kΩ unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	250	350	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 9)	R_{ONP}	-	200	320	mΩ	PV_{CC}=5V
Nch FET ON-Resistance (Note 9)	R_{ONN}	-	150	270	mΩ	PV_{CC}=5V
ADJ Voltage	V_{ADJ}	0.780	0.800	0.820	V	
Output Voltage (Note 9)	V_{OUT}	-	1.200	-	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	V_{OUT}=H
ITH Source Current	I_{THSO}	10	20	-	μA	V_{OUT}=L
UVLO Threshold Voltage	V_{UVLOTh}	3.5	3.7	3.9	V	V_{CC}=H to L
UVLO Hysteresis Voltage	$V_{UVLOHys}$	50	100	200	mV	
Soft Start Time	t_{SS}	2.5	5	10	ms	
Timer Latch Time	t_{LATCH}	0.5	1	2	ms	

(Note 9) Design Guarantee（Outgoing inspection is not done on all products）

BD9120HFN (Ta=25°C, V_{CC}=PV_{CC}=3.3V, V_{EN}=V_{CC}, R_1=20kΩ, R_2=10kΩ unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	200	400	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=3.3V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 9)	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=3.3V
Nch FET ON-Resistance (Note 9)	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=3.3V
ADJ Voltage	V_{ADJ}	0.780	0.800	0.820	V	
Output Voltage(Note 9)	V_{OUT}	-	1.200	-	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	V_{OUT}=H
ITH Source Current	I_{THSO}	10	20	-	μA	V_{OUT}=L
UVLO Threshold Voltage	V_{UVLO1}	2.400	2.500	2.600	V	V_{CC}=H to L
UVLO Hysteresis Voltage	V_{UVLO2}	2.425	2.550	2.700	V	V_{CC}=L to H
Soft Start Time	t_{SS}	0.5	1	2	ms	
Timer Latch Time	t_{LATCH}	1	2	3	ms	SCP/TSD operated
Output Short Circuit Threshold Voltage	V_{SCP}	-	V_{OUT}x0.5	V_{OUT}x0.7	V	V_{OUT}=H to L

(Note 9) Design Guarantee（Outgoing inspection is not done on all products）

Block Diagram

[BD9106FVM, BD9107FVM]

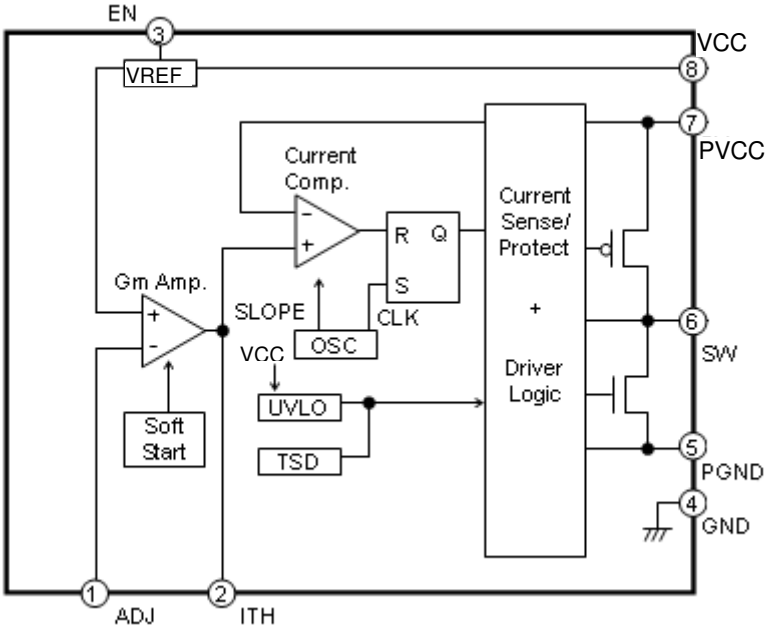


Figure 6. BD9106FVM, BD9107FVM Block Diagram

[BD9109FVM]

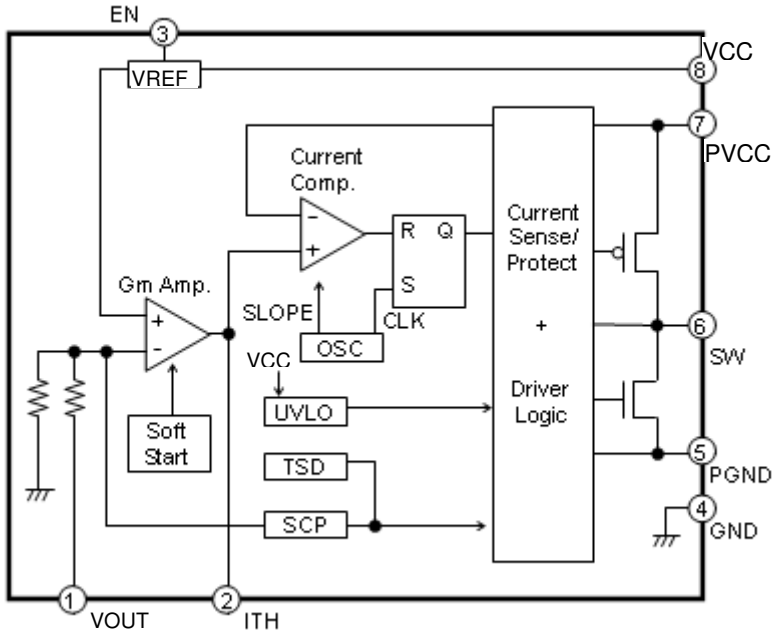


Figure 7. BD9109FVM Block Diagram

[BD9110NV]

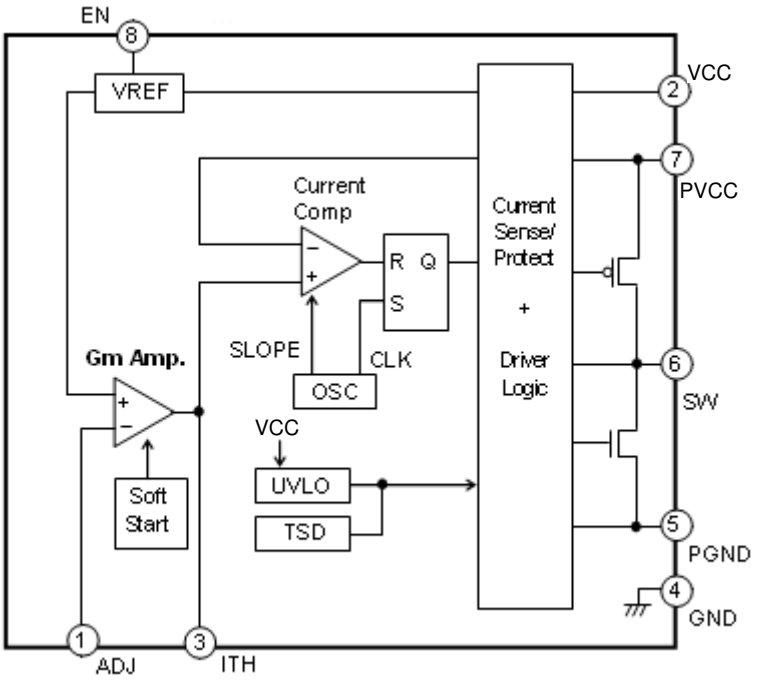


Figure 8. BD9110NV Block Diagram

[BD9120HFN]

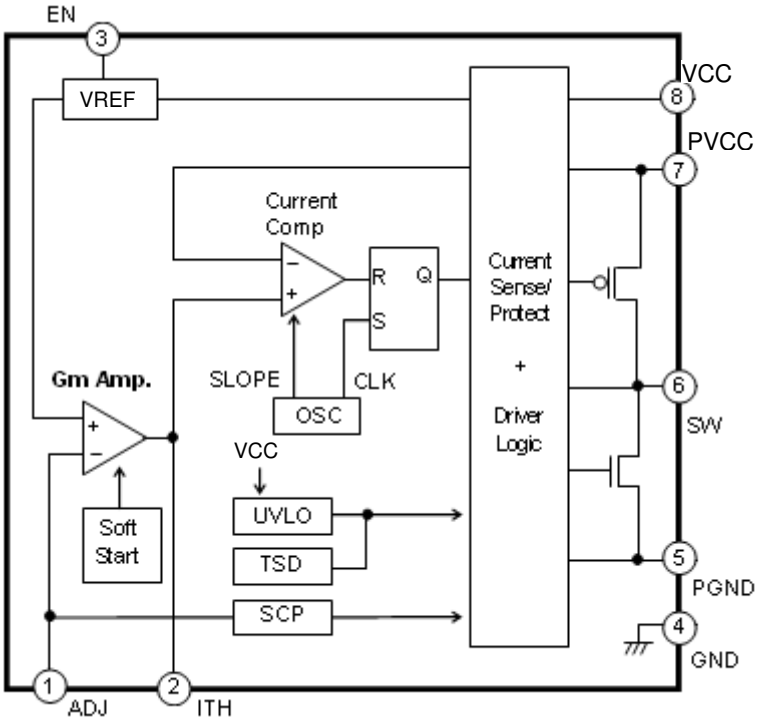


Figure 9. BD9120HFN Block Diagram

Typical Performance Curves

[BD9106FVM]

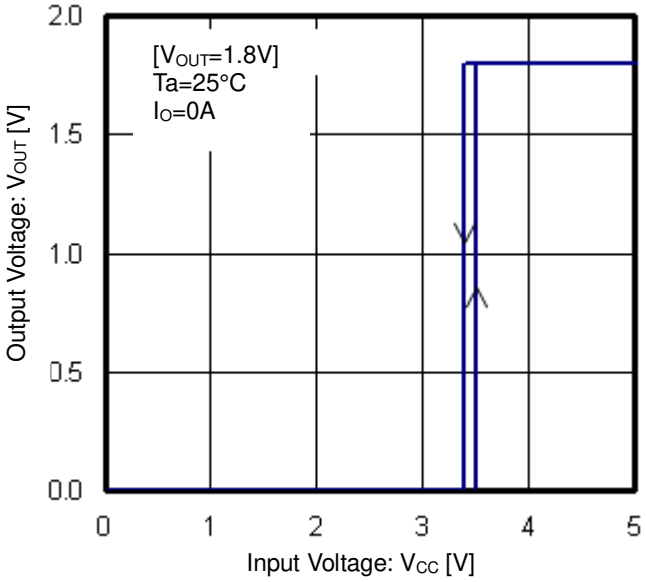


Figure 10. Output Voltage vs Input Voltage

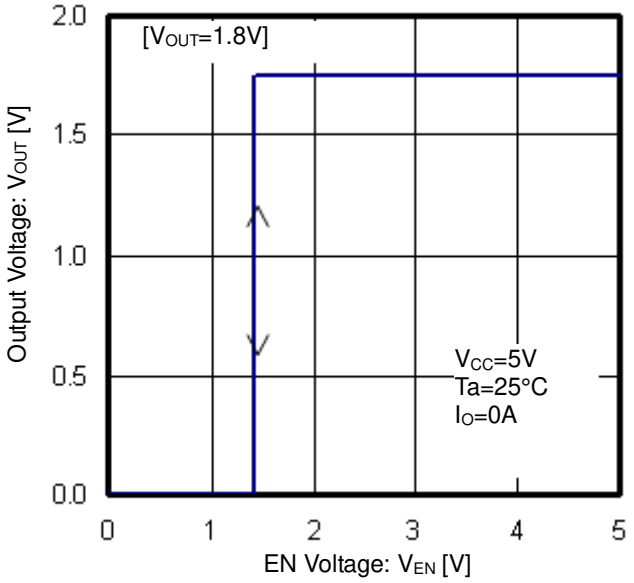


Figure 11. Output Voltage vs EN Voltage

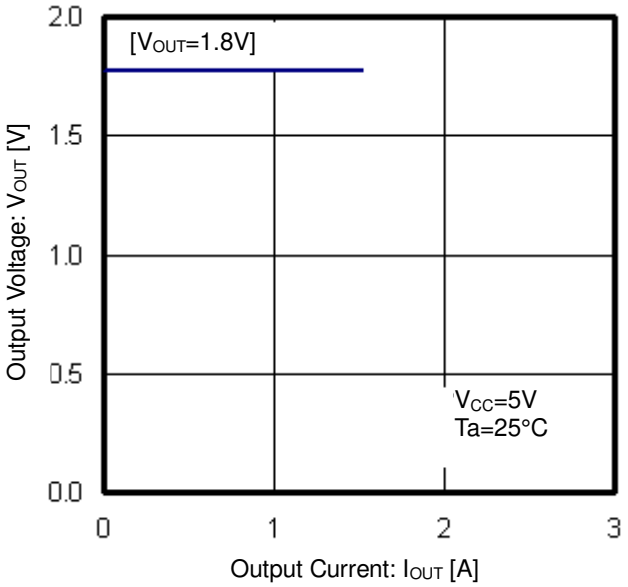


Figure 12. Output Voltage vs Output Current

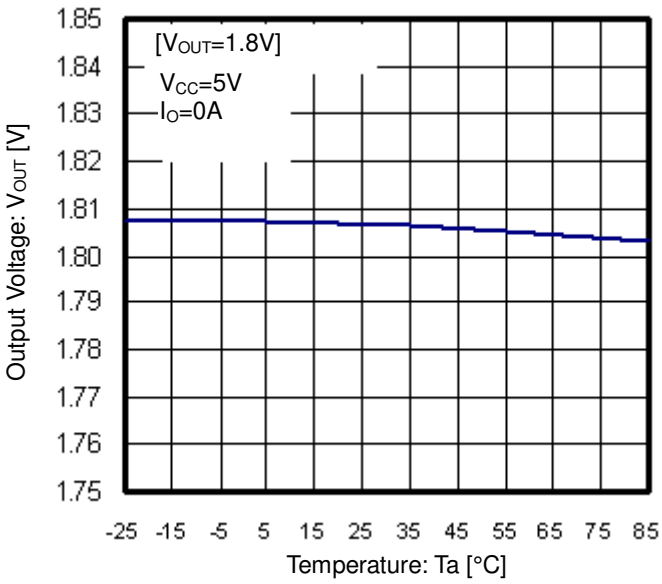


Figure 13. Output Voltage vs Temperature

Typical Performance Curves – continued

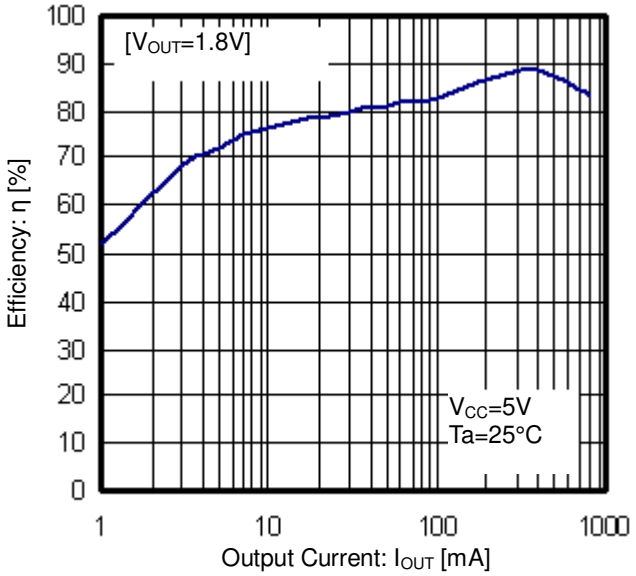


Figure 14. Efficiency vs Output Current

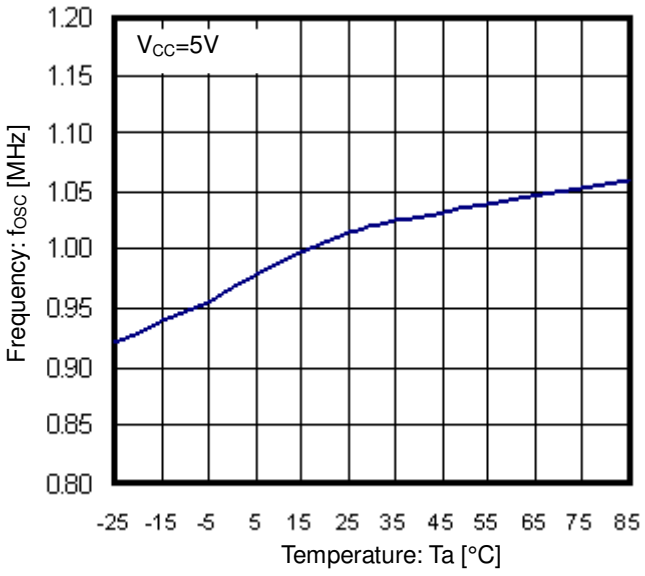


Figure 15. Frequency vs Temperature

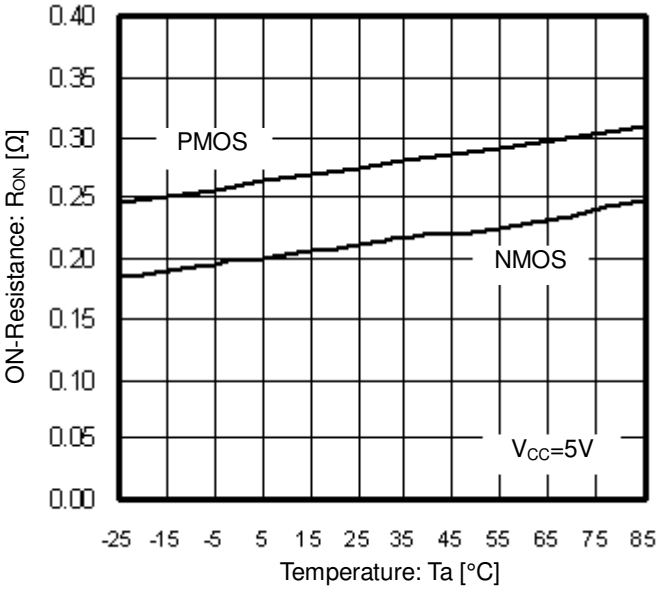


Figure 16. ON-Resistance vs Temperature

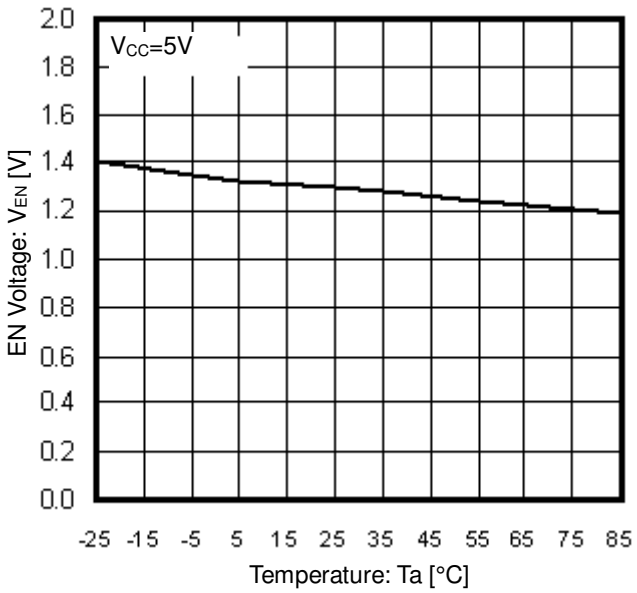


Figure 17. EN Voltage vs Temperature

Typical Performance Curves – continued

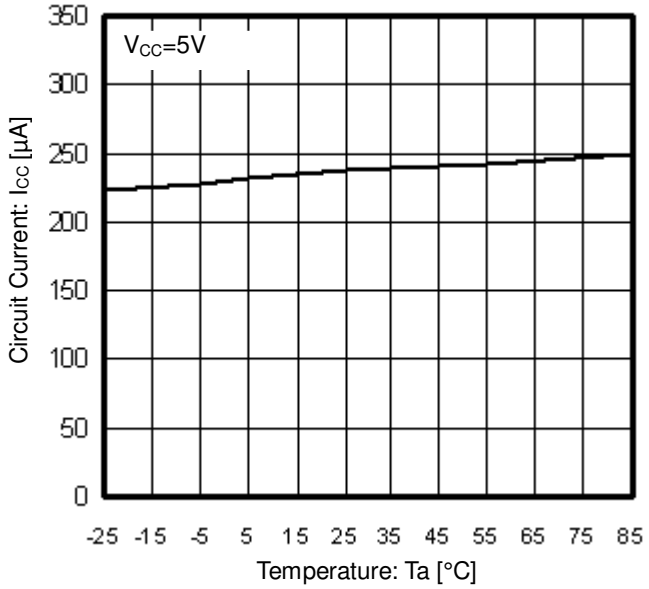


Figure 18. Circuit Current vs Temperature

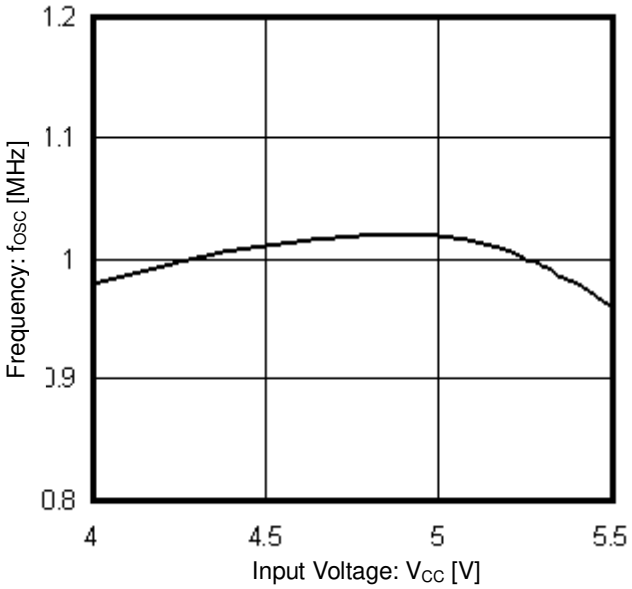


Figure 19. Frequency vs Input Voltage

Typical Waveforms

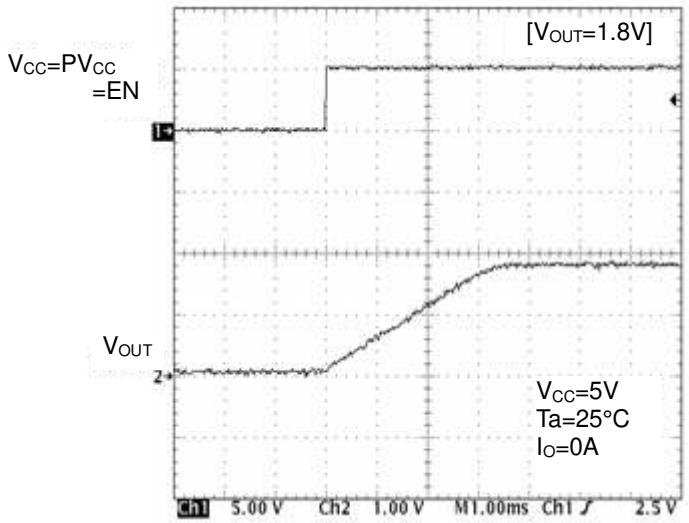


Figure 20. Soft Start Waveform

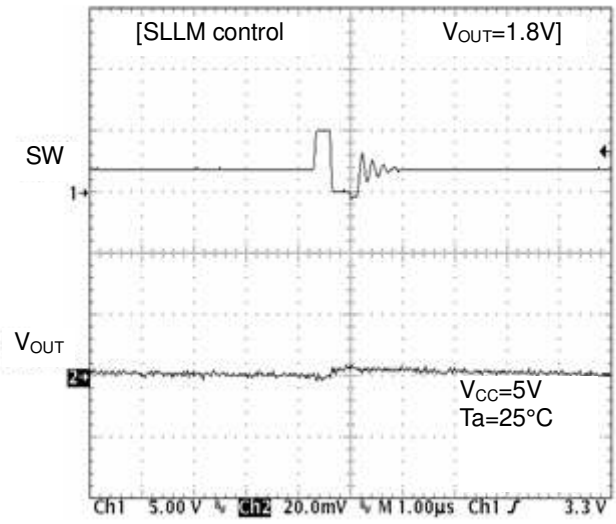


Figure 21. SW Waveform
(I_O=10mA)

Typical Waveforms – continued

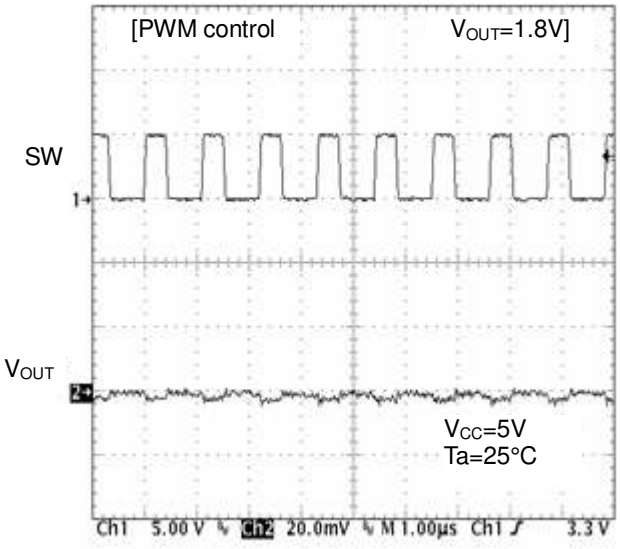


Figure 22. SW Waveform
(I_O=200mA)

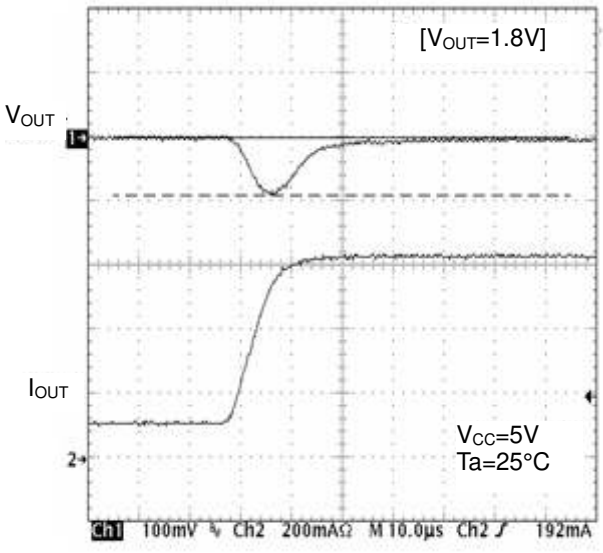


Figure 23. Transient Response
(I_O=100mA to 600mA, 10µs)

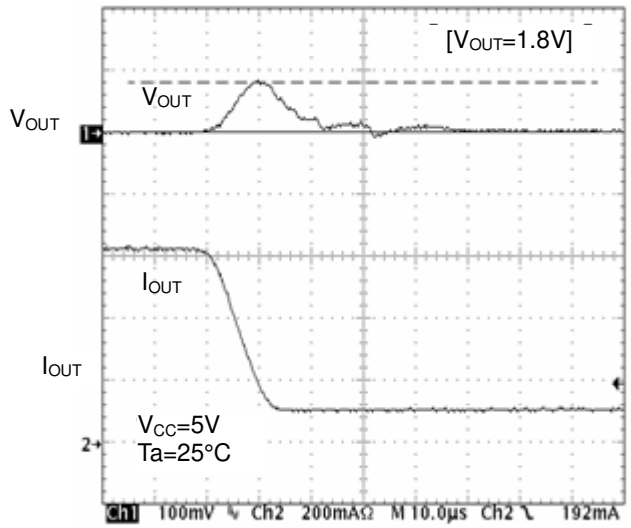


Figure 24. Transient response
(Io=600mA to100mA, 10µs)

Typical Performance Curves

[BD9107FVM]

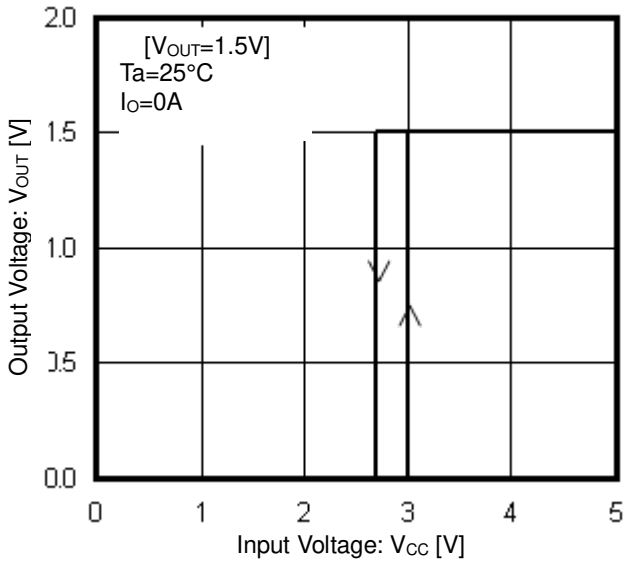


Figure 25. Output Voltage vs Input Voltage

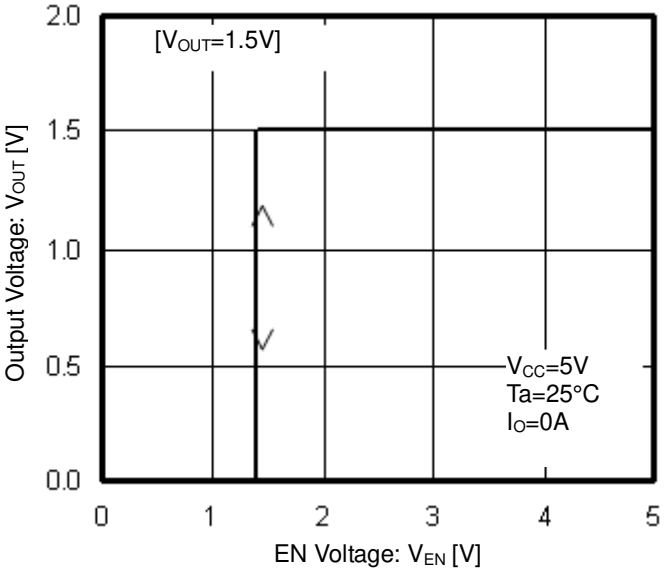


Figure 26. Output Voltage vs EN Voltage

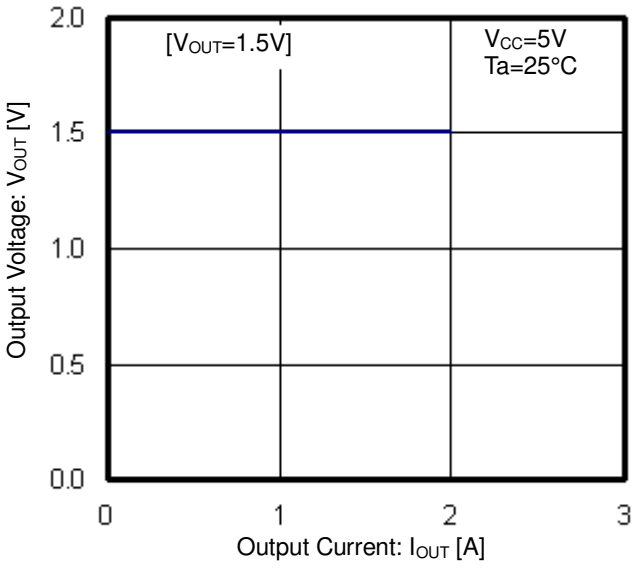


Figure 27. Output Voltage vs Output Current

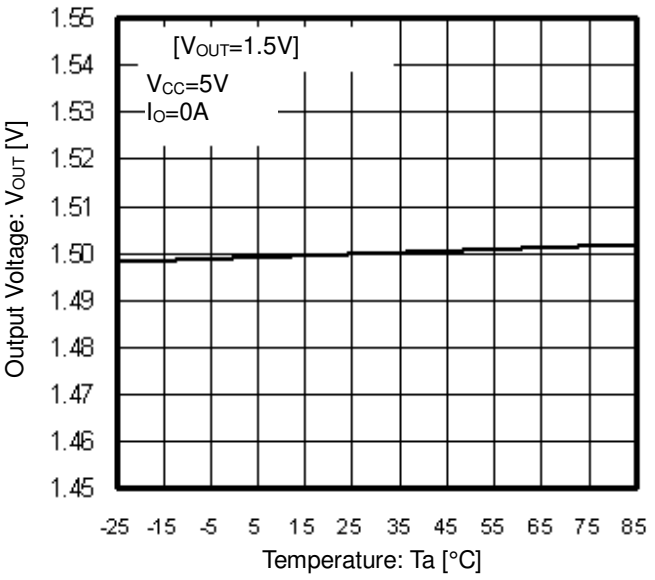


Figure 28. Output Voltage vs Temperature

Typical Performance Curves – continued

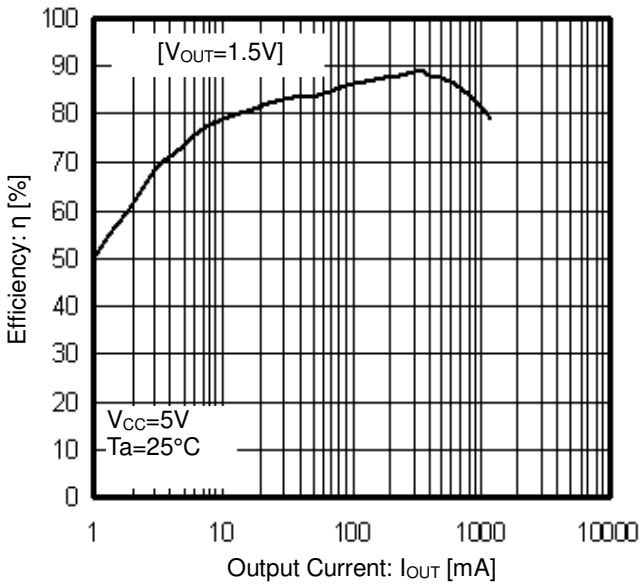


Figure 29. Efficiency vs Output Current

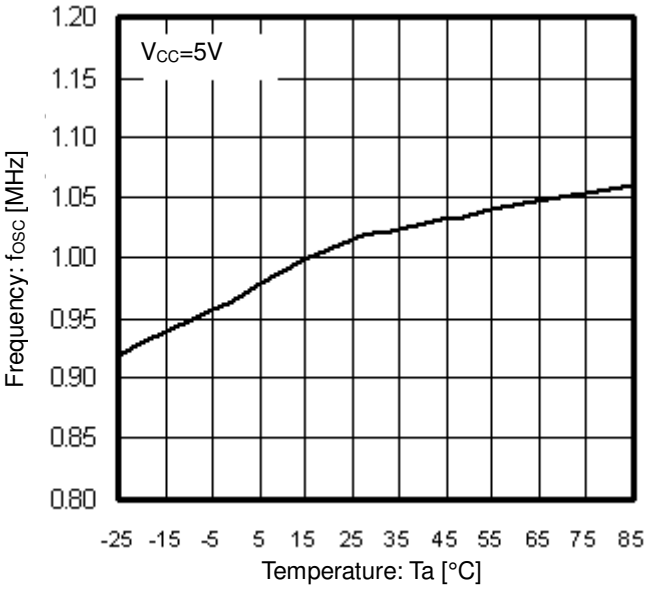


Figure 30. Frequency vs Temperature

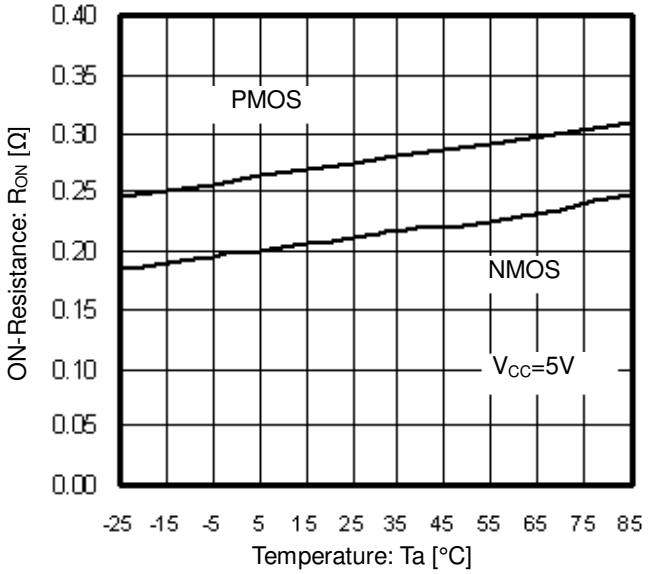


Figure 31. ON-Resistance vs Temperature

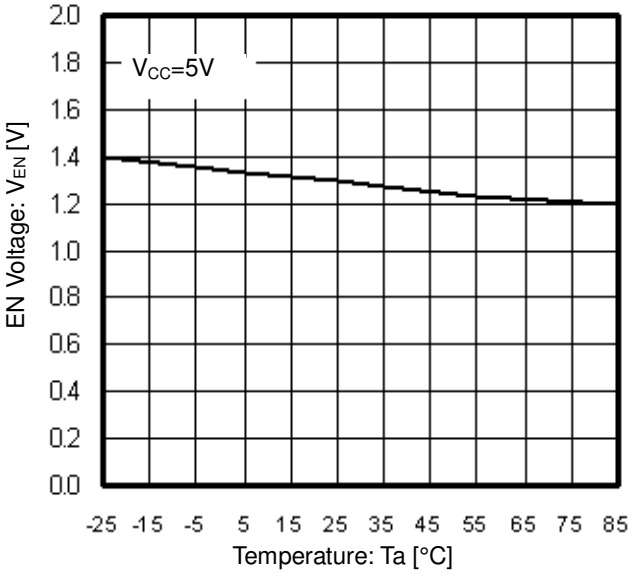


Figure 32. EN Voltage vs Temperature

Typical Performance Curves – continued

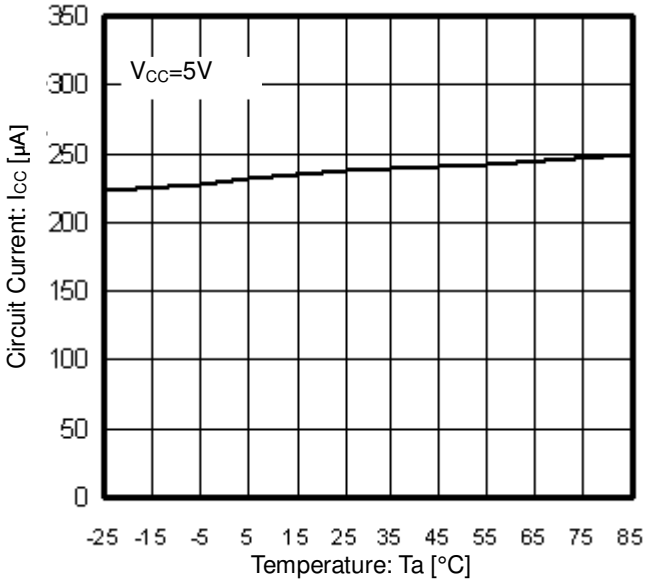


Figure 33. Circuit Current vs Temperature

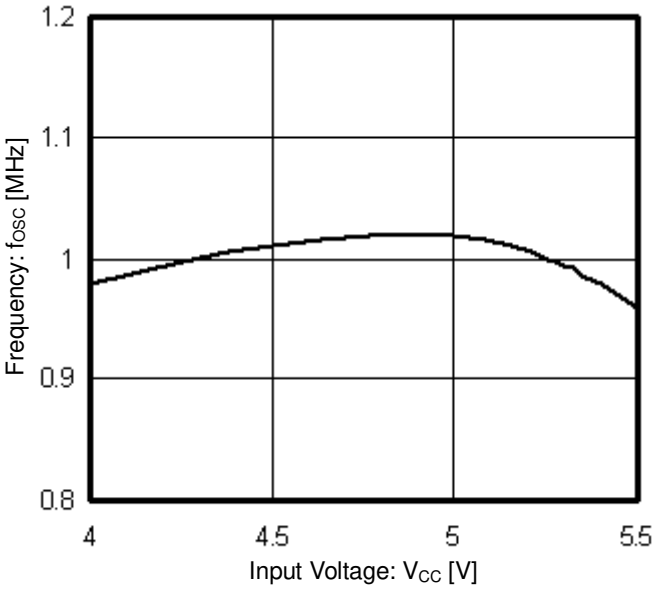


Figure 34. Frequency vs Input Voltage

Typical Waveforms

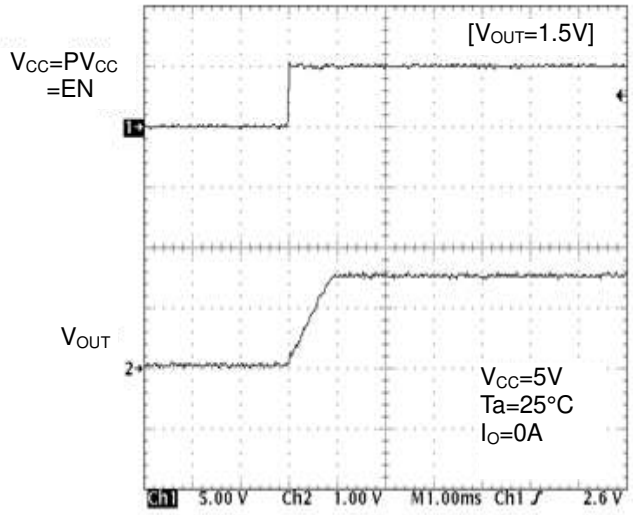


Figure 35. Soft Start Waveform

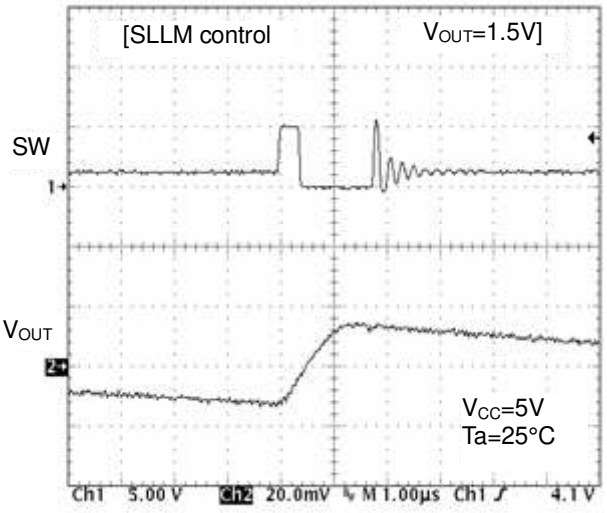


Figure 36. SW Waveform
(I_O=10mA)

Typical Waveforms – continued

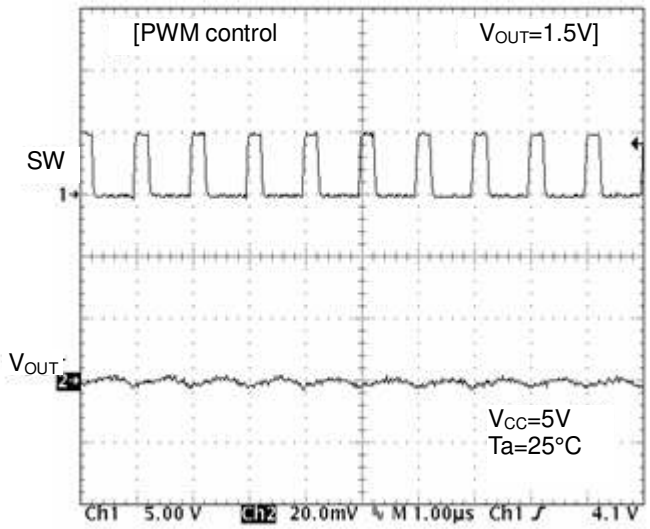


Figure 37. SW Waveform
(I_O=500mA)

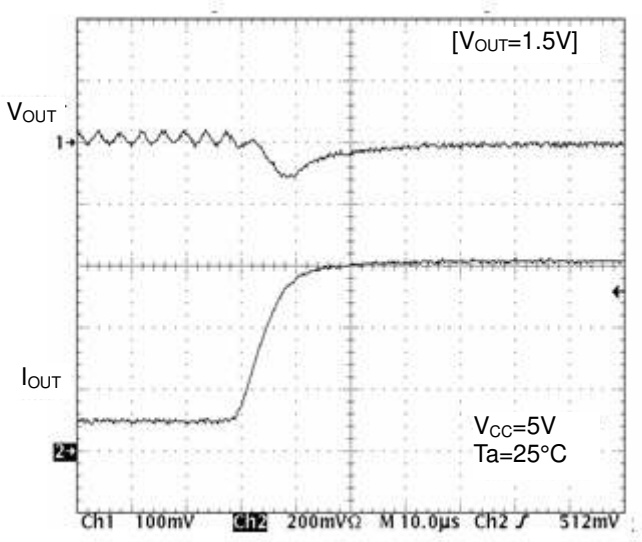


Figure 38. Transient Response
(I_O=100mA to 600mA, 10µs)

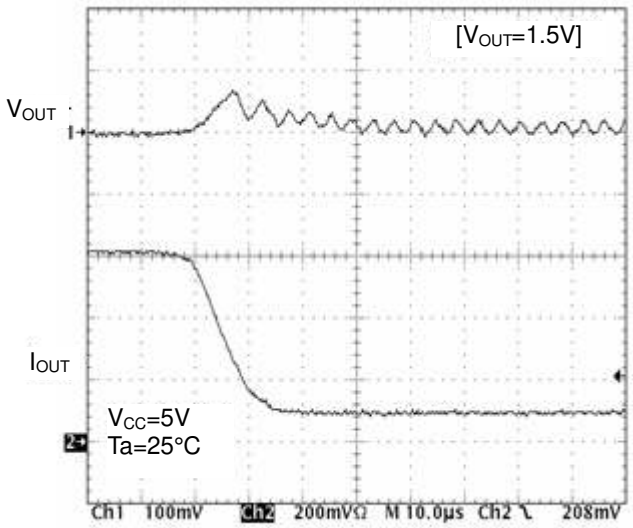


Figure 39. Transient Response
(I_O=600mA to 100mA, 10µs)

Typical Performance Curves

[BD9109FVM]

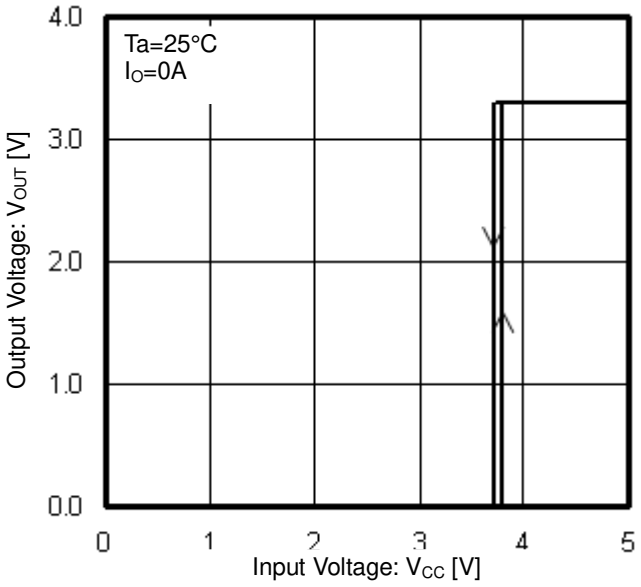


Figure 40. Output Voltage vs Input Voltage

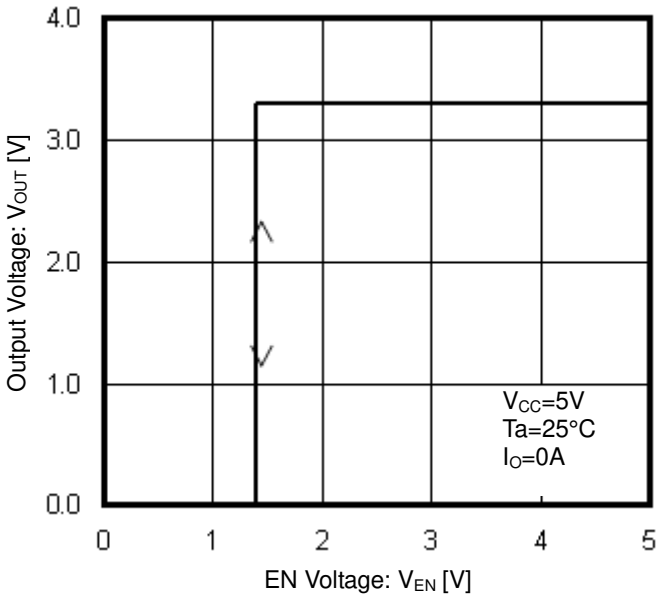


Figure 41. Output Voltage vs EN Voltage

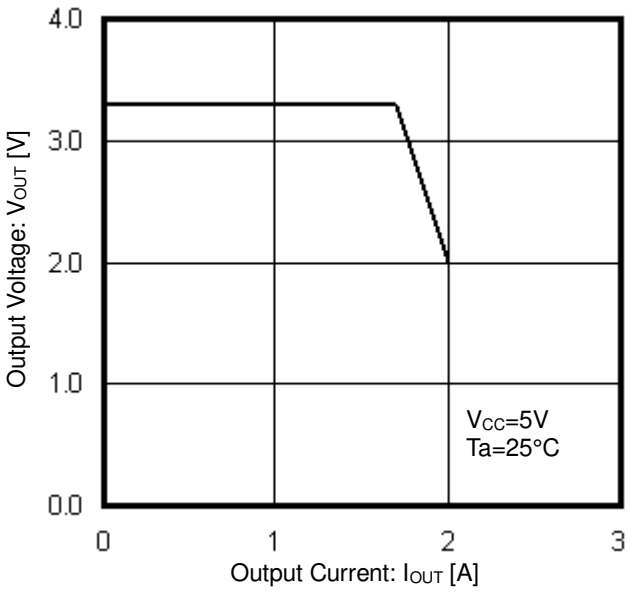


Figure 42. Output Voltage vs Output Current

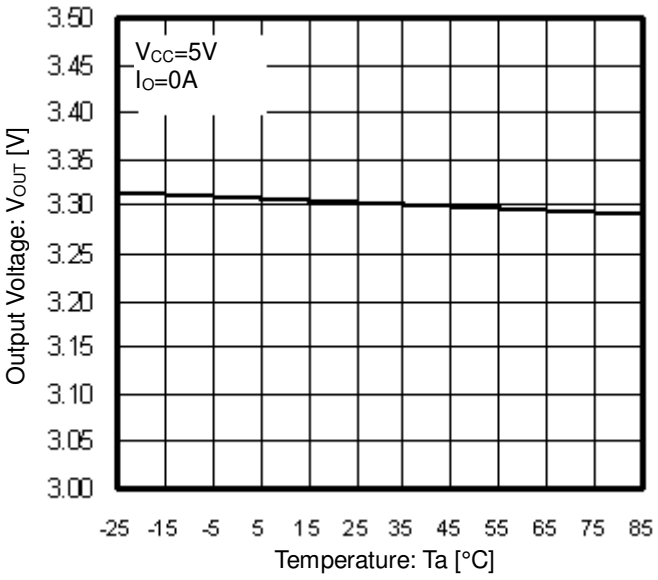


Figure 43. Output Voltage vs Temperature

Typical Performance Curves – continued

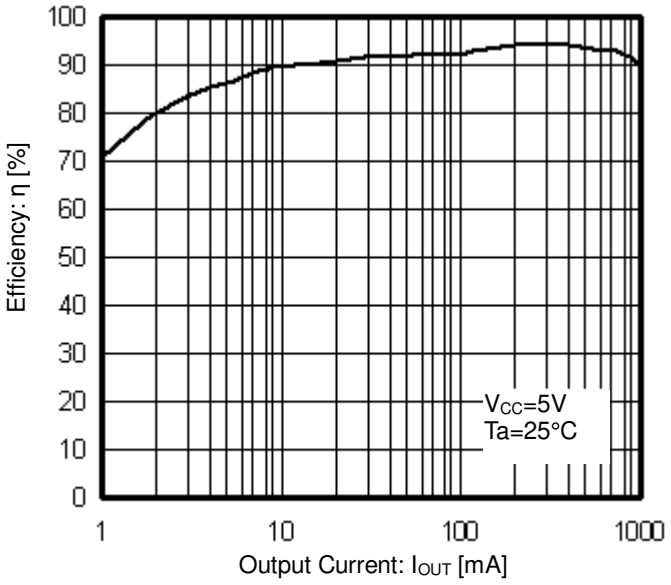


Figure 44. Efficiency vs Output Current

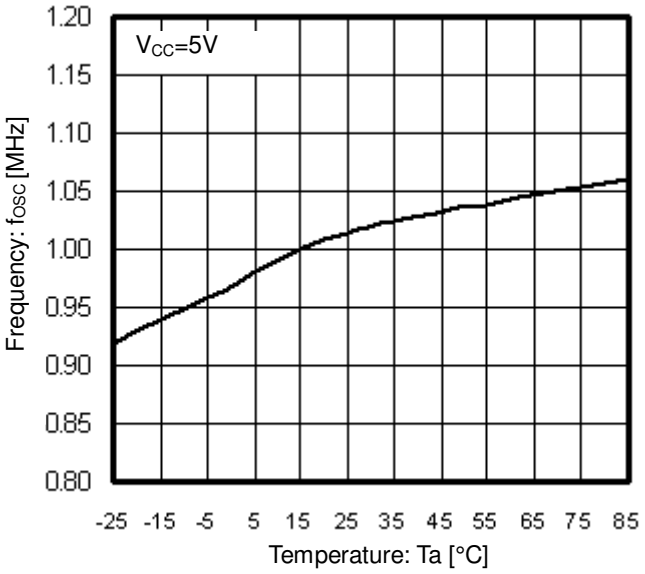


Figure 45. Frequency vs Temperature

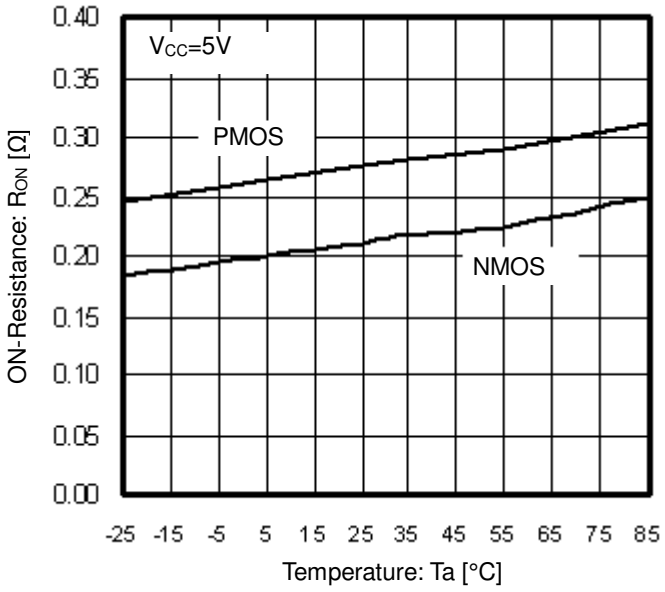


Figure 46. ON-Resistance vs Temperature

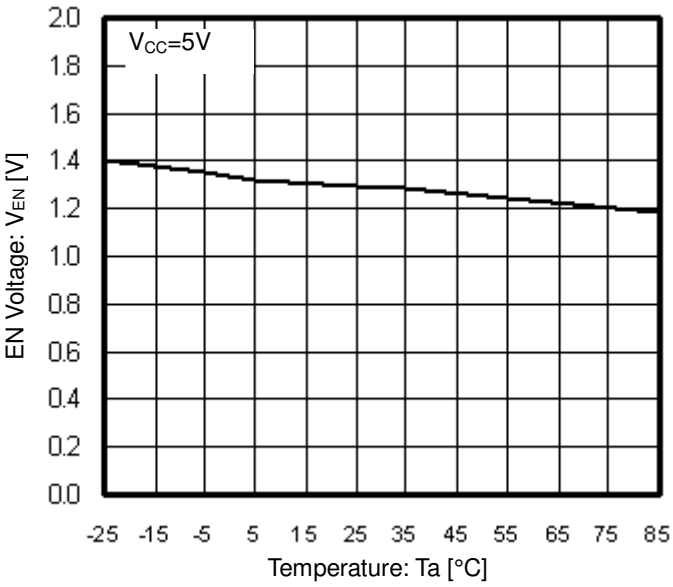


Figure 47. EN Voltage vs Temperature

Typical Performance Curves – continued

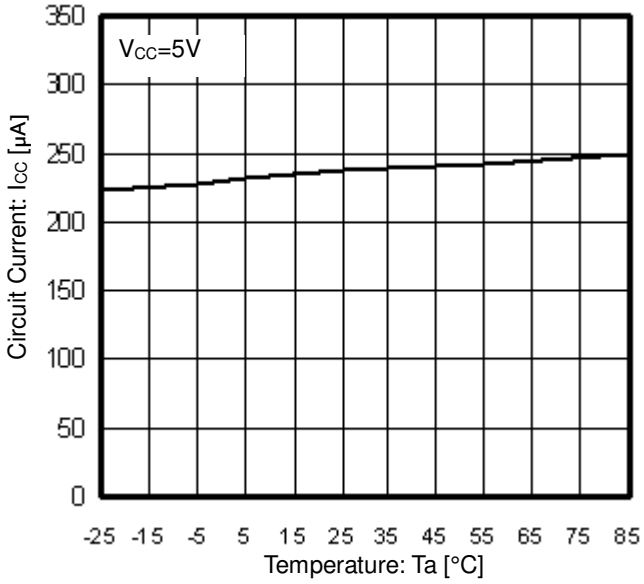


Figure 48. Circuit Current vs Temperature

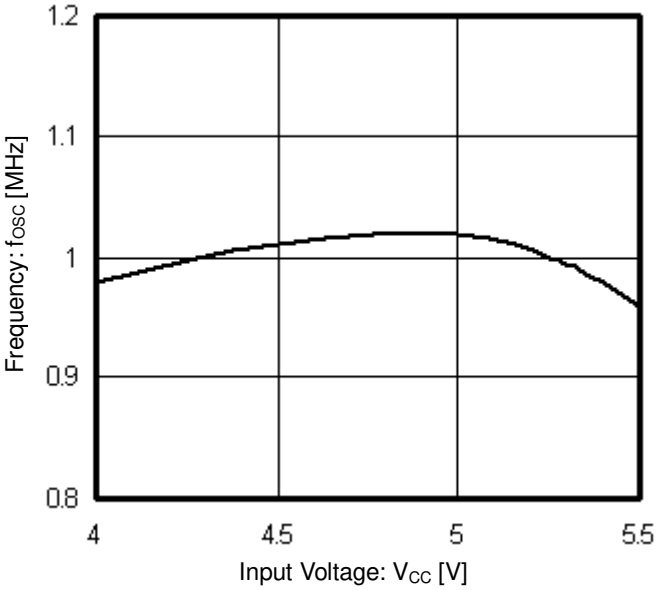


Figure 49. Frequency vs Input Voltage

Typical Waveforms

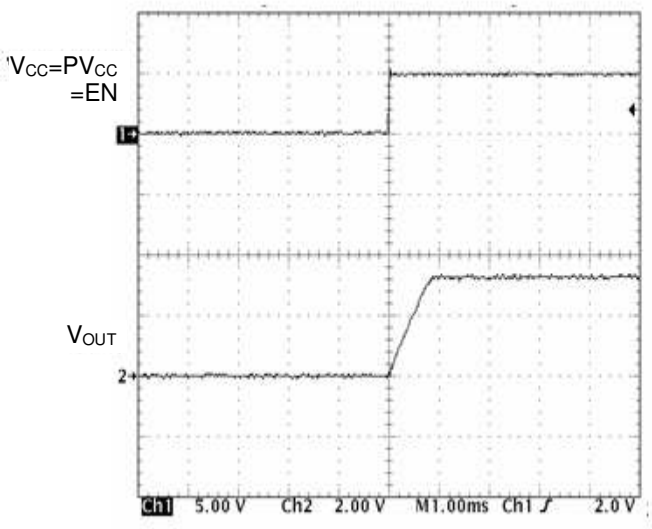


Figure 50. Soft Start Waveform

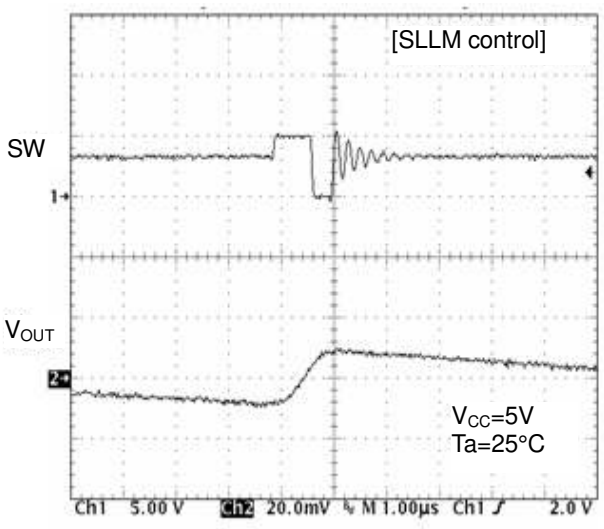


Figure 51. SW Waveform
(I_O=10mA)

Typical Waveforms – continued

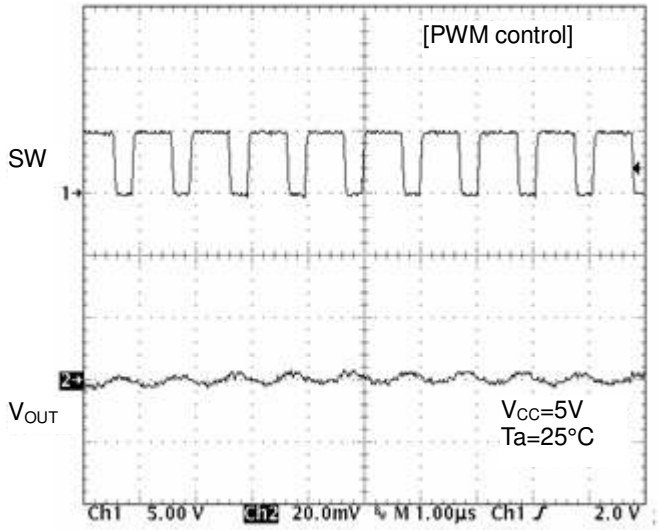


Figure 52. SW Waveform
(I_O=500mA)

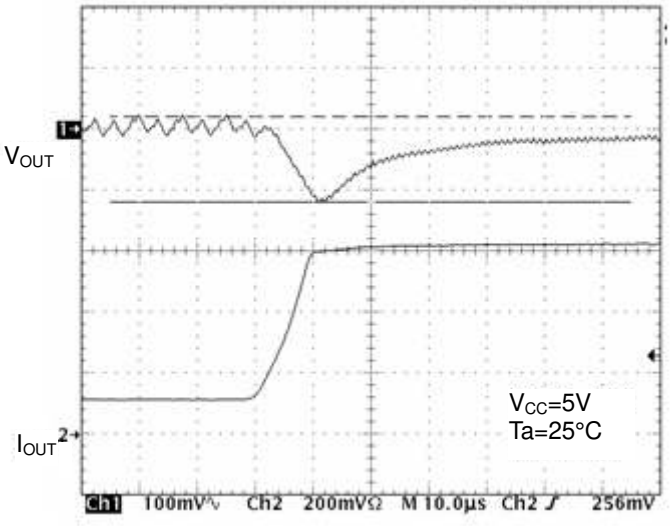


Figure 53. Transient Response
(I_O=100mA to 600mA, 10µs)

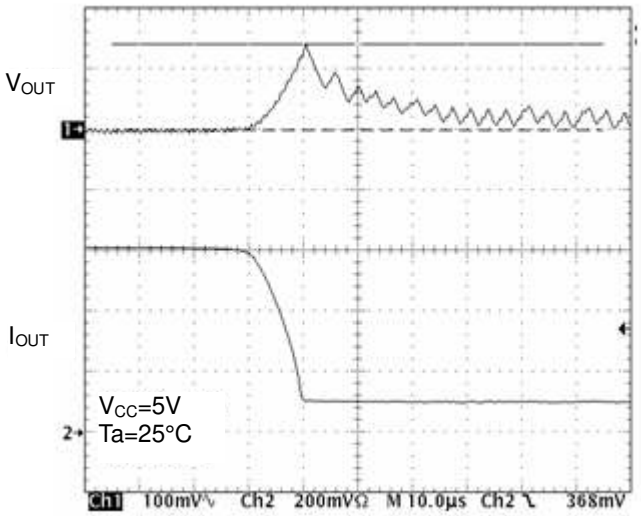


Figure 54. Transient Response
(I_O=600mA to 100mA, 10µs)

Typical Performance Curves

[BD9110NV]

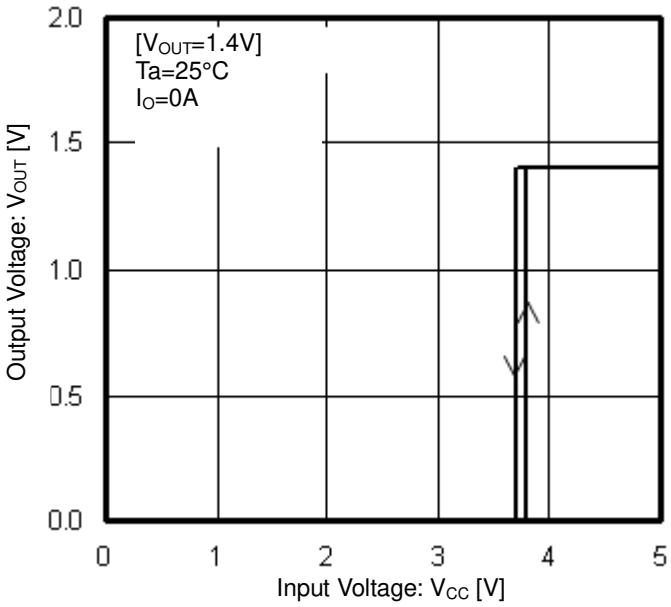


Figure 55. Output Voltage vs Input Voltage

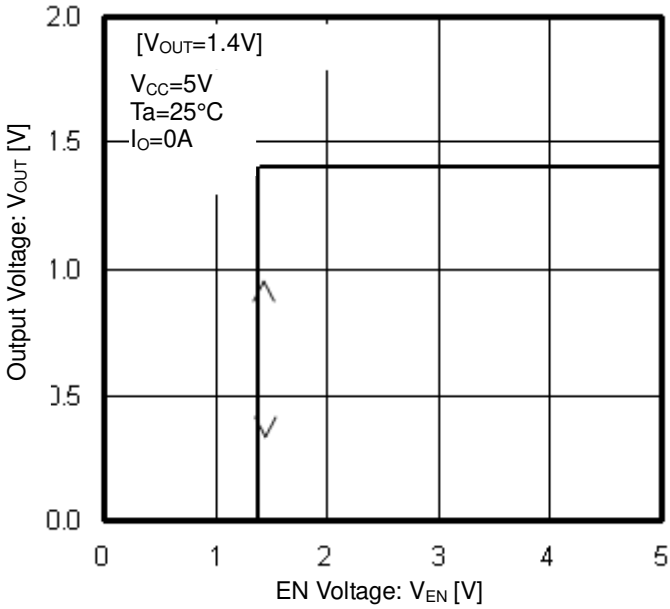


Figure 56. Output Voltage vs EN Voltage

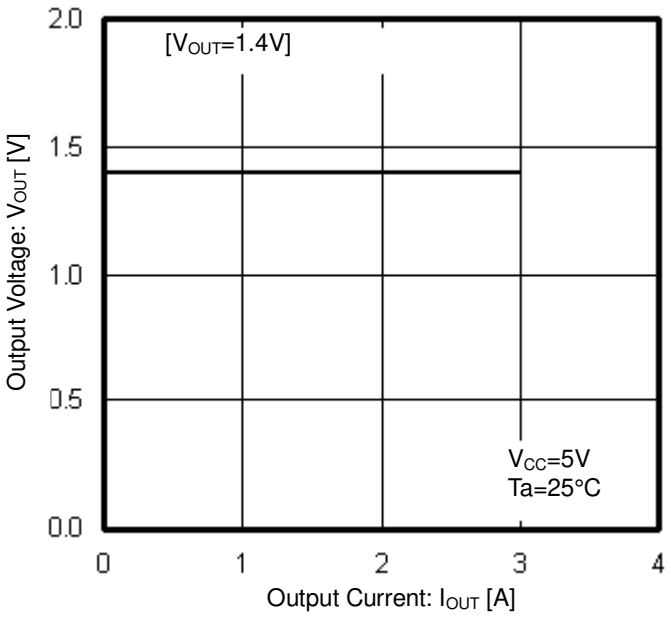


Figure 57. Output Voltage vs Output Current

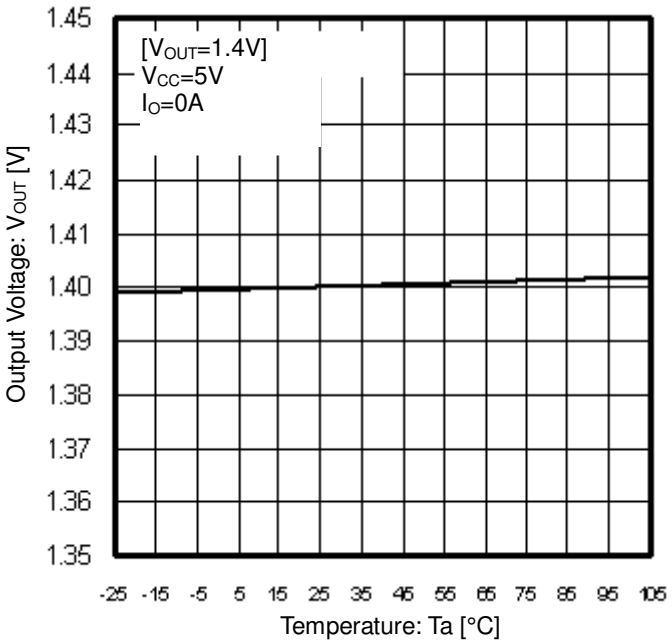


Figure 58. Output Voltage vs Temperature

Typical Performance Curves – continued

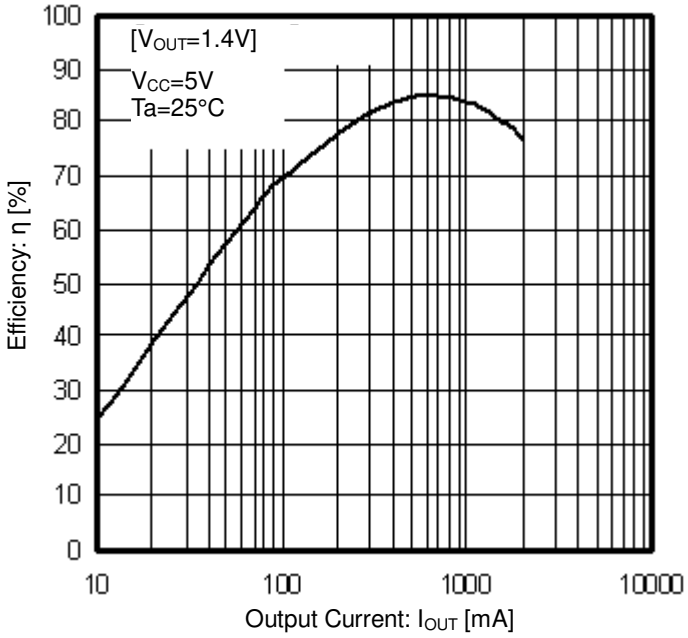


Figure 59. Efficiency vs Output Current

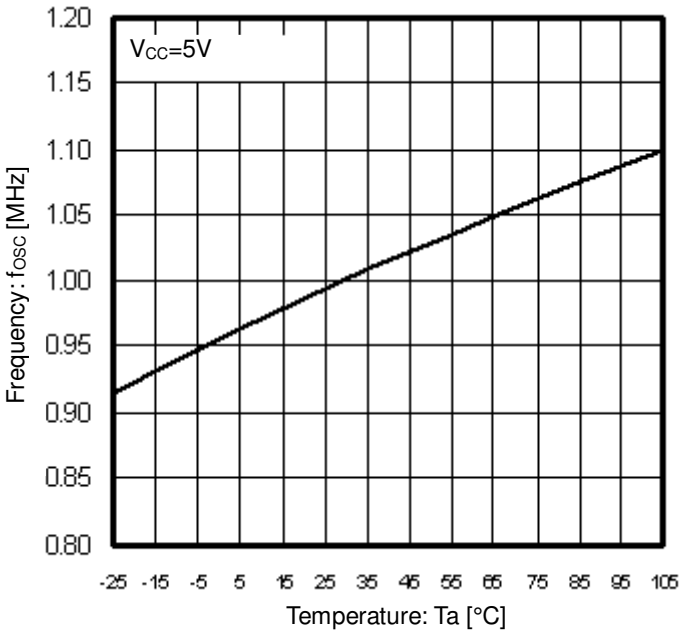


Figure 60. Frequency vs Temperature

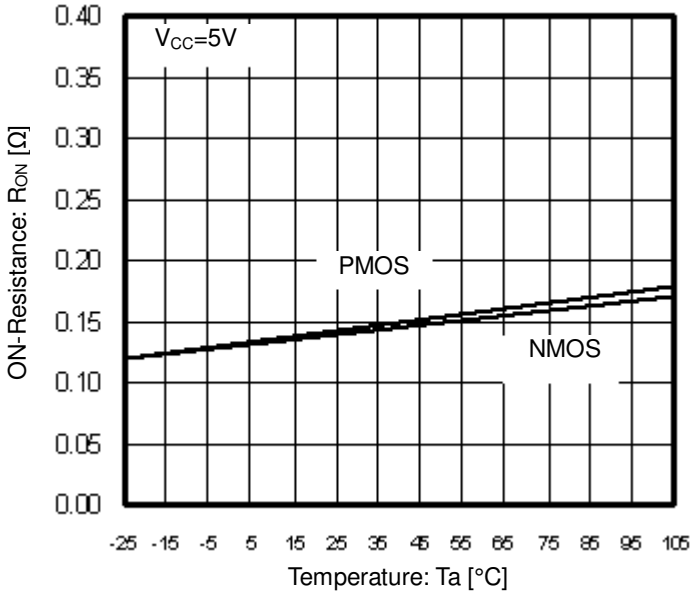


Figure 61. ON-Resistance vs Temperature

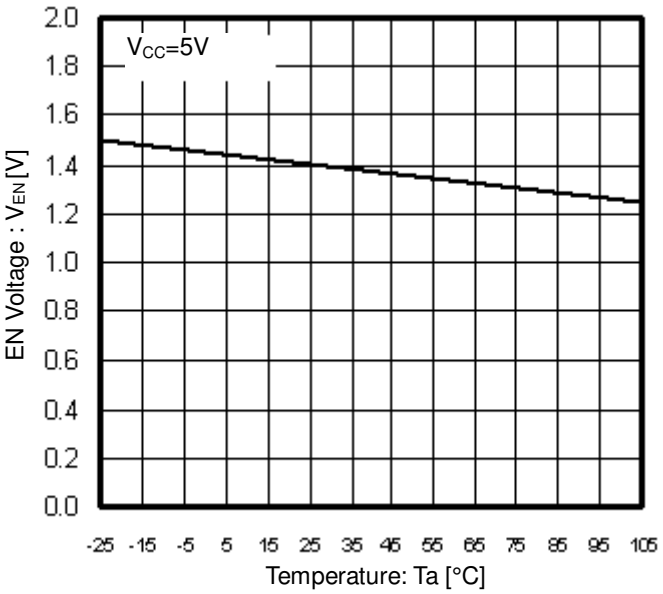


Figure 62. EN Voltage vs Temperature

Typical Performance Curves – continued

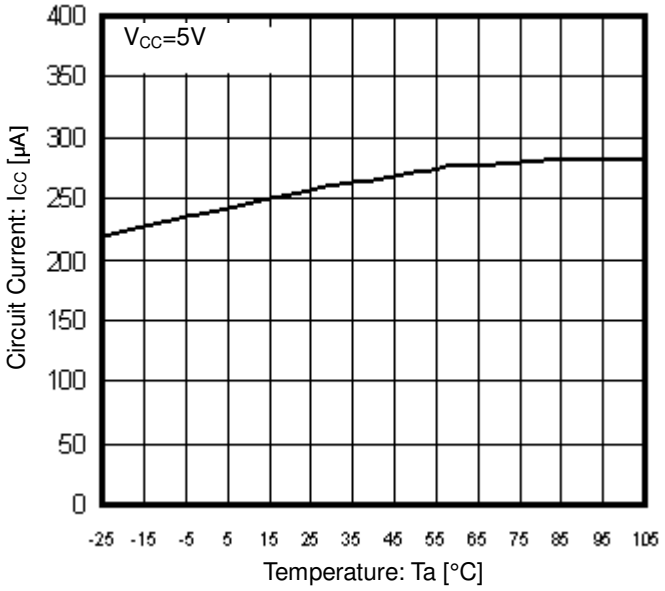


Figure 63. Circuit Current vs Temperature

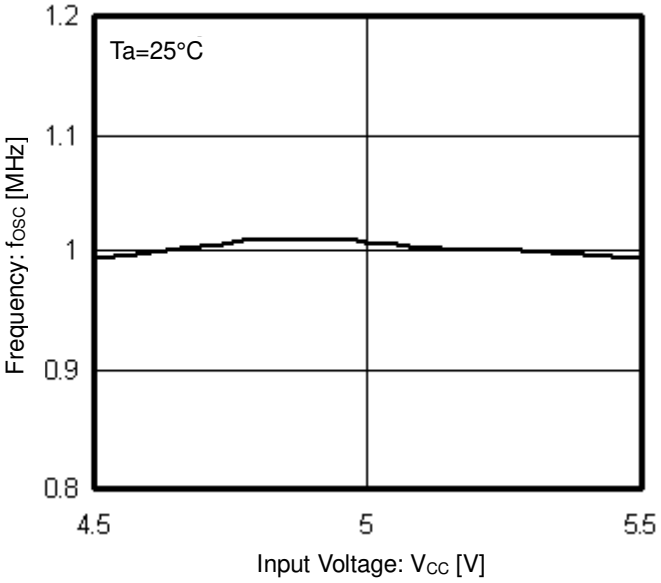


Figure 64. Frequency vs Input Voltage

Typical Waveforms

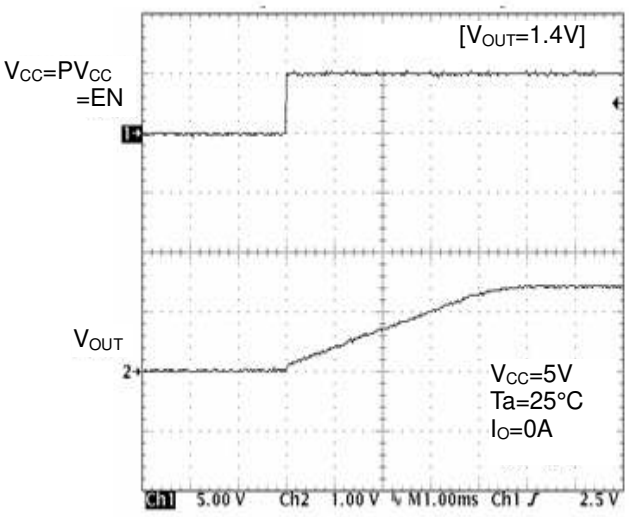


Figure 65. Soft Start Waveform

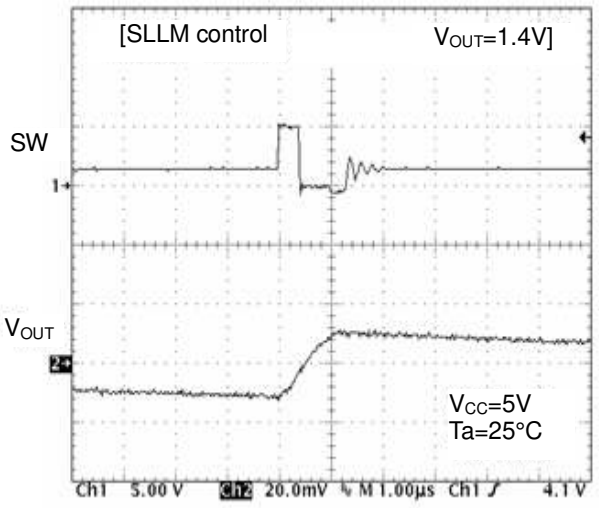


Figure 66. SW Waveform
(I_O=10mA)

Typical Waveforms – continued

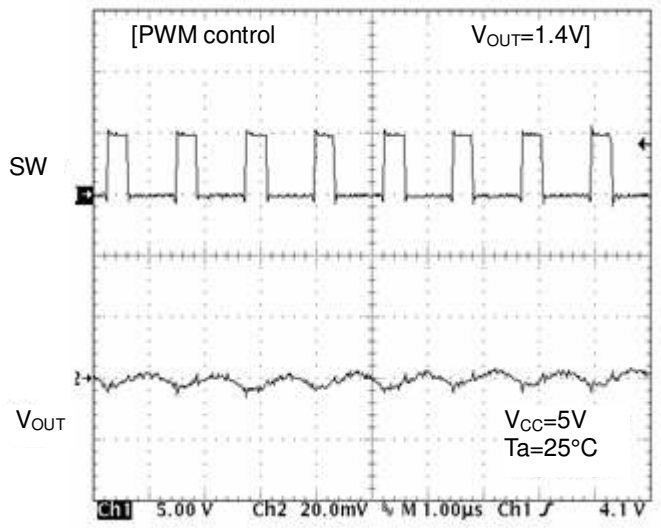


Figure 67. SW Waveform
(I_O=500mA)

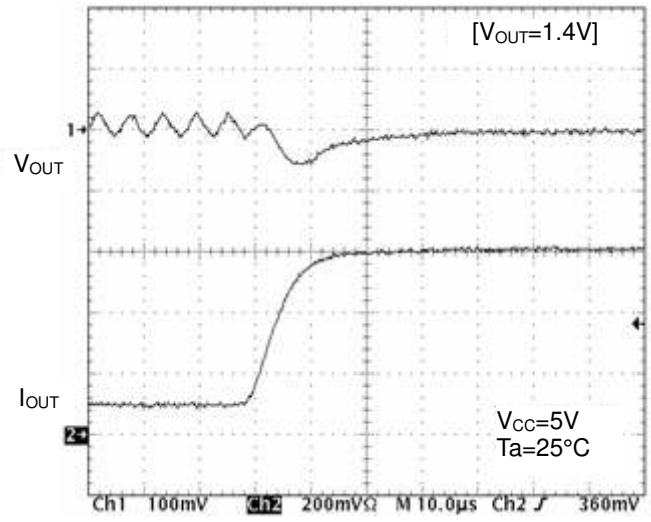


Figure 68. Transient Response
(I_O=100mA to 600mA, 10µs)

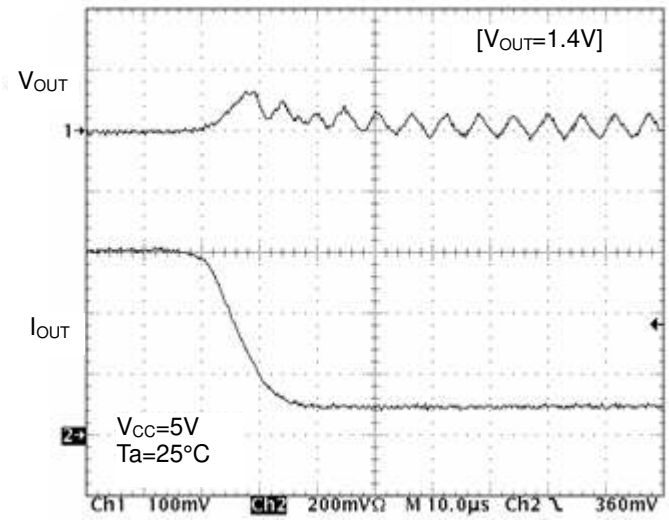


Figure 69. Transient Response
(I_O=600mA to 100mA, 10µs)

Typical Performance Curves

[BD9120HFN]

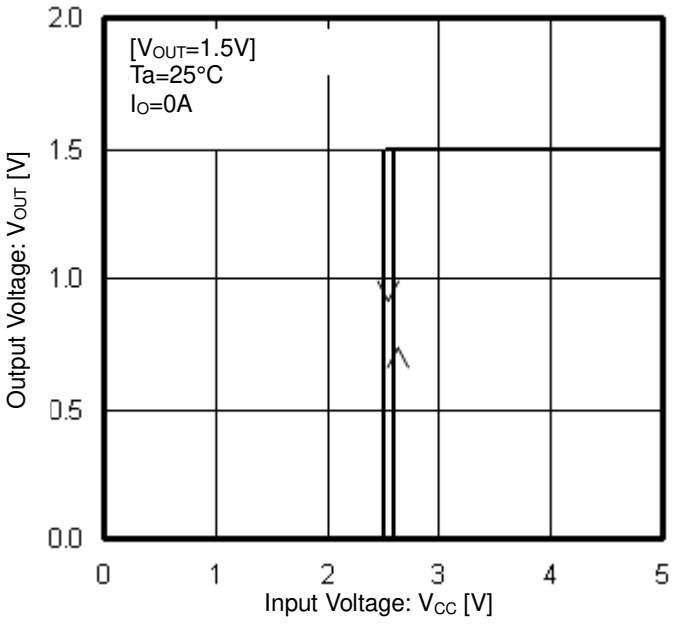


Figure 70. Output Voltage vs Input Voltage

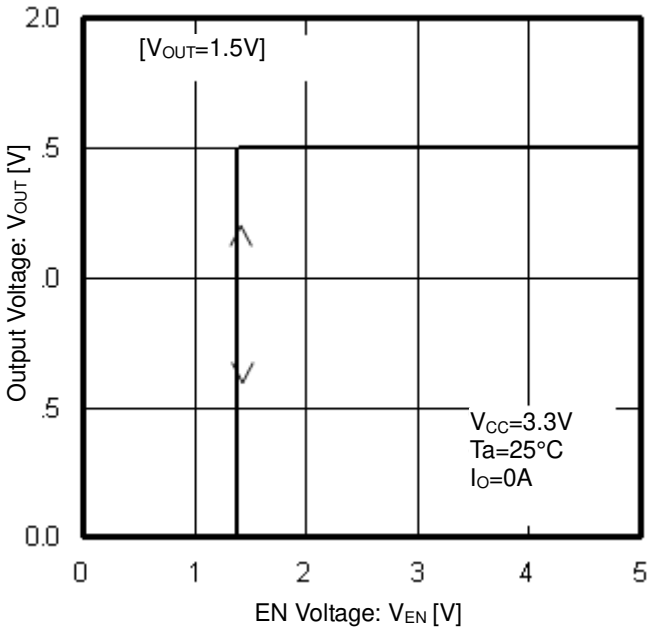


Figure 71. Output Voltage vs EN Voltage

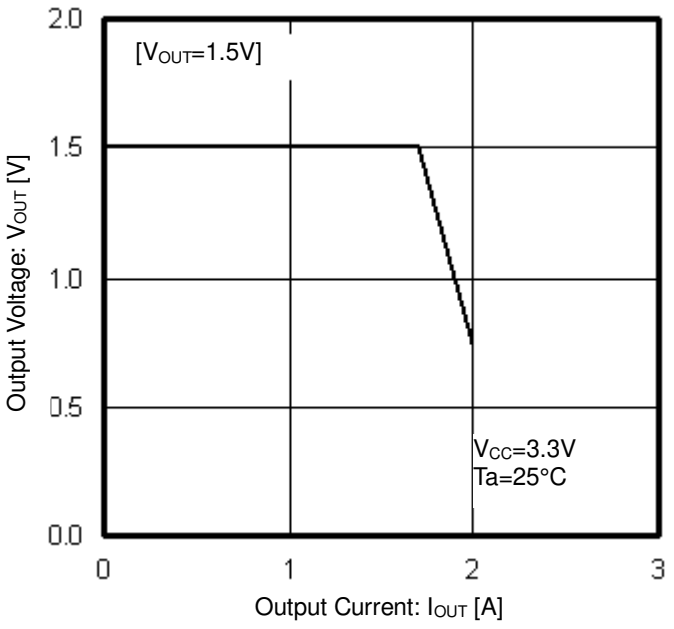


Figure 72. Output Voltage vs Output Current

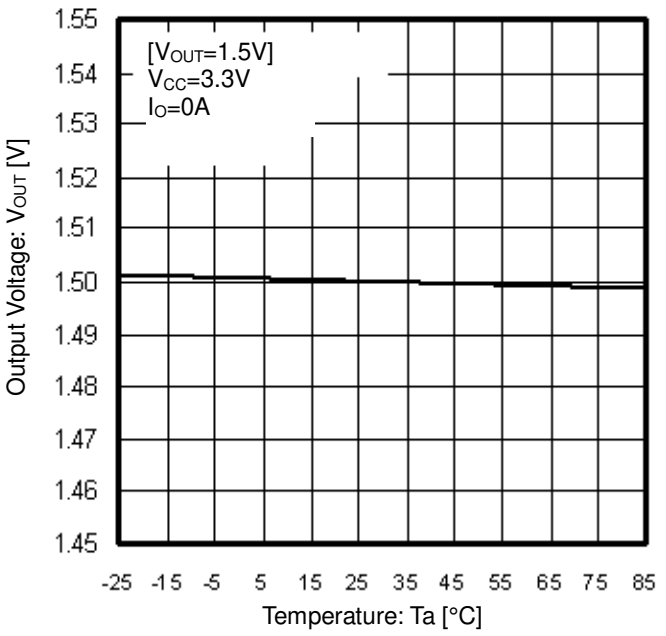


Figure 73. Output Voltage vs Temperature

Typical Performance Curves – continued

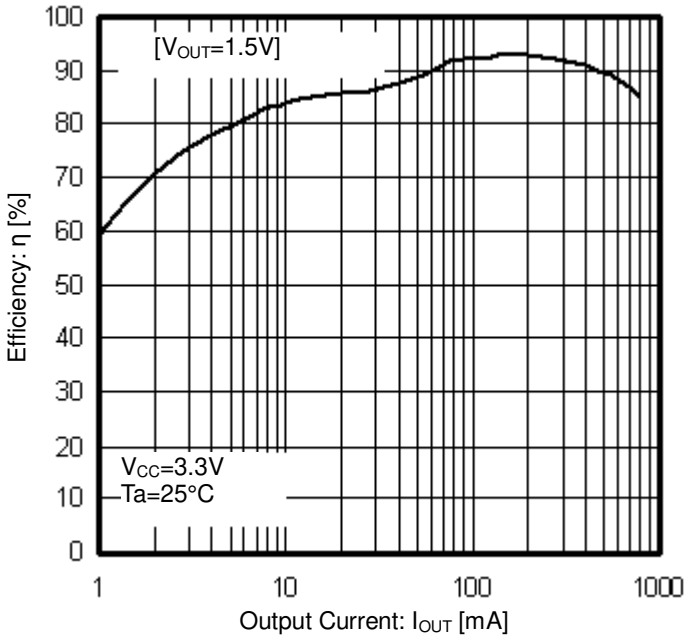


Figure 74. Efficiency vs Output Current

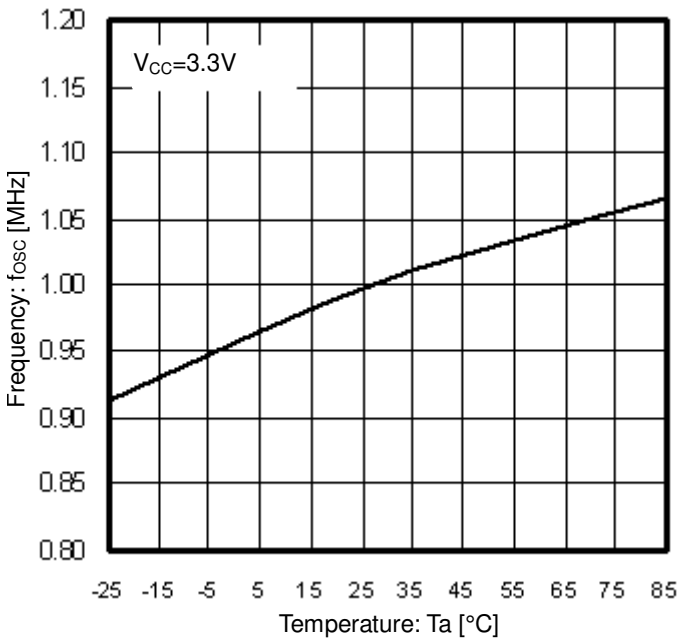


Figure 75. Frequency vs Temperature

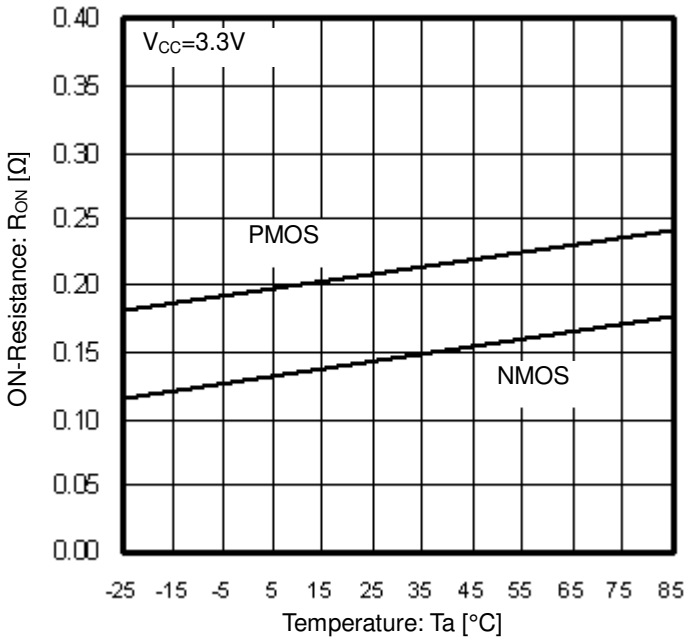


Figure 76. ON-Resistance vs Temperature

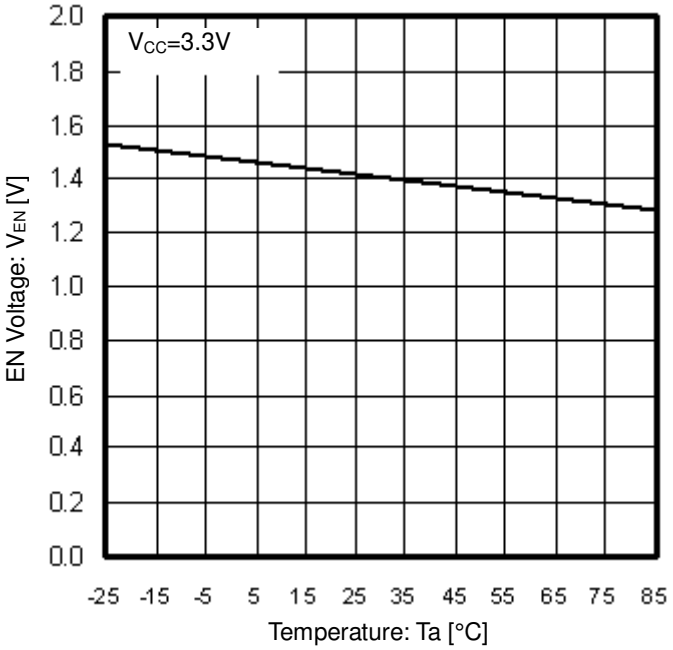


Figure 77. EN Voltage vs Temperature

Typical Performance Curves – continued

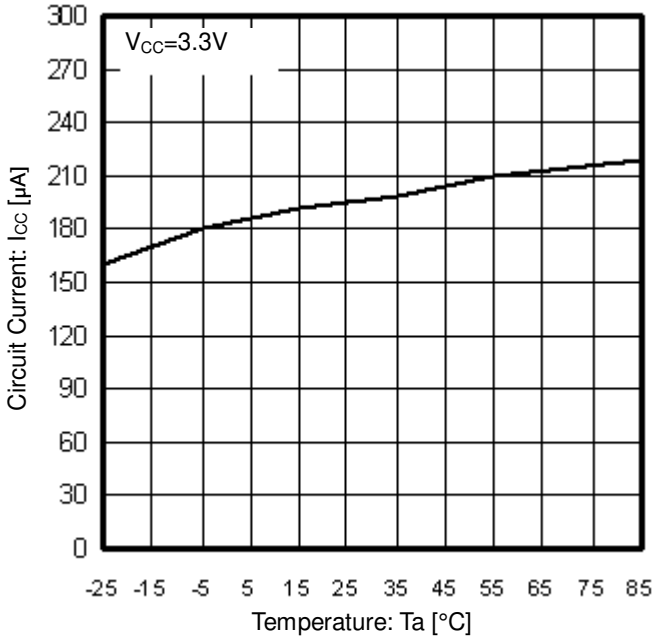


Figure 78. Circuit Current vs Temperature

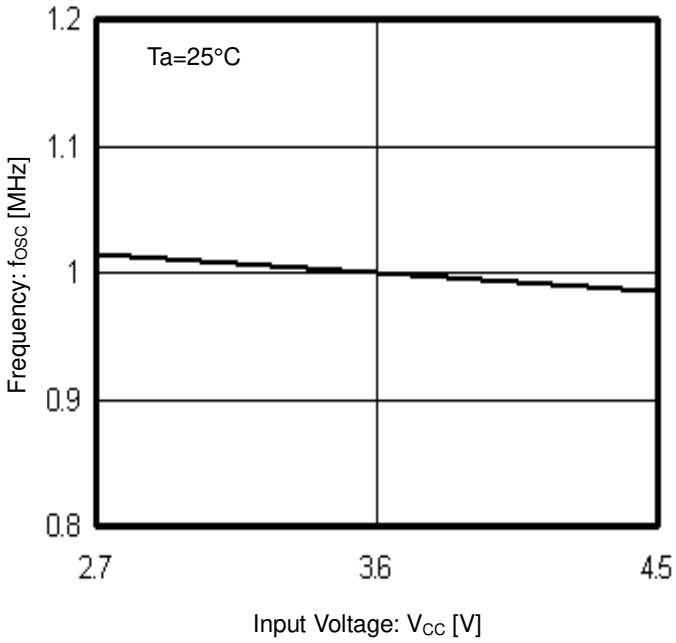


Figure 79. Frequency vs Input Voltage

Typical Waveforms

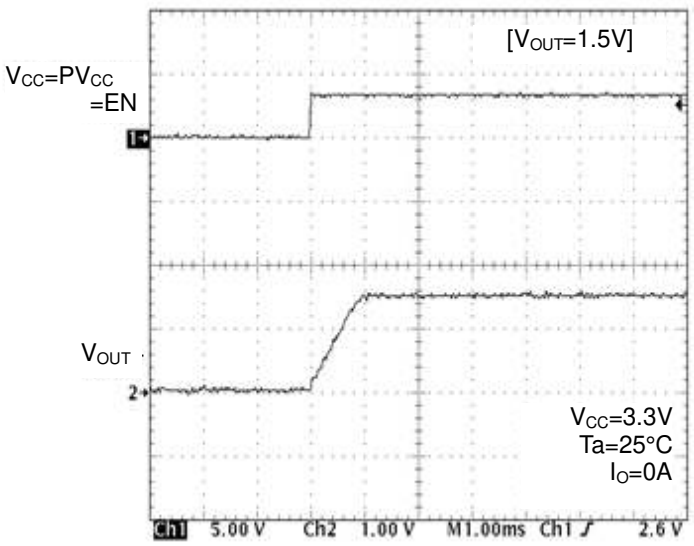


Figure 80. Soft Start Waveform

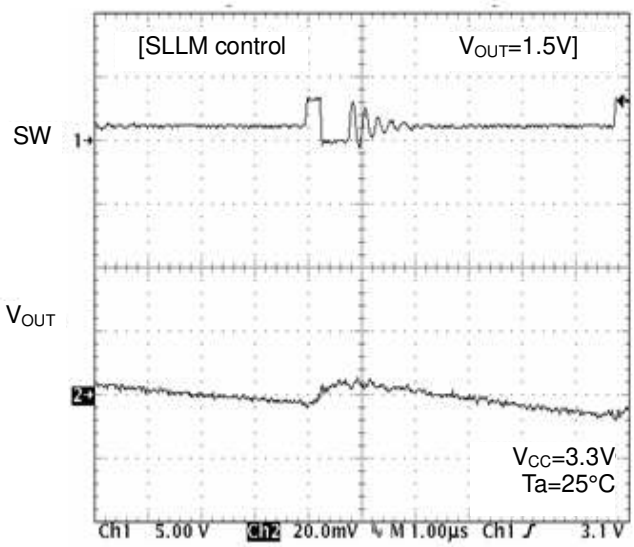


Figure 81. SW Waveform
(I_O=10mA)

Typical Waveforms – continued

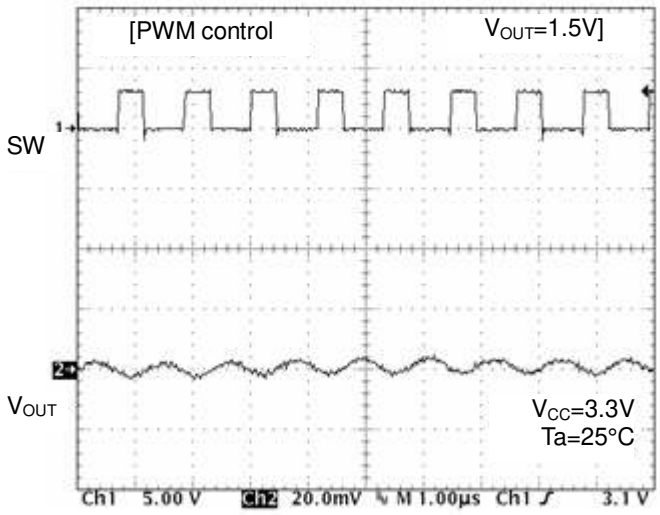


Figure 82. SW Waveform
(I_O=200mA)

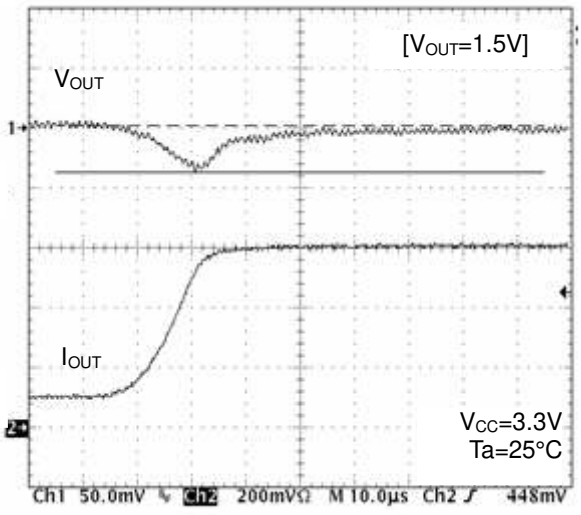


Figure 83. Transient Response
(I_O=100mA to 600mA, 10µs)

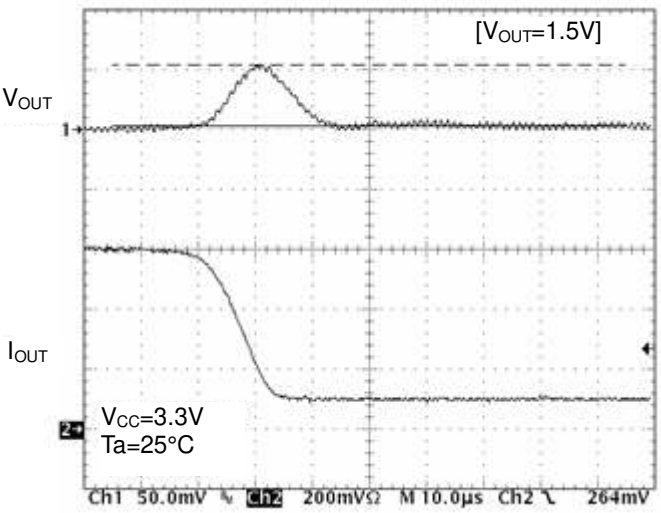


Figure 84. Transient Response
(I_O=600mA to 100mA, 10µs)

Application Information

1. Operation

BD9106FVM, BD9107FVM, BD9109FVM, BD9110NV, and BD9120HFN are synchronous step-down switching regulators that achieve fast transient response by employing current mode PWM control system. They utilize switching operation either in **PWM (Pulse Width Modulation) mode** for heavier load, or **SLLM™ (Simple Light Load Mode)** operation for lighter load to improve efficiency.

(1) Synchronous Rectifier

Integrated synchronous rectification using two MOSFETS reduces power dissipation and increases efficiency when compared to converters using external diodes. Internal shoot-through current limiting circuit further reduces power dissipation.

(2) Current Mode PWM Control

The PWM control signal of this IC depends on two feedback loops, the voltage feedback and the inductor current feedback.

(a) PWM (Pulse Width Modulation) Control

The clock signal coming from OSC has a frequency of 1Mhz. When OSC sets the RS latch, the P-Channel MOSFET is turned on and the N-Channel MOSFET is turned off. The opposite happens when the current comparator (Current Comp) resets the RS latch i.e. the P-Channel MOSFET is turned off and the N-Channel MOSFET is turned on. Current Comp's output is a comparison of two signals, the current feedback control signal "SENSE" which is a voltage proportional to the current IL, and the voltage feedback control signal, FB.

(b) SLLM™ (Simple Light Load Mode) control

When the control mode is shifted by PWM from heavier load to lighter load or vice versa, the switching pulse is designed to turn OFF with the device held operating in normal PWM control loop. This allows linear operation without voltage drop or deterioration in transient response during the sudden load changes. Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed such that the RESET signal is continuously sent even if the load is changed to light mode where the switching is tuned OFF and the switching pulses disappear. Activating the switching discontinuously reduces the switching dissipation and improves the efficiency.

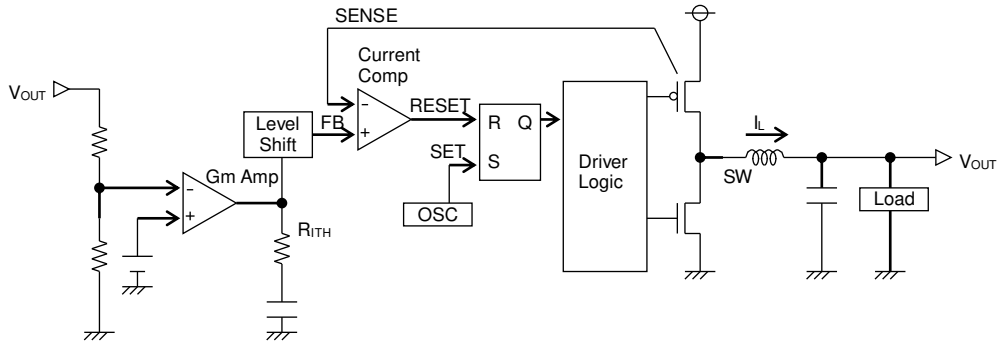


Figure 85. Diagram of Current Mode PWM Control

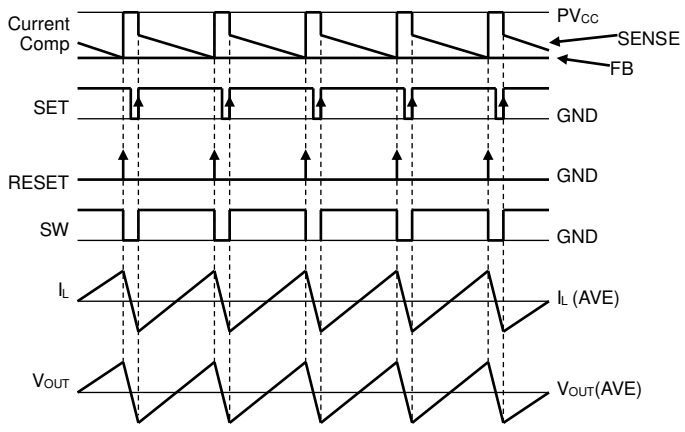


Figure 86. PWM Switching Timing Chart

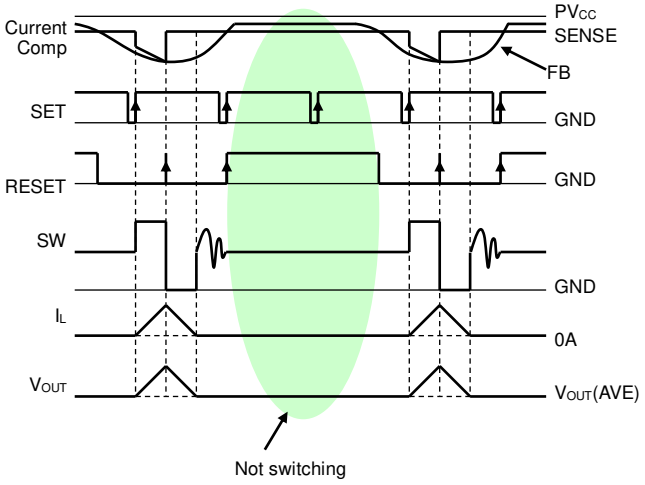


Figure 87. SLLM Switching Timing Chart

2. Description of Functions

(1) Soft-Start Function
During start-up, the soft-start circuit gradually establishes the output voltage to limit the input current. This prevents the overshoot in the output voltage and inrush current.

(2) Shutdown Function
When the EN terminal is “low”, the device operates in Standby Mode and all functional blocks, including reference voltage circuit, internal oscillator and drivers, are turned OFF. Circuit current during standby is 0μA (Typ).

(3) UVLO Function
The UVLO circuit detects whether the supplied input voltage is sufficient to obtain the output voltage of this IC. The UVLO threshold, which has a hysteresis of 50mV to 300mV (Typ), prevents output bouncing.

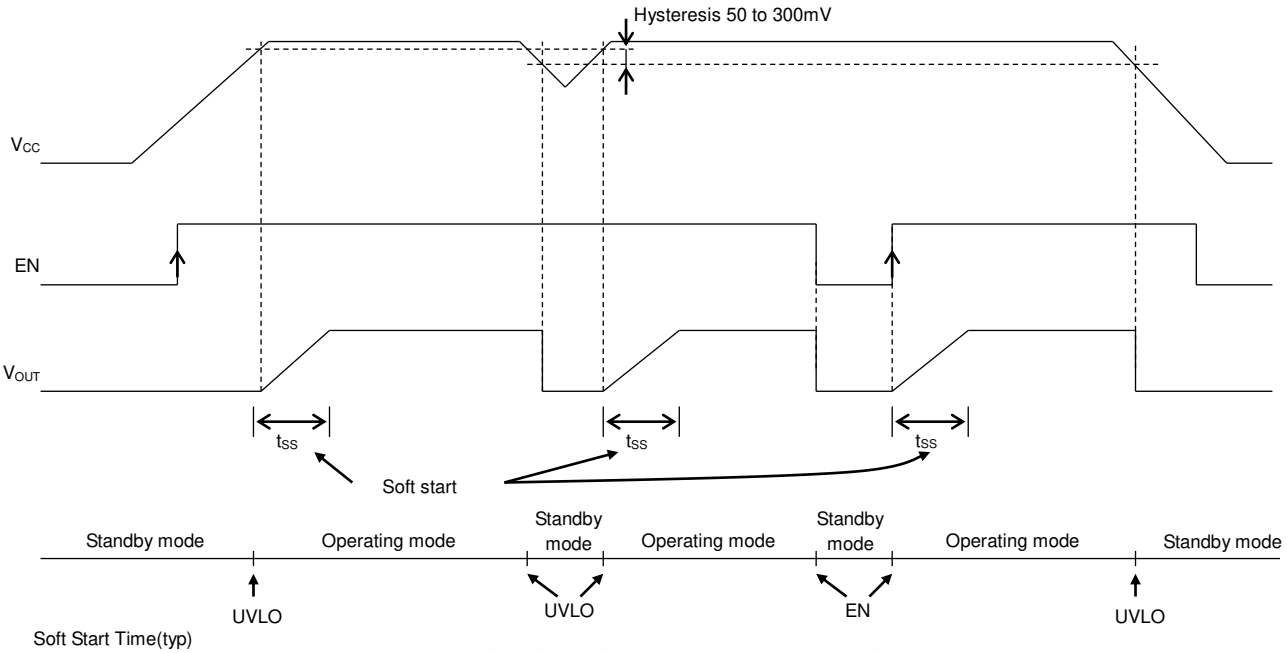


Figure 88. Soft Start, Shutdown, UVLO Timing Chart

	BD9106FVM	BD9107FVM	BD9109FVM	BD9110NV	BD9120HFN	Unit
t_{SS}	3	1	1	5	1	ms

(4) Short-circuit Protection with Time Delay Function
To protect the IC from breakdown, the short-circuit protection turns the output off when the internal current limiter is activated continuously for a fixed time (t_{LATCH}) or more. The output that is kept off may be turned on again by restarting EN or by resetting UVLO.

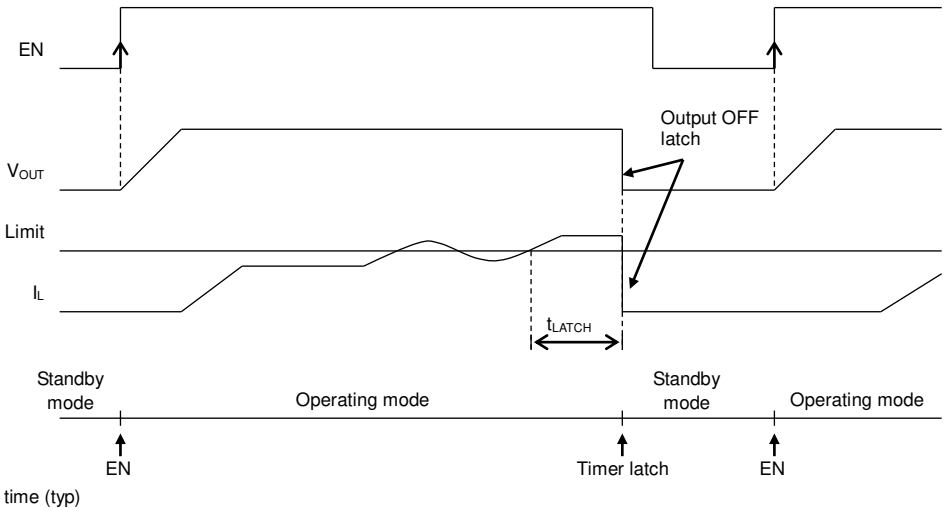


Figure 89. Short-circuit Protection with Time Delay Diagram

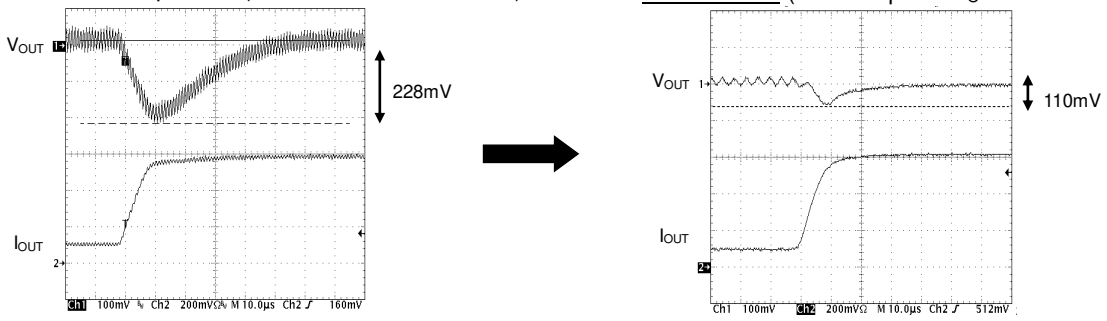
	BD9106FVM	BD9107FVM	BD9109FVM	BD9110NV	BD9120HFN	Unit
t_{LATCH}	1	1	2	1	2	ms

Note: In addition to current limit circuit, output short detect circuit is built-in on BD9109FVM and BD9120HFN. If output voltage falls below 2V(typ, BD9109FVM) or V_{OUT}x0.5(typ,BD9120HFN), output voltage will hold turned OFF.

3. Information on Advantages

Advantage 1 : Offers fast transient response by using current mode control system

Conventional product (V_{OUT} of which is 3.3 volts) BD9109FVM (Load response I_O=100mA to 600mA)



Voltage drop due to sudden change in load was reduced by about 50%.

Figure 90. Comparison of Transient Response

Advantage 2 : Offers high efficiency for all load ranges.

(1) For lighter load:
This IC utilizes the current mode control called SLLM™, which reduces various dissipations such as switching dissipation (P_{SW}), gate charge/discharge dissipation, ESR dissipation of output capacitor (P_{ESR}) and ON-Resistance dissipation (P_{RON}) that may otherwise cause reduction in efficiency.

↓

Achieves efficiency improvement for lighter load.

(2) For heavier load:
This IC utilizes the synchronous rectifying mode and uses low ON-Resistance MOSFET power transistors.

{ ON-Resistance of High side MOSFET: 200mΩ to 350mΩ (Typ)
{ ON-Resistance of Low side MOSFET: 150mΩ to 250mΩ (Typ)

↓

Achieves efficiency improvement for heavier load.
Offers high efficiency for all load ranges with the improvements mentioned above.

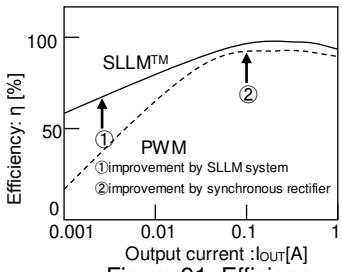


Figure 91. Efficiency

Advantage 3 : ·Supplied in smaller package due to small-sized power MOSFETs.
(3 packages are MOSP8, HSON8, SON008V5060)
·Allows reduction in size of application products

↓

Reduces mounting area required.

{ ·Output capacitor C_O required for current mode control: 10 µF ceramic capacitor
{ ·Inductance L required for the operating frequency of 1 MHz: 4.7 µH inductor
(BD9110NV: Co=22µF, L=2.2µH)

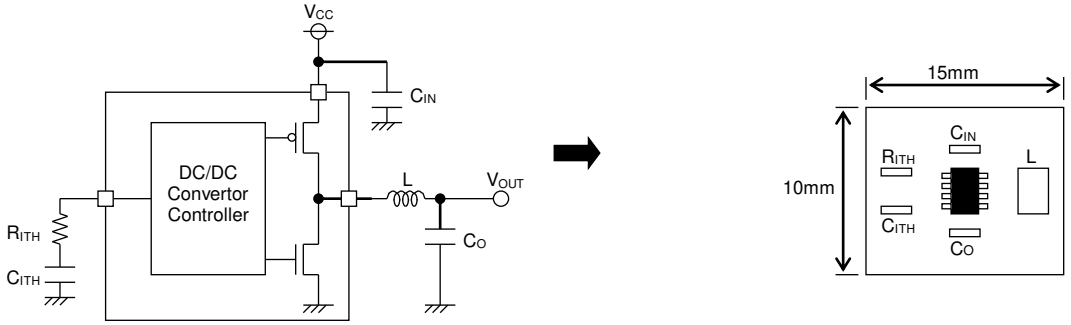


Figure 92. Example Application

4. Switching Regulator Efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{P_{OUT}}{P_{OUT} + Pd\alpha} \times 100 \quad [\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors Pdα as follows:

Dissipation factors:

(1) ON-Resistance Dissipation of Inductor and FET : Pd(I^2R)

$$Pd(I^2R) = {I_{OUT}}^2 \times (R_{COIL} + R_{ON})$$

Where:
R_{COIL} is the DC resistance of inductor
R_{ON} is the ON-Resistance of FET
I_{OUT} is the output current

(2) Gate Charge/Discharge Dissipation : Pd(Gate)

$$Pd(GATE) = C_{gs} \times f \times V^2$$

Where:
C_{gs} is the gate capacitance of FET
f is the switching frequency
V is the gate driving voltage of FET

(3) Switching Dissipation : Pd(SW)

$$Pd(SW) = \frac{{V_{IN}}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$$

Where:
C_{RSS} is the reverse transfer capacitance of FET
I_{DRIVE} is the peak current of gate

(4) ESR Dissipation of Capacitor : Pd(ESR)

$$Pd(ESR) = {I_{RMS}}^2 \times ESR$$

Where:
I_{RMS} is the ripple current of capacitor
ESR is the equivalent series resistance

(5) Operating Current Dissipation of IC : Pd(IC)

$$Pd(IC) = V_{IN} \times I_{CC}$$

Where:
I_{CC} is the circuit current

5. Consideration on Permissible Dissipation and Heat Generation

Since these ICs function with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON-Resistance of FET are considered. This is because conduction losses are the most significant among other dissipations mentioned above, such as gate charge/discharge dissipation and switching dissipation.

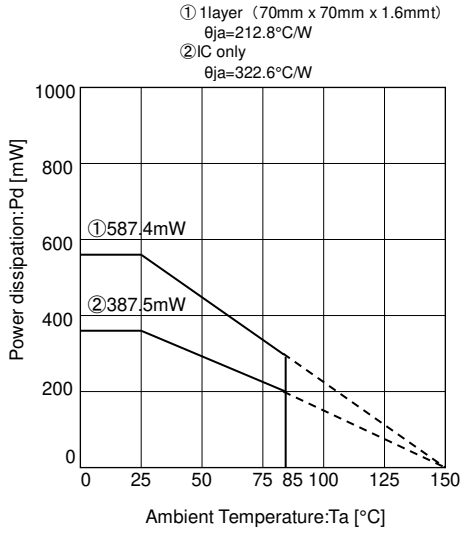


Figure 93. Thermal Derating Curve (MSOP8)

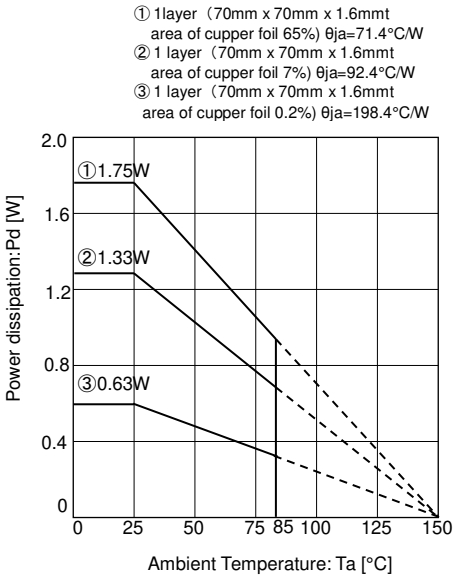


Figure 94. Thermal Derating Curve (HSON8)

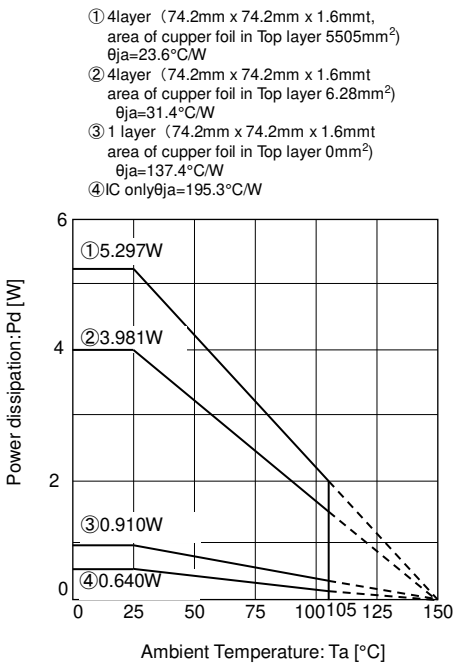


Figure 95. Thermal Derating Curve (SON008V5060)

If V_{CC}=5V, V_{OUT}=3.3V, R_{COIL}=0.15Ω, R_{ONP}=0.35Ω, R_{ONN}=0.25Ω
I_{OUT}=0.8A, for example,

$D=V_{OUT}/V_{CC}=3.3/5=0.66$

$R_{ON}=0.66\times0.35+(1-0.66)\times0.25$
$=0.231+0.085$
$=0.316[\Omega]$

$$P = 0.8^2 \times (0.15 + 0.316)$$
$$\approx 298[mV]$$

$$P = I_{OUT}{}^2 \times (R_{COIL} + R_{ON})$$
$$R_{ON} = D \times R_{ONP} + (1 - D) \times R_{ONN}$$

Where:
D is the ON duty ($=V_{OUT}/V_{CC}$)
R_{COIL} is the DC resistance of coil
R_{ONP} is the ON-Resistance of P-channel MOS FET
R_{ONN} is the ON-Resistance of N-channel MOS FET
I_{OUT} is the Output current

Since R_{ONP} is greater than R_{ONN} in these ICs, the dissipation increases as the ON duty becomes greater. Taking into consideration the dissipation shown above, thermal design must be carried out with allowable sufficient margin.

6. Selection of Components Externally Connected

(1) Selection of inductor (L)

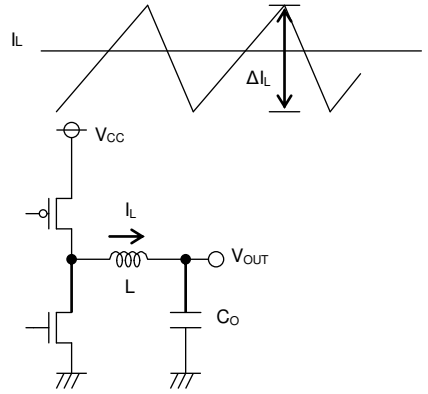


Figure 96. Output Ripple Current

The inductance significantly depends on output ripple current. As seen in equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \quad [A] \quad \cdots(1)$$

Appropriate ripple current at output should be +/-30% of the maximum output current.

$$\Delta I_L = 0.3 \times I_{OUTMax} \quad [A] \quad \cdots(2)$$

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \quad [H] \quad \cdots(3)$$

Where:
ΔI_L is the Output ripple current, and
f is the Switching frequency

Note: Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency.
The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5V, V_{OUT}=3.3V, f=1MHz, ΔI_L=0.3x0.8A=0.24A, for example, (BD9109FVM)

$$L = \frac{(5 - 3.3) \times 3.3}{0.24 \times 5 \times 1M} = 4.675\mu \rightarrow 4.7 \quad [\mu H]$$

Note: Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

(2) Selection of Output Capacitor (C_O)

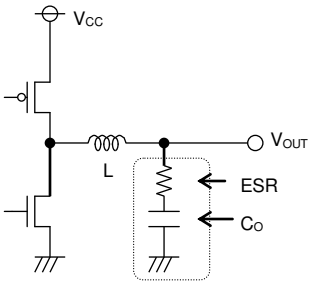


Figure 97. Output Capacitor

Output capacitor should be selected with the consideration of the stability region and the equivalent series resistance required to minimize ripple voltage.

Output ripple voltage is determined by the equation (4):

$$\Delta V_{OUT} = \Delta I_L \times ESR \quad [V] \quad \cdots(4)$$

Where:
ΔI_L is the Output ripple current, and
ESR is the Equivalent series resistance of output capacitor

Note: Rating of the capacitor should be determined allowing sufficient margin against output voltage.
Less ESR allows reduction in output ripple voltage.

The output rise time must be designed to fall within the soft-start time, and the capacitance of output capacitor should be determined with consideration on the requirements of equation (5):

$$C_O \leq \frac{t_{SS} \times (I_{LIMIT} - I_{OUT})}{V_{OUT}} \quad \cdots(5)$$

Where:
t_{SS}: Soft-Start time
I_{LIMIT}: Over current detection level, 2A(Typ)

In case of BD9109FVM, for instance, and if V_{OUT}=3.3V, I_{OUT}=0.8A, and t_{SS}=1ms,

$$C_O \leq \frac{1m \times (2 - 0.8)}{3.3} \approx 364 \quad [\mu F]$$

Inappropriate capacitance may cause problem in startup. A 10µF to 100µF ceramic capacitor is recommended.

(3) Selection of Input Capacitor (C_{IN})

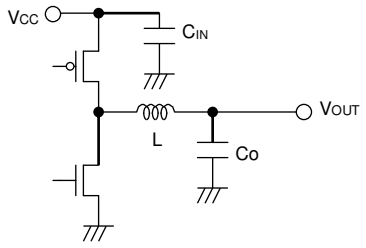


Figure 98. Input Capacitor

Input capacitor must be a low ESR capacitor with a capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current I_{RMS} is given by the equation (6):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}} \quad [\mathrm{A}] \cdots (6)$$

< Worst case > I_{RMSMax}

When V_{CC} is twice the V_{OUT}, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=3.3V, and I_{OUTMax}=0.8A, (BD9109FVM)

$$I_{RMS} = 0.8 \times \frac{\sqrt{3.3(5-3.3)}}{5} = 0.38 \quad [A_{RMS}]$$

A low ESR 10µF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

(4) Determination of R_{ITH}, C_{ITH} for Phase Compensation

As the Current Mode Control is designed to limit the inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of an output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

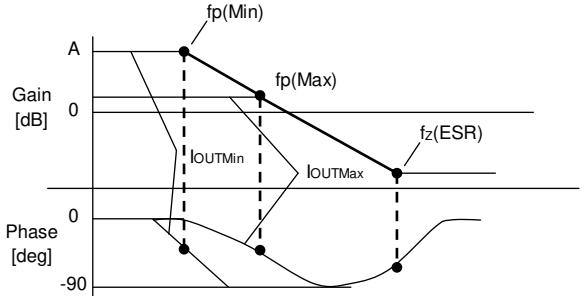


Figure 99. Open Loop Gain Characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$f_{Z(ESR)} = \frac{1}{2\pi \times ESR \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency decreases.

$$fp(Min) = \frac{1}{2\pi \times R_{OMax} \times C_O} \quad [Hz] \leftarrow with\ lighter\ load$$

$$fp(Max) = \frac{1}{2\pi \times R_{OMin} \times C_O} \quad [Hz] \leftarrow with\ heavier\ load$$

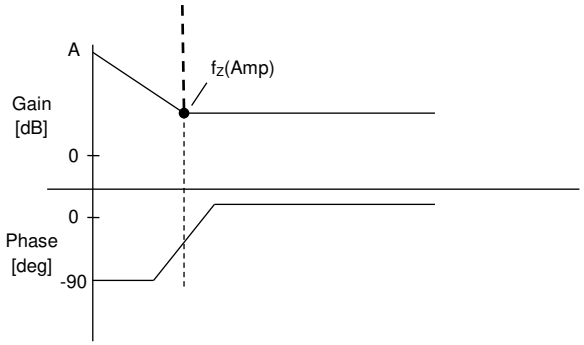


Figure 100. Error Amp Phase Compensation Characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR is reduced to half.)

$$f_Z(Amp) = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

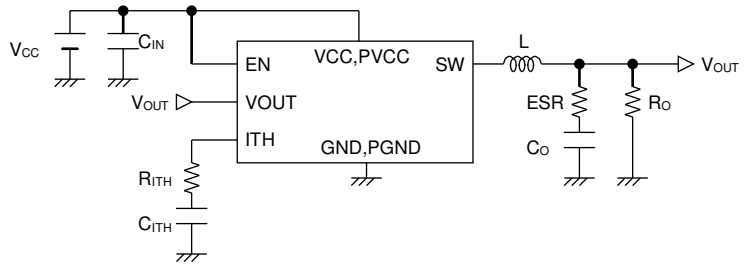


Figure 101. Typical Application

Stable feedback loop may be achieved by canceling the pole fp (Min) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz(Amp) = fp(Min)$$

$$\longrightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax} \times C_O}$$

(5) Setting the Output Voltage (except for BD9109FVM)

The output voltage V_{OUT} is determined by the equation (7):

$$V_{OUT} = (R_2 / R_1 + 1) \times V_{ADJ} \quad \cdots (7)$$

Where:
V_{ADJ} is the Voltage at ADJ terminal (0.8V Typ)

The required output voltage may be determined by adjusting R_1 and R_2.

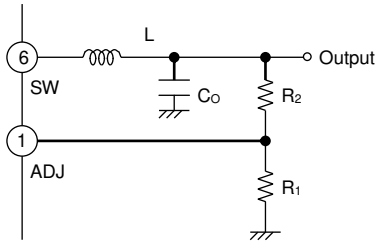


Figure 102. Determination of Output Voltage

{ Adjustable output voltage range : 1.0V to 1.5V/ BD9107FVM, BD9120HFN
1.0V to 2.5V/BD9106FVM, BD9110NV }

Use 1 kΩ to 100 kΩ resistor for R_1. If a resistor with resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage, etc.

7. Cautions on PC Board Layout

BD9106FVM, BD9107FVM, BD9109FVM, BD9120HFN

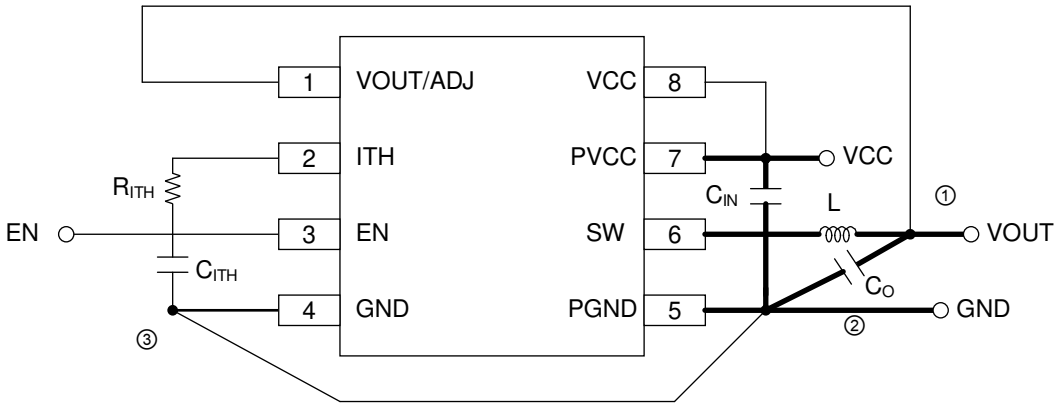


Figure 103. Layout Diagram

BD9110NV

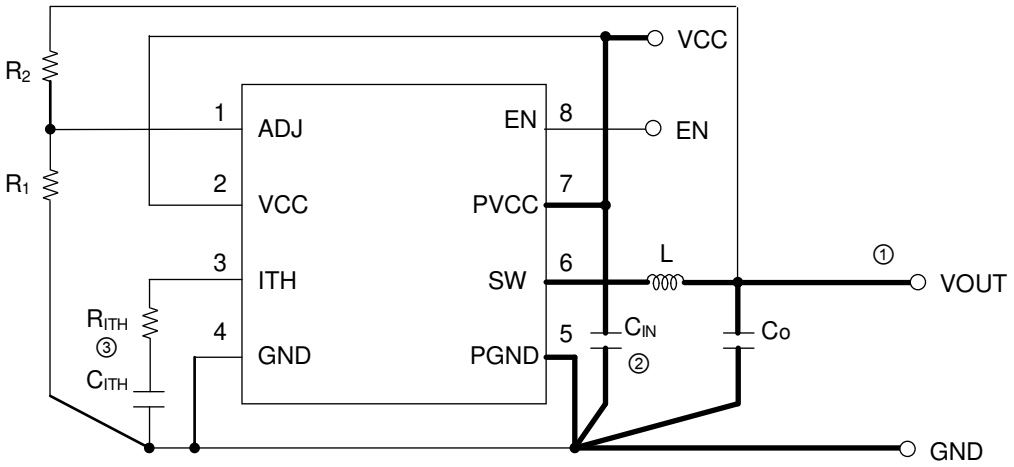


Figure 104. Layout Diagram

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.

② Lay out the input ceramic capacitor C_{IN} closer to the pins PVCC and PGND, and the output capacitor C_O closer to the pin PGND.

③ Lay out C_{ITH} and R_{ITH} between the pins ITH and GND as neat as possible with least necessary wiring.

Note: The package of HSON8 (BD9120HFN) and SON008V5050 (BD9110NV) has thermal FIN on the reverse of the package. The package thermal performance may be enhanced by bonding the FIN to GND plane which take a large area of PCB.

8. Recommended Components Lists On Above Application

[BD9106FVM]

Symbol	Part	Value		Manufacturer	Series
L	Coil	4.7μH		Sumida	CMD6D11B
				TDK	VLF5014AT-4R7M1R1
C_{IN}	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_O	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_{ITH}	Ceramic capacitor	750pF		Murata	GRM18series
R_{ITH}	Resistance	V_{OUT}=1.0V	18kΩ	ROHM	MCR10 1802
		V_{OUT}=1.2V	22kΩ	ROHM	MCR10 2202
		V_{OUT}=1.5V	22kΩ	ROHM	MCR10 2202
		V_{OUT}=1.8V	27kΩ	ROHM	MCR10 2702
		V_{OUT}=2.5V	36kΩ	ROHM	MCR10 3602

[BD9107FVM]

Symbol	Part	Value		Manufacturer	Series
L	Coil	4.7μH		Sumida	CMD6D11B
				TDK	VLF5014AT-4R7M1R1
C_{IN}	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_O	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_{ITH}	Ceramic capacitor	1000pF		Murata	GRM18series
R_{ITH}	Resistance	V_{OUT}=1.0V	4.3kΩ	ROHM	MCR10 4301
		V_{OUT}=1.2V	6.8kΩ	ROHM	MCR10 6801
		V_{OUT}=1.5V	9.1kΩ	ROHM	MCR10 9101
		V_{OUT}=1.8V	12kΩ	ROHM	MCR10 1202

[BD9109FVM]

Symbol	Part	Value	Manufacturer	Series
L	Coil	4.7μH	Sumida	CMD6D11B
			TDK	VLF5014AT-4R7M1R1
C_{IN}	Ceramic capacitor	10μF	Kyocera	CM316X5R106K10A
C_O	Ceramic capacitor	10μF	Kyocera	CM316X5R106K10A
C_{ITH}	Ceramic capacitor	330pF	Murata	GRM18series
R_{ITH}	Resistance	30kΩ	ROHM	MCR10 3002

[BD9110NV]

Symbol	Part	Value		Manufacturer	Series
L	Coil	2.2μH		TDK	LTF5022T-2R2N3R2
C_{IN}	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_O	Ceramic capacitor	22μF		Kyocera	CM316B226K06A
C_{ITH}	Ceramic capacitor	1000pF		Murata	GRM18series
R_{ITH}	Resistance	V_{OUT}=1.0V	12kΩ	ROHM	MCR10 1202
		V_{OUT}=1.2V			
		V_{OUT}=1.5V			
		V_{OUT}=1.8V			
		V_{OUT}=2.5V			

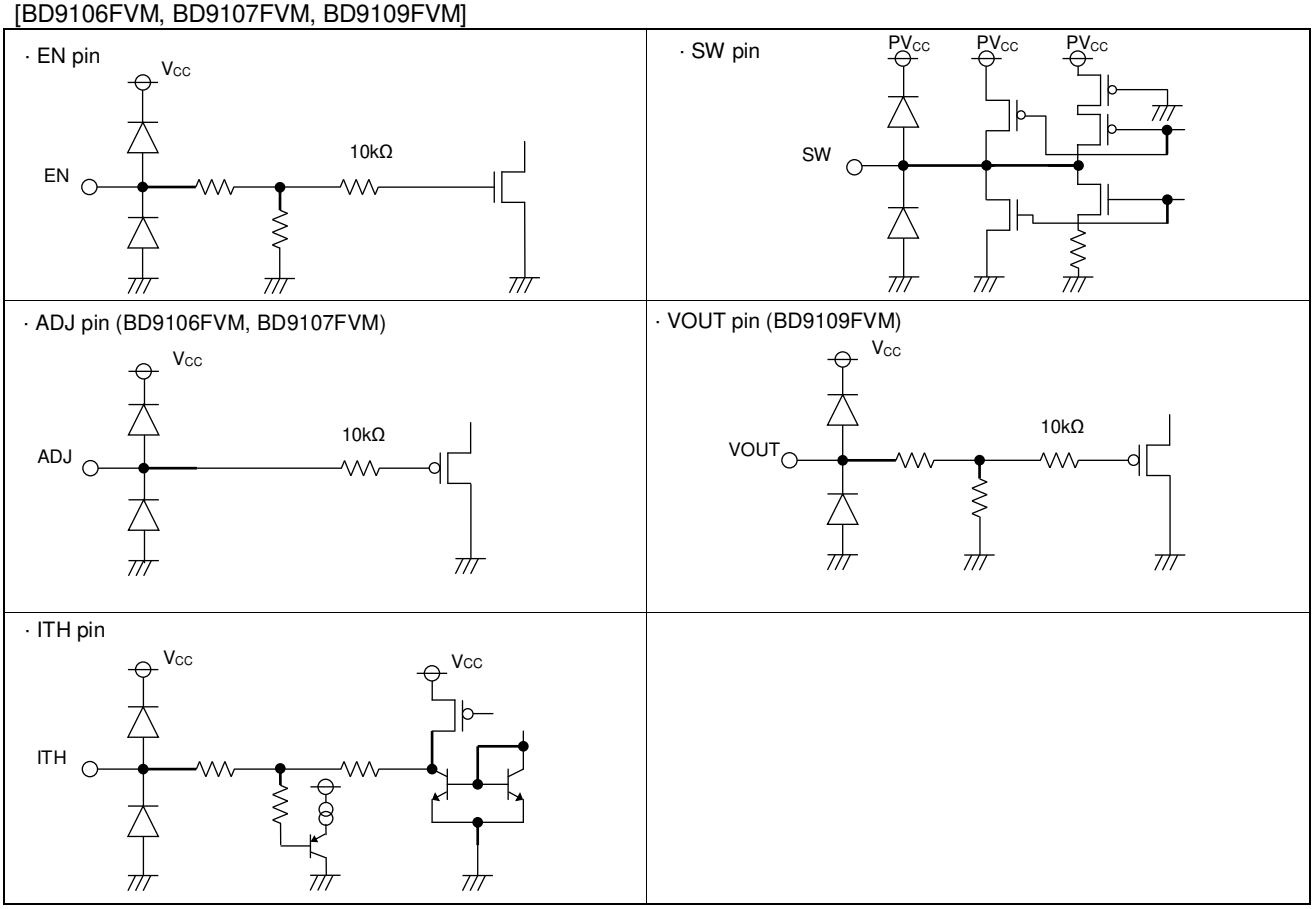
[BD9120HFN]

Symbol	Part	Value		Manufacturer	Series
L	Coil	4.7μH		Sumida	CMD6D11B
				TDK	VLF5014AT-4R7M1R1
C_{IN}	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_O	Ceramic capacitor	10μF		Kyocera	CM316X5R106K10A
C_{ITH}	Ceramic capacitor	680pF		Murata	GRM18series
R_{ITH}	Resistance	V_{OUT}=1.0V	8.2kΩ	ROHM	MCR10 8201
		V_{OUT}=1.2V	8.2kΩ	ROHM	MCR10 8201
		V_{OUT}=1.5V	4.7kΩ	ROHM	MCR10 4701

Note:The parts list presented above is an example of recommended parts. Although the parts are the same, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode established between the SW and PGND pins.

I/O Equivalent Circuit

[BD9106FVM, BD9107FVM, BD9109FVM]



[BD9110NV, BD9120HFN]

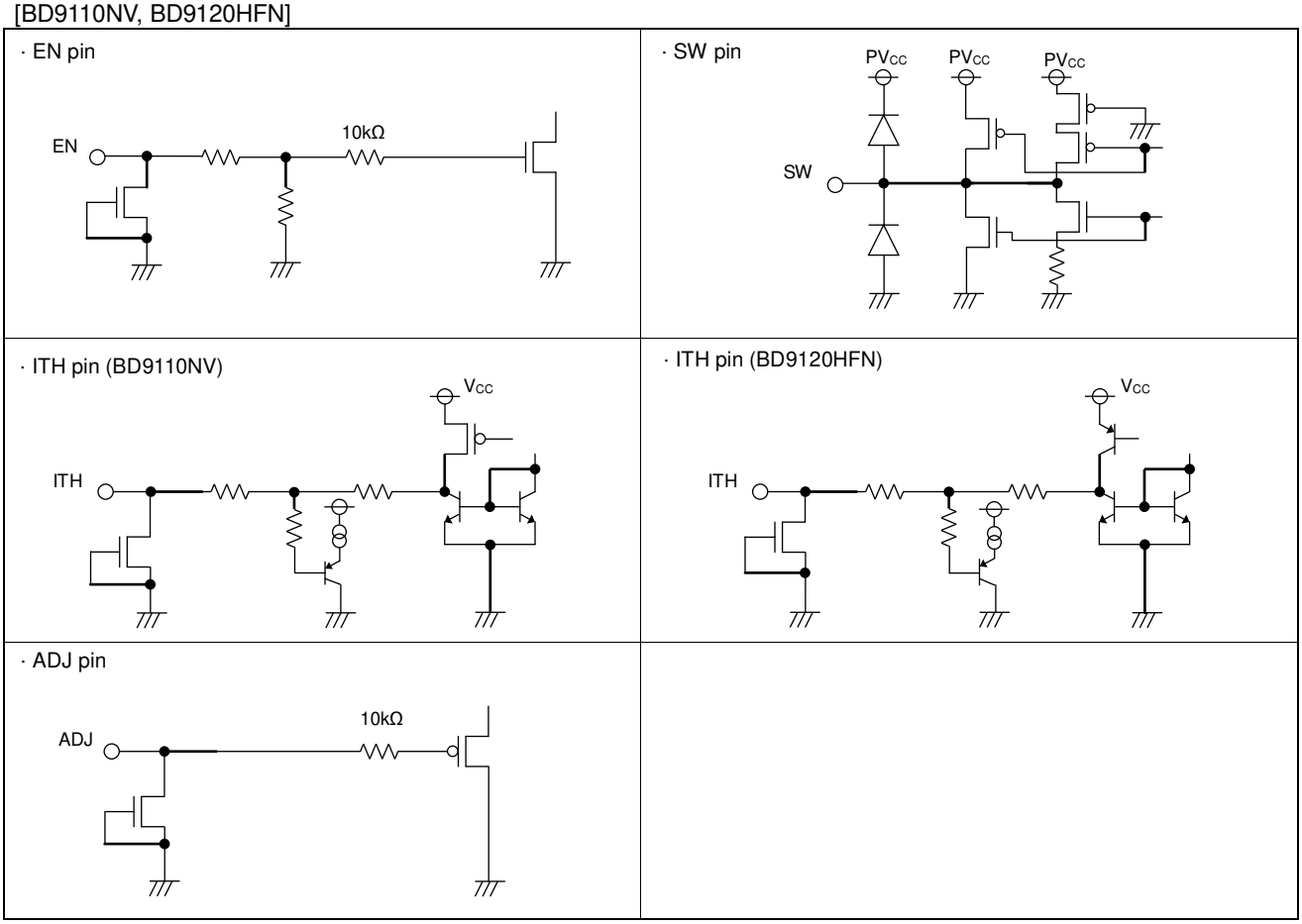


Figure 105. I/O Equivalent Circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

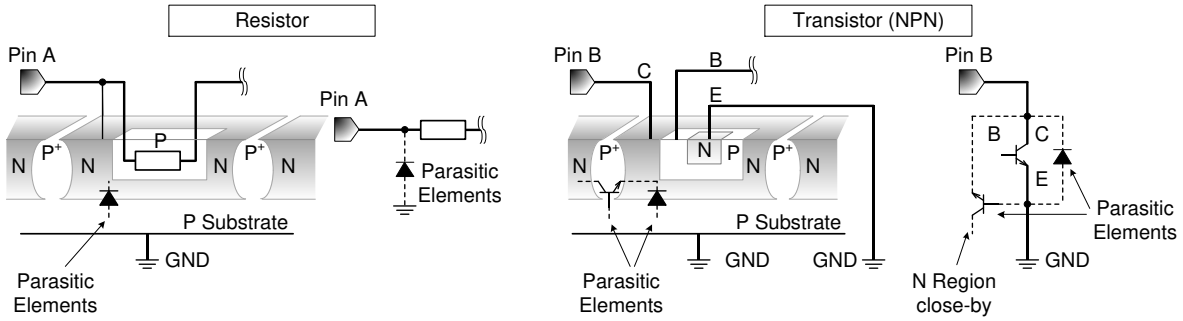
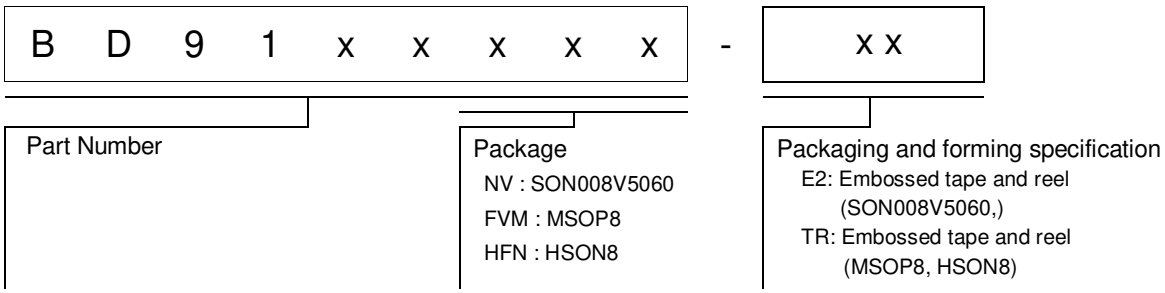


Figure 106. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

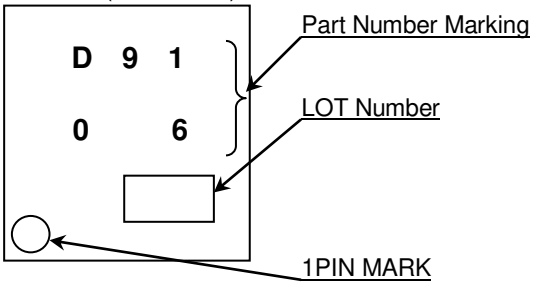
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

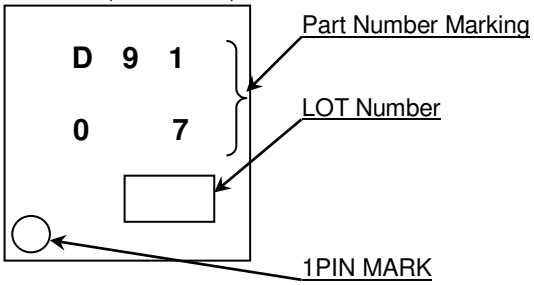


Marking Diagrams

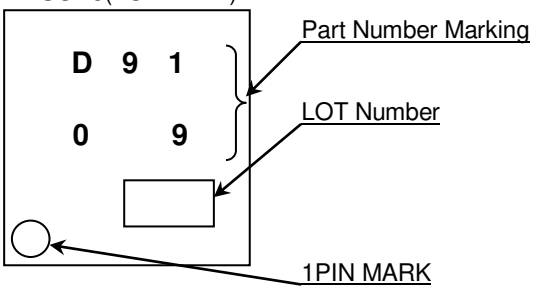
BD9106FVM
MSOP8(TOP VIEW)



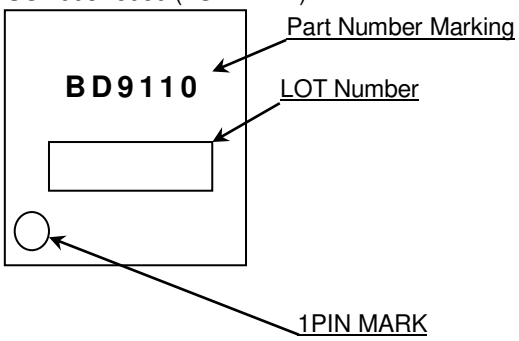
BD9107FVM
MSOP8(TOP VIEW)



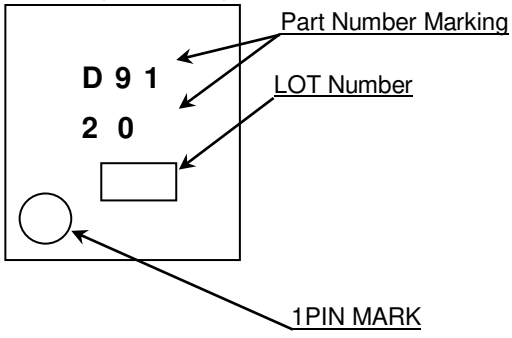
BD9109FVM
MSOP8(TOP VIEW)



BD9110NV
SON008V5060 (TOP VIEW)

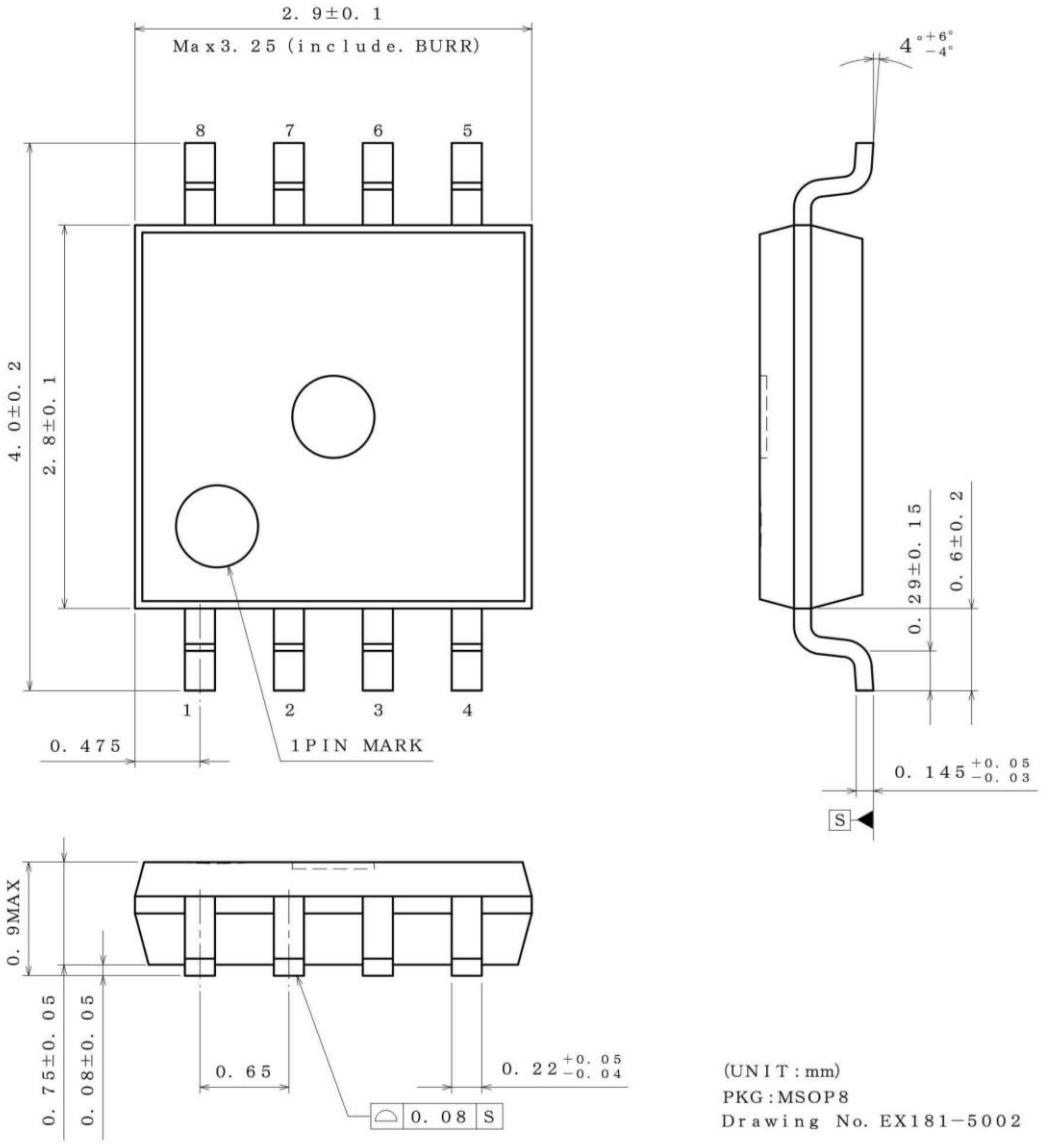


BD9120HFN
HSON8 (TOP VIEW)



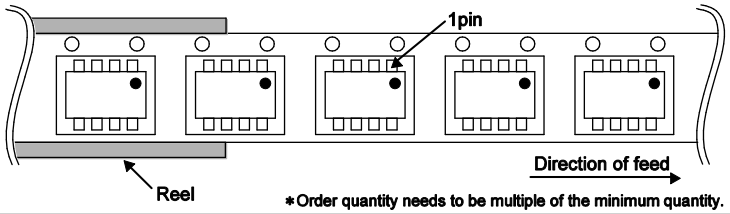
Physical Dimension Tape and Reel information

Package Name	MSOP8



<Tape and Reel information>

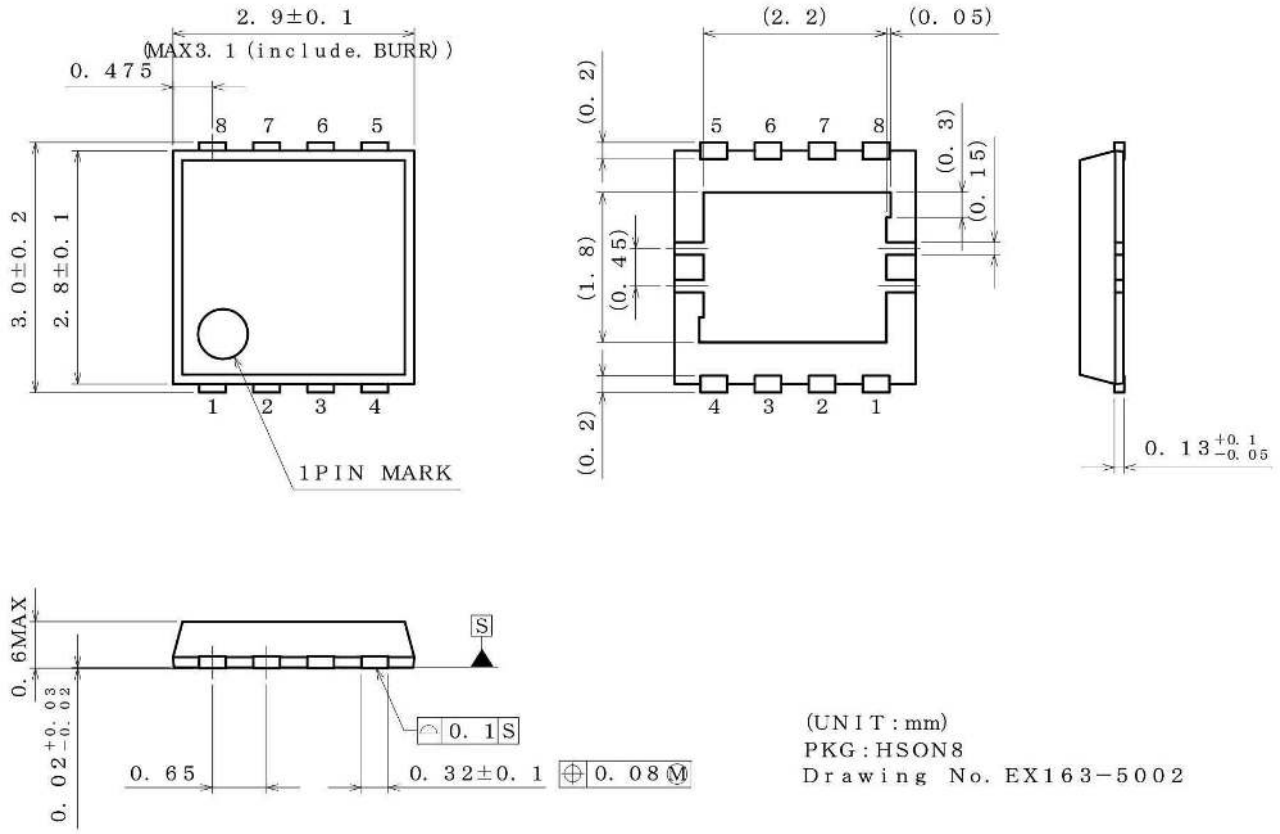
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

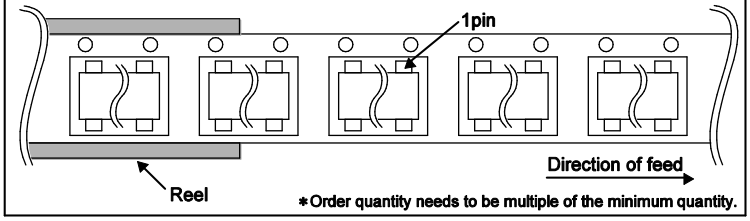
Physical Dimension Tape and Reel information - continued

Package Name	HSON8



<Tape and Reel information>

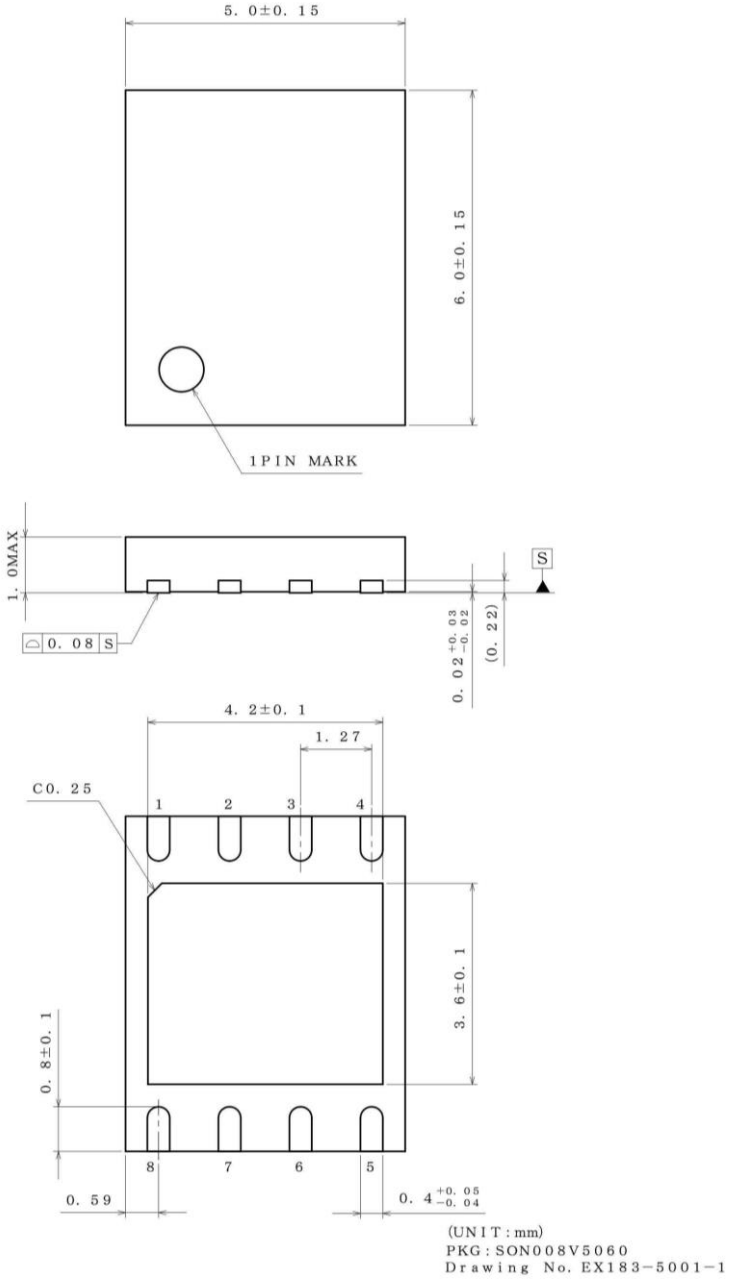
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

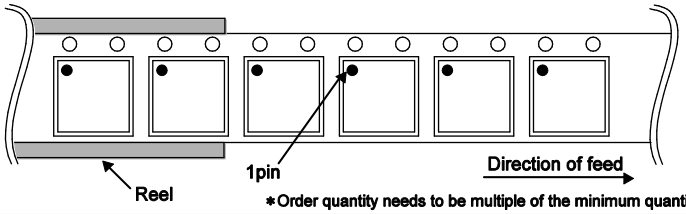
Physical Dimension Tape and Reel information - continued

Package Name	SON008V5060



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
17.Jan.2012	001	New Release
20.Sep.2013	002	Revise the items about Power dissipation
02.Oct.2014	003	Applied the ROHM Standard Style and improved understandability
03.Apr.2019	004	Revise the items about Ordering Information

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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