PCA9959

24-channel SPI serial bus 63 mA/5.5 V constant current LED driver

Rev. 1.3 — 23 May 2022 Product data sheet

1 General description

PCA9959 is a daisy-chain SPI-compatible 4-wire serial bus controlled 24-channel constant preset current LED driver, optimized for dimming and blinking 63 mA Red/Green/Blue/Amber (RGBA) LEDs.

Each LED output has its own 6-bit resolution (64 steps) preset current configuration, with an absolute accuracy of ±8 %.

PCA9959 supports up to four groups of LED gradation control, with each LED channel assigned to one of the groups. For each group, PCA9959 supports 64-grid brightness control, with the time duration of each grid adjustable from 2.5 µs to 1 ms. Each LED output can be off or on, set at its individual preset current value within each grid. Once gradation control is enabled, PCA9959 automatically changes each LED preset current with the setup from grid0 to grid63; once finished, it can hold grid63 or repeat from grid0 as configured.

PCA9959 operates with a supply voltage range of 2.7 V to 5.5 V and the constant preset current sink LED outputs allow up to 5.5 V for the LED supply.

This device has built-in open short load and overtemperature detection circuitry. The error information from the corresponding register can be read via the 4-wire serial bus. Additionally, a thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCA9959 device is designed to use a 4-wire read/write serial bus with higher data clock frequency (up to 10 MHz).

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9959 devices at the same time.

2 Features and benefits

- 24 LED drivers, each output programmable at:
  - Off
  - On
  - 6 bits programmable LED brightness
  - Programmable LED output delay to reduce EMI and surge currents
- Gradation control for all channels
  - Each channel can assign to one of four gradation control groups
  - 64 grids for gradation control for each channel
  - Programmable grid duration time
  - Four preset current options for each channel during gradation control
- 24 constant preset current output channels can sink up to 63 mA, and tolerate up to 5.5 V when OFF

- Output preset current adjusted through an external resistor (REXT input)
- Output preset current accuracy
  - ±8 % absolute accuracy with 60 mA output current
  - ±6.5 % absolute accuracy with 30 mA output current
  - Maximum ±5 % channel to channel variation
  - Maximum ±7 % device to device variation
- Open/short load/overtemperature detection mode to detect individual LED errors
- 4-wire serial bus interface with 10 MHz data clock rate
- Active LOW Output Enable ($\overline{OE}$) input pin
- Internal power-on reset
- No glitch on LEDn outputs on power-up
- Low standby preset current
- Operating power supply voltage (V_{DD}) range of 2.7 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- -40 °C to +85 °C operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds 2 kV HBM per JESD22-A114
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Available in HVQFN40 package

3 Applications

- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices
- Fade-in and fade-out for breathlight control

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9959HN	P9959	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 5 x 5 x 0.85 mm	SOT1369-5

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9959HN	PCA9959HNMP	HVQFN40	Reel 13" Q2 DP	6000	T_{amb} = -40 °C to +85 °C

5 Block diagram

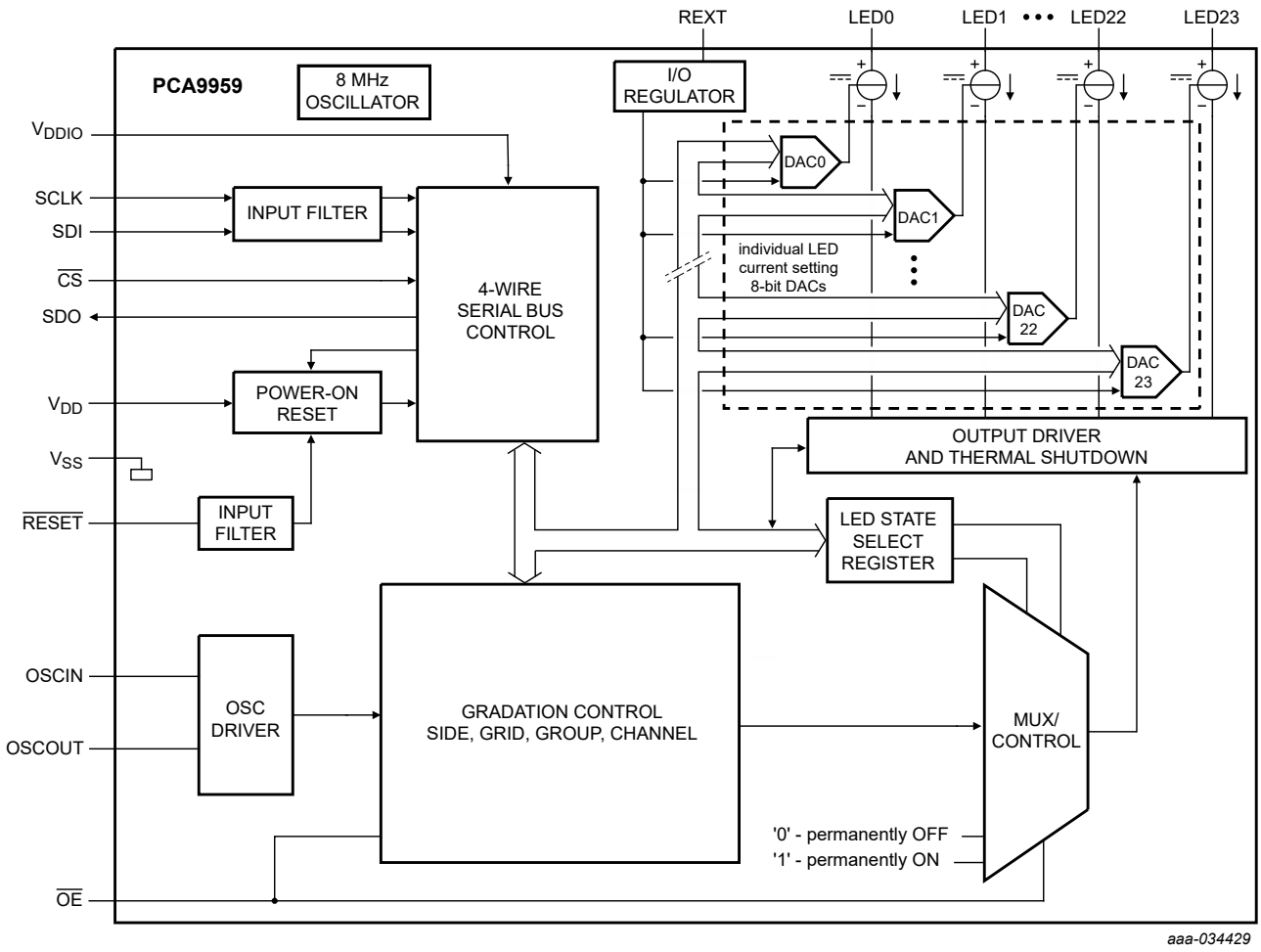
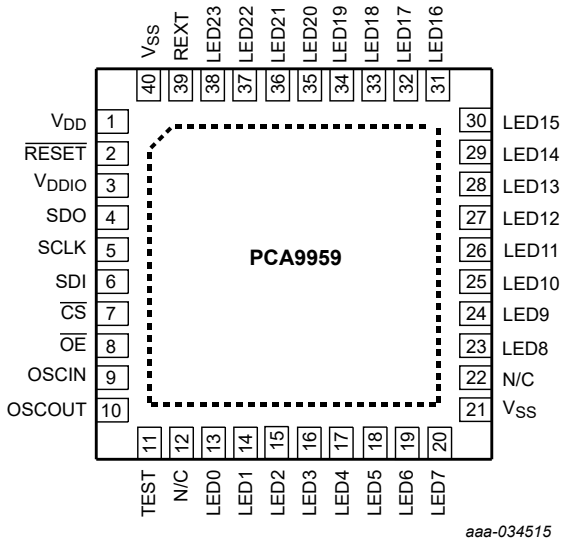


Figure 1. Block diagram of PCA9959

6 Pinning information

6.1 Pinning



1. Thermal pad; connected to V_{SS}.

Figure 2. Pin configuration for HVQFN40

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
REXT	39	I	current set resistor input; resistor to ground
SDO	4	O	serial data output
$\overline{CS}$	7	I	active LOW chip select - when held HIGH the SDO pin is held LOW
$\overline{OE}$	8	I	active LOW output enable for LEDs
LED0	13	O	LED driver 0
LED1	14	O	LED driver 1
LED2	15	O	LED driver 2
LED3	16	O	LED driver 3
LED4	17	O	LED driver 4
LED5	18	O	LED driver 5
LED6	19	O	LED driver 6
LED7	20	O	LED driver 7
LED8	23	O	LED driver 8
LED9	24	O	LED driver 9
LED10	25	O	LED driver 10
LED11	26	O	LED driver 11

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
LED12	27	O	LED driver 12
LED13	28	O	LED driver 13
LED14	29	O	LED driver 14
LED15	30	O	LED driver 15
LED16	31	O	LED driver 16
LED17	32	O	LED driver 17
LED18	33	O	LED driver 18
LED19	34	O	LED driver 19
LED20	35	O	LED driver 20
LED21	36	O	LED driver 21
LED22	37	O	LED driver 22
LED23	38	O	LED driver 23
$\overline{\text{RESET}}$	2	I	active LOW reset input with external 10 kΩ pull-up resistor
SCLK	5	I	serial clock line
SDI	6	I	serial data input
V_{SS}	21, 40 [1]	ground	supply ground
V_{DDIO}	3	power supply	supply rail of SPI interface
V_{DD}	1	power supply	supply voltage
N/C	12, 22	N/A	no connection
OSCIN	9	I/O	oscillator input
OSCOUT	10	I/O	oscillator output
TEST	11	factory test	internal pull down - connect to GND or leave floating

[1] HVQFN40 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7 Functional description

Refer to Figure 1.

7.1 Register address and data

Following a chip select ($\overline{CS}$) asserted condition (from HIGH to LOW), the data transfers are (16 × n) bits wide (where 'n' is the number of slaves in the chain) with MSB transferred first. The first seven bits are the address of the register to be accessed. The eighth bit indicates the types of access — read (= 1) or write (= 0). The second group of 8 bits consists of data as shown in Figure 3.

See Section 8 for more detail.

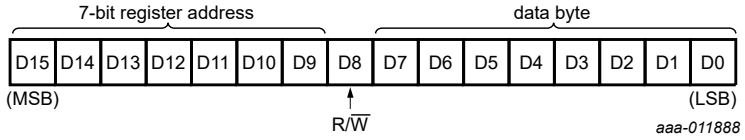


Figure 3. Register address and data format for each slave

7.2 Register definitions

Table 4. Register summary - default values

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	0	0	0	0	MODE2	read/write	Mode register 2
02h	0	0	0	0	0	0	0	0	EFLAG0	read only	output error flag 0
03h	0	0	0	0	0	0	0	0	EFLAG1	read only	output error flag 1
04h	0	0	0	0	0	0	0	0	EFLAG2	read only	output error flag 2
05h	0	0	0	0	0	0	0	0	EFLAG3	read only	output error flag 3
06h	0	0	0	0	0	0	0	0	EFLAG4	read only	output error flag 4
07h	0	0	0	0	0	0	0	0	EFLAG5	read only	output error flag 5
08h	0	0	0	0	0	0	0	0	GRID_DUR	read/write	grid duration control
09h	0	0	0	0	0	0	0	0	GRD_CTL	read/write	grid configuration
0Ah	0	0	0	0	0	0	0	0	SIDE_CTL	read/write	side control
0Bh	0	0	0	0	0	0	0	0	PAGE_SEL	read/write	page select
0Ch-1Fh	0	0	0	0	0	0	0	0	reserved[1]	read only	not used
20h	0	0	0	0	0	0	0	0	GRID0	read/write	grid0 configuration
21h	0	0	0	0	0	0	0	0	GRID1	read/write	grid1 configuration
22h	0	0	0	0	0	0	0	0	GRID2	read/write	grid2 configuration
23h	0	0	0	0	0	0	0	0	GRID3	read/write	grid3 configuration
24h	0	0	0	0	0	0	0	0	GRID4	read/write	grid4 configuration
25h	0	0	0	0	0	0	0	0	GRID5	read/write	grid5 configuration

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
26h	0	0	0	0	0	0	0	0	GRID6	read/write	grid6 configuration
27h	0	0	0	0	0	0	0	0	GRID7	read/write	grid7 configuration
28h	0	0	0	0	0	0	0	0	GRID8	read/write	grid8 configuration
29h	0	0	0	0	0	0	0	0	GRID9	read/write	grid9 configuration
2Ah	0	0	0	0	0	0	0	0	GRID10	read/write	grid10 configuration
2Bh	0	0	0	0	0	0	0	0	GRID11	read/write	grid11 configuration
2Ch	0	0	0	0	0	0	0	0	GRID12	read/write	grid12 configuration
2Dh	0	0	0	0	0	0	0	0	GRID13	read/write	grid13 configuration
2Eh	0	0	0	0	0	0	0	0	GRID14	read/write	grid14 configuration
2Fh	0	0	0	0	0	0	0	0	GRID15	read/write	grid15 configuration
30h	0	0	0	0	0	0	0	0	GRID16	read/write	grid16 configuration
31h	0	0	0	0	0	0	0	0	GRID17	read/write	grid17 configuration
32h	0	0	0	0	0	0	0	0	GRID18	read/write	grid18 configuration
33h	0	0	0	0	0	0	0	0	GRID19	read/write	grid19 configuration
34h	0	0	0	0	0	0	0	0	GRID20	read/write	grid20 configuration
35h	0	0	0	0	0	0	0	0	GRID21	read/write	grid21 configuration
36h	0	0	0	0	0	0	0	0	GRID22	read/write	grid22 configuration
37h	0	0	0	0	0	0	0	0	GRID23	read/write	grid23 configuration
38h	0	0	0	0	0	0	0	0	GRID24	read/write	grid24 configuration
39h	0	0	0	0	0	0	0	0	GRID25	read/write	grid25 configuration
3Ah	0	0	0	0	0	0	0	0	GRID26	read/write	grid26 configuration
3Bh	0	0	0	0	0	0	0	0	GRID27	read/write	grid27 configuration
3Ch	0	0	0	0	0	0	0	0	GRID28	read/write	grid28 configuration
3Dh	0	0	0	0	0	0	0	0	GRID29	read/write	grid29 configuration
3Eh	0	0	0	0	0	0	0	0	GRID30	read/write	grid30 configuration
3Fh	0	0	0	0	0	0	0	0	GRID31	read/write	grid31 configuration
40h	0	0	0	0	0	0	0	0	GRID32	read/write	grid32 configuration
41h	0	0	0	0	0	0	0	0	GRID33	read/write	grid33 configuration
42h	0	0	0	0	0	0	0	0	GRID34	read/write	grid34 configuration
43h	0	0	0	0	0	0	0	0	GRID35	read/write	grid35 configuration
44h	0	0	0	0	0	0	0	0	GRID36	read/write	grid36 configuration
45h	0	0	0	0	0	0	0	0	GRID37	read/write	grid37 configuration
46h	0	0	0	0	0	0	0	0	GRID38	read/write	grid38 configuration
47h	0	0	0	0	0	0	0	0	GRID39	read/write	grid39 configuration
48h	0	0	0	0	0	0	0	0	GRID40	read/write	grid40 configuration
49h	0	0	0	0	0	0	0	0	GRID41	read/write	grid41 configuration

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
4Ah	0	0	0	0	0	0	0	0	GRID42	read/write	grid42 configuration
4Bh	0	0	0	0	0	0	0	0	GRID43	read/write	grid43 configuration
4Ch	0	0	0	0	0	0	0	0	GRID44	read/write	grid44 configuration
4Dh	0	0	0	0	0	0	0	0	GRID45	read/write	grid45 configuration
4Eh	0	0	0	0	0	0	0	0	GRID46	read/write	grid46 configuration
4Fh	0	0	0	0	0	0	0	0	GRID47	read/write	grid47 configuration
50h	0	0	0	0	0	0	0	0	GRID48	read/write	grid48 configuration
51h	0	0	0	0	0	0	0	0	GRID49	read/write	grid49 configuration
52h	0	0	0	0	0	0	0	0	GRID50	read/write	grid50 configuration
53h	0	0	0	0	0	0	0	0	GRID51	read/write	grid51 configuration
54h	0	0	0	0	0	0	0	0	GRID52	read/write	grid52 configuration
55h	0	0	0	0	0	0	0	0	GRID53	read/write	grid53 configuration
56h	0	0	0	0	0	0	0	0	GRID54	read/write	grid54 configuration
57h	0	0	0	0	0	0	0	0	GRID55	read/write	grid55 configuration
58h	0	0	0	0	0	0	0	0	GRID56	read/write	grid56 configuration
59h	0	0	0	0	0	0	0	0	GRID57	read/write	grid57 configuration
5Ah	0	0	0	0	0	0	0	0	GRID58	read/write	grid58 configuration
5Bh	0	0	0	0	0	0	0	0	GRID59	read/write	grid59 configuration
5Ch	0	0	0	0	0	0	0	0	GRID60	read/write	grid60 configuration
5Dh	0	0	0	0	0	0	0	0	GRID61	read/write	grid61 configuration
5Eh	0	0	0	0	0	0	0	0	GRID62	read/write	grid62 configuration
5Fh	0	0	0	0	0	0	0	0	GRID63	read/write	grid63 configuration
20h	0	0	0	0	0	0	0	0	CH0_CFG1	read/write	channel0 configuration 1
21h	0	0	0	0	0	0	0	0	CH0_CFG2	read/write	channel0 configuration 2
22h	0	0	0	0	0	0	0	0	CH0_CFG3	read/write	channel0 configuration 3
23h	0	0	0	0	0	0	0	0	CH0_CFG4	read/write	channel0 configuration 4
24h	0	0	0	0	0	0	0	0	CH1_CFG1	read/write	channel1 configuration 1
25h	0	0	0	0	0	0	0	0	CH1_CFG2	read/write	channel1 configuration 2
26h	0	0	0	0	0	0	0	0	CH1_CFG3	read/write	channel1 configuration 3
27h	0	0	0	0	0	0	0	0	CH1_CFG4	read/write	channel1 configuration 4
28h	0	0	0	0	0	0	0	0	CH2_CFG1	read/write	channel2 configuration 1
29h	0	0	0	0	0	0	0	0	CH2_CFG2	read/write	channel2 configuration 2
2Ah	0	0	0	0	0	0	0	0	CH2_CFG3	read/write	channel2 configuration 3
2Bh	0	0	0	0	0	0	0	0	CH2_CFG4	read/write	channel2 configuration 4
2Ch	0	0	0	0	0	0	0	0	CH3_CFG1	read/write	channel3 configuration 1
2Dh	0	0	0	0	0	0	0	0	CH3_CFG2	read/write	channel3 configuration 2

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
2Eh	0	0	0	0	0	0	0	0	CH3_CFG3	read/write	channel3 configuration 3
2Fh	0	0	0	0	0	0	0	0	CH3_CFG4	read/write	channel3 configuration 4
30h	0	0	0	0	0	0	0	0	CH4_CFG1	read/write	channel4 configuration 1
31h	0	0	0	0	0	0	0	0	CH4_CFG2	read/write	channel4 configuration 2
32h	0	0	0	0	0	0	0	0	CH4_CFG3	read/write	channel4 configuration 3
33h	0	0	0	0	0	0	0	0	CH4_CFG4	read/write	channel4 configuration 4
34h	0	0	0	0	0	0	0	0	CH5_CFG1	read/write	channel5 configuration 1
35h	0	0	0	0	0	0	0	0	CH5_CFG2	read/write	channel5 configuration 2
36h	0	0	0	0	0	0	0	0	CH5_CFG3	read/write	channel5 configuration 3
37h	0	0	0	0	0	0	0	0	CH5_CFG4	read/write	channel5 configuration 4
38h	0	0	0	0	0	0	0	0	CH6_CFG1	read/write	channel6 configuration 1
39h	0	0	0	0	0	0	0	0	CH6_CFG2	read/write	channel6 configuration 2
3Ah	0	0	0	0	0	0	0	0	CH6_CFG3	read/write	channel6 configuration 3
3Bh	0	0	0	0	0	0	0	0	CH6_CFG4	read/write	channel6 configuration 4
3Ch	0	0	0	0	0	0	0	0	CH7_CFG1	read/write	channel7 configuration 1
3Dh	0	0	0	0	0	0	0	0	CH7_CFG2	read/write	channel7 configuration 2
3Eh	0	0	0	0	0	0	0	0	CH7_CFG3	read/write	channel7 configuration 3
3Fh	0	0	0	0	0	0	0	0	CH7_CFG4	read/write	channel7 configuration 4
40h	0	0	0	0	0	0	0	0	CH8_CFG1	read/write	channel8 configuration 1
41h	0	0	0	0	0	0	0	0	CH8_CFG2	read/write	channel8 configuration 2
42h	0	0	0	0	0	0	0	0	CH8_CFG3	read/write	channel8 configuration 3
43h	0	0	0	0	0	0	0	0	CH8_CFG4	read/write	channel8 configuration 4
44h	0	0	0	0	0	0	0	0	CH9_CFG1	read/write	channel9 configuration 1
45h	0	0	0	0	0	0	0	0	CH9_CFG2	read/write	channel9 configuration 2
46h	0	0	0	0	0	0	0	0	CH9_CFG3	read/write	channel9 configuration 3
47h	0	0	0	0	0	0	0	0	CH9_CFG4	read/write	channel9 configuration 4
48h	0	0	0	0	0	0	0	0	CH10_CFG1	read/write	channel10 configuration 1
49h	0	0	0	0	0	0	0	0	CH10_CFG2	read/write	channel10 configuration 2
4Ah	0	0	0	0	0	0	0	0	CH10_CFG3	read/write	channel10 configuration 3
4Bh	0	0	0	0	0	0	0	0	CH10_CFG4	read/write	channel10 configuration 4
4Ch	0	0	0	0	0	0	0	0	CH11_CFG1	read/write	channel11 configuration 1
4Dh	0	0	0	0	0	0	0	0	CH11_CFG2	read/write	channel11 configuration 2
4Eh	0	0	0	0	0	0	0	0	CH11_CFG3	read/write	channel11 configuration 3
4Fh	0	0	0	0	0	0	0	0	CH11_CFG4	read/write	channel11 configuration 4
50h	0	0	0	0	0	0	0	0	CH12_CFG1	read/write	channel12 configuration 1
51h	0	0	0	0	0	0	0	0	CH12_CFG2	read/write	channel12 configuration 2

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
52h	0	0	0	0	0	0	0	0	CH12_CFG3	read/write	channel12 configuration 3
53h	0	0	0	0	0	0	0	0	CH12_CFG4	read/write	channel12 configuration 4
54h	0	0	0	0	0	0	0	0	CH13_CFG1	read/write	channel13 configuration 1
55h	0	0	0	0	0	0	0	0	CH13_CFG2	read/write	channel13 configuration 2
56h	0	0	0	0	0	0	0	0	CH13_CFG3	read/write	channel13 configuration 3
57h	0	0	0	0	0	0	0	0	CH13_CFG4	read/write	channel13 configuration 4
58h	0	0	0	0	0	0	0	0	CH14_CFG1	read/write	channel14 configuration 1
59h	0	0	0	0	0	0	0	0	CH14_CFG2	read/write	channel14 configuration 2
5Ah	0	0	0	0	0	0	0	0	CH14_CFG3	read/write	channel14 configuration 3
5Bh	0	0	0	0	0	0	0	0	CH14_CFG4	read/write	channel14 configuration 4
5Ch	0	0	0	0	0	0	0	0	CH15_CFG1	read/write	channel15 configuration 1
5Dh	0	0	0	0	0	0	0	0	CH15_CFG2	read/write	channel15 configuration 2
5Eh	0	0	0	0	0	0	0	0	CH15_CFG3	read/write	channel15 configuration 3
5Fh	0	0	0	0	0	0	0	0	CH15_CFG4	read/write	channel15 configuration 4
60h	0	0	0	0	0	0	0	0	CH16_CFG1	read/write	channel16 configuration 1
61h	0	0	0	0	0	0	0	0	CH16_CFG2	read/write	channel16 configuration 2
62h	0	0	0	0	0	0	0	0	CH16_CFG3	read/write	channel16 configuration 3
63h	0	0	0	0	0	0	0	0	CH16_CFG4	read/write	channel16 configuration 4
64h	0	0	0	0	0	0	0	0	CH17_CFG1	read/write	channel17 configuration 1
65h	0	0	0	0	0	0	0	0	CH17_CFG2	read/write	channel17 configuration 2
66h	0	0	0	0	0	0	0	0	CH17_CFG3	read/write	channel17 configuration 3
67h	0	0	0	0	0	0	0	0	CH17_CFG4	read/write	channel17 configuration 4
68h	0	0	0	0	0	0	0	0	CH18_CFG1	read/write	channel18 configuration 1
69h	0	0	0	0	0	0	0	0	CH18_CFG2	read/write	channel18 configuration 2
6Ah	0	0	0	0	0	0	0	0	CH18_CFG3	read/write	channel18 configuration 3
6Bh	0	0	0	0	0	0	0	0	CH18_CFG4	read/write	channel18 configuration 4
6Ch	0	0	0	0	0	0	0	0	CH19_CFG1	read/write	channel19 configuration 1
6Dh	0	0	0	0	0	0	0	0	CH19_CFG2	read/write	channel19 configuration 2
6Eh	0	0	0	0	0	0	0	0	CH19_CFG3	read/write	channel19 configuration 3
6Fh	0	0	0	0	0	0	0	0	CH19_CFG4	read/write	channel19 configuration 4
70h	0	0	0	0	0	0	0	0	CH20_CFG1	read/write	channel20 configuration 1
71h	0	0	0	0	0	0	0	0	CH20_CFG2	read/write	channel20 configuration 2
72h	0	0	0	0	0	0	0	0	CH20_CFG3	read/write	channel20 configuration 3
73h	0	0	0	0	0	0	0	0	CH20_CFG4	read/write	channel20 configuration 4
74h	0	0	0	0	0	0	0	0	CH21_CFG1	read/write	channel21 configuration 1
75h	0	0	0	0	0	0	0	0	CH21_CFG2	read/write	channel21 configuration 2

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
76h	0	0	0	0	0	0	0	0	CH21_CFG3	read/write	channel21 configuration 3
77h	0	0	0	0	0	0	0	0	CH21_CFG4	read/write	channel21 configuration 4
78h	0	0	0	0	0	0	0	0	CH22_CFG1	read/write	channel22 configuration 1
79h	0	0	0	0	0	0	0	0	CH22_CFG2	read/write	channel22 configuration 2
7Ah	0	0	0	0	0	0	0	0	CH22_CFG3	read/write	channel22 configuration 3
7Bh	0	0	0	0	0	0	0	0	CH22_CFG4	read/write	channel22 configuration 4
7Ch	0	0	0	0	0	0	0	0	CH23_CFG1	read/write	channel23 configuration 1
7Dh	0	0	0	0	0	0	0	0	CH23_CFG2	read/write	channel23 configuration 2
7Eh	0	0	0	0	0	0	0	0	CH23_CFG3	read/write	channel23 configuration 3
7Fh	0	0	0	0	0	0	0	0	CH23_CFG4	read/write	channel23 configuration 4

[1] Reserved registers should not be written to and always reads back as zeros.

7.2.1 MODE1 — Mode register 1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	R/W	0*	reserved
5	-	R/W	0*	reserved
4	SLEEP	R/W	0*	Normal mode[1].
			1	Low-power mode. Internal oscillator off[2][3]. All LEDs keep the status defined in Grid0
3	OFFSET_DIS	R/W	0*	50 ns delay offset between channel(x) and channel(x+1) when turning on/off or changing current; the delay is not applied when all channels turned off by $\overline{OE}$
			1	No delay offset
2	CLK20M_TYP	R/W	0*	use Ceralock resonator between OSCIN and OSCOUT to generate 20 MHz clock for gradation control
			1	use 20 MHz external clock presented on OSCIN pin for gradation control
1	-	R/W	0*	reserved
0	-	R/W	0*	reserved

[1] It takes 500 µs max for the internal oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if registers are accessed within the 500 µs window.
[2] No gradation control is possible when the internal oscillator is off.
[3] External clock is only for gradation control; state machine always uses internal clock

7.2.2 MODE2 — Mode register 2

Table 6. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	OVERTEMP	read only	0*	OK
			1	overtemperature condition
6	ERROR	read only	0*	no error at LED outputs
			1	any open or short-circuit detected in error flag registers (EFLAGn)
5	EXCLKPRS	read only	0*	no valid external clock presented, the clock range is defined as f_{EXTCLK}
			1	external clock detected in correct range
4	CLRERR	write only	0*	self clear after write ‘1’
			1	Write ‘1’ to clear all error status bits in EFLAGn register and ERROR (bit 6). The EFLAGn and ERROR bit is set to ‘1’ if open or short-circuit is detected again.
3	AUTO_ SWITCHOFF_ DIS	R/W	0*	Disable the channel for which open or short error is detected and enable it again when write ‘1’ to CLRERR, clears all error status bits in EFLAGn registers and ERROR bit
			1	The channel won’t turn off when open/short is detected
2	-	read only	0*	reserved
1	-	read only	0*	reserved
0	-	read only	0*	reserved

7.2.3 LED error detection

The PCA9959 is capable of detecting an LED open or short condition at its open-drain LED outputs. Users recognize these faults by reading the status of a pair of error bits (ERRx) in error flag registers (EFLAGn) for each channel. Output status must be set to OFF for those unused LED output channels. If the output is selected to be ON, that channel is tested.

The user can poll the ERROR status bit (bit 6 in MODE2 register) to check if there is a fault condition in any of the 24 channels. The EFLAGn registers can then be read to determine which channels are at fault and the type of fault in those channels. The error status reported by the EFLAGn register is real time information that self-clears once the error is fixed and writes ‘1’ to CLRERR bit (bit 4 in MODE2 register).

By default, the channel for which open or short error is detected is turned off, and it can only be enabled again when write ‘1’ to CLRERR clears all error status bits in EFLAGn registers and ERROR bit. This auto switch off feature can be turned off by set register AUTO_SWITCHOFF_DIS to ‘1’; in this case the channel does not turn off when open or short error is detected.

The LED error detection mechanism is to execute open and/or short detection during gradation operation, and to report error bits in the error flag registers accordingly.

PCA9959 executes either open or short detection alternately in each grid operation except Grid63, and both open and short detection are executed in Grid63 operation.

The following test results can be observed when one shot mode (GRD_EN = 1 and GRD_MODE = 0) is used in different gradation operation.

- One grid mode:
  1. Set LED CHx Group x(0-3) current set y(1-3) value, such as LED CH0 -> Group 0 -> Current set 1 = 0x11
  2. Set only one grid of Grid0 to Grid62, such as GD16_G0 = Current set 1
  3. Set GRD_EN = 1 and GRD_MODE = 0, set one shot mode
  4. Assert $\overline{OE}$ pin and deassert $\overline{OE}$ pin
  5. Observe either open or short detection is executed alternately in Grid16 gradation operation and reported error bits in the error flag registers.
  6. Go to step 4.
- Two or more grids mode:
  1. Set LED CHx Group x(0-3) current set y(1-3) value, such as LED CH0 -> Group 0 -> Current set 1 = 0x11
  2. Set two or more grids of Grid0 to Grid62, such as GD16_G0 = Current set 1 and GD17_G0 = Current set 1
  3. Set GRD_EN = 1 and GRD_MODE = 0, set one shot mode
  4. Assert $\overline{OE}$ pin and deassert $\overline{OE}$ pin
  5. Observe both of open and short detection are executed during Grid 16 and Grid17 gradation operation and reported error bits in the error flag registers.
  6. Go to step 4.
- Grid63 only mode:
  1. Set LED CHx Group x(0-3) current set y(1-3) value, such as LED CH0 -> Group 0 -> Current set 1 = 0x11
  2. Set only Grid63, such as GD63_G0 = Current set 1
  3. Set GRD_EN = 1 and GRD_MODE = 0, set one shot mode
  4. Assert $\overline{OE}$ pin and deassert $\overline{OE}$ pin
  5. Observe both of open and short detection are executed in Grid63 gradation operation and reported error bits in the error flag registers.
     Because of GRD_MODE = 0 (One shot mode, all LED hold status of Grid63 after Grid63 executed) setting, PCA9959 holds LED status at Grid63 after one shot mode is completed; it has time to complete both short and open detection on LED channels which are lit at Grid63.
  6. Go to step 4.

Note: When $\overline{OE}$ pin is asserted with GRD_EN = 0 (Gradation stops), OPEN is not detected and reported to the error flag registers even if LED pins matched OPEN condition. In the same operation, SHORT is detected and reported to the error flag registers if LED pins matched SHORT condition.

Table 7. EFLAG0 to EFLAG5 - Error flag registers (address 02h to 07h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
02h	EFLAG0	7:6	ERR3	R only	00*	Error status for LED3 output
		5:4	ERR2	R only	00*	Error status for LED2 output
		3:2	ERR1	R only	00*	Error status for LED1 output
		1:0	ERR0	R only	00*	Error status for LED0 output
03h	EFLAG1	7:6	ERR7	R only	00*	Error status for LED7 output
		5:4	ERR6	R only	00*	Error status for LED6 output
		3:2	ERR5	R only	00*	Error status for LED5 output
		1:0	ERR4	R only	00*	Error status for LED4 output
04h	EFLAG2	7:6	ERR11	R only	00*	Error status for LED11 output
		5:4	ERR10	R only	00*	Error status for LED10 output
		3:2	ERR9	R only	00*	Error status for LED9 output
		1:0	ERR8	R only	00*	Error status for LED8 output
05h	EFLAG3	7:6	ERR15	R only	00*	Error status for LED15 output
		5:4	ERR14	R only	00*	Error status for LED14 output
		3:2	ERR13	R only	00*	Error status for LED13 output
		1:0	ERR12	R only	00*	Error status for LED12 output
06h	EFLAG4	7:6	ERR19	R only	00*	Error status for LED19 output
		5:4	ERR18	R only	00*	Error status for LED18 output
		3:2	ERR17	R only	00*	Error status for LED17 output
		1:0	ERR16	R only	00*	Error status for LED16 output
07h	EFLAG5	7:6	ERR23	R only	00*	Error status for LED23 output
		5:4	ERR22	R only	00*	Error status for LED22 output
		3:2	ERR21	R only	00*	Error status for LED21 output
		1:0	ERR20	R only	00*	Error status for LED20 output

Table 8. ERRx bit description

LED error detection status	ERRx		Description
	Bit 1	Bit 0	
No error	0	0	In normal operation and no error
Short-circuit	0	1	Detected LED short-circuit condition
Open-circuit	1	0	Detected LED open-circuit condition
DNE (Do Not Exist)	1	1	This condition does not exist

7.2.3.1 Open-circuit detection principle

The PCA9959 LED open-circuit detection compares the effective preset current level I_O with the open load detection threshold preset current $I_{th(det)}$. If I_O is below the threshold $I_{th(det)}$, the PCA9959 detects an open load condition. This error status can be read out as an error flag through the EFLAGn registers. For open-circuit error detection of an output channel, that channel must be ON.

Table 9. Open-circuit detection

State of output port	Condition of output preset current	Error status code	Description
OFF	I_O = 0 mA	0	detection not possible
ON	$I_O < I_{th(det)}$[1]	1	open-circuit
	$I_O \geq I_{th(det)}$[1]	this channel open error status bit is 0	normal

[1] $I_{th(det)} = 0.5 \times I_{O(target)}$ (typical). This threshold may be different for each I/O and only depends on R_{ext} and chosen output current.

7.2.3.2 Short-circuit detection principle

The LED short-circuit detection compares the effective output voltage level (V_O) with the shorted-load detection threshold voltages $V_{th(trig)}$. If V_O is above the $V_{th(trig)}$ threshold, the PCA9959 detects a shorted-load condition. If V_O is below the $V_{th(trig)}$ threshold, no error is detected and error bit is set to '0'. This error status can be read out as an error flag through the EFLAGn registers. For short-circuit error detection of an output channel, that channel must be ON.

Table 10. Short-circuit detection

State of output port	Condition of output voltage	Error status code	Description
OFF	-	0	detection not possible
ON	$V_O \geq V_{th(trig)}$[1]	1	short-circuit
	$V_O < V_{th(trig)}$[1]	this channel short error status bit is 0	normal

[1] $V_{th} \cong 1.96$ V.

Remark: The error status distinguishes between an LED short condition and an LED open condition. Upon detecting an LED short or open, the corresponding LED outputs should be turned OFF to prevent heat dissipation for a short in the chip. Although an open event is not harmful, the outputs should be turned OFF for both occasions to repair the LED string.

7.2.4 Overtemperature protection

If the PCA9959 chip temperature exceeds its limit ($T_{th(otp)}$ (rising) maximum, see Table 25), all output channels are disabled until the temperature drops below its limit minus a small hysteresis ($T_{th(otp)}$ (hysteresis) maximum, see Table 25). When an overtemperature situation is encountered, the OVERTEMP flag (bit 7) is set in the MODE2 register. Once the die temperature falls below the $T_{th(otp)}$ rising - $T_{th(otp)}$ hysteresis, the chip returns to the same condition it was prior to the overtemperature event and the OVERTEMP flag is cleared.

7.2.5 GRID_DUR, Grid duration control

Table 11. GRID_DUR - Grid duration control (address 08h) bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7:6	TSTEP	R/W	00*	Time step for duration control, 00 for 2.5 µs
			01	5 µs
			10	10 µs
			11	20 µs
5:0	DURCNT	R/W	000000*	Counter for duration control, the duration time for each grid is calculated by TSTEP*(DURCNT+1)

7.2.6 GRD_CTL, Gradation control

Table 12. GRD_CTL - Gradation control register (address 09h) bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	GRD_EN	R/W	0*	Gradation stops, all LEDs return to Grid0
			1	Gradation starts from Grid0
6	GRD_MODE	R/W	0*	One short mode, all LEDs hold status of Grid63 after Grid63 executed.
			1	Recurrence mode, all LEDs turn to Grid0 after Grid63 executed
5	-	R/W	0*	reserved
4	-	R/W	0*	reserved
3	-	R/W	0*	reserved
2	-	R/W	0*	reserved
1	-	R/W	0*	reserved
0	-	R/W	0*	reserved

7.2.7 SIDE_CTL, Side control

Table 13. SIDE_CTL - Side control register (address 0Ah) bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	SIDE_CFG	R/W	0*	The side to be written to through register on Page0 and Page1, 0 for Side 0
			1	1 for Side 1
6	SIDE_EXE	R/W	0*	The Side to be executed, 0 for Side 0
			1	1 for Side 1
5	-	R/W	0*	reserved
4	-	R/W	0*	reserved
3	-	R/W	0*	reserved

Table 13. SIDE_CTL - Side control register (address 0Ah) bit description...*continued*

*Legend: * default value*

Bit	Symbol	Access	Value	Description
2	-	R/W	0*	reserved
1	-	R/W	0*	reserved
0	-	R/W	0*	reserved

7.2.8 PAGE_SEL, register page select

Table 14. PAGE_SEL - page select register (address 0Bh) bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	PAGE_SEL	R/W	0*	Choose page 0 when accessing register from 20h to 7Fh
			1	Choose page 1 when accessing register from 20h to 7Fh
6	-	R/W	0*	reserved
5	-	R/W	0*	reserved
4	-	R/W	0*	reserved
3	-	R/W	0*	reserved
2	-	R/W	0*	reserved
1	-	R/W	0*	reserved
0	-	R/W	0*	reserved

7.2.9 GRID0 to GRID63, GRID configuration

Table 15. GRID0 to GRID63 - GRID configuration registers 0 to 63 (Page0, address 20h to 5Fh) bit description

*Legend: * default value*

Address	Register	Symbol				Access	Value	Description
		7:6	5:4	3:2	1:0			
20h	GRID0	GD0_G3	GD0_G2	GD0_G1	GD0_G0	R/W	0000 0000*	Grid0 configuration
21h	GRID1	GD1_G3	GD1_G2	GD1_G1	GD1_G0	R/W	0000 0000*	Grid1 configuration
22h	GRID2	GD2_G3	GD2_G2	GD2_G1	GD2_G0	R/W	0000 0000*	Grid2 configuration
23h	GRID3	GD3_G3	GD3_G2	GD3_G1	GD3_G0	R/W	0000 0000*	Grid3 configuration
24h	GRID4	GD4_G3	GD4_G2	GD4_G1	GD4_G0	R/W	0000 0000*	Grid4 configuration
25h	GRID5	GD5_G3	GD5_G2	GD5_G1	GD5_G0	R/W	0000 0000*	Grid5 configuration
26h	GRID6	GD6_G3	GD6_G2	GD6_G1	GD6_G0	R/W	0000 0000*	Grid6 configuration
27h	GRID7	GD7_G3	GD7_G2	GD7_G1	GD7_G0	R/W	0000 0000*	Grid7 configuration
28h	GRID8	GD8_G3	GD8_G2	GD8_G1	GD8_G0	R/W	0000 0000*	Grid8 configuration
29h	GRID9	GD9_G3	GD9_G2	GD9_G1	GD9_G0	R/W	0000 0000*	Grid9 configuration
2Ah	GRID10	GD10_G3	GD10_G2	GD10_G1	GD10_G0	R/W	0000 0000*	Grid10 configuration

Table 15. GRID0 to GRID63 - GRID configuration registers 0 to 63 (Page0, address 20h to 5Fh) bit description*...continued*

*Legend: * default value*

Address	Register	Symbol				Access	Value	Description
2Bh	GRID11	GD11_G3	GD11_G2	GD11_G1	GD11_G0	R/W	0000 0000*	Grid11 configuration
2Ch	GRID12	GD12_G3	GD12_G2	GD12_G1	GD12_G0	R/W	0000 0000*	Grid12 configuration
2Dh	GRID13	GD13_G3	GD13_G2	GD13_G1	GD13_G0	R/W	0000 0000*	Grid13 configuration
2Eh	GRID14	GD14_G3	GD14_G2	GD14_G1	GD14_G0	R/W	0000 0000*	Grid14 configuration
2Fh	GRID15	GD15_G3	GD15_G2	GD15_G1	GD15_G0	R/W	0000 0000*	Grid15 configuration
30h	GRID16	GD16_G3	GD16_G2	GD16_G1	GD16_G0	R/W	0000 0000*	Grid16 configuration
31h	GRID17	GD17_G3	GD17_G2	GD17_G1	GD17_G0	R/W	0000 0000*	Grid17 configuration
32h	GRID18	GD18_G3	GD18_G2	GD18_G1	GD18_G0	R/W	0000 0000*	Grid18 configuration
33h	GRID19	GD19_G3	GD19_G2	GD19_G1	GD19_G0	R/W	0000 0000*	Grid19 configuration
34h	GRID20	GD20_G3	GD20_G2	GD20_G1	GD20_G0	R/W	0000 0000*	Grid20 configuration
35h	GRID21	GD21_G3	GD21_G2	GD21_G1	GD21_G0	R/W	0000 0000*	Grid21 configuration
36h	GRID22	GD22_G3	GD22_G2	GD22_G1	GD22_G0	R/W	0000 0000*	Grid22 configuration
37h	GRID23	GD23_G3	GD23_G2	GD23_G1	GD23_G0	R/W	0000 0000*	Grid23 configuration
38h	GRID24	GD24_G3	GD24_G2	GD24_G1	GD24_G0	R/W	0000 0000*	Grid24 configuration
39h	GRID25	GD25_G3	GD25_G2	GD25_G1	GD25_G0	R/W	0000 0000*	Grid25 configuration
3Ah	GRID26	GD26_G3	GD26_G2	GD26_G1	GD26_G0	R/W	0000 0000*	Grid26 configuration
3Bh	GRID27	GD27_G3	GD27_G2	GD27_G1	GD27_G0	R/W	0000 0000*	Grid27 configuration
3Ch	GRID28	GD28_G3	GD28_G2	GD28_G1	GD28_G0	R/W	0000 0000*	Grid28 configuration
3Dh	GRID29	GD29_G3	GD29_G2	GD29_G1	GD29_G0	R/W	0000 0000*	Grid29 configuration
3Eh	GRID30	GD30_G3	GD30_G2	GD30_G1	GD30_G0	R/W	0000 0000*	Grid30 configuration
3Fh	GRID31	GD31_G3	GD31_G2	GD31_G1	GD31_G0	R/W	0000 0000*	Grid31 configuration
40h	GRID32	GD32_G3	GD32_G2	GD32_G1	GD32_G0	R/W	0000 0000*	Grid32 configuration
41h	GRID33	GD33_G3	GD33_G2	GD33_G1	GD33_G0	R/W	0000 0000*	Grid33 configuration
42h	GRID34	GD34_G3	GD34_G2	GD34_G1	GD34_G0	R/W	0000 0000*	Grid34 configuration
43h	GRID35	GD35_G3	GD35_G2	GD35_G1	GD35_G0	R/W	0000 0000*	Grid35 configuration
44h	GRID36	GD36_G3	GD36_G2	GD36_G1	GD36_G0	R/W	0000 0000*	Grid36 configuration
45h	GRID37	GD37_G3	GD37_G2	GD37_G1	GD37_G0	R/W	0000 0000*	Grid37 configuration
46h	GRID38	GD38_G3	GD38_G2	GD38_G1	GD38_G0	R/W	0000 0000*	Grid38 configuration
47h	GRID39	GD39_G3	GD39_G2	GD39_G1	GD39_G0	R/W	0000 0000*	Grid39 configuration
48h	GRID40	GD40_G3	GD40_G2	GD40_G1	GD40_G0	R/W	0000 0000*	Grid40 configuration
49h	GRID41	GD41_G3	GD41_G2	GD41_G1	GD41_G0	R/W	0000 0000*	Grid41 configuration
4Ah	GRID42	GD42_G3	GD42_G2	GD42_G1	GD42_G0	R/W	0000 0000*	Grid42 configuration
4Bh	GRID43	GD43_G3	GD43_G2	GD43_G1	GD43_G0	R/W	0000 0000*	Grid43 configuration
4Ch	GRID44	GD44_G3	GD44_G2	GD44_G1	GD44_G0	R/W	0000 0000*	Grid44 configuration
4Dh	GRID45	GD45_G3	GD45_G2	GD45_G1	GD45_G0	R/W	0000 0000*	Grid45 configuration

Table 15. GRID0 to GRID63 - GRID configuration registers 0 to 63 (Page0, address 20h to 5Fh) bit description...*continued*

*Legend: * default value*

Address	Register	Symbol				Access	Value	Description
4Eh	GRID46	GD46_G3	GD46_G2	GD46_G1	GD46_G0	R/W	0000 0000*	Grid46 configuration
4Fh	GRID47	GD47_G3	GD47_G2	GD47_G1	GD47_G0	R/W	0000 0000*	Grid47 configuration
50h	GRID48	GD48_G3	GD48_G2	GD48_G1	GD48_G0	R/W	0000 0000*	Grid48 configuration
51h	GRID49	GD49_G3	GD49_G2	GD49_G1	GD49_G0	R/W	0000 0000*	Grid49 configuration
52h	GRID50	GD50_G3	GD50_G2	GD50_G1	GD50_G0	R/W	0000 0000*	Grid50 configuration
53h	GRID51	GD51_G3	GD51_G2	GD51_G1	GD51_G0	R/W	0000 0000*	Grid51 configuration
54h	GRID52	GD52_G3	GD52_G2	GD52_G1	GD52_G0	R/W	0000 0000*	Grid52 configuration
55h	GRID53	GD53_G3	GD53_G2	GD53_G1	GD53_G0	R/W	0000 0000*	Grid53 configuration
56h	GRID54	GD54_G3	GD54_G2	GD54_G1	GD54_G0	R/W	0000 0000*	Grid54 configuration
57h	GRID55	GD55_G3	GD55_G2	GD55_G1	GD55_G0	R/W	0000 0000*	Grid55 configuration
58h	GRID56	GD56_G3	GD56_G2	GD56_G1	GD56_G0	R/W	0000 0000*	Grid56 configuration
59h	GRID57	GD57_G3	GD57_G2	GD57_G1	GD57_G0	R/W	0000 0000*	Grid57 configuration
5Ah	GRID58	GD58_G3	GD58_G2	GD58_G1	GD58_G0	R/W	0000 0000*	Grid58 configuration
5Bh	GRID59	GD59_G3	GD59_G2	GD59_G1	GD59_G0	R/W	0000 0000*	Grid59 configuration
5Ch	GRID60	GD60_G3	GD60_G2	GD60_G1	GD60_G0	R/W	0000 0000*	Grid60 configuration
5Dh	GRID61	GD61_G3	GD61_G2	GD61_G1	GD61_G0	R/W	0000 0000*	Grid61 configuration
5Eh	GRID62	GD62_G3	GD62_G2	GD62_G1	GD62_G0	R/W	0000 0000*	Grid62 configuration
5Fh	GRID63	GD63_G3	GD63_G2	GD63_G1	GD63_G0	R/W	0000 0000*	Grid63 configuration

Table 16. GDxx_Gy bit description

Group LED configuration	GDxx_Gy		Description
	Bit 1	Bit 0	
OFF	0	0	LEDs in Group y is OFF
preset current 1	0	1	Drive preset current1 set in corresponding register CHx_CFG2 to LED
preset current 2	1	0	Drive preset current2 set in corresponding register CHx_CFG3 to LED
preset current 3	1	1	Drive preset current3 set in corresponding register CHx_CFG4 to LED

7.2.10 CH0_CFG1/2/3 to CH23_CFG1/2/3, Channel configuration

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
20h	CH0_CFG1	7:3	-	R only	00000*	reserved

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description*...continued*

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
		2:1	CH0_GRP	R/W	00*	LED 0 group configuration
		0	CH0_EN	R/W	0*	LED 0 enable
21h	CH0_CFG2	7:6	-	R only	00*	reserved
		5:0	CH0_CUR1	R/W	000000*	LED 0 preset current 1
22h	CH0_CFG3	7:6	-	R only	00*	reserved
		5:0	CH0_CUR2	R/W	000000*	LED 0 preset current 2
23h	CH0_CFG4	7:6	-	R only	00*	reserved
		5:0	CH0_CUR3	R/W	000000*	LED 0 preset current 3
24h	CH1_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH1_GRP	R/W	00*	LED 1 group configuration
		0	CH1_EN	R/W	0*	LED 1 enable
25h	CH1_CFG2	7:6	-	R only	00*	reserved
		5:0	CH1_CUR1	R/W	000000*	LED 1 preset current 1
26h	CH1_CFG3	7:6	-	R only	00*	reserved
		5:0	CH1_CUR2	R/W	000000*	LED 1 preset current 2
27h	CH1_CFG4	7:6	-	R only	00*	reserved
		5:0	CH1_CUR3	R/W	000000*	LED 1 preset current 3
28h	CH2_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH2_GRP	R/W	00*	LED 2 group configuration
		0	CH2_EN	R/W	0*	LED 2 enable
29h	CH2_CFG2	7:6	-	R only	00*	reserved
		5:0	CH2_CUR1	R/W	000000*	LED 2 preset current 1
2Ah	CH2_CFG3	7:6	-	R only	00*	reserved
		5:0	CH2_CUR2	R/W	000000*	LED 2 preset current 2
2Bh	CH2_CFG4	7:6	-	R only	00*	reserved
		5:0	CH2_CUR3	R/W	000000*	LED 2 preset current 3
2Ch	CH3_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH3_GRP	R/W	00*	LED 3 group configuration
		0	CH3_EN	R/W	0*	LED 3 enable
2Dh	CH3_CFG2	7:6	-	R only	00*	reserved
		5:0	CH3_CUR1	R/W	000000*	LED 3 preset current 1
2Eh	CH3_CFG3	7:6	-	R only	00*	reserved
		5:0	CH3_CUR2	R/W	000000*	LED 3 preset current 2
2Fh	CH3_CFG4	7:6	-	R only	00*	reserved
		5:0	CH3_CUR3	R/W	000000*	LED 3 preset current 3
30h	CH4_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH4_GRP	R/W	00*	LED 4 group configuration
		0	CH4_EN	R/W	0*	LED 4 enable

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description*...continued*

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
31h	CH4_CFG2	7:6	-	R only	00*	reserved
		5:0	CH4_CUR1	R/W	000000*	LED 4 preset current 1
32h	CH4_CFG3	7:6	-	R only	00*	reserved
		5:0	CH4_CUR2	R/W	000000*	LED 4 preset current 2
33h	CH4_CFG4	7:6	-	R only	00*	reserved
		5:0	CH4_CUR3	R/W	000000*	LED 4 preset current 3
34h	CH5_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH5_GRP	R/W	00*	LED 5 group configuration
		0	CH5_EN	R/W	0*	LED 5 enable
35h	CH5_CFG2	7:6	-	R only	00*	reserved
		5:0	CH5_CUR1	R/W	000000*	LED 5 preset current 1
36h	CH5_CFG3	7:6	-	R only	00*	reserved
		5:0	CH5_CUR2	R/W	000000*	LED 5 preset current 2
37h	CH5_CFG4	7:6	-	R only	00*	reserved
		5:0	CH5_CUR3	R/W	000000*	LED 5 preset current 3
38h	CH6_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH6_GRP	R/W	00*	LED 6 group configuration
		0	CH6_EN	R/W	0*	LED 6 enable
39h	CH6_CFG2	7:6	-	R only	00*	reserved
		5:0	CH6_CUR1	R/W	000000*	LED 6 preset current 1
3Ah	CH6_CFG3	7:6	-	R only	00*	reserved
		5:0	CH6_CUR2	R/W	000000*	LED 6 preset current 2
3Bh	CH6_CFG4	7:6	-	R only	00*	reserved
		5:0	CH6_CUR3	R/W	000000*	LED 6 preset current 3
3Ch	CH7_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH7_GRP	R/W	00*	LED 7 group configuration
		0	CH7_EN	R/W	0*	LED 7 enable
3Dh	CH7_CFG2	7:6	-	R only	00*	reserved
		5:0	CH7_CUR1	R/W	000000*	LED 7 preset current 1
3Eh	CH7_CFG3	7:6	-	R only	00*	reserved
		5:0	CH7_CUR2	R/W	000000*	LED 7 preset current 2
3Fh	CH7_CFG4	7:6	-	R only	00*	reserved
		5:0	CH7_CUR3	R/W	000000*	LED 7 preset current 3
40h	CH8_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH8_GRP	R/W	00*	LED 8 group configuration
		0	CH8_EN	R/W	0*	LED 8 enable
41h	CH8_CFG2	7:6	-	R only	00*	reserved
		5:0	CH8_CUR1	R/W	000000*	LED 8 preset current 1

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description*...continued*

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
42h	CH8_CFG3	7:6	-	R only	00*	reserved
		5:0	CH8_CUR2	R/W	000000*	LED 8 preset current 2
43h	CH8_CFG4	7:6	-	R only	00*	reserved
		5:0	CH8_CUR3	R/W	000000*	LED 8 preset current 3
44h	CH9_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH9_GRP	R/W	00*	LED 9 group configuration
		0	CH9_EN	R/W	0*	LED 9 enable
45h	CH9_CFG2	7:6	-	R only	00*	reserved
		5:0	CH9_CUR1	R/W	000000*	LED 9 preset current 1
46h	CH9_CFG3	7:6	-	R only	00*	reserved
		5:0	CH9_CUR2	R/W	000000*	LED 9 preset current 2
47h	CH9_CFG4	7:6	-	R only	00*	reserved
		5:0	CH9_CUR3	R/W	000000*	LED 9 preset current 3
48h	CH10_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH10_GRP	R/W	00*	LED 10 group configuration
		0	CH10_EN	R/W	0*	LED 10 enable
49h	CH10_CFG2	7:6	-	R only	00*	reserved
		5:0	CH10_CUR1	R/W	000000*	LED 10 preset current 1
4Ah	CH10_CFG3	7:6	-	R only	00*	reserved
		5:0	CH10_CUR2	R/W	000000*	LED 10 preset current 2
4Bh	CH10_CFG4	7:6	-	R only	00*	reserved
		5:0	CH10_CUR3	R/W	000000*	LED 10 preset current 3
4Ch	CH11_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH11_GRP	R/W	00*	LED 11 group configuration
		0	CH11_EN	R/W	0*	LED 11 enable
4Dh	CH11_CFG2	7:6	-	R only	00*	reserved
		5:0	CH11_CUR1	R/W	000000*	LED 11 preset current 1
4Eh	CH11_CFG3	7:6	-	R only	00*	reserved
		5:0	CH11_CUR2	R/W	000000*	LED 11 preset current 2
4Fh	CH11_CFG4	7:6	-	R only	00*	reserved
		5:0	CH11_CUR3	R/W	000000*	LED 11 preset current 3
50h	CH12_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH12_GRP	R/W	00*	LED 12 group configuration
		0	CH12_EN	R/W	0*	LED 12 enable
51h	CH12_CFG2	7:6	-	R only	00*	reserved
		5:0	CH12_CUR1	R/W	000000*	LED 12 preset current 1
52h	CH12_CFG3	7:6	-	R only	00*	reserved
		5:0	CH12_CUR2	R/W	000000*	LED 12 preset current 2

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description*...continued*

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
53h	CH12_CFG4	7:6	-	R only	00*	reserved
		5:0	CH12_CUR3	R/W	000000*	LED 12 preset current 3
54h	CH13_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH13_GRP	R/W	00*	LED 13 group configuration
		0	CH13_EN	R/W	0*	LED 13 enable
55h	CH13_CFG2	7:6	-	R only	00*	reserved
		5:0	CH13_CUR1	R/W	000000*	LED 13 preset current 1
56h	CH13_CFG3	7:6	-	R only	00*	reserved
		5:0	CH13_CUR2	R/W	000000*	LED 13 preset current 2
57h	CH13_CFG4	7:6	-	R only	00*	reserved
		5:0	CH13_CUR3	R/W	000000*	LED 13 preset current 3
58h	CH14_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH14_GRP	R/W	00*	LED 14 group configuration
		0	CH14_EN	R/W	0*	LED 14 enable
59h	CH14_CFG2	7:6	-	R only	00*	reserved
		5:0	CH14_CUR1	R/W	000000*	LED 14 preset current 1
5Ah	CH14_CFG3	7:6	-	R only	00*	reserved
		5:0	CH14_CUR2	R/W	000000*	LED 14 preset current 2
5Bh	CH14_CFG4	7:6	-	R only	00*	reserved
		5:0	CH14_CUR3	R/W	000000*	LED 14 preset current 3
5Ch	CH15_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH15_GRP	R/W	00*	LED 15 group configuration
		0	CH15_EN	R/W	0*	LED 15 enable
5Dh	CH15_CFG2	7:6	-	R only	00*	reserved
		5:0	CH15_CUR1	R/W	000000*	LED 15 preset current 1
5Eh	CH15_CFG3	7:6	-	R only	00*	reserved
		5:0	CH15_CUR2	R/W	000000*	LED 15 preset current 2
5Fh	CH15_CFG4	7:6	-	R only	00*	reserved
		5:0	CH15_CUR3	R/W	000000*	LED 15 preset current 3
60h	CH16_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH16_GRP	R/W	00*	LED 16 group configuration
		0	CH16_EN	R/W	0*	LED 16 enable
61h	CH16_CFG2	7:6	-	R only	00*	reserved
		5:0	CH16_CUR1	R/W	000000*	LED 16 preset current 1
62h	CH16_CFG3	7:6	-	R only	00*	reserved
		5:0	CH16_CUR2	R/W	000000*	LED 16 preset current 2
63h	CH16_CFG4	7:6	-	R only	00*	reserved
		5:0	CH16_CUR3	R/W	000000*	LED 16 preset current 3

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description*...continued*

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
64h	CH17_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH17_GRP	R/W	00*	LED 17 group configuration
		0	CH17_EN	R/W	0*	LED 17 enable
65h	CH17_CFG2	7:6	-	R only	00*	reserved
		5:0	CH17_CUR1	R/W	000000*	LED 17 preset current 1
66h	CH17_CFG3	7:6	-	R only	00*	reserved
		5:0	CH17_CUR2	R/W	000000*	LED 17 preset current 2
67h	CH17_CFG4	7:6	-	R only	00*	reserved
		5:0	CH17_CUR3	R/W	000000*	LED 17 preset current 3
68h	CH18_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH18_GRP	R/W	00*	LED 18 group configuration
		0	CH18_EN	R/W	0*	LED 18 enable
69h	CH18_CFG2	7:6	-	R only	00*	reserved
		5:0	CH18_CUR1	R/W	000000*	LED 18 preset current 1
6Ah	CH18_CFG3	7:6	-	R only	00*	reserved
		5:0	CH18_CUR2	R/W	000000*	LED 18 preset current 2
6Bh	CH18_CFG4	7:6	-	R only	00*	reserved
		5:0	CH18_CUR3	R/W	000000*	LED 18 preset current 3
6Ch	CH19_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH19_GRP	R/W	00*	LED 19 group configuration
		0	CH19_EN	R/W	0*	LED 19 enable
6Dh	CH19_CFG2	7:6	-	R only	00*	reserved
		5:0	CH19_CUR1	R/W	000000*	LED 19 preset current 1
6Eh	CH19_CFG3	7:6	-	R only	00*	reserved
		5:0	CH19_CUR2	R/W	000000*	LED 19 preset current 2
6Fh	CH19_CFG4	7:6	-	R only	00*	reserved
		5:0	CH19_CUR3	R/W	000000*	LED 19 preset current 3
70h	CH20_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH20_GRP	R/W	00*	LED 20 group configuration
		0	CH20_EN	R/W	0*	LED 20 enable
71h	CH20_CFG2	7:6	-	R only	00*	reserved
		5:0	CH20_CUR1	R/W	000000*	LED 20 preset current 1
72h	CH20_CFG3	7:6	-	R only	00*	reserved
		5:0	CH20_CUR2	R/W	000000*	LED 20 preset current 2
73h	CH20_CFG4	7:6	-	R only	00*	reserved
		5:0	CH20_CUR3	R/W	000000*	LED 20 preset current 3
74h	CH21_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH21_GRP	R/W	00*	LED 21 group configuration

Table 17. CH0_CFG1/2/3 to CH23_CFG1/2/3 - channel configuration registers (Page 1, address 20h to 7Ah) bit description...*continued*

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
		0	CH21_EN	R/W	0*	LED 21 enable
75h	CH21_CFG2	7:6	-	R only	00*	reserved
		5:0	CH21_CUR1	R/W	000000*	LED 21 preset current 1
76h	CH21_CFG3	7:6	-	R only	00*	reserved
		5:0	CH21_CUR2	R/W	000000*	LED 21 preset current 2
77h	CH21_CFG4	7:6	-	R only	00*	reserved
		5:0	CH21_CUR3	R/W	000000*	LED 21 preset current 3
78h	CH22_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH22_GRP	R/W	00*	LED 22 group configuration
		0	CH22_EN	R/W	0*	LED 22 enable
79h	CH22_CFG2	7:6	-	R only	00*	reserved
		5:0	CH22_CUR1	R/W	000000*	LED 22 preset current 1
7Ah	CH22_CFG3	7:6	-	R only	00*	reserved
		5:0	CH22_CUR2	R/W	000000*	LED 22 preset current 2
7Bh	CH22_CFG4	7:6	-	R only	00*	reserved
		5:0	CH22_CUR3	R/W	000000*	LED 22 preset current 3
7Ch	CH23_CFG1	7:3	-	R only	00000*	reserved
		2:1	CH23_GRP	R/W	00*	LED 23 group configuration
		0	CH23_EN	R/W	0*	LED 23 enable
7Dh	CH23_CFG2	7:6	-	R only	00*	reserved
		5:0	CH23_CUR1	R/W	000000*	LED 23 preset current 1
7Eh	CH23_CFG3	7:6	-	R only	00*	reserved
		5:0	CH23_CUR2	R/W	000000*	LED 23 preset current 2
7Fh	CH23_CFG4	7:6	-	R only	00*	reserved
		5:0	CH23_CUR3	R/W	000000*	LED 23 preset current 3

Table 18. CHx_CFG1 - Channel x configuration 1 bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7:3	-	R only	00000*	reserved
2:1	CHx_GRP	R/W	00*	Group assignment for channel x. 00 for Group0
			01	01 for Group1
			10	10 for Group2
			11	11 for Group3
0	CHx_EN	R/W	0*	Channel x output enable, 0 for disable
			1	1 for enable

Table 19. CHx_CFG2 - Channel x configuration 2 bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7:6	-	R only	00*	reserved
5:0	CHx_CUR1	R/W	000000*	preset current setting 1, preset current value is CHx_CUR1 × (1 mA if R_{ext} = 1 kΩ, or 0.25 mA if R_{ext} = 4 kΩ)

Table 20. CHx_CFG3 - Channel x configuration 3 bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7:6	-	R only	00*	reserved
5:0	CHx_CUR2	R/W	000000*	preset current setting 2, preset current value is CHx_CUR2 × (1 mA if R_{ext} = 1 kΩ, or 0.25 mA if R_{ext} = 4 kΩ)

Table 21. CHx_CFG4 - Channel x configuration 4 bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7:6	-	R only	00*	reserved
5:0	CHx_CUR3	R/W	000000*	preset current setting 3, preset current value is CHx_CUR3 × (1 mA if R_{ext} = 1 kΩ, or 0.25 mA if R_{ext} = 4 kΩ)

Register CHx_EN is used to turn off the LED; if '0' other registers in CHx_CFG1/2/3/4 and corresponding GRIDx are ignored.

Register CHx_CUR1/2/3 defines three preset current values with 6 bits of resolution, up to 63 mA with R_{ext} = 1 kΩ.

Registers CHx_GRP assigns the channel to one of four groups for gradation control.

These three preset values can be selected on group level in grid configuration register GRID0~63 during gradation control.

Each LED channel also has two sets of configuration registers, Side 0 and Side 1. At the same time only one of the Side 0/1 takes effect to control LED brightness, the other can be configured for different brightness configuration, if needed.

The PCA9959 can switch between Side 0/1 with register SIDE_CTL.

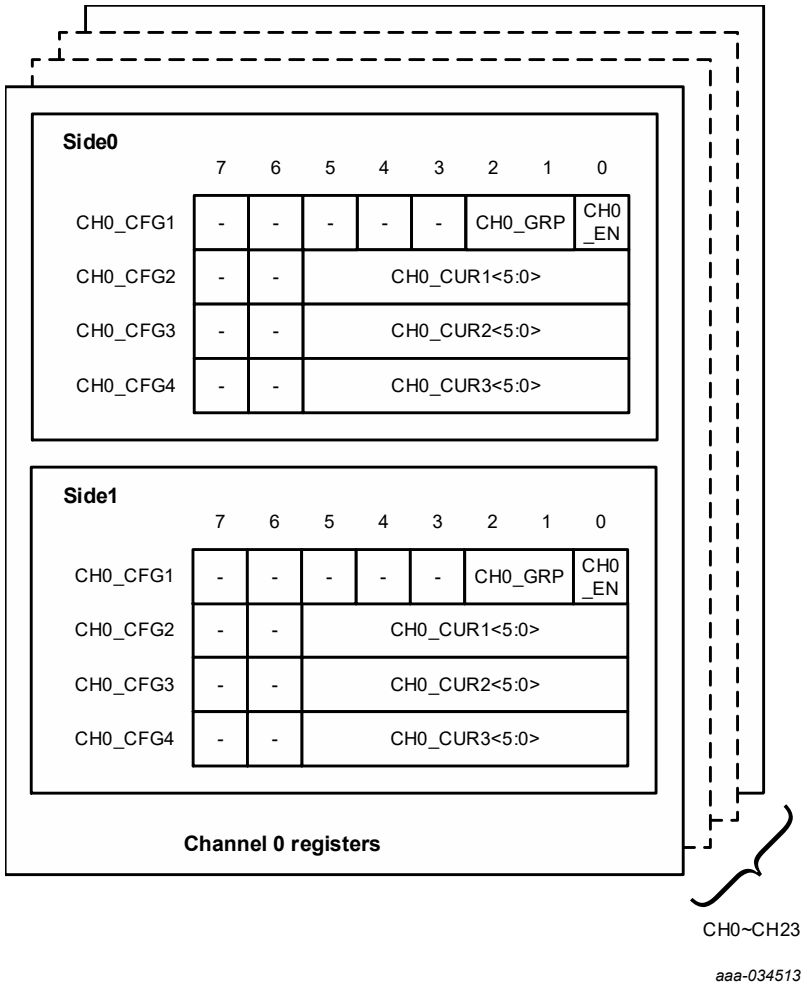


Figure 4. Channel 0~23 configuration registers

7.2.11 LED preset current outputs

In LED display applications, PCA9959 provides nearly no preset current variations, the absolute accuracy is less than ±8 % when driving 63 mA current.

7.2.11.1 Adjusting output preset current

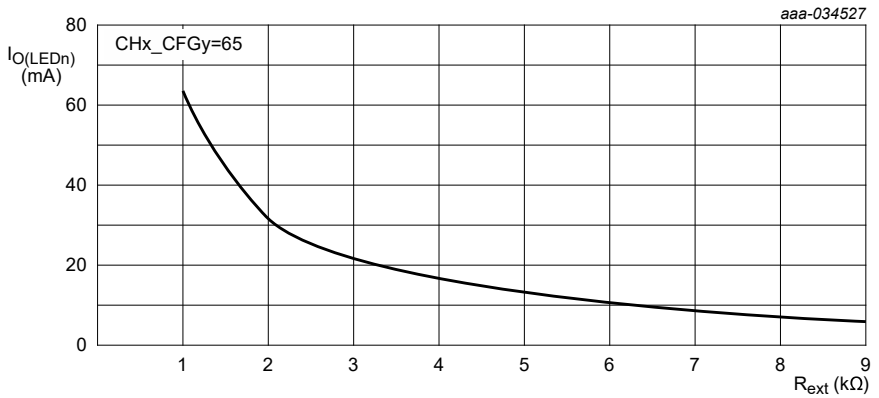
The PCA9959 scales up the reference preset current (I_{ref}) set by the external resistor (R_{ext}) to sink the output preset current (I_O) at each output port. The maximum output preset current for the outputs can be set using R_{ext}.

Each of the 24 channel output preset current has three options defined in register CHx_CFG2/3/4, with 6 bits resolution and up to I_{ref}.

Equation 1 and Equation 2 can be used to calculate the minimum and maximum constant preset current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_MIN = \left(\frac{1000mV}{R_{ext}}\right)(\text{minimum constant current}) \quad (1)$$

$$I_{O}\_LED\_MAX = (63 \times I_{O}\_LED\_MIN) = \left(\frac{1000mV}{R_{ext}} \times 63\right) \quad (2)$$



$I_{O(LEDn)}$ (mA) = CH_CURy (defined in current GRID and CHx_GRP) × 1 / R_{ext} (kΩ)
maximum $I_{O(LEDn)}$ (mA) = 63 × 1 / R_{ext} (kΩ)
Remark: Default CH_CURy at power-up = 0.

Figure 5. Maximum I_{LED} versus R_{ext}

Example 1: If R_{ext} = 1 kΩ, I_{O}_LED_MIN = 1 mA, I_{O}_LED_MAX = 63 mA (as shown in Figure 5).

For example, with R_{ext} = 1 kΩ, each channel has three preset values configured by registers CHGx_CFG2/3/4; each of them can be programmed in 64 steps and in 1.0 mA increments to a maximum output preset current of 63 mA independently.

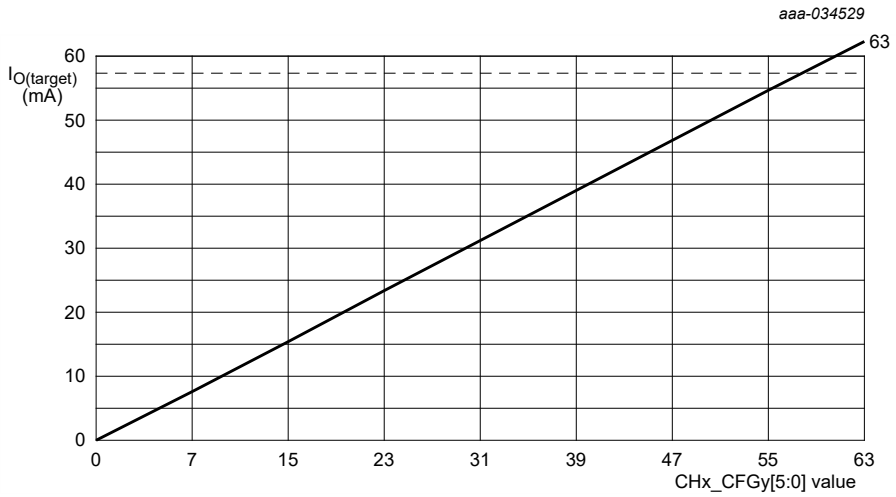


Figure 6. $I_{O(target)}$ versus CHx_CFG2/3/4 value with R_{ext} = 1 kΩ

7.2.12 Gradation control

The PCA9959 is designed to use 64 grids to program gradation sequence on each group.

Each channel can be assigned to one of the four groups with register CHx_CFG1, as described in Section 7.2.10.

There are two sets of configuration registers for gradation control, Side 0 and Side 1. At the same time only one of the Side 0/1 takes effect to control the LED, the other can be configured for different configuration, if needed.

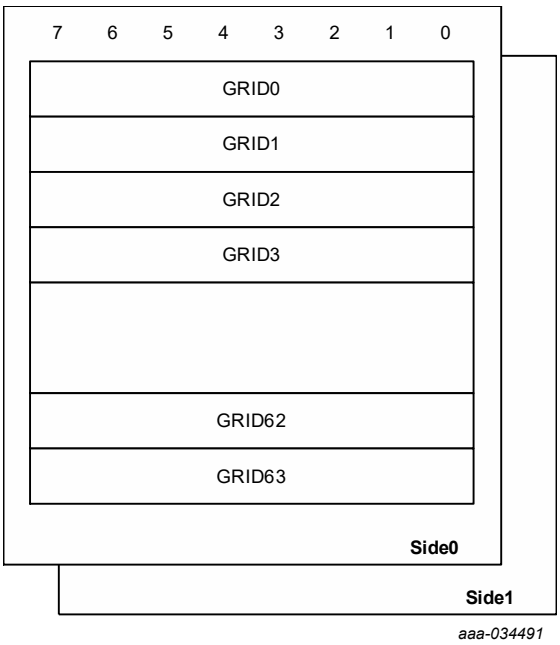


Figure 7. Two sides of 64 grid configuration registers

Each of the grid registers (GRID0~GRID63), as shown in Figure 8, contains current selection for every one of four groups.

For each group, every grid register has two bits to choose the output current from four preset options. Every channel within the group chooses the same option, however the absolute output current within the group may not be necessarily equal; for each channel the output current with the selected option is defined in CHx_CFG2/3/4 registers, as described in Section 7.2.10. For example:

- During GRID0, if GD0_G3 = 00, all output channels in group 4 are off,
- During GRID3, if GD3_G2 = 01, all output channels in group 3 choose preset current 1 as output, if corresponding CHx_EN = 1,
- During GRID12, if GD12_G1 = 10, all output channels in group 2 choose preset current 2 as output, if corresponding CHx_EN = 1,
- During GRID63, if GD63_G0 = 11, all output channels in group 1 choose preset current 3 as output, if corresponding CHx_EN = 1.

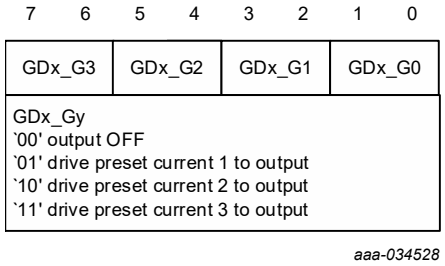


Figure 8. GRIDx register

As $\overline{OE}$ is LOW and GRD_EN is '1', gradation control begins.

1. The register set defined in register SIDE_EXE is effective.
2. GRID0 takes effect first. GD0_G3/2/1/0 chooses output current for each channel in four groups; the output current is set within 50 us from OFF status for worst case.
3. The grid number automatically increments. After current set, GRID0 lasts for the time of GRID_DUR, then register GRID1 takes over, and output current is set within 200 ns for worst case.
4. The grid takes effect one by one from GRID0 to GRID63; this progress can only be interrupted when $\overline{OE}$ becomes HIGH or GRD_EN is deasserted.
5. After GRID63 lights LED for GRID_DUR, if GRD_MODE is 0 (One short mode), output status stays with GRID63 until reconfigured by disabling GRD_EN or by making $\overline{OE}$ HIGH; if GRD_MODE is '1' (recurrent mode), output status starts from GRID0 and repeats above procedure from step 1.
6. CHx_EN can mask the above control sequence and turn off corresponding channel if it equals 0.
7. The 24-channel output has skew less than ±1 µs.
8. During the gradation sequence, if $\overline{OE}$ becomes HIGH or GRD_EN deasserted, the sequence stops immediately; after restart, the sequence begins from GRID0.
9. During the gradation sequence, changing the configuration for GRID or each output is possible; the accessed side is defined in register SIDE_CFG. Although it's possible SIDE_CFG is the same as SIDE_EXE, it's highly recommended not to change the Side being executed, but to switch between sides after the other is fully configured instead.
10. SIDE_EXE does not take effect immediately after change; it waits until GRID63 finishes current side and takes effect from GRID0 in next sequence, e.g., manual restart by $\overline{OE}$ or GRD_EN or auto repeat in recurrence mode.
11. The accuracy of GRID_DUR depends on the external clock from OSCIN pin.

7.2.13 OFFSET — LEDn output delay offset register

The PCA9959 can be programmed to have 50 ns delay for Grid current transition between two adjacent LED outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

This delay applies to any current change from GRD_EN or between Grids.

This delay also applies to $\overline{OE}$ pin when it becomes LOW, but does not apply to $\overline{OE}$ pin when it becomes HIGH, which means all LEDs turn off at the same time when $\overline{OE}$ deasserts.

The order in which the LED outputs are enabled is always be the same (channel 0 changes first and channel 23 changes last).

OFFSET_DIS can turn off the delay when it equals 1, by default the OFFSET_DIS = 0.

Example: If the value in the OFFSET_DIS register is 0 the corresponding delay = 50 ns delay between successive outputs.

channel 0 changes at time 0 ns
channel 1 changes at time 50 ns
channel 2 changes at time 100 ns
channel 3 changes at time 150 ns
channel 4 changes at time 200 ns
channel 5 changes at time 250 ns
channel 6 changes at time 300 ns
channel 7 changes at time 350 ns
channel 8 changes at time 400 ns
channel 9 changes at time 450 ns
channel 10 changes at time 500 ns
channel 11 changes at time 550 ns
channel 12 changes at time 600 ns
channel 13 changes at time 650 ns
channel 14 changes at time 700 ns
channel 15 changes at time 750 ns
channel 16 changes at time 800 ns
channel 17 changes at time 850 ns
channel 18 changes at time 900 ns
channel 19 changes at time 950 ns
channel 20 changes at time 1000 ns
channel 21 changes at time 1050 ns
channel 22 changes at time 1100 ns
channel 23 changes at time 1150 ns

This delay applies both to $\overline{OE}$ pin when asserted, or every current transition between Grids or any other events besides $\overline{OE}$ pin when deasserted, at which moment all LEDs turn off at the same time.

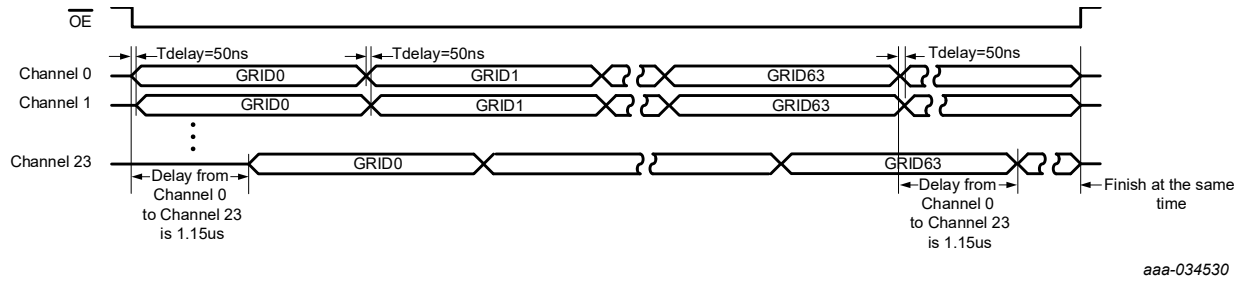


Figure 9. Example of Delay offset

7.3 Active LOW output enable input

The active LOW output enable ($\overline{OE}$) pin on PCA9959 allows to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to $\overline{OE}$ pin, all the LED outputs are enabled.
- When a HIGH level is applied to $\overline{OE}$ pin, all the LED outputs are high-impedance.

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9959 devices at the same time.

7.4 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9959 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9959 registers and serial bus state machine are initialized to their default states (all zeros) causing all the channels to be deselected. Thereafter, V_{DD} must be pulled lower than 1 V and stay LOW for longer than 20 µs. The device resets itself, and allows 2 ms for the device to fully wake up.

7.5 Hardware reset recovery

When a reset of PCA9959 is activated using an active LOW input on the $\overline{RESET}$ pin, a reset pulse width of 2.5 µs minimum is required. The maximum wait time after $\overline{RESET}$ pin is released is 1.5 ms.

8 Characteristics of the 4-wire SPI serial-bus interface

The PCA9959 communicates through a daisy-chain SPI-compatible 4-wire serial interface. The interface has three inputs and one output: serial clock (SCLK), active LOW chip select ($\overline{CS}$), serial data in (SDI) and serial data output (SDO). $\overline{CS}$ must be LOW to clock data into the device, and SDI must be stable when sampled on the rising edge of SCLK. The PCA9959 ignores all activity on SCLK and SDI except when $\overline{CS}$ is LOW.

8.1 SPI-compatible 4-wire serial interface signals

$\overline{CS}$

The active LOW chip select line is used to activate and access the SPI slaves. As long as $\overline{CS}$ is HIGH, all slaves reject the clock signal or data, and output SDO is driven in LOW, therefore SPI parallel connection is not supported. Whenever this pin is in a logic LOW state, data can be transferred between the master (controller) and all slaves (targets).

SCLK

Serial clock is provided by SPI master and determines the speed of the data transfer. All receiving and sending data are done synchronously (clocks the internal SPI shift register and the output driver) to this clock.

SDI

Serial Data In is read on the rising edge of SCLK into the internal 16-bit shift registers. On the rising edge of $\overline{CS}$, the input data is latched into the internal registers of the device. The device ignores all activity on SDI when $\overline{CS}$ is deasserted.

SDO

Serial Data Out is the pin on which the internal 16-bit shift registers data is shifted out serially. SDO is driven LOW until the $\overline{CS}$ pin goes to a logic LOW state. New data appears at the SDO pin following the falling edge of SCLK.

All slave devices can be daisy-chained by connecting the SDO of one device to the SDI of the next device, and driving SCLK and $\overline{CS}$ lines in parallel. Figure 10 depicts how the slaves are connected to the master. All slave devices are accessed at the same

time with $\overline{CS}$. An access requires (16 × n) clock cycles, where 'n' is the number of slave devices. As long as $\overline{CS}$ is LOW, the SPI registers are working as simple shift registers and shifting through the SDI data without interpreting the different control and data bits. When $\overline{CS}$ goes back to HIGH, the bits in the SPI registers are interpreted and the SPI logic is activated.

Only the first slave in the chain receives the control and data bits directly from the SPI Master. Every other slave in the network receives its SDI data from the SDO output of the preceding slave in the chain, and the SDO of the last slave is then connected to the data input (MISO) of SPI Master. Each slave has 16-bit shift registers shifted in from SDI and shifted out to SDO, along with the SCLK clock. The whole chain acts as a 48-bit (n × 16-bit, where 'n' is number of slaves) big shift register.

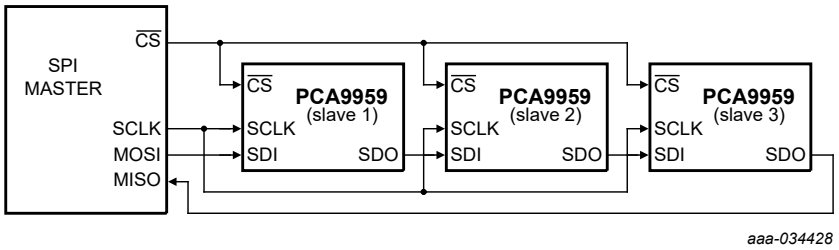


Figure 10. System level connection

8.2 Data format

As shown in Figure 11, the data transfers are 16-bit × n bits wide (where 'n' is the number of slaves) with MSB transferred first. The first 7 bits, D[15:9], form the address of the register to be accessed, the eighth bit (D8) indicates the types of access, either read (= 1) or write (= 0), and the last 8 bits, D[7:0], consist of data. Register read and write sequences (described in the following sections) always begin from the bus idle condition. The bus idle condition refers to $\overline{CS}$ being HIGH and SCLK being in a LOW state.

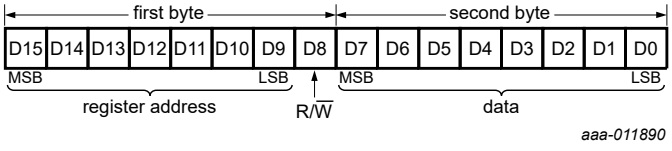


Figure 11. Data format

8.3 Write access sequence

The registers are written using the following write sequence (from a bus idle condition) when the system has three slaves daisy-chained together:

1. All the slave devices in chain are involved in a write or read operation. Every slave device in the chain is a portion of one big shift register.
2. Drive $\overline{CS}$ LOW. This enables the internal 16-bit shift register.
3. Shift 16 × n bits of data (where 'n' is the number of slaves) into the first slave device in a MSB-first fashion. Data is shifted on the rising edge of SCLK and must be stable during the rising edge of SCLK.
4. The 8th bit of the data for every 16 bits (each device) must be a '0', indicating it is a write transfer.

5. After the last bit of data is transferred, drive SCLK LOW and deassert $\overline{CS}$ (drive it HIGH).
6. When $\overline{CS}$ goes from LOW to HIGH, the data in the shift register is latched into the device registers.

If fewer than 16 bits of data are transferred before deasserting $\overline{CS}$, then the data is ignored and the register is not updated. The write transfer format is shown in Figure 12.

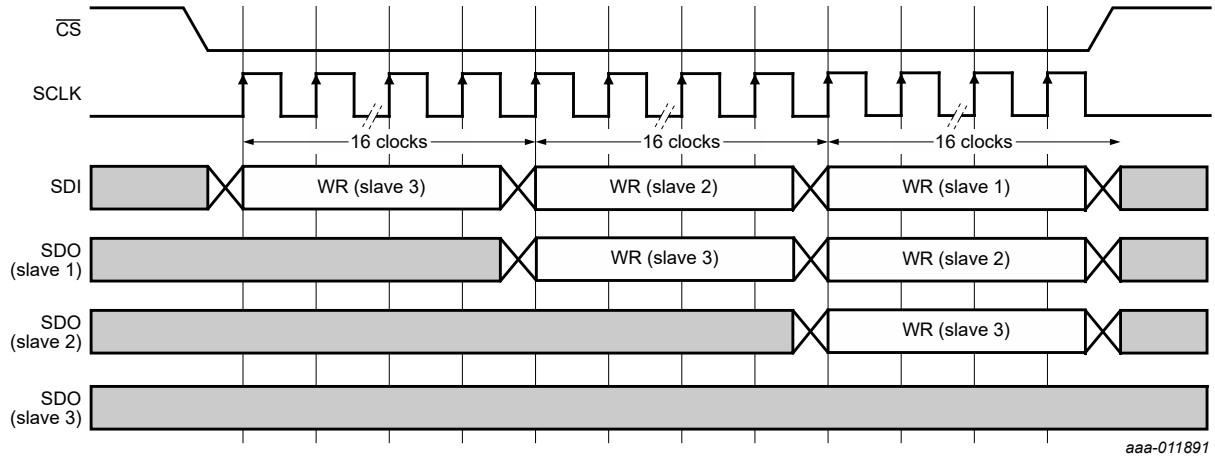


Figure 12. Write access

8.4 Read access sequence

The registers are read using the following read sequence (from a bus idle condition) when the system has three slaves daisy-chained as shown in Figure 13.

1. The master sends the first three 2-byte read instructions with 48 clocks, where the first byte is a 7-bit register address, an eighth bit set to one, followed by dummy data byte (all ones).
2. The Read instruction is decoded when $\overline{CS}$ is deasserted (from LOW to HIGH).
3. The read data is shifted out on SDO when $\overline{CS}$ is asserted again (from HIGH to LOW).
4. The master sends the second three 2-byte 'No Operation' (NOP) operations (all ones) with 48 clocks and reads the requested data on MISO in sequence where the first byte is dummy data (don't care), followed by the read data byte.
5. A read cycle consists of asserting and deasserting of $\overline{CS}$ twice.

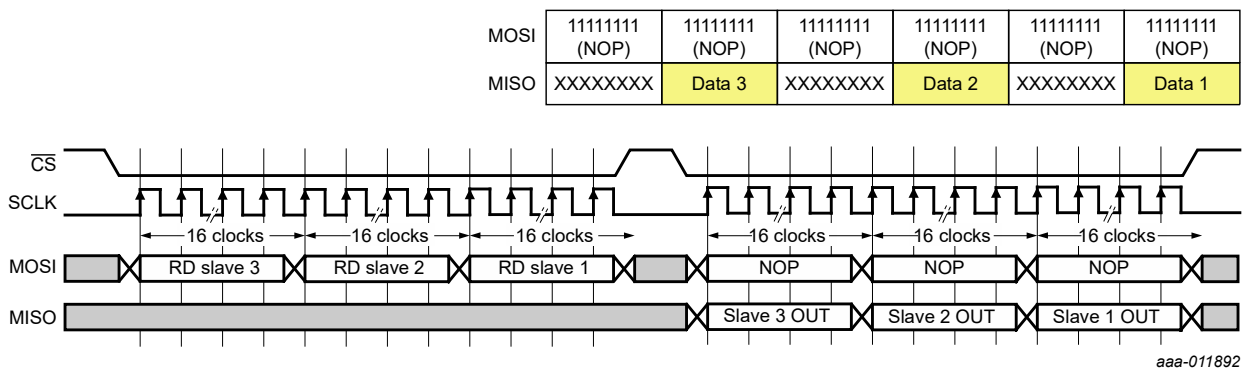


Figure 13. Read access

8.5 Overlapped read and write access sequence

The registers are read and write overlapped using the following sequence (from a bus idle condition) when the system has three slaves daisy-chained as shown in Figure 14.

1. The second phase of the read cycle can be used to send in write data or the next read instruction. This increases the bus utility and hence efficiency.
2. The master sends the first three 2-byte read instructions with 48 clocks, where the first byte is a 7-bit register address, the eighth bit is set to one, followed by dummy data byte (all ones).
3. The read instruction is decoded when $\overline{CS}$ is deasserted (from LOW to HIGH).
4. Start to shift read data out on SDO when $\overline{CS}$ is asserted again (from HIGH to LOW) and start to send in the next read or write instruction on the SDI line.

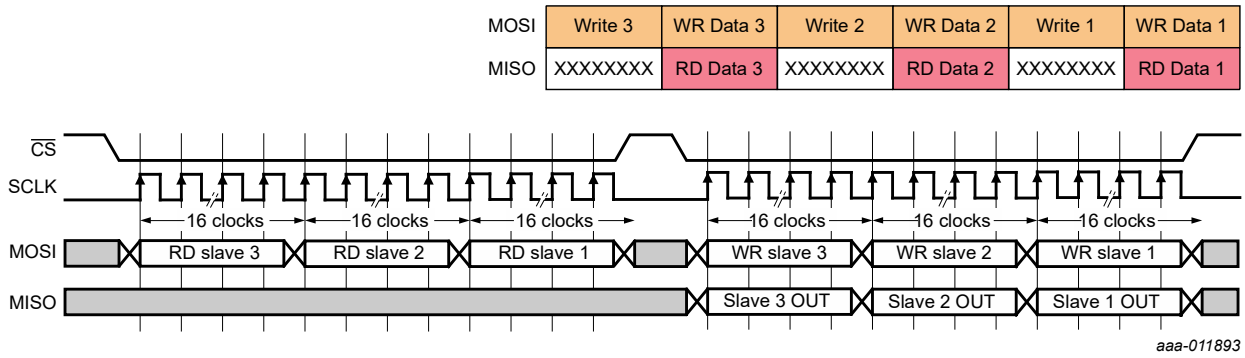
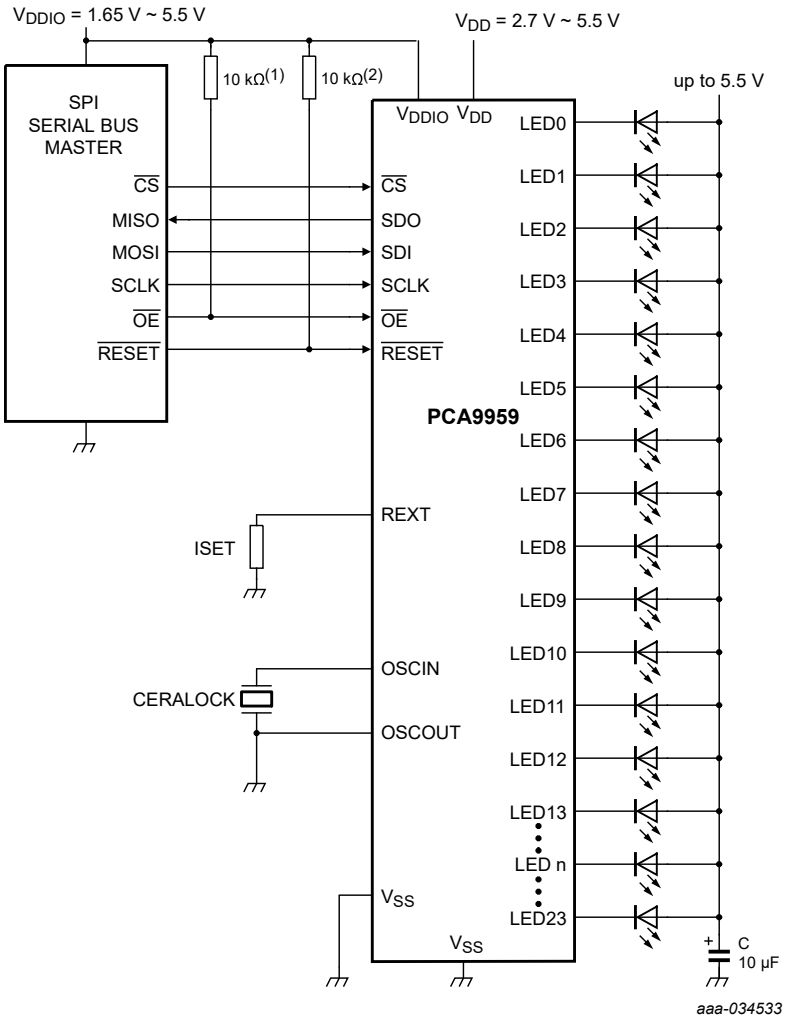


Figure 14. Overlapped read and write access

9 Application design-in information



1. $\overline{OE}$ requires pull-up resistor if control signal from the master is open-drain
2. $\overline{RESET}$ requires a pull-up resistor of <100 kΩ if not used or connected to open-drain output

Figure 15. Typical application

9.1 Thermal considerations

Since the PCA9959 device integrates 24 linear preset current sources, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Perhaps the major contributor for device's overheating is the LED forward voltage mismatch. This is because it can cause significant voltage differences between the LED of the same type (for example, 2 V to 3 V), which ultimately translates into higher power dissipation in the device. The voltage drop across the LED channels of the device is given by the difference between the supply voltage and the LED forward voltage of each LED. Reducing this to a minimum (for example, 0.5 V) helps to keep the power dissipation down. Therefore LEDs binning is recommended to minimize LED voltage forward variation and reduce power dissipation in the device.

In order to ensure that the device does not go into thermal shutdown when operating under certain application conditions, its junction temperature (T_j) should be calculated to ensure that it is below the overtemperature threshold limit (130 °C). The T_j of the device depends on the ambient temperature (T_{amb}), total power dissipation of device (P_{tot}), and thermal resistance.

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{tot} \quad (3)$$

where:

T_j = junction temperature
T_{amb} = ambient temperature
$R_{th(j\text{-}a)}$ = junction to ambient thermal resistance
P_{tot} = (device) total power dissipation

An example of this calculation is show below:

Conditions:

T_{amb} = 50 °C
$R_{th(j\text{-}a)}$ = 39 °C/W (per JEDEC 51 standard for multilayer PCB)
I_{LED} = 60 mA / channel
$I_{DD(max)}$ = 20 mA
V_{DD} = 3.3 V
LEDs per channel = 1 LEDs / channel
LED $V_{F(typ)}$ = 3 V per LED
LED V_F mismatch = 0.2 V per LED
$V_{reg(drv)}$ = 0.5 V (This is present only in the LED string with the highest LED forward voltage.)
V_{sup} = LED $V_{F(typ)}$ + LED V_F mismatch + $V_{reg(drv)}$ = 3 V + 0.2 V + 0.5 V = 3.7 V

P_{tot} calculation:

P_{tot} = IC_power + LED drivers_power;
IC_power = (I_{DD} × V_{DD})
IC_power = (0.02 A × 3.3 V) = 0.066 W
LED drivers_power = [(24 - 1) × (I_{LED}) × (LED V_F mismatch + $V_{reg(drv)}$)] + (I_{LED} × $V_{reg(drv)}$)
LED drivers_power = [23 × 0.06 A × (0.2 V + 0.5 V)] + (0.06 A × 0.5 V)] = 0.996 W
P_{tot} = 0.66 W + 0.996 W = 1.626 W

T_j calculation:

T_j = T_{amb} + $R_{th(j\text{-}a)}$ × P_{tot}
T_j = 50 °C + (30 °C/W × 1.626 W) = 98.78 °C

This confirms that the junction temperature is below the minimum overtemperature threshold of 130 °C, which ensures the device does not go into thermal shutdown under these conditions.

It is important to mention that the value of the thermal resistance junction-to-ambient ($R_{th(j\text{-}a)}$) strongly depends in the PCB design. Therefore, the thermal pad of the device should be attached to a big enough PCB copper area to ensure proper thermal

dissipation (similar to JEDEC 51 standard). Several thermal vias in the PCB thermal pad should be used as well to increase the effectiveness of the heat dissipation (for example, 15 thermal vias). The thermal vias should be distributed evenly in the PCB thermal pad.

Finally, it is important to point out that this calculation should be taken as a reference only and therefore evaluations should still be performed under the application environment and conditions to confirm proper system operation.

9.2 Clock considerations

PCA9959 has two clocks: one is 8 MHz from internal oscillator and the other is 20 MHz high accuracy clock from external.

The external clock can be generated by CERALOCK or forced by external clock source (controlled by register bit CLOCK20M_TYP), this clock is used only for LED gradation, for accurate grid duration control, the external devices are chosen to generate 20 MHz clock frequency with maximum ±0.5 % variation over all temperature range.

There is an external clock detection circuit integrated in PCA9959, while the detected clock frequency is out of 20 MHz by ±15 %, the register EXTCLKPRS is reset to 0 to alert the host.

Please note that the status of register EXTCLKPRS is only a flag indicator; it does not lead to any actions. Gradation control does not stop while EXTCLKPRS = 0, it continues to run with the clock presented on CLKIN pin. When there is no external clock, gradation procedure holds last Grid until clock is recovered, unless $\overline{OE}$ or GRD_EN or SLEEP stops current gradation control.

The internal 8 MHz clock is used for state machine and all other functions besides grid duration control.

9.3 PCA9959 configuration considerations

As there are multiple clocks in the system (8 MHz internal clock, 20 MHz LED gradation clock, SPI clock), to avoid potential conflicts of internal register configurations, or misinterpretations of the configuration, the below configuration procedure is strongly recommended to be followed:

1. Deassert $\overline{OE}$ (from LOW to HIGH)
2. Choose the side to be programmed using SIDE_CFG (0 for Side 0)
3. Program the 64 GRID Registers in the selected Side
4. Program 24 LED Channels Configuration Register in selected Side
5. Select Gradation Mode (One Shot/Recurrence)
6. Program TSTEP and DURCNT in GRD_DUR register
7. Program offset delay enable function (on/off)
8. Enable Gradation Control GRD_EN to start gradation
9. Assert $\overline{OE}$ (from HIGH to LOW)

Note: Steps 8 and 9 are interchangeable. Gradation starts when both $\overline{OE}$ and GRID_EN are asserted.

The status of outputs and internal oscillators are controlled by three input/registers, $\overline{OE}$, GRD_EN and Sleep Mode. Table 22 clarifies the relations and priorities.

Table 22. Control scheme of outputs status and internal oscillator

$\overline{OE}$	Sleep Mode	GRD_EN	Output status	Internal OSC
1	0	x	high-impedance	On
1	1	x	high-impedance	Off
0	0	0	Grid0	On
0	0	1	Gradation mode	On
0	1	x	high-impedance	Off

10 Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.0	V
V_{DDIO}	supply voltage of interface			-0.5	+6.0	V
$V_{I/O}$(others)	voltage on an input/output pin besides OSCIN and OSCOUT			V_{SS} - 0.5	5.5	V
$V_{I/O}$(OSCIN, OSCOUT)	voltage on pin OSCIN and OSCOUT			V_{SS} - 0.5	2.0	V
$V_{drv(LED)}$	LED driver voltage			V_{SS} - 0.5	+6.0	V
$I_{O(LEDn)}$	output preset current on pin LEDn			-	70	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C		-	3.3	W
		T_{amb} = 85 °C		-	1.3	W
T_{stg}	storage temperature			-65	+150	°C
T_{amb}	ambient temperature			-40	+85	°C
T_j	junction temperature			-40	+125	°C

11 Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVQFN40	[1]	35.6	°C/W
$R_{th(j\text{-case top})}$	thermal resistance between the junction and the case top	HVQFN40		17.9	°C/W
$R_{th(j\text{-case bottom})}$	thermal resistance between the junction and the case bottom	HVQFN40		8.5	°C/W
$R_{th(j\text{-board})}$	thermal resistance between the junction and the board	HVQFN40	[1]	27.2	°C/W

[1] Per JEDEC 51 standard for multilayer PCB and Wind Speed (m/s) = 0.

12 Static characteristics

Table 25. Static characteristics

V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply							
V_{DD}	supply voltage			2.7	-	5.5	V
V_{DDIO}	supply voltage of SPI interface			1.65	-	5.5	V
I_{DD}	supply preset current	on pin V_{DD}; operating mode; f_{SCLK} = 10 MHz					
		R_{ext} = 1 kΩ; all outputs off		-			mA
		R_{ext} = 1 kΩ; all outputs drive 63 mA		-	10		mA
I_{DDIO}	supply current	on pin V_{DDIO}; operating mode; f_{SCLK} = 10 MHz; keep writing mode register (01h) with 00h		-	-	650	µA
I_{stb}	standby preset current	on pin V_{DD}; no load; f_{SCLK} = 0 Hz; MODE1[4] = 1; $V_I = V_{DD}$					
		V_{DD} = 3.3 V		-	170	600	µA
		V_{DD} = 5.5 V		-	170	700	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}		-	2	-	V
V_{PDR}	power-down reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[2][3]	-	1	-	V
Inputs $\overline{CS}$, SDI, SCLK; output SDO							
V_{IL}	LOW-level input voltage			-0.5	-	+0.3V_{DDIO}	V
V_{IH}	HIGH-level input voltage			0.7V_{DDIO}	-	5.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = -3 mA at SDO		0.8V_{DDIO}	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA at SDO		-	-	0.2V_{DDIO}	V
I_L	leakage preset current	$V_I = V_{DDIO}$ or V_{SS}		-1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	6	10	pF
preset current controlled outputs							
$I_{O(LEDn)}$	output preset current on pin LEDn	V_O = 0.5 V; CHx_CURy = 3Fh; R_{ext} = 1 kΩ	[3]	58.3	63	67.7	mA
$\Delta I_{O\_Absolute}$	absolute output current variation	V_O = 0.5 V, CHx_CURy>= 08h; R_{ext} = 1 kΩ; refer to ideal value; guaranteed by design				±7.5	%
		V_O = 0.5 V, CHx_CURy < 08h; R_{ext} = 1 kΩ; refer to ideal value; guaranteed by design				±8	%
$\Delta I_{O\_mis\_p2p}$	part to part output current mismatch	all channels on; V_O = 0.5 V; CHx_CURy= 3Fh; R_{ext} = 1 kΩ; average value of 24 output current of each device, comparing to ideal value	[4]	-	-	±7	%

Table 25. Static characteristics...*continued*

V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$\Delta I_{O\_mis\_c2c}$	channel to channel output current mismatch	all channels on; V_O = 0.5 V; CHx_CURy= 3Fh; R_{ext} = 1 kΩ; average value of 24 output current of each device, comparing to ideal value	[5]	-	-	±5	%
$V_{reg(drv)}$	driver regulation voltage	minimum regulation voltage; output current set to 63 mA; R_{ext} = 1 kΩ		0.5		5.5	V
$I_{L(off)}$	off-state leakage preset current	V_O = 5 V		-	-	1	µA
V_{trip}	trip voltage	short LED protection; error flag trips during verification test if $V_O \geq V_{trip}$; R_{ext} = 2 kΩ		1.85	1.96	-	V
$\overline{OE}$ input, $\overline{RESET}$ input							
V_{IL}	LOW-level input voltage			-0.5	-	+0.3V_{DDIO}	V
V_{IH}	HIGH-level input voltage			0.7V_{DDIO}	-	5.5	V
I_{LI}	input leakage preset current			-1	-	+1	µA
C_i	input capacitance		[3]	-	3.7	5	pF
Overtemperature protection							
$T_{th(otp)}$	overtemperature protection threshold temperature	rising	[3]	130	-	150	°C
		hysteresis	[3]	15	-	30	°C

[1] Typical limits at V_{DD} = 3.3 V, T_{amb} = 25 °C.
[2] V_{DD} must be lowered to 1 V in order to reset part.
[3] Value not tested in production, but guaranteed by design and characterization.
[4] Part-to-part mismatch is calculated:

$$\Delta\% = \left(\frac{\left(\frac{I_{O(LED0)}+I_{O(LED1)}+\ldots+I_{O(LED22)}+I_{O(LED23)}}{24} - idealoutputcurrent \right)}{idealoutputcurrent} \right) \times 100$$

where 'ideal output preset current' = 63 mA (R_{ext} = 1 kΩ, CHx_CURy = 3Fh).

[5] Channel-to-channel mismatch is calculated:

$$\Delta\% = \left(\frac{I_{O(LEDn)}(\text{where n = 0 to 23})}{\left(\frac{I_{O(LED0)}+I_{O(LED1)}+\ldots+I_{O(LED22)}+I_{O(LED23)}}{24} \right)} - 1 \right) \times 100$$

13 Dynamic characteristics

Table 26. Dynamic characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{EXTCLK}	External clock frequency range, out of this range register EXTCLKPRS resets to 0			17	20	23	MHz
f_{SCLK}	SCLK clock frequency			0	-	10	MHz
t_{LOW}	LOW period of the SCLK clock			50	-	-	ns
t_{HIGH}	HIGH period of the SCLK clock			50	-	-	ns

Table 26. Dynamic characteristics[1] *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{DS}	data set-up time			10	-	-	ns
t_{DH}	data hold time			20	-	-	ns
t_{CSS}	chip select asserted to SCLK rise set-up time			10	-	-	ns
t_{CSH}	SCLK fall to chip select deasserted hold time			0	-	-	ns
t_{CS_HI}	minimum chip select deasserted HIGH time			40	-	-	ns
$t_{d(SDO)}$	SDO delay time	C_L = 50 pF		-	-	40	ns
t_{GRID_SW}	Grid switch time, the LED current reaches 90 % of target Grid(n) minus current Grid(n-1)				100	500	ns
$t_{d(LED0)}$	The latency time between $\overline{OE}$ pin assertion to LED channel 0 output on			-	-	1 [2]	ms
$t_{OE(disable)}$	$\overline{OE}$ pin disable (HIGH) period time			250	-	-	ns
$t_{OE(enable)}$	$\overline{OE}$ pin enable (LOW) period time			250	-	-	ns

[1] All parameters tested at V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = +25 °C. Specifications over temperature are guaranteed by design.
[2] Guaranteed by design.

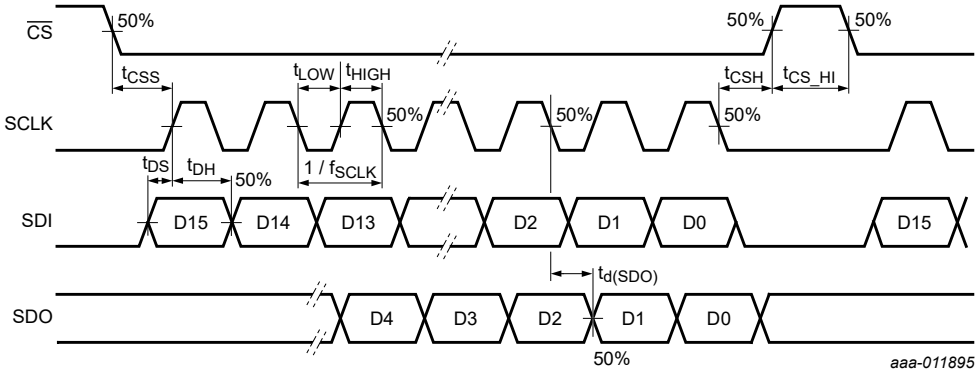


Figure 16. Definition of timing

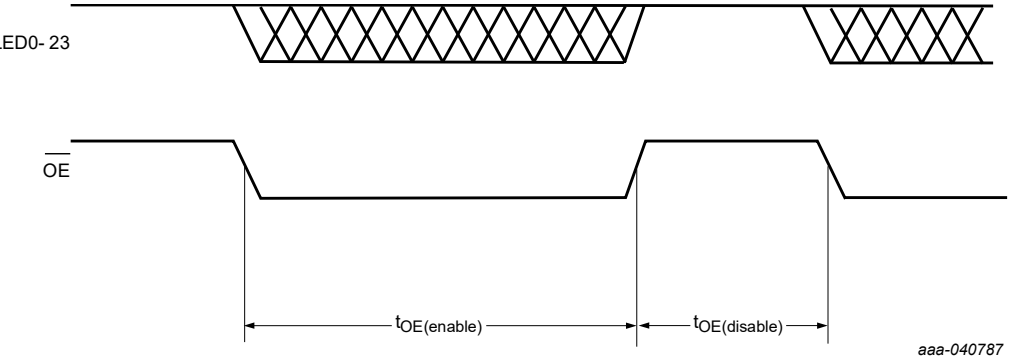
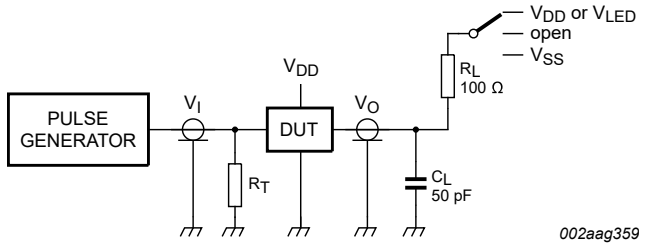


Figure 17. $\overline{OE}$ pin timing

14 Test information



R_L = Load resistor for LEDn.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Figure 18. Test circuitry for switching times

15 Package outline

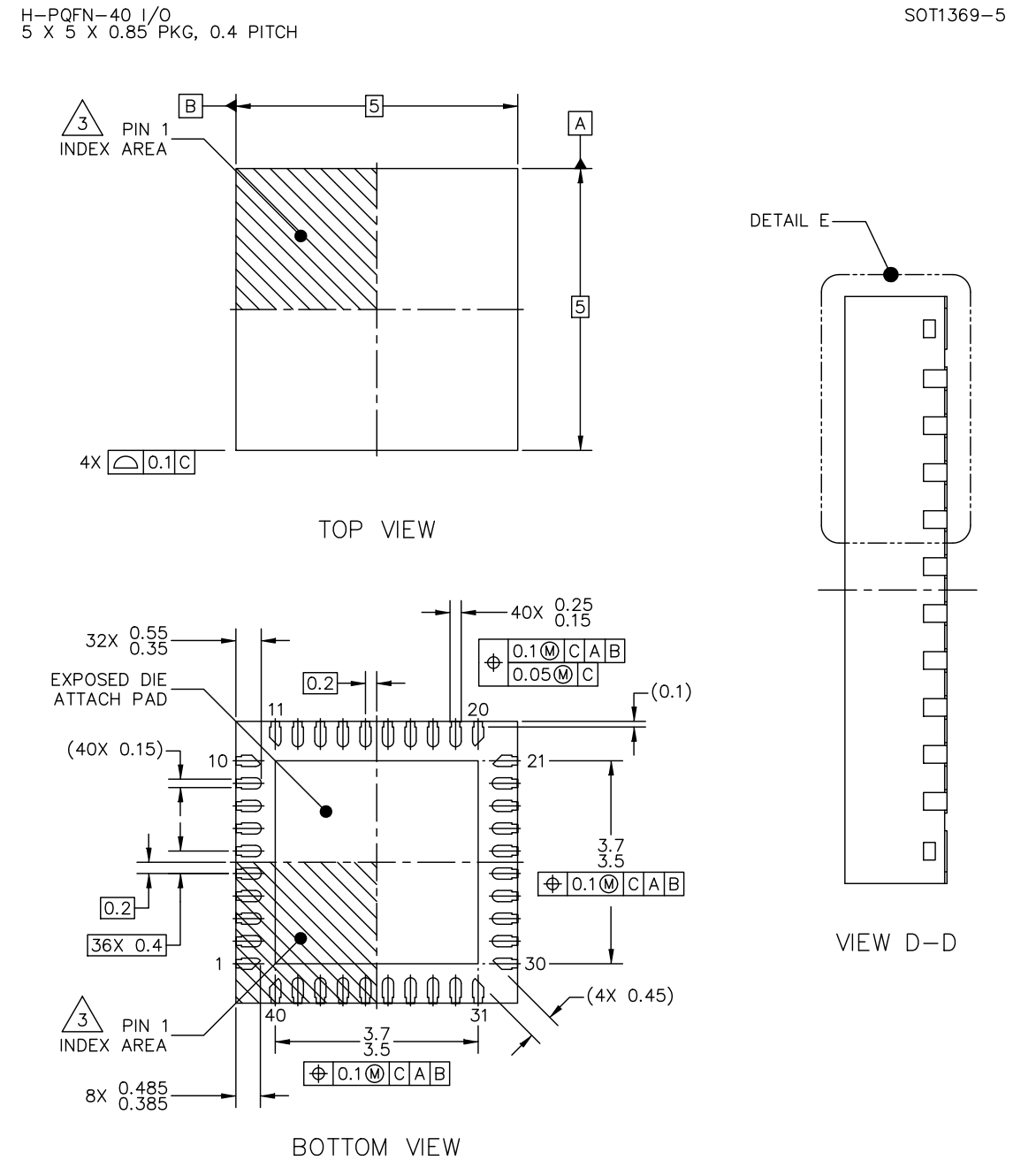
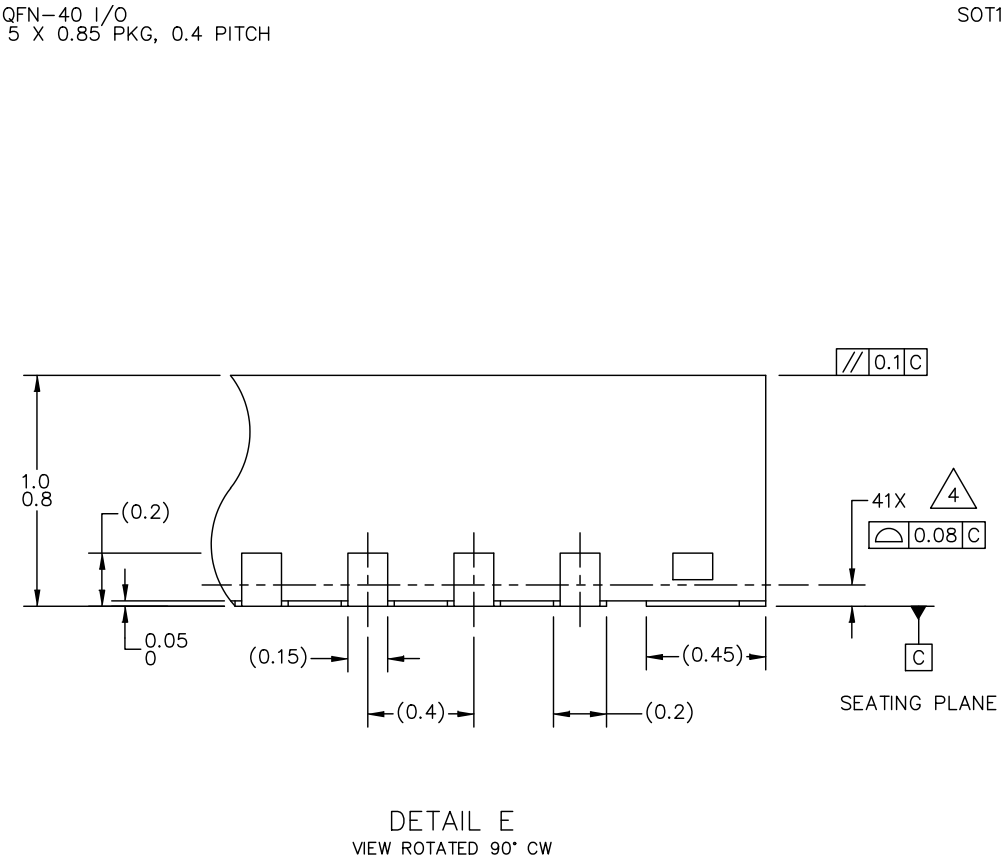


Figure 19. Package outline SOT1369-5 (HVQFN40) (1 of 3)



DATE: 20 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01371D	REVISION: O	

Figure 20. Package outline SOT1369-5 (HVQFN40) (2 of 3)

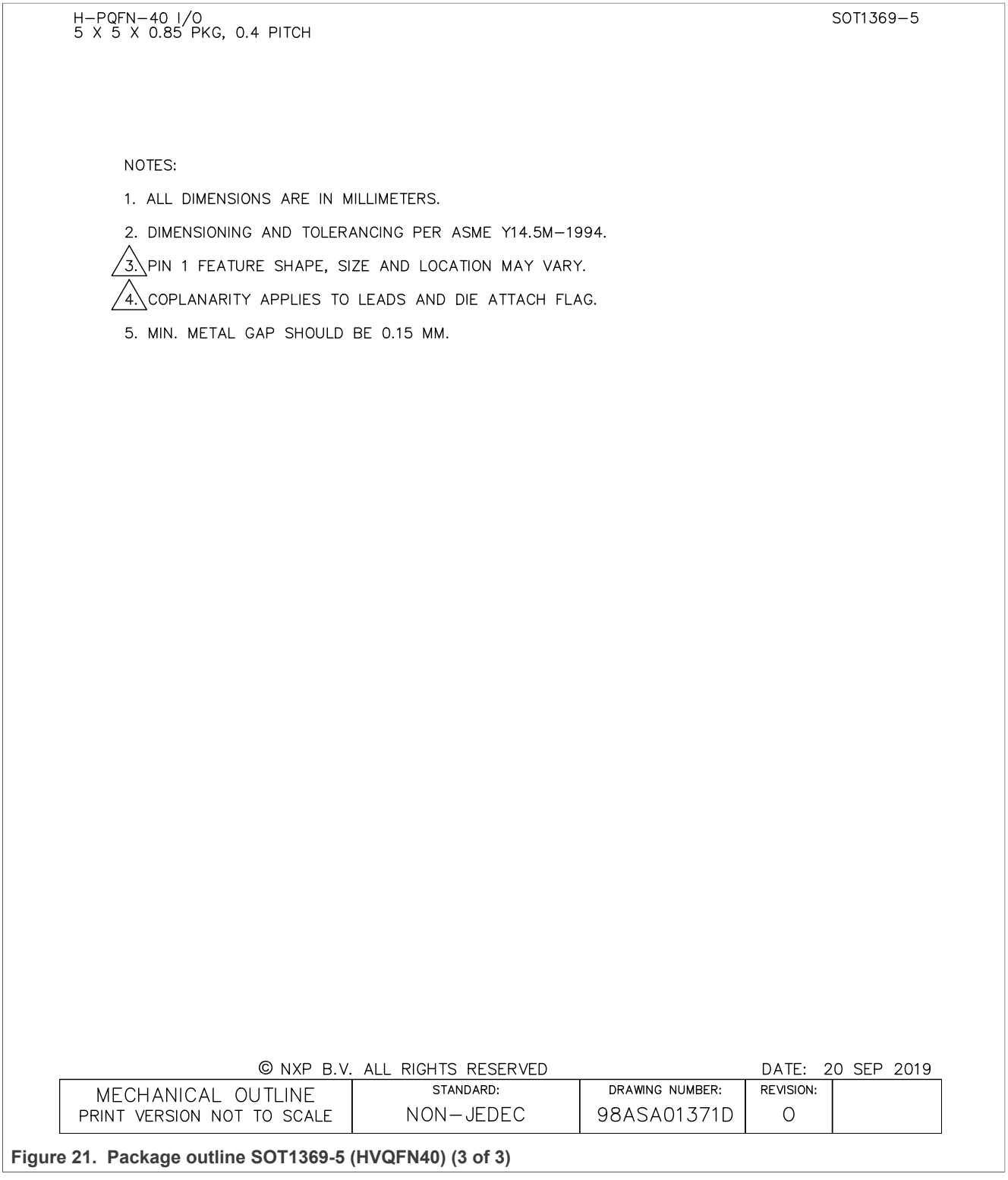


Figure 21. Package outline SOT1369-5 (HVQFN40) (3 of 3)

16 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 27 and Table 28

Table 27. SnPb eutectic process (from J-STD-020D)

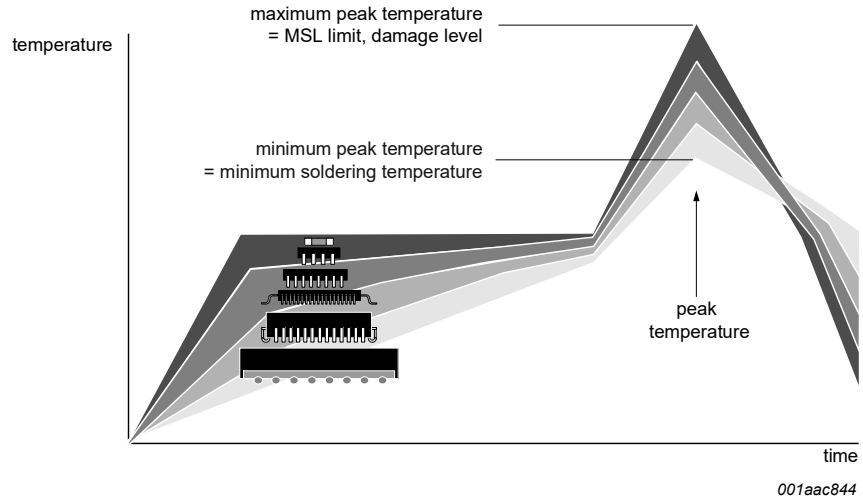
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 28. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Figure 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18 Soldering: PCB footprints

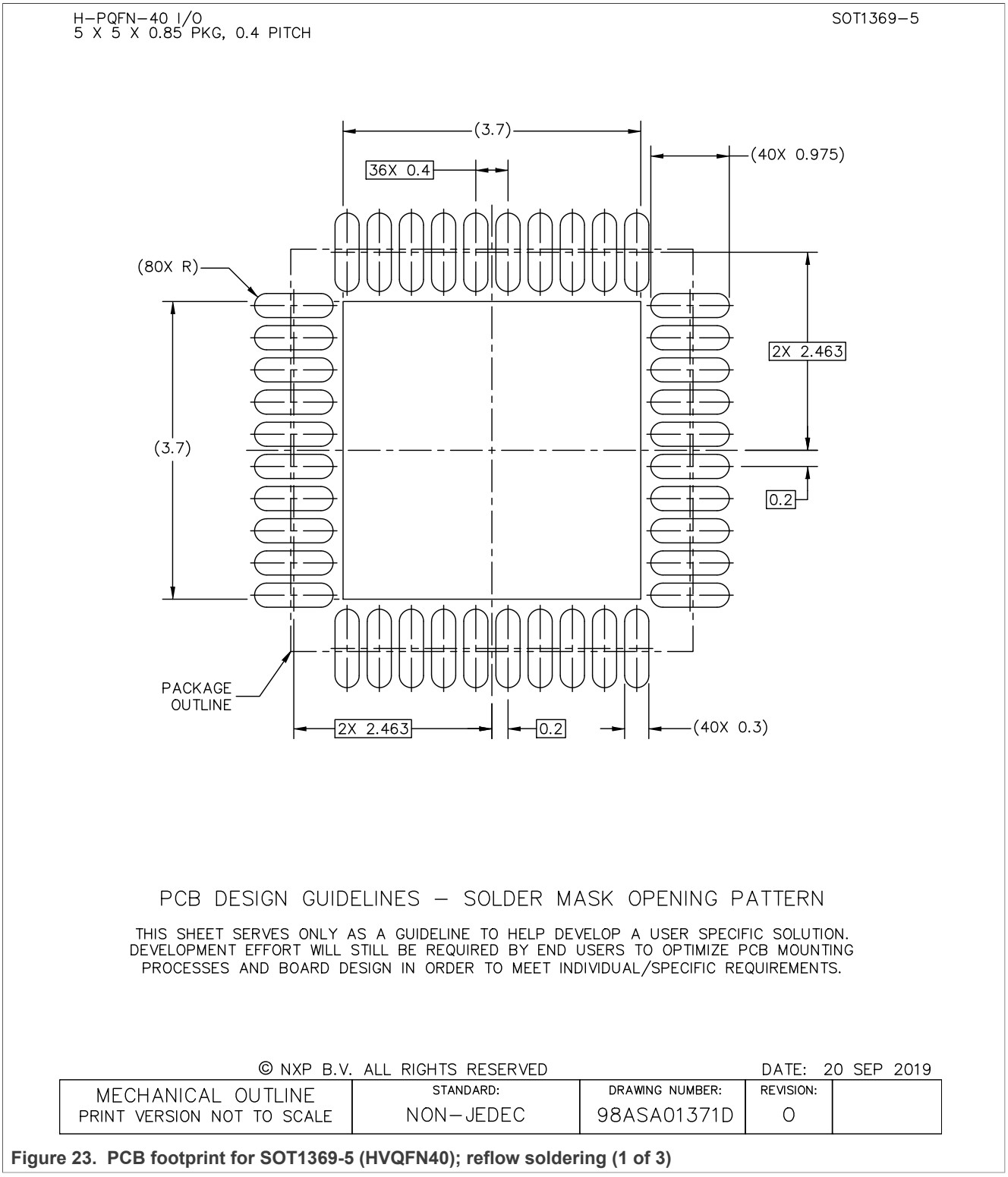


Figure 23. PCB footprint for SOT1369-5 (HVQFN40); reflow soldering (1 of 3)

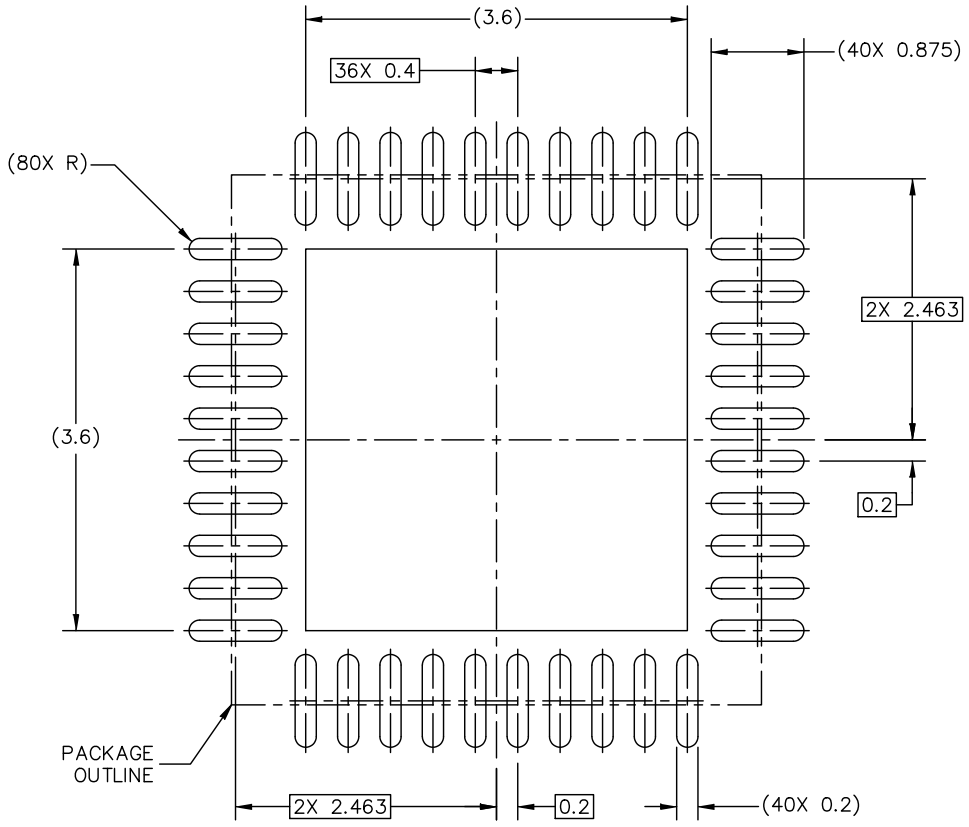


Figure 24. PCB footprint for SOT1369-5 (HVQFN40); reflow soldering (2 of 3)

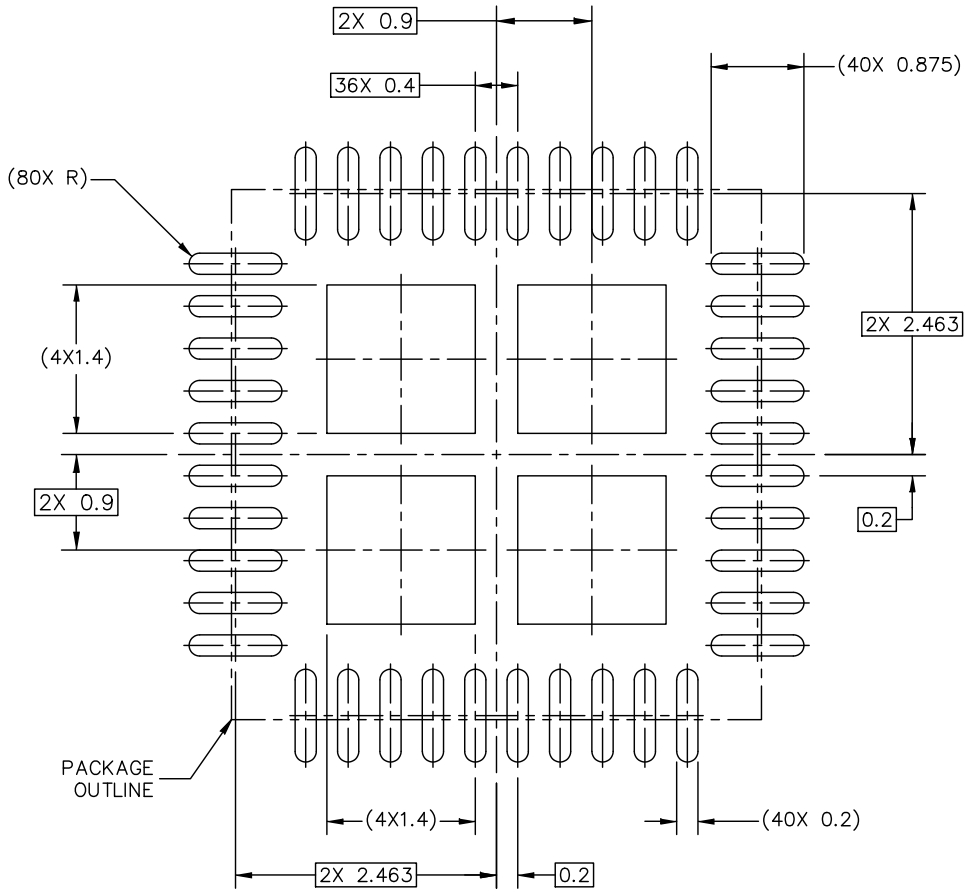


Figure 25. PCB footprint for SOT1369-5 (HVQFN40); reflow soldering (3 of 3)

19 Abbreviations

Table 29. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DAC	Digital-to-Analog Converter
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	MicroController Unit
MISO	Master In, Slave Out
MOSI	Master Out, Slave In
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus
SPI	Serial Peripheral Interface

20 Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9959 v.1.3	20220523	Product data sheet	202205022I	PCA9959 v.1.2
Modifications:	• Section 7.2.10: Removed "+1" from calculation in Table 19, Table 20, Table 21 • Table 21: Corrected typo in title ("2 bit" to "4 bit") and description ("CUR1" to "CUR3")			
PCA9959 v.1.2	20211022	Product data sheet	202110025I	PCA9959 v.1.1
Modifications:	• Table 3: Updated description for $\overline{CS}$ • Section 13: Added $\overline{OE}$ pin enable/disable min time and Figure 17 • Section 8.1: Updated SDO information in sections $\overline{CS}$ and SDO			
PCA9959 v.1.1	20200810	Product data sheet	202007043I	PCA9959 v.1.0
Modifications:	• Table 25: Added Vtrip min value of 1.85 V • Section 7.2.3: Added LED error detection mechanism in open and/or short detection during gradation operation description			
PCA9959 v.1.0	20191024	Product data sheet	-	-

21 Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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