

# NUF9005MN

## Low Capacitance 8 Line EMI Filter with ESD Protection

This device is an 8 line EMI filter array for wireless applications. Greater than -25 dB attenuation is obtained at frequencies from 800 MHz to 2.2 GHz. It also offers ESD protection—clamping transients from static discharges. ESD protection is provided across all capacitors.

### Features

- EMI Filtering and ESD Protection
- Integration of 40 Discrete Components
- Compliance with IEC61000-4-2 (Level 4) > 14 kV (Contact)
- DFN Package, 1.6 x 4.0 mm
- Moisture Sensitivity Level 1
- ESD Ratings: Machine Model = C  
Human Body Model = 3B
- This is a Pb-Free Device

### Benefits

- Reduces EMI/RFI Emissions on a Data Line
- Integrated Solution Offers Cost and Space Savings
- Reduces Parasitic Inductances Which Offer a More “Ideal” Low Pass Filter Response
- Integrated Solution Improves System Reliability

### Applications

- EMI Filtering and ESD Protection for Data Lines
- Wireless Phones
- Handheld Products
- Notebook Computers
- LCD Displays

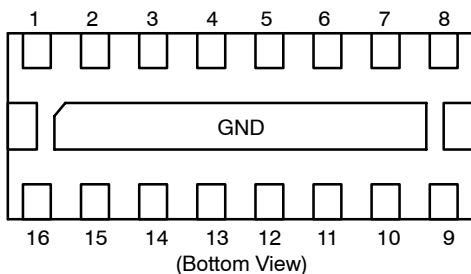
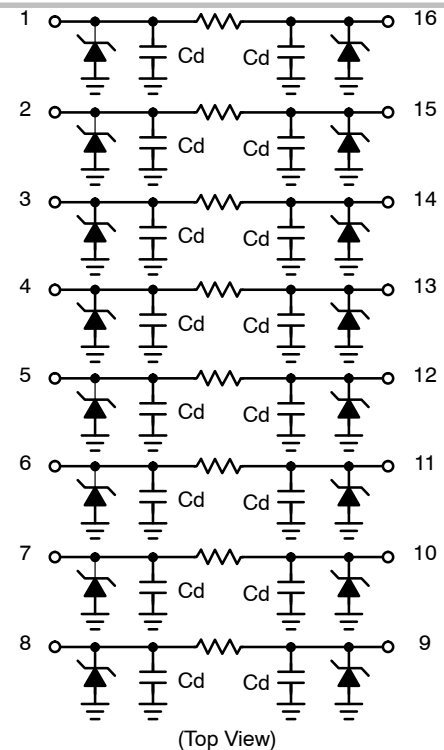


Figure 1. Pin Connections

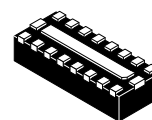


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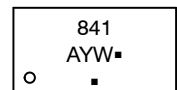


(Top View)



16 DFN16  
CASE 506AC

### MARKING DIAGRAM



- 841 = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(\*Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NUF9005MNT4G	DFN16 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
ESD Discharge IEC61000-4-2 Contact Discharge	$V_{PP}$	14	kV
Steady-State Power per Resistor @ 25°C	$P_R$	328	mW
Operating Temperature Range	$T_{OP}$	-40 to 85	°C
Storage Temperature Range	$T_{STG}$	-55 to 150	°C
Maximum Lead Temperature for Soldering Purposes (1.8 in from case for 10 seconds)	$T_L$	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

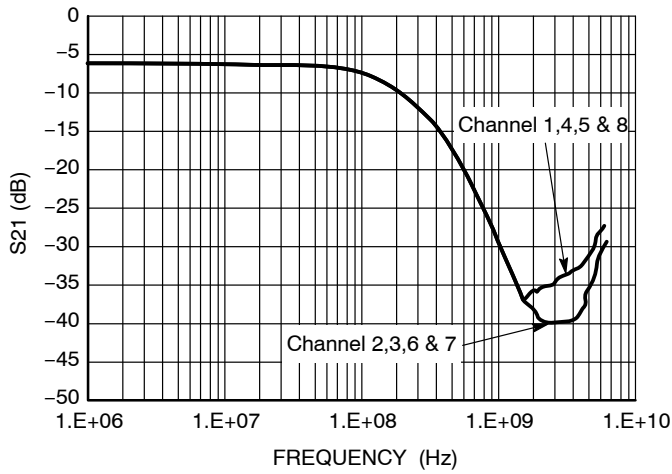
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Reverse Working Voltage	$V_{RWM}$				5.0	V
Breakdown Voltage	$V_{BR}$	$I_R = 1.0 \text{ mA}$	6.0	7.0	8.0	V
Leakage Current	$I_R$	$V_{RWM} = 3.3 \text{ V}$			100	nA
Resistance	$R_A$	$I_R = 20 \text{ mA}$	85	100	115	$\Omega$
Capacitance (Notes 1 and 2)	$C_d$		10	12	15	pF
Cut-Off Frequency (Note 3)	$f_{3dB}$	Above this frequency, appreciable attenuation occurs		175		MHz

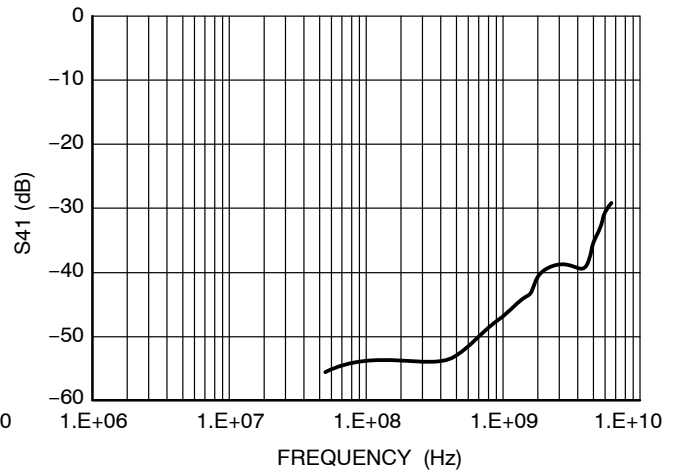
1. Measured at 25°C,  $V_R = 2.5 \text{ V}$ ,  $f = 1.0 \text{ MHz}$ .
2. Total Line Capacitance is 2 times the Diode Capacitance ( $C_d$ ).
3. 50  $\Omega$  source and 50  $\Omega$  load termination.

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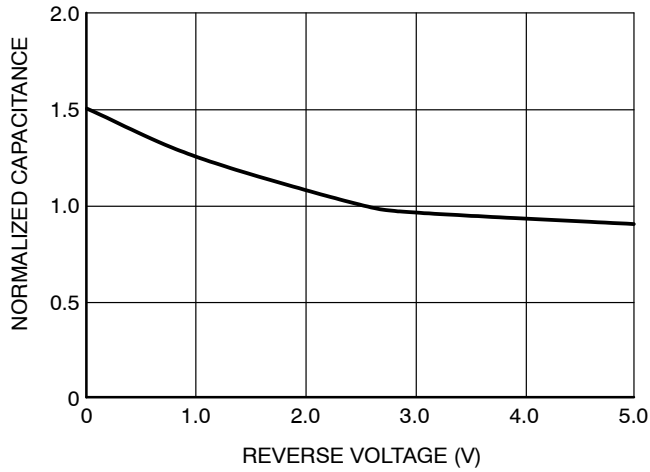
## TYPICAL PERFORMANCE CURVES ( $T_A = 25^\circ\text{C}$ unless otherwise specified)



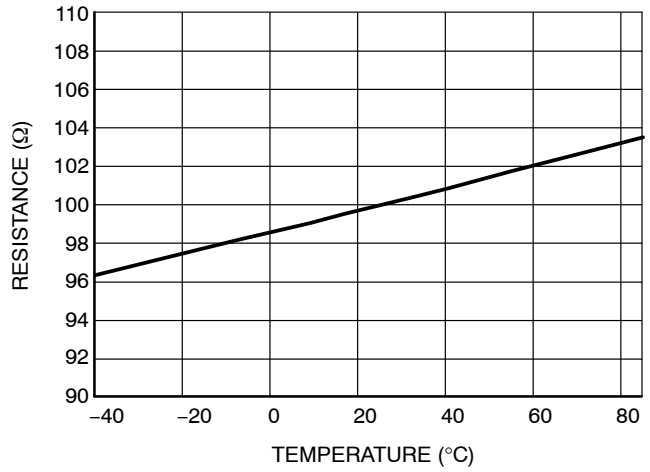
**Figure 2. Typical Insertion Loss Characteristic (S21 Measurement)**



**Figure 3. Analog Crosstalk Curve (S41 Measurement)**



**Figure 4. Typical Capacitance vs. Reverse Biased Voltage (Normalized Capacitance  $C_d$  at 2.5 V)**

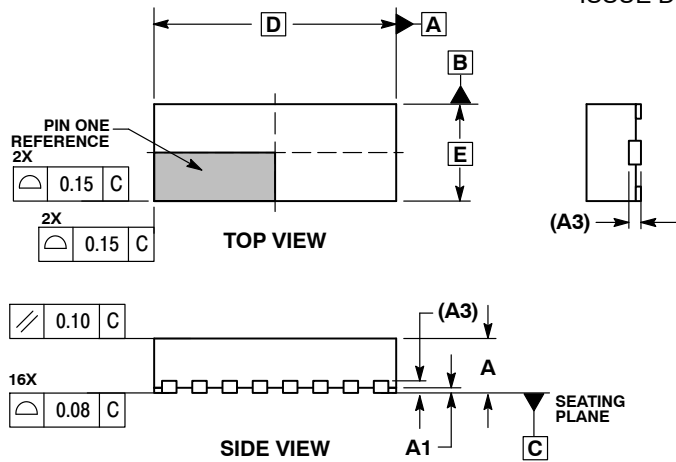


**Figure 5. Typical Resistance over Temperature**

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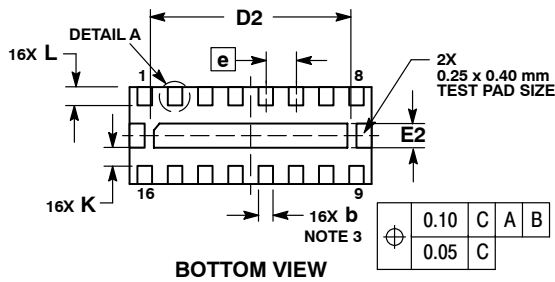
## PACKAGE DIMENSIONS

DFN16, 4x1.6, 0.5P  
CASE 506AC  
ISSUE D

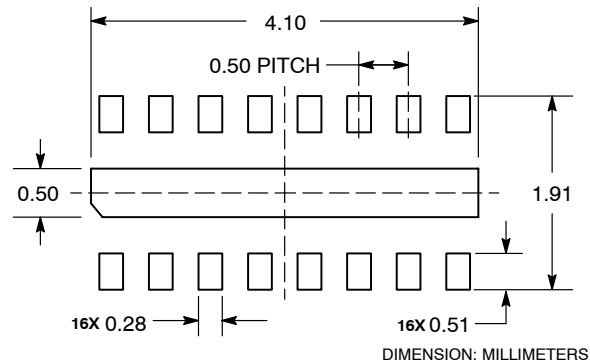


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION b APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	4.00 BSC	
D2	3.10	3.30
E	1.60 BSC	
E2	0.30	0.50
e	0.50 BSC	
K	0.20	---
L	0.20	0.40
L1	0.00	0.15



### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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