

## DRV3202-Q1 3-Phase Brushless Motor Driver

*Not Recommended for New Designs*

### 1 Features

- 3-Phase Pre-drivers for N-channel MOS Field Effect Transistors (MOSFETs)
- Pulse Width Modulation (PWM) Frequency up to 20 kHz
- Fault Diagnostics
- Charge Pump
- Phase Comparators
- Phase Monitoring Sample and Hold Op-Amps
- Central Processing Unit (CPU) Reset Generator
- Serial Port I/F (SPI)
- Motor Current Sense
- 80-pin HTQFP
- Controller Area Network (CAN)
- 5-V Regulator

### 2 Applications

Automotive

### 3 Description

The DRV3202-Q1 device is a field effect transistor (FET) pre-driver designed for 3-phase motor control and its application such as an oil pump or a water pump. It is equipped with three high-side pre-FET drivers and three low-side drivers which are controlled by an external microcontroller (MCU). The power for the high side is supplied by a charge pump and no bootstrap cap is needed. For commutation, this integrated circuit (IC) sends a conditional motor drive signal and output to the MCU. Diagnostics provide undervoltage, overvoltage, overcurrent, overtemperature and power bridge faults. The motor current can be measured using an integrated current sense amplifier and comparator in a battery common-mode range, which allows the motor current to be used in a high-side current sense application. Gain is attained by external resistors. If the MCU does not have enough bandwidth, the phase monitoring sample and hold amplifiers can hold phase information until the MCU is ready to process it. The interfaces include SPI and CAN. The pre-driver and other internal settings can be configured through the SPI. The CAN is used to communicate with other electronic control units (ECUs).

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV3202-Q1	HTQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.1 Functional Block Diagram .....	19
<b>2 Applications</b> .....	<b>1</b>	7.2 Feature Description .....	19
<b>3 Description</b> .....	<b>1</b>	7.3 Device Functional Modes .....	31
<b>4 Revision history</b> .....	<b>2</b>	7.4 Register Maps .....	31
<b>5 Pin Configuration and Functions</b> .....	<b>4</b>	<b>8 Device and Documentation Support</b> .....	<b>35</b>
<b>6 Specifications</b> .....	<b>6</b>	8.1 Receiving Notification of Documentation Updates ..	35
6.1 Absolute Maximum Ratings .....	6	8.2 Community Resources .....	35
6.2 ESD Ratings .....	6	8.3 Trademarks .....	35
6.3 Thermal Information .....	6	8.4 Electrostatic Discharge Caution .....	35
6.4 Electrical Characteristics .....	7	8.5 Glossary .....	35
6.5 Supply Voltage and Current .....	12	<b>9 Mechanical, Packaging, and Orderable</b>	
<b>7 Detailed Description</b> .....	<b>19</b>	<b>Information</b> .....	<b>35</b>

## 4 Revision history

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Changed device status to NRND .....	1

Changes from Original (October, 2012) to Revision A	Page
• Changed max rating for PHTM, PH1M, PH2M, and PH3M from -2 –40 V to -1–40 V. ....	4
• Changed O to IO for pin 44 and 45. ....	5
• Deleted Table 1 Pin Equivalent Circuits. ....	6
• Changed VCANH and VCANL to VCAN_H and VCAN_L in CAN receiver section .....	7
• Added 3 new parameters to VCC and VDD Electrical Characteristics table. Changed min, typ, and max values VLRVCC, CVCC, TVCC1, TVCC2, VDDOV, TVDD. Added table note. ....	8
• Changed VCANH and VCANL to VCAN_H and VCAN_L in CAN AC characteristic section. ....	8
• Changed CANH_D to VCANH_D, CANL_D to VCANL_D, and VCANH - VCANL to VCAN_H - VCAN_L in CAN timing chart. ....	8
• Changed $V_{chv1\_12}$ to $V_{chv1\_1}$ , $V_{chv1\_20}$ to $V_{chv1\_2}$ , $V_{chv2\_12}$ to $V_{chv2\_1}$ , $V_{chv2\_20}$ to $V_{chv2\_2}$ , $V_{chv3\_12}$ to $V_{chv3\_1}$ , $V_{chv3\_20}$ to $V_{chv3\_2}$ .....	9
• Added min and typ values to $V_{chvmax}$ parameter. ....	9
• Changed min, typ and max values for $V_{chv1\_0}$ through $V_{chv3\_2}$ ; changed typ $R_{on}$ value from 10 to 8. ....	9
• Removed $R_{ONH\_H}$ row, removed cross-references from $R_{ONH\_HP}$ and $R_{ONH\_HN}$ , added conditions to $R_{ONH\_HP}$ and $R_{ONH\_HN}$ ; changed typ and max values for $R_{ONH\_HN}$ .....	9
• Removed "side" from $V_{OH\_L}$ and $V_{OL\_L}$ description, changed high side and low side to pull up and pull down respectively for $R_{ONH\_L}$ and $R_{ONL\_L}$ . Changed values for $R_{ONL\_L}$ from 10 typ to 7 typ and from 20 max to 14 max in pre-driver electrical characteristics table. ....	9
• Changed Turn-off time from $T_{off\_h}$ to $T_{off\_l}$ .....	9
• Changed min value for $V_{inm}$ from -2 to -1. ....	10
• Added $C1 = 4.7$ pF to $T_{set\_TR1}$ , $T_{set\_TR2}$ , $T_{set\_TF1}$ , and $T_{set\_TF2}$ conditions in motor current sense electrical characteristics ...	10
• Changed max current limit from 500 to 550. ....	12
• Added typ and max values to VB monitor electrical characteristics table .....	12
• Changed max $I_{VB}$ from 40 to 35 mA. ....	12
• Changed ICANH to IA_CANH and ICANL to IA_CANL in CAN testing condition image .....	14

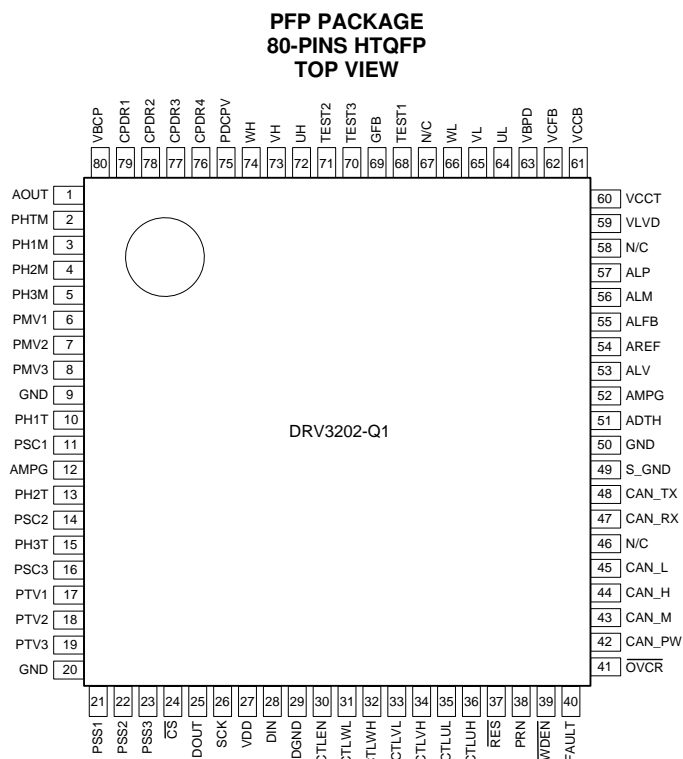
- Changed CANTX to CAN\_TX and CANH and CANL to CAN\_H and CAN\_L in CAN reset function image. .... 15
- Changed CANH and CANL to CAN\_H and CAN\_L in description section; changed CANH, CANL, and CANM to CAN\_H, CAN\_L, and CAN\_M in block diagram. .... 22
- Changed charge pump description..... 22
- Changed pre-driver description and updated block diagram..... 23
- Updated phase comparator description. .... 24
- Changed motor current sense description and motor current sense block diagram..... 25
- Updated Sample and Hold Mode Block Diagram..... 25
- Changed V<sub>CC</sub> Block Diagram..... 27
- Changed VB Monitor description..... 28
- Changed thermal shutdown description. .... 29
- Changed location of EN in Figure 34. .... 30
- Changed MCU RESET column to  $\overline{\text{RES}}$  column; changed values..... 31

DRV3202-Q1

SLVSBJ4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

## 5 Pin Configuration and Functions



### Pin Functions

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
1	AOUT	O	-0.3–6 V	Test mode output
2	PHTM	I	-1–40 V	Phase comparator reference input
3	PH1M	I	-1–40 V	Phase comparator input
4	PH2M	I	-1–40 V	Phase comparator input
5	PH3M	I	-1–40 V	Phase comparator input
6	PMV1	O	-0.3–6 V	Phase comparator output
7	PMV2	O	-0.3–6 V	Phase comparator output
8	PMV3	O	-0.3–6 V	Phase comparator output
9, 20, 50	GND	I	-0.3–0.3 V	GND
10	PH1T	I	-2–40 V	Phase amplifier input
11	PSC1	O	-0.3–6 V	Sample and hold filter output
12	AMPG	I	-0.3–0.3 V	Quiet GND
13	PH2T	I	-2–40 V	Phase amplifier input
14	PSC2	O	-0.3–6 V	Sample and hold filter output
15	PH3T	I	-2–40 V	Phase amplifier input
16	PSC3	O	-0.3–6 V	Sample and hold filter output
17	PTV1	O	-0.3–6 V	Phase amplifier output
18	PTV2	O	-0.3–6 V	Phase amplifier output
19	PTV3	O	-0.3–6 V	Phase amplifier output
21	PSS1	I	-0.3–6 V	Sample and hold control signal input
22	PSS2	I	-0.3–6 V	Sample and hold control signal input
23	PSS3	I	-0.3–6 V	Sample and hold control signal input

**Pin Functions (continued)**

NO.	PIN		MAX RATING	FUNCTION
	NAME	TYPE		
24	$\overline{\text{CS}}$	I	–0.3–6 V	SPI chip select
25	DOUT	O	–0.3–6 V	SPI data output
26	SCK	I	–0.3–6 V	SPI clock
27	VDD	O	–0.3–3.6 V	Digital supply output
28	DIN	I	–0.3–6 V	SPI data input
29	DGND	I	–0.3–0.3 V	Digital GND
30	CTLEN	I	–0.3–6 V	Pre-driver parallel enable input
31	CTLWL	I	–0.3–6 V	Pre-driver parallel input
32	CTLWH	I	–0.3–6 V	Pre-driver parallel input
33	CTLVL	I	–0.3–6 V	Pre-driver parallel input
34	CTLVH	I	–0.3–6 V	Pre-driver parallel input
35	CTLUL	I	–0.3–6 V	Pre-driver parallel input
36	CTLUH	I	–0.3–6 V	Pre-driver parallel input
37	$\overline{\text{RES}}$	O	–0.3–6 V	Reset output
38	PRN	I	–0.3–6 V	Pulse input
39	$\overline{\text{WDEN}}$	I	–0.3–6 V	Reset generator enable input
40	FAULT	O	–0.3–6 V	Diagnosis output
41	$\overline{\text{OVCR}}$	I	–0.3–6 V	Over current reset input
42	CAN_PW	I	–0.3–6 V	CAN supply input
43	CAN_M	O	–27–40 V	CAN transceiver middle point terminal
44	CAN_H	IO	–27–40 V	CAN transceiver positive terminal
45	CAN_L	IO	–27–40 V	CAN transceiver negative terminal
46, 58, 67	N/C	—	—	Not connected
47	CAN_RX	O	–0.3–6 V	CAN digital output
48	CAN_TX	I	–0.3–6 V	CAN digital input
49	S_GND	I	–0.3–0.3 V	CAN GND
51	ADTH	I	–0.3–6 V	Motor overcurrent threshold input
52	AMPG	I	–0.3–0.3 V	Quiet GND
53	ALV	O	–0.3–6 V	Motor current sense amp output
54	AREF	O	–0.3–40 V	Motor current sense reference output
55	ALFB	O	–0.3–40 V	Motor current sense amp feedback
56	ALM	I	–0.3–40 V	Motor current sense amp negative input
57	ALP	I	–0.3–40 V	Motor current sense amp positive input
59	VLVD	I	–0.3–6 V	V <sub>CC</sub> undervoltage threshold input
60	VCCT	I	–0.3–6 V	V <sub>CC</sub> supply input
61	VCCB	O	–0.3–40 V	V <sub>CC</sub> regulator base drive for PNP external transistor
62	VCFB	I	–0.3–40 V	V <sub>CC</sub> regulator current sense input
63	VBPD	I	–0.3–40 V	VB input
64	UL	O	–0.3–20 V	Pre-driver output
65	VL	O	–0.3–20 V	Pre-driver output
66	WL	O	–0.3–20 V	Pre-driver output
68	TEST1	I	–0.3–6 V	Test input
69	GFB	I	–0.3–0.3 V	Power GND
70	TEST3	I	–0.3–20 V	Test input
71	TEST2	I	–0.3–6 V	Test input
72	UH	O	–0.3–40 V	Pre-driver output

**DRV3202-Q1**

SLVSBJ4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

**Pin Functions (continued)**

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
73	VH	O	–0.3–40 V	Pre-driver output
74	WH	O	–0.3–40 V	Pre-driver output
75	PDCPV	O	–0.3–40 V	Charge pump output
76	CPDR4	O	–0.3–40 V	Charge pump output
77	CPDR3	O	–0.3–40 V	Charge pump output
78	CPDR2	O	–0.3–40 V	Charge pump output
79	CPDR1	O	–0.3–40 V	Charge pump output
80	VBCP	I	–0.3–4 0V	VB input

**6 Specifications****6.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$T_A$	Operating temperature range	–40	125	degree
$T_J$	Junction temperature	–40	150	degree
$T_s$	Storage temperature	–55	150	degree

**6.2 ESD Ratings**

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge <sup>(1)</sup>	Human-body model (HBM)	±2000
		Charged-device model (CDM)	±500

(1) ESD testing is performed according to the ACE-Q100 standard.

**6.3 Thermal Information**

THERMAL METRIC <sup>(1)</sup>		DRV3202-Q1	UNIT
		PPF (HTQFP)	
		80 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	23.0	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	7.5	°C/W
$\theta_{JB}$	Junction-to-board thermal resistance	7.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	7.4	°C/W
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.4 Electrical Characteristics

VB = 12 V, TA = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>WATCHDOG</b>							
VSTN	Function start V <sub>CC</sub> voltage $\overline{\text{RES}}$	Refer to <a href="#">Figure 1</a>	–	0.8	1.3	V	
t <sub>ON</sub>	Power-on time $\overline{\text{RES}}$		32	40	48	ms	
t <sub>OFF</sub>	Clock off reset time $\overline{\text{RES}}$		64	80	96	ms	
t <sub>RL</sub>	Reset pulse low time $\overline{\text{RES}}$		16	20	24	ms	
t <sub>RH</sub>	Reset pulse high time $\overline{\text{RES}}$		64	80	96	ms	
t <sub>RES</sub>	Reset delay time $\overline{\text{RES}}$		30	71.5	90	μs	
P <sub>wth</sub>	Pulse width PRN		200	–	–	ns	
<b>SPI</b>							
F <sub>op</sub>	Operating frequency	Refer to <a href="#">Figure 2</a>	DC	–	4	MHz	
T <sub>lead</sub>	Enable lead time		100	–	–	ns	
T <sub>wait</sub>	Wait time between two successive communications		5	–	–	μs	
T <sub>lag</sub>	Enable lag time		100	–	–	ns	
T <sub>pw</sub>	SCLK pulse width		100	–	–	ns	
T <sub>su</sub>	Data setup time		80	–	–	ns	
T <sub>h</sub>	Data hold time		80	–	–	ns	
T <sub>dis</sub>	Disable time		–	–	80	ns	
T <sub>del</sub>	Data delay time (SCK to DOUT)		C <sub>L</sub> = 50 pF, Refer to <a href="#">Figure 2</a>	–	–	80	ns
<b>CAN (TRANSMITTER SECTION)</b>							
VCAN <sub>H</sub>	Bus voltage recessive	CAN <sub>TX</sub> = V <sub>CC</sub> , I <sub>CANH</sub> = I <sub>CANL</sub> = 0, see <a href="#">Figure 3</a>	2	2.5	3	V	
VCAN <sub>L</sub>			2	2.5	3	V	
V <sub>DIFF</sub> = (VCAN <sub>H</sub> – VCAN <sub>L</sub> )	Differential output voltage		–500	0	50	mV	
VCAN <sub>H</sub>	Bus voltage recessive 2		CAN <sub>TX</sub> = V <sub>CCRL</sub> = 60 Ω between CAN <sub>H</sub> and CAN <sub>L</sub> , see <a href="#">Figure 3</a> and <a href="#">Figure 4</a>	2.25	2.5	2.75	V
VCAN <sub>L</sub>	Bus voltage recessive 2			2.25	2.5	2.75	V
VCAN <sub>H</sub> <sub>D</sub>	Dominant state CAN <sub>H</sub> output voltage		CAN <sub>TX</sub> = 0 V, R <sub>L</sub> = 60 Ω between CAN <sub>H</sub> and CAN <sub>L</sub> , see <a href="#">Figure 3</a>	2.75	3.5	4.5	V
VCAN <sub>L</sub> <sub>D</sub>	Dominant state CAN <sub>L</sub> output voltage			0.5	1.5	2.25	V
V <sub>DIFF</sub> = (VCAN <sub>H</sub> <sub>D</sub> – VCAN <sub>L</sub> <sub>D</sub> )	Differential output voltage		CAN <sub>TX</sub> = 0 V, R <sub>L</sub> = 60 Ω between CAN <sub>H</sub> and CAN <sub>L</sub>	1.5	2	3	V
IA <sub>CANH</sub>	CAN <sub>H</sub> short circuit threshold current		CAN <sub>TX</sub> = 0 V	70	–	160	mA
IA <sub>CANL</sub>	CAN <sub>L</sub> short circuit threshold current	CAN <sub>TX</sub> = 0 V	70	–	160	mA	
t <sub>OVCAN</sub>	Overcurrent to output switch-off delay	Refer to <a href="#">Figure 6</a>	200			ns	
T <sub>RESCAN</sub>	Self recovery time	Refer to <a href="#">Figure 6</a>	8	25	50	μs	
<b>CAN (RECEIVER SECTION)</b>							
V <sub>DOM</sub>	Differential input voltage for dominant state (V <sub>DIFF</sub> = VCAN <sub>H</sub> – VCAN <sub>L</sub> )	VCAN <sub>L</sub> = –12 V to 12 V, CAN <sub>TX</sub> = V <sub>CC</sub>	900			mV	
V <sub>REC</sub>	Differential input voltage for recessive state (V <sub>DIFF</sub> = VCAN <sub>H</sub> – VCAN <sub>L</sub> )	VCAN <sub>L</sub> = –12 V to 12 V, CAN <sub>TX</sub> = V <sub>CC</sub>			500	mV	
V <sub>hys</sub>	Differential input hysteresis		80	150	–	mV	

**DRV3202-Q1**

SLVSB4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

**Electrical Characteristics (continued)**

VB = 12 V, TA = -40°C to 125°C (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{com} = \frac{VCAN\_H - VCAN\_L}{2}$ Input common mode voltage range		-12	-	12	V
R <sub>IN</sub>	Input resistance CAN_H, CAN_L CAN_TX = V <sub>CC</sub>	5	-	50	kΩ
R <sub>DIFF</sub>	Differential input resistance CAN_TX = V <sub>CC</sub>	10	-	100	kΩ
C <sub>IN</sub> (1)	Input capacitance to ground CAN_H, CAN_L CAN_TX = V <sub>CC</sub>	-	20	46	pF
C <sub>DIFF</sub> (1)	Differential input capacitance to ground CAN_TX = V <sub>CC</sub>	-	10	-	pF
C <sub>IN</sub> (1)	Input capacitance between CAN_H and CAN_L CAN_TX = V <sub>CC</sub>	-	-	46	pF
<b>CAN (AC CHARACTERISTIC)</b>					
t <sub>TDhHS</sub>	Delay time from CAN_TX to VDIFF = VCAN_H - VCAN_L Refer to <a href="#">Figure 3</a>	-	-	100	ns
t <sub>TDIHS</sub>	Refer to <a href="#">Figure 3</a>	-	-	100	ns
t <sub>DRHS</sub>	Delay time from VDIFF = VCAN_H - VCAN_L to CAN_RX Refer to <a href="#">Figure 3</a>	-	-	150	ns
t <sub>TRIHS</sub>	Delay time from CAN_TX to CAN_RX Refer to <a href="#">Figure 3</a>	-	-	300	ns
t <sub>TRhHS</sub>	Refer to <a href="#">Figure 3</a>	-	-	300	ns
SRHS_R	Slew rate, CAN_H, rise Threshold set to 20%–80%		20	85	ns
SRHS_F	Slew rate, CAN_H, fall Threshold set to 80%–20%		20	85	ns
SRLS_R	Slew rate, CAN_L, rise Threshold set to 20%–80%		20	85	ns
SRLS_F	Slew rate, CAN_L, fall Threshold set to 80%–20%		20	85	ns
<b>CAN (SPLIT, OPTIONAL)</b>					
VCAN_M <sub>I</sub>	Output voltage I <sub>source</sub> , I <sub>sink</sub> = 500 μA	0.3	0.5	0.7	V <sub>CC</sub>
VCAN_M <sub>U</sub>	Output voltage, unloaded condition R <sub>measure</sub> > 1 MΩ	0.45	0.5	0.55	V <sub>CC</sub>
<b>CAN (POWER OFF CONDITION)</b>					
R <sub>IN</sub>	Input resistance CAN_H, CAN_L VB = 0 V	10	-	100	kΩ

(1) Specified by design



**Electrical Characteristics (continued)**

VB = 12 V, TA = -40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CHARGE PUMP<sup>(1)</sup></b>						
V <sub>chv1_0</sub>	Output voltage	VB = 5.3 V, I <sub>load</sub> = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 7	VB + 8	VB + 9	V
V <sub>chv1_1</sub>		VB = 5.3 V, I <sub>load</sub> = 5 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 6	VB + 7	VB + 8	V
V <sub>chv1_2</sub>		VB = 5.3 V, I <sub>load</sub> = 8 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 5	VB + 6	VB + 7	V
V <sub>chv2_0</sub>		VB = 12 V, I <sub>load</sub> = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 13	VB + 14	VB + 15	V
V <sub>chv2_1</sub>		VB = 12 V, I <sub>load</sub> = 11 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 13	VB + 14	VB + 15	V
V <sub>chv2_2</sub>		VB = 12 V, I <sub>load</sub> = 18 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 12.5	VB + 13.5	VB + 15	V
V <sub>chv3_0</sub>		VB = 18 V, I <sub>load</sub> = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 13	VB + 14	VB + 15	V
V <sub>chv3_1</sub>		VB = 18 V, I <sub>load</sub> = 13 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 13	VB + 14	VB + 15	V
V <sub>chv3_2</sub>		VB = 18 V, I <sub>load</sub> = 22 mA, C1 = C2 = 47 nF, CCP = 2.2 μF	VB + 13	VB + 14	VB + 15	V
V <sub>chvmax</sub>	Maximum voltage		35	37.5	40	V
V <sub>chvUV</sub>	Undervoltage detection threshold		VB + 4	VB + 4.5	VB + 5	V
T <sub>chv</sub> <sup>(1)</sup>	Rise time	VB = 5.3 V, C1 = C2 = 47 nF, CCP = 2.2 μF, V <sub>chvUV</sub> released		1	2	ms
R <sub>on</sub>	On resistance S1~S4			8		Ω
<b>HIGH SIDE PRE-DRIVER</b>						
V <sub>OH_H</sub>	Output voltage high	I <sub>sink</sub> = 10 mA, U(V/W)H – GFB	V <sub>chv</sub> – 2.7	V <sub>chv</sub> – 1.35		V
V <sub>OL_H</sub>	Output voltage low	I <sub>source</sub> = 10 mA, U(V/W)H – GFB		60	120	mV
R <sub>ONH_HP</sub>	ON resistance pull up (Pch)	U(V/W)H = PDCPV - 1 V		135	270	Ω
R <sub>ONH_HN</sub>	ON resistance pull up (Nch)	U(V/W)H = PDCPV - 2.5 V		8	16	Ω
R <sub>ONL_H</sub>	ON resistance pull down			6	12	Ω
T <sub>on_h</sub> <sup>(1)</sup>	Turn-on time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 11 nF, R <sub>L</sub> = 0 Ω from 20% to 80%	100	300	500	ns
T <sub>off_h</sub> <sup>(1)</sup>	Turn-off time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 11 nF, R <sub>L</sub> = 0 Ω from 80% to 20%	100	300	500	ns
T <sub>h-ondly</sub> <sup>(1)</sup>	Output delay time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 11 nF, R <sub>L</sub> = 0 Ω to 20%, see Figure 7	100	200	400	ns
T <sub>h-offdly</sub> <sup>(1)</sup>	Output delay time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 11 nF, R <sub>L</sub> = 0 Ω to 80%, see Figure 7	100	200	400	ns
<b>LOW SIDE PRE-DRIVER</b>						
V <sub>OH_L</sub>	Output voltage high	I <sub>sink</sub> = 10 mA, U(V/W)L – GFB	VB – 0.14	VB-0.07		V
V <sub>OL_L</sub>	Output voltage low	I <sub>source</sub> = 10 mA, U(V/W)L – GFB		70	140	mV
R <sub>ONH_L</sub>	ON resistance pull up			7	14	Ω
R <sub>ONL_L</sub>	ON resistance pull down			7	14	Ω
T <sub>on_l</sub> <sup>(1)</sup>	Turn-on time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 22 nF, R <sub>L</sub> = 0 Ω from 20% to 80%	100	300	800	ns
T <sub>off_l</sub> <sup>(1)</sup>	Turn-off time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 22 nF, R <sub>L</sub> = 0 Ω from 80% to 20%	100	300	800	ns

DRV3202-Q1

SLVSB4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

Electrical Characteristics (continued)

VB = 12 V, TA = -40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>I-ondly</sub> <sup>(1)</sup>	Output delay time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 22 nF, R <sub>L</sub> = 0 Ω to 20%, see Figure 7	100	200	400	ns
T <sub>I-offdly</sub> <sup>(1)</sup>	Output delay time	VB = 5.3 ~ 18 V, C <sub>L</sub> = 22 nF, R <sub>L</sub> = 0 Ω to 80%, see Figure 7	100	200	400	ns
V <sub>CLAMP</sub>	VGS protection voltage		16	18	20	V
T <sub>diff1</sub> <sup>(1)</sup>	Differential time 1	VB = 5.3 ~ 18 V (T <sub>h-on</sub> ) – (T <sub>h-off</sub> ), see Figure 7	-300		300	ns
T <sub>diff2</sub> <sup>(1)</sup>	Differential time 2	VB = 5.3 ~ 18 V (T <sub>l-on</sub> ) – (T <sub>h-off</sub> ), see Figure 7	-300		300	ns
<b>PHASE COMPARATOR</b>						
V <sub>iofs</sub>	Input offset voltage		-15	-	15	mV
V <sub>inp</sub>	Input voltage range (PHTM)	VB = 5.3 ~ 18 V	1.325	-	4.5	V
V <sub>inm</sub>	Input voltage range (PHxM)		-1	-	VB	V
V <sub>ihys</sub>	Input hysteresis voltage		100	200	400	mV
V <sub>OH</sub>	Output high voltage	I <sub>sink</sub> = 2.5 mA	0.9 × V <sub>CC</sub>	-	-	V
V <sub>OL</sub>	Output low voltage	I <sub>source</sub> = 2.5 mA	-	-	0.1 × V <sub>CC</sub>	V
T <sub>res_tr</sub> <sup>(1)</sup>	Response time (rising)	C <sub>L</sub> = 100 pF	-	0.2	0.5	μs
T <sub>res_tf</sub> <sup>(1)</sup>	Response time (falling)	C <sub>L</sub> = 100 pF	-	0.4	1	μs
<b>MOTOR CURRENT SENSE<sup>(2)</sup></b>						
V <sub>Ofs</sub>	Input offset voltage		-5		5	mV
V <sub>O_0</sub>	Output voltage (ALV)	VB = 5.3 ~ 18 V, I <sub>motor</sub> = 0 A		1		V
V <sub>Line</sub>	Linearity (ALV)	VB = 5.3 ~ 18 V, R <sub>shunt</sub> = 1 mΩ, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ	-2%	30	2%	mV/A
V <sub>Gain</sub>	Gain		10		30	
T <sub>set_TR1</sub>	Settling time (Rise) ALV ±1%	VB = 5.3 ~ 18 V, R <sub>shunt</sub> = 1 mΩ, C1 = 4.7 pF, C <sub>L</sub> = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I <sub>motor</sub> = 0 → 30 A, (ALV : 1 → 1.9 V)	-	1	2.5	μs
T <sub>set_TR2</sub>	Settling time (Rise) ALV ±1%	VB = 5.3 ~ 18 V, R <sub>shunt</sub> = 1 mΩ, C1 = 4.7 pF, C <sub>L</sub> = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I <sub>motor</sub> = 0 → 100 A, (ALV : 1 → 4 V)	-	1	2.5	μs
T <sub>set_TF1</sub>	Settling time (Fall) ALV ±1%	VB = 5.3 ~ 18 V, R <sub>shunt</sub> = 1 mΩ, C1 = 4.7 pF, C <sub>L</sub> = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I <sub>motor</sub> = 30 → 0 A, (ALV : 1.9 → 1 V)	-	1	2.5	μs
T <sub>set_TF2</sub>	Settling time (Fall) ALV ±1%	VB = 5.3 ~ 18 V, R <sub>shunt</sub> = 1 mΩ, C1 = 4.7 pF, C <sub>L</sub> = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I <sub>motor</sub> = 100 → 0 A, (ALV : 4 → 1 V)	-	1	2.5	μs

(2) Motor current is converted to voltage in test

**Electrical Characteristics (continued)**
 $V_B = 12\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVAD	Overcurrent threshold	150-A detection, $R_{shunt} = 1\text{ m}\Omega$ , $R_{11} = R_{12} = 1\text{ k}\Omega$ , $R_{21} = R_{22} = 30\text{ k}\Omega$ , $R_3 = 8.2\text{ k}\Omega$ , $R_4 = 10\text{ k}\Omega$	-10%	150	10%	A
TDEL_OV AD <sup>(1)</sup>	Propagation delay (Rise or fall)		–	–	1.5	$\mu\text{s}$
<b>PHASE AMPLIFIER</b>						
$V_{ofs\_SH}$	Output offset voltage, sample and hold mode	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1	-50	–	50	mV
$V_{ofs\_TH}$	Output offset voltage, through mode	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1	-50	–	50	mV
$V_{in\_cm}$	Common mode input range	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1–4	1.5		$V_B - 1.5$	V
$V_{out\_max}$	Maximum output voltage	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1–4	4.5	–	–	V
$V_{out\_min}$	Minimum output voltage	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1–4	–	–	0.5	V
$V_{gain}^{(3)}$	Gain		–	1 2 3 4	–	
$V_{out\_SH0}$	Output voltage, sample and hold mode	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1–4, PHxT = $V_B / 2$	–	2.5	–	V
$V_{out\_TH0}$	Output voltage, through mode	$V_B = 5.3\text{--}18\text{ V}$ , Gain = 1–4 PHxT = $V_B / 2$	–	2.5	–	V
$V_{out\_SH1}$	Output voltage, sample and hold mode	$V_B = 12\text{ V}$ , Gain = 1, PHxT = 1.5 V	–	1.375	–	V
$V_{out\_TH1}$	Output voltage, through mode	$V_B = 12\text{ V}$ , Gain = 1, PHxT = 1.5 V	–	1.375	–	V
$V_{out\_SH2}$	Output voltage, sample and hold mode	$V_B = 12\text{ V}$ , Gain = 1, PHxT = 10.5 V	–	3.625	–	V
$V_{out\_TH2}$	Output voltage, through mode	$V_B = 12\text{ V}$ , Gain = 1, PHxT = 10.5 V	–	3.625	–	V
STL_SHT R	Settling time (rise), sample and hold mode PTVx $\pm 1\%$	$V_B = 12\text{ V}$ , Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 1.5 V $\geq$ 10.5 V, (PTVx = 1.375 V $\rightarrow$ 3.625 V), see <a href="#">Figure 12</a>		1.5	3	$\mu\text{s}$
STL_THTR	Settling time (rise), through mode PTVx $\pm 1\%$	$V_B = 12\text{ V}$ , Gain = 1, PTVx = 100 pF, PHxT = 1.5 V $\geq$ 10.5 V, (PTVx = 1.375 V $\rightarrow$ 3.625 V), see <a href="#">Figure 13</a>		1.5	3	$\mu\text{s}$
STL_SHT F	Settling time (fall), sample and hold mode PTVx $\pm 1\%$	$V_B = 12\text{ V}$ , Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 10.5 V $\geq$ 1.5 V, (PTVx = 3.625 V $\rightarrow$ 1.375 V), see <a href="#">Figure 12</a>		1.5	3	$\mu\text{s}$
STL_THTF	Settling time (fall), through mode PTVx $\pm 1\%$	$V_B = 12\text{ V}$ , Gain = 1, PTVx = 100 pF, PHxT = 10.5 V $\geq$ 1.5V, (PTVx = 3.625 V $\rightarrow$ 1.375 V), see <a href="#">Figure 13</a>		1.5	3	$\mu\text{s}$
SH Error Voltage	Falling voltage	$V_B = 5.3\text{--}18\text{ V}$ , PSC = 470 pF, TH = 1 mS, see <a href="#">Figure 11</a>		5	75	mV
<b>V<sub>CC</sub></b>						
$V_{CC}$	Output voltage	$V_B = 5.3\text{--}18\text{ V}$ , $I_{load} = 5\text{--}150\text{ mA}$	4.9	5	5.1	V
IBVCC	Base current		1.5			mA
hfePNP	DC current gain of external VCC		100			

(3)  $V_{gain}$  is an SPI setting

**DRV3202-Q1**

SLVSB4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

**Electrical Characteristics (continued)**VB = 12 V, T<sub>A</sub> = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLRVCC	Load regulation	VB = 5.3–18 V, I <sub>load</sub> = 5–150 mA	–50	–	50	mV
CVCC	Load capacitance		22		100	μF
RVCC	ESR of external capacitance				300	mΩ
VCCUV	Undervoltage detection threshold	R1 = 7.5 kΩ, R2 = 10 kΩ, VCCUV > 4 V	3.97	4.07	4.17	V
VCCUVHYS	Undervoltage detection threshold hysteresis			100		mV
VCCOV	Overvoltage detection threshold		6	6.5	7	V
ICLVCC	Current limit	R <sub>sns</sub> = 0.51 Ω	300	400	550	mA
TVCC1	Rise time	V <sub>CC</sub> > UVVCC, CVCC = 22 μF		0.3	0.5	ms
TVCC2	Rise time	V <sub>CC</sub> > UVVCC, CVCC = 100 μF		1	1.5	ms
<b>V<sub>DD</sub></b>						
V <sub>DD</sub>	Output voltage	VB = 5.3–18 V, I <sub>load</sub> = 0–2 mA	3	3.3	3.6	V
CVDD	Load capacitance			1		μF
VDDUV	Undervoltage detection threshold		2.2	2.3	2.4	V
VDDOV	Overvoltage detection threshold		4.1	4.3	4.5	V
T <sub>vdd</sub> <sup>(1)</sup>	Rise time	V <sub>DD</sub> > VDDUV, CVDD = 1 μF		75	150	μs
<b>VB MONITOR</b>						
V <sub>stop</sub>	Pre-driver stop VB voltage		26.5	27.5	28.5	V
<b>THERMAL SHUT DOWN</b>						
TSD <sup>(1)</sup>	Thermal shut down threshold		155	175	195	°C
<b>OSCILLATOR</b>						
OSC	OSC frequency		9	10	11	MHz
<b>INPUT BUFFER 1</b>						
V <sub>IH</sub>	Input threshold logic high		0.7 × V <sub>CC</sub>			V
V <sub>IL</sub>	Input threshold logic low		0.3 × V <sub>CC</sub>			V
R <sub>u</sub>	Input pullup resistance		50	100	150	kΩ
R <sub>u</sub> (CAN_TX)	Input pullup resistance		12.5	25	37.5	kΩ
R <sub>d</sub>	Input pulldown resistance		50	100	150	kΩ
<b>OUTPUT BUFFER 1 AND 2</b>						
V <sub>OH</sub>	Output level logic high	I <sub>sink</sub> = 2.5 mA	0.9 × V <sub>CC</sub>			V
V <sub>OL</sub>	Output level logic low	I <sub>source</sub> = 2.5 mA	0.1 × V <sub>CC</sub>			V
<b>OUTPUT BUFFER 3</b>						
R <sub>RES</sub>	Pullup resistor		1.5	3	4.5	kΩ
V <sub>OL</sub>	Output level logic low	I <sub>source</sub> = 2 mA	0.1 × V <sub>CC</sub>			V

**6.5 Supply Voltage and Current**VB = 12 V, T<sub>A</sub> = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY INPUT</b>						
VB	VB Supply voltage		5.3	12	18	V
I <sub>VB</sub>	VB Operating current	VB = 5.3 ~ 18 V, CAN_TX = High, No PWM		20	35	mA

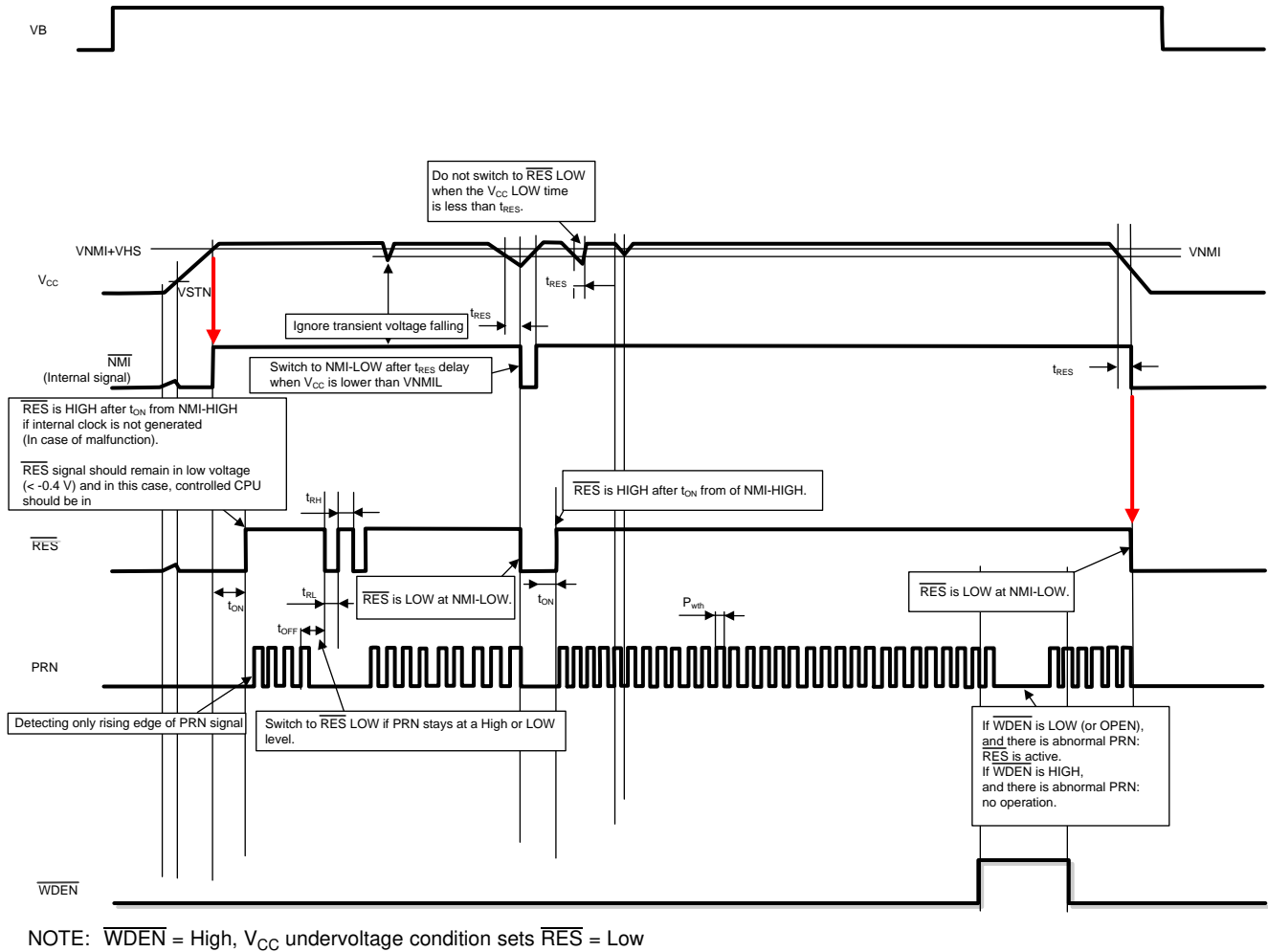


Figure 1. Watchdog Timing Chart

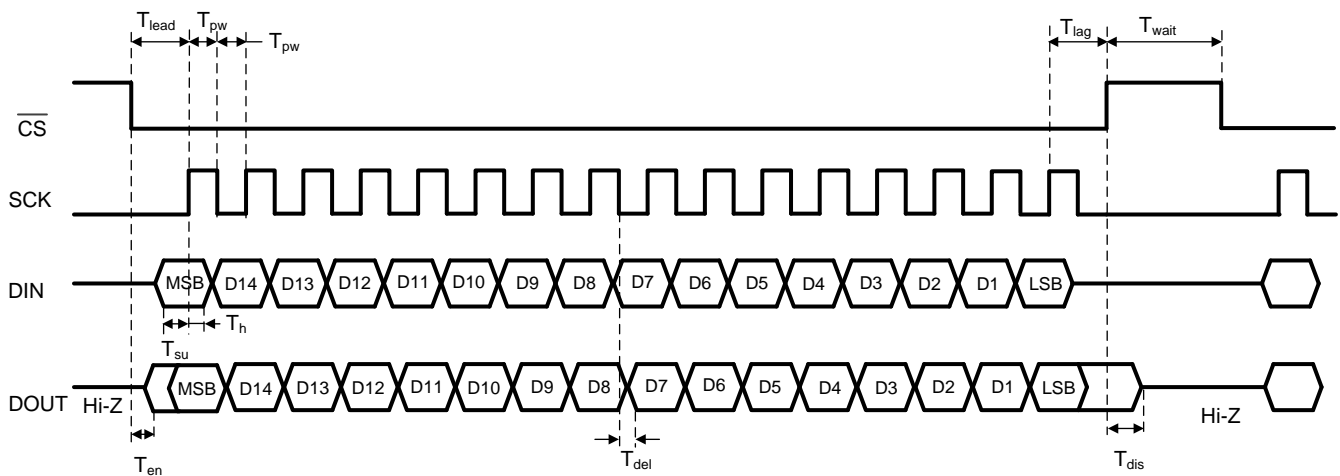


Figure 2. SPI AC Timing Definition

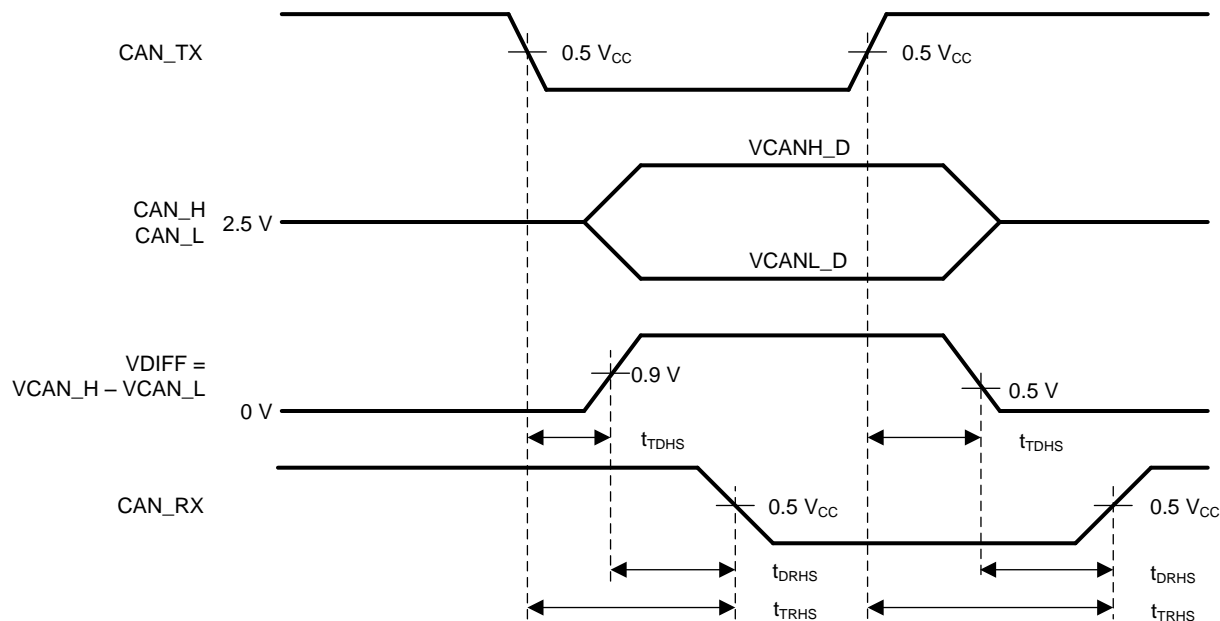
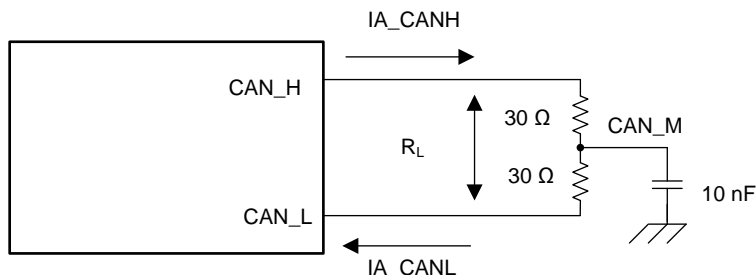


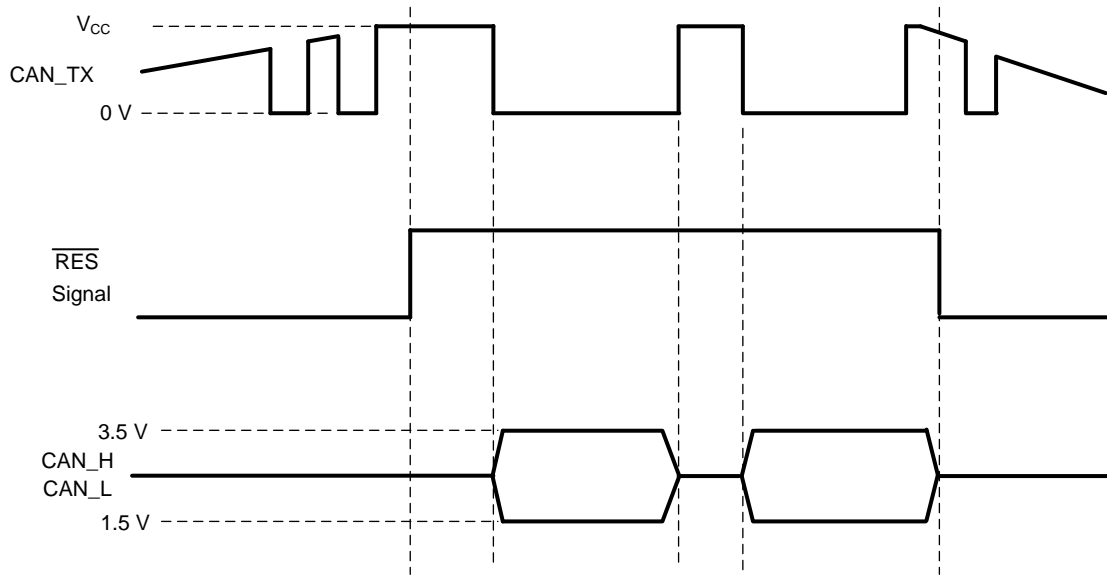
Figure 3. CAN Timing Chart



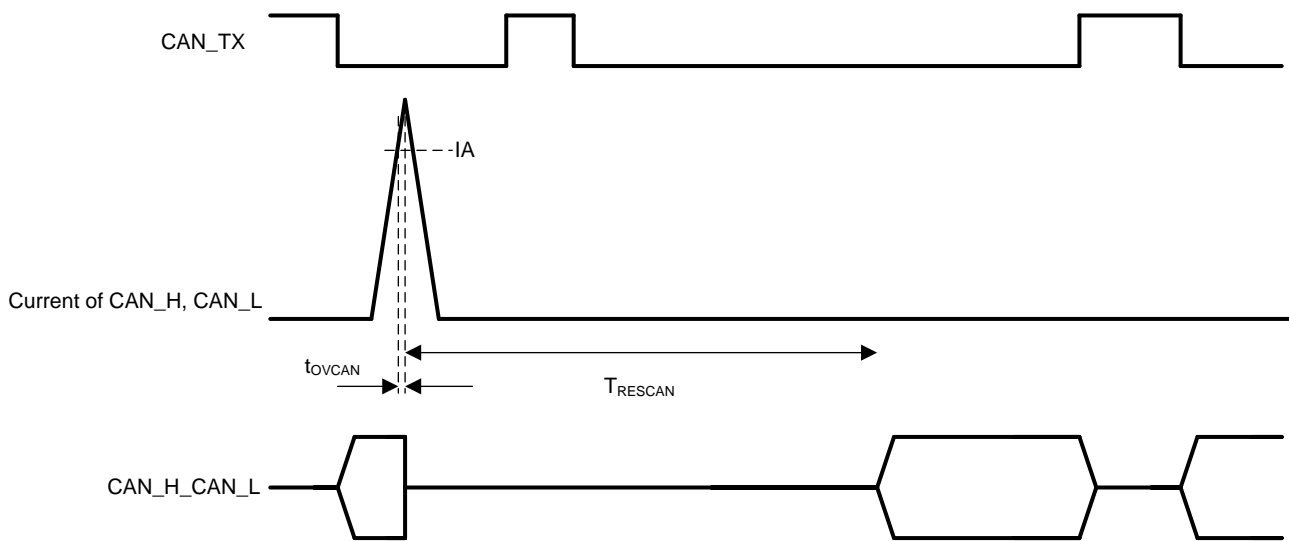
Test circuit for measurement of AC characteristics and slew rate.

NOTE: If CAN\_L is shorted to GND, try to keep transmission (no overcurrent event).

Figure 4. CAN Testing Condition



**Figure 5. CAN Reset Function**



The CANOC in CANFLAG is set high if overcurrent condition exists.

**Figure 6. Overcurrent Event**

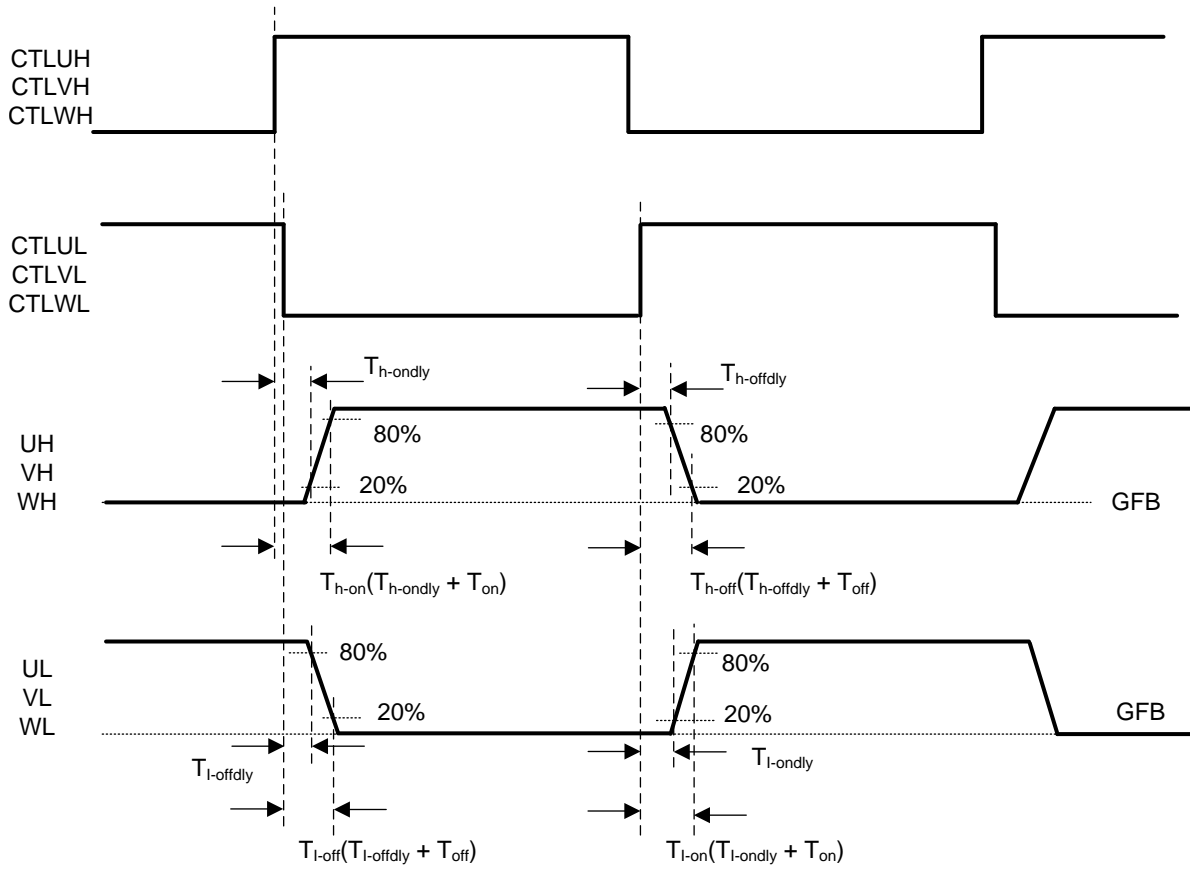


Figure 7. Delay Time from Input to Output

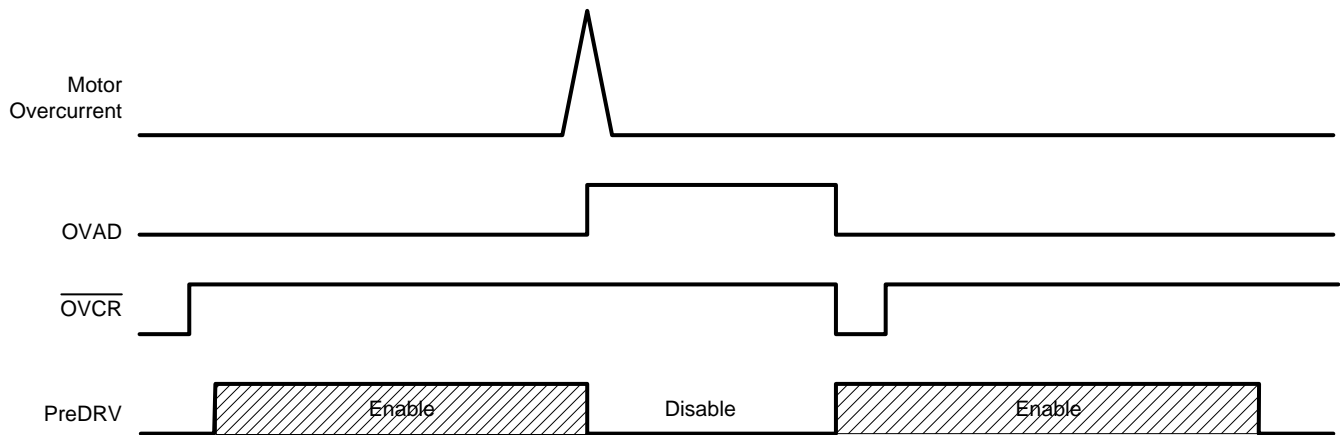
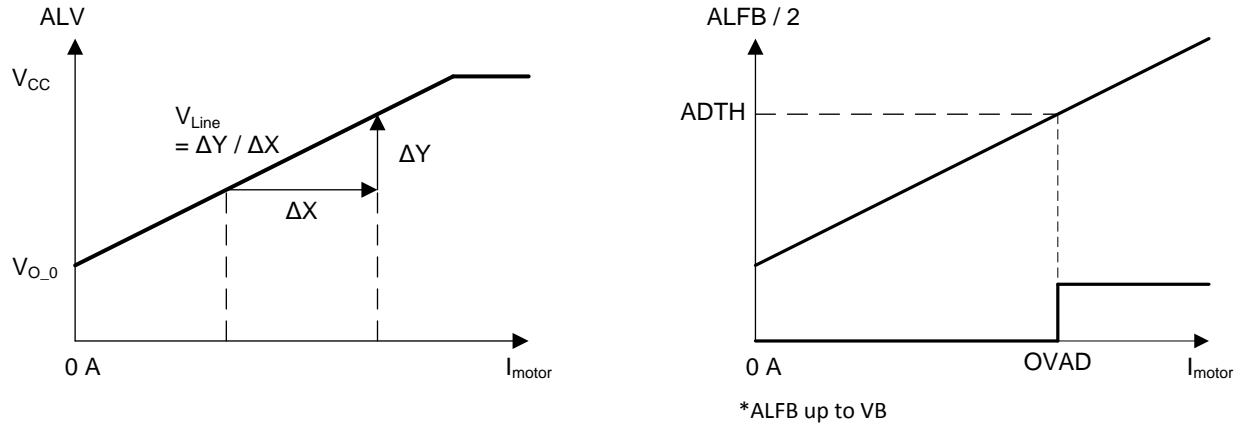
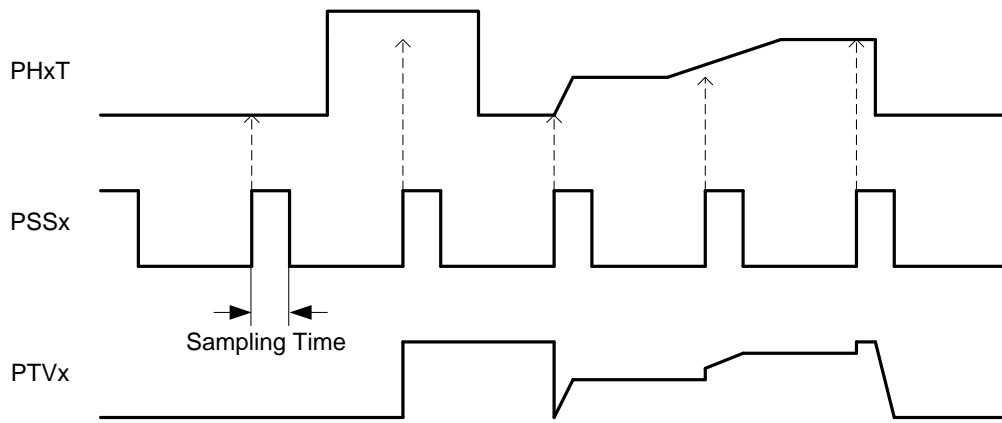


Figure 8. Motor Overcurrent Event

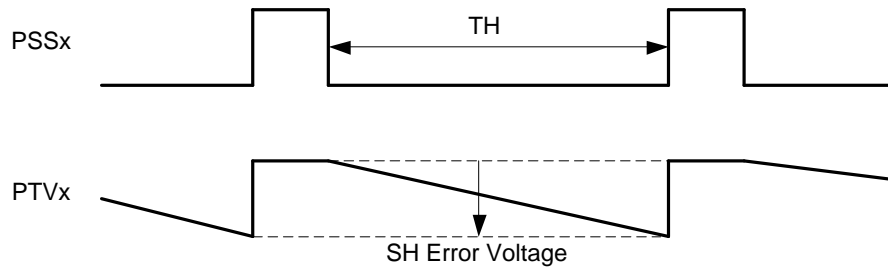




**Figure 9. Motor Current Sense and Overcurrent**



**Figure 10. Sampling Timing Chart**



**Figure 11. Holding Timing Chart**

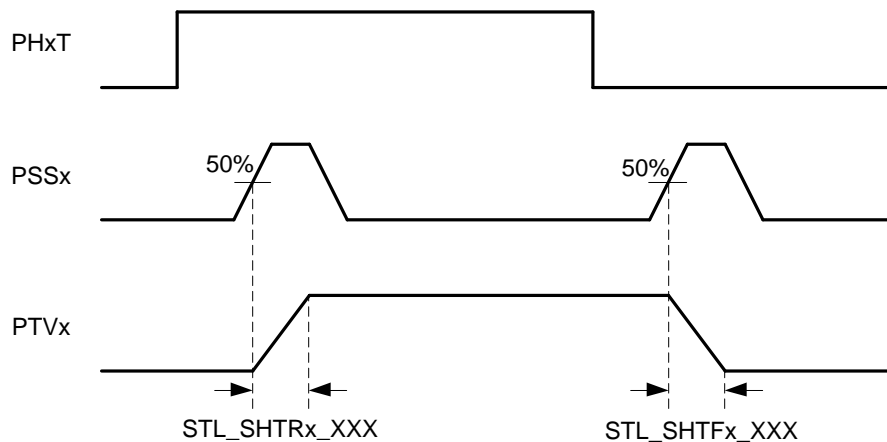


Figure 12. Settling Time Timing Chart (Sample and Hold Mode)

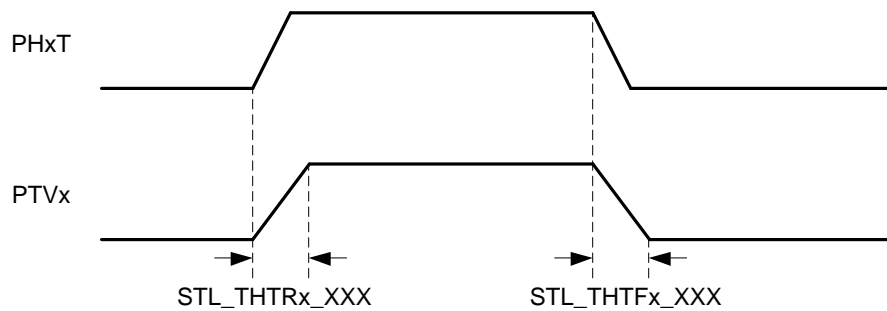
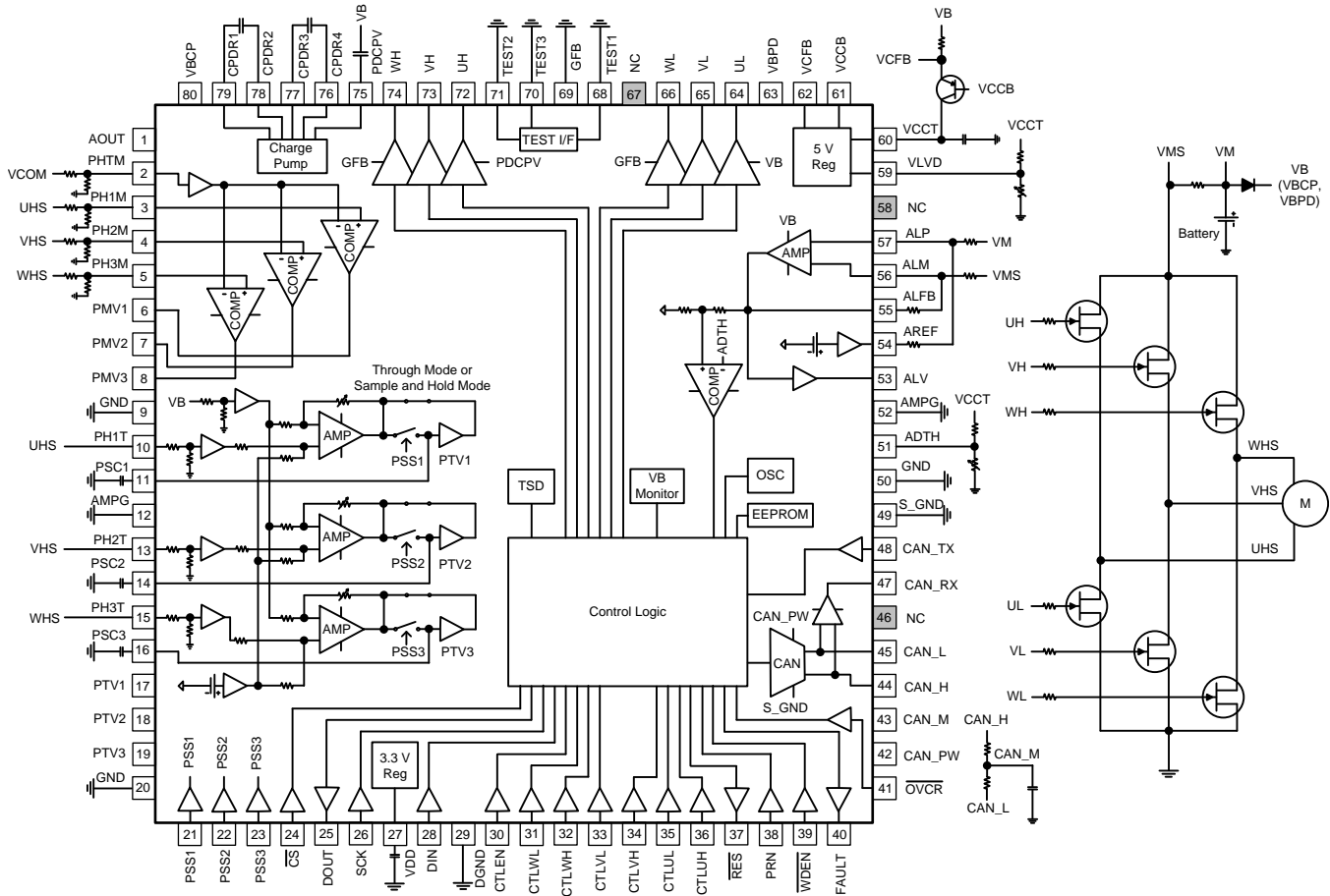


Figure 13. Settling Time Timing Chart (Through Mode)

## 7 Detailed Description

### 7.1 Functional Block Diagram



## 7.2 Feature Description

### 7.2.1 Watchdog

The watchdog monitors the PRN signal and  $V_{CC}$  supply level and generates a reset to the MCU through the  $\overline{RES}$  pin if the status of the PRN is not normal or the  $V_{CC}$  is lower than the specified threshold level. The watchdog can be disabled if WDEN is set high.



**Feature Description (continued)**

- **$\overline{\text{CS}}$  – Chip Select**
  - This input signal is utilized to select this IC by CPU.
  - This input signal is normally high and the communication is possible only when it is forced low.
  - When this input signal falls, the communication between this IC and the CPU starts.
  - Transmitted data is latched and the DOUT pin comes out of high impedance.
  - When this input signal rises, the communication stops.
  - The DOUT pin goes into high impedance. Then, the internal input register updates with the received bits (only if the clock pulse numbers are right and the key bit of the DIN signals is correct).
  - The next falling edge starts another communication.
  - There is a minimum waiting time between two communications ( $T_{\text{wait}}$ ).
  - The pin has an internal pullup.
- **SCK – Synchronization Serial Clock**
  - This input signal is utilized to synchronize the communication by CPU.
  - It is normally high and the correct clock pulse number is 16.
  - At each falling edge, the CPU writes a new bit on the DIN input and this IC writes a new bit on the DOUT pin. At each rising edge, this IC reads the new bit on the DIN pin and the CPU reads the new bit on the DOUT pin.
  - The maximum clock frequency is 4 MHz.
  - The pin has an internal pullup.
- **DIN – Serial Input Data**
  - This input signal is used to receive 16-bit data.
  - The bits are received in order from the MSB (first) to the LSB (last).
  - The pin has an internal pullup.
- **DOUT – Serial Output Data**
  - This output signal is used to transmit 16-bit data.
  - It is a 3-state output and it is in high impedance mode when  $\overline{\text{CS}}$  is high.
  - The serial data bits are transmitted in order from the MSB (first) to the LSB (last).

Feature Description (continued)

7.2.3 CAN

The CAN data from CAN control logic is transmitted to other systems through the CAN bus. The receiver compares the CAN\_H–CAN\_L voltage levels against an internally generated reference and the result is output through CAN\_TX. It has overcurrent protection, shown in Figure 6.

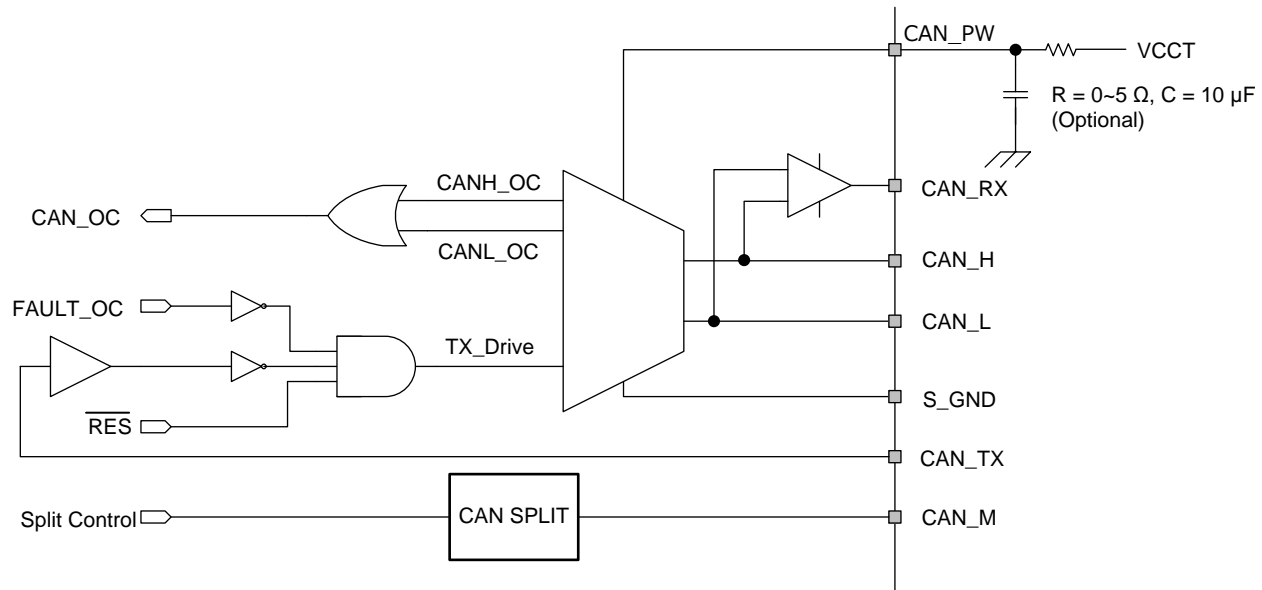
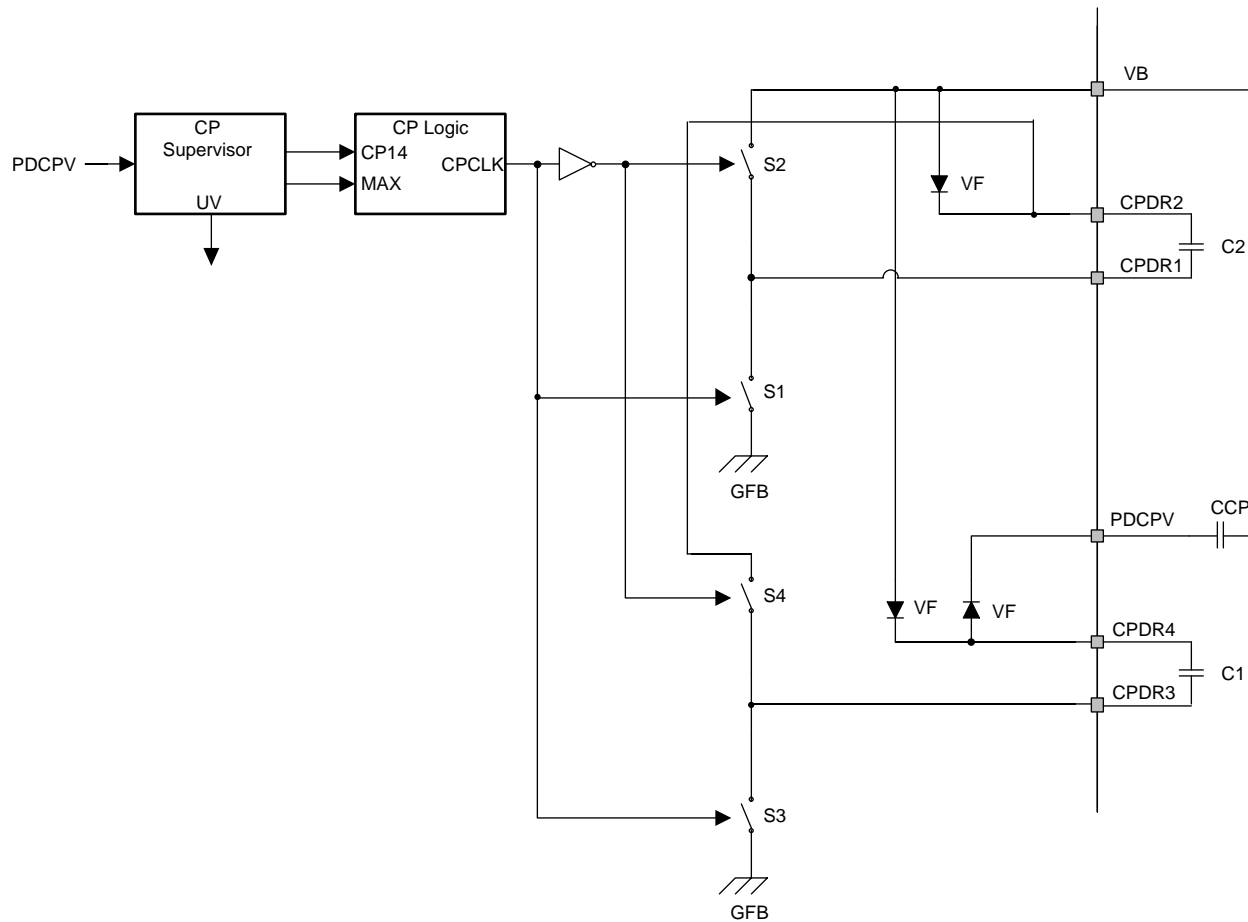


Figure 16. CAN Block Diagram

7.2.4 Charge Pump

The charge pump block generates the supply for high-side and low-side pre-drivers to maintain the gate voltage on the external FETs. External storage cap (CCP) and bucket caps (C1, C2) are used to support pre-driver slope and switching frequency requirements. R1 and R2 can reduce switching current if required. The charge pump has a voltage supervisor for over and undervoltage, and a selectable stop condition for pre-drivers.

**Feature Description (continued)**



**Figure 17. Charge Pump Block Diagram**

**7.2.5 Pre-Driver**

The pre-driver block provides three high-side pre-drivers and three low-side pre-drivers to drive external N-channel MOSFETs. The turn on side of the high-side pre-drivers supply the large N-channel transistor current to quickly charge and PMOS support output voltage up to PDCPV. The turn off side supplies the large N-channel transistor current to quickly discharge, while the low-side pre-drivers supply the large N-channel transistor current for charge and discharge. The output voltage of the low-side pre-driver is controlled by VB and it has VGS protection to make less than 18 V. The pre-driver has a stop condition in some fault conditions (§16 Error Detection).

DRV3202-Q1

SLVSB4B –OCTOBER 2012–REVISED JULY 2016

www.ti.com

Feature Description (continued)

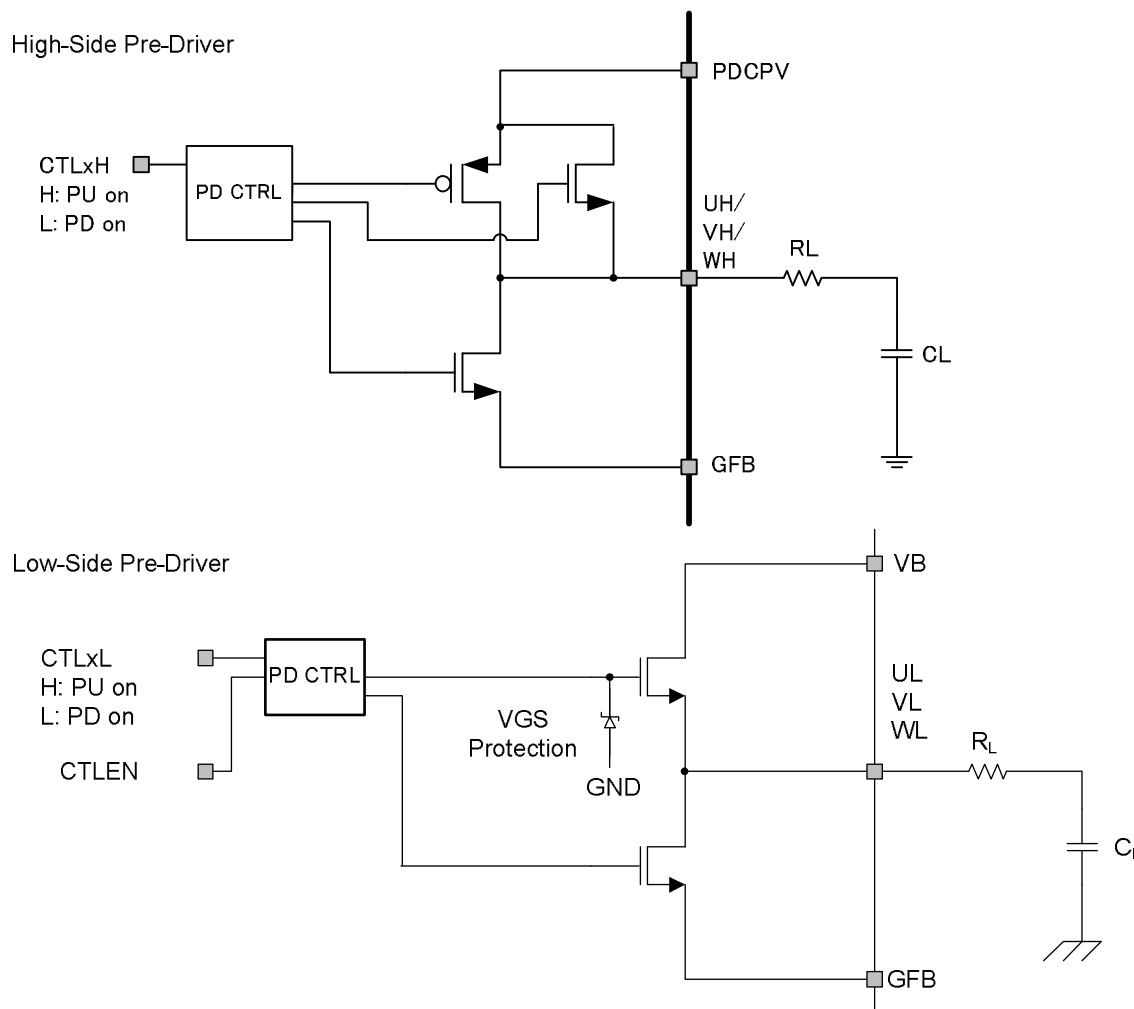


Figure 18. Pre-Driver Block Diagram

7.2.6 Phase Comparator

A 3-channel comparator module monitors the external FET by detecting voltage across the drain-source for high-side and low-side FETs. PHTM is the threshold level of comparators usable for sensorless communication. Figure 19 shows an example of the threshold level. There is no detection when CTLEN = Low.

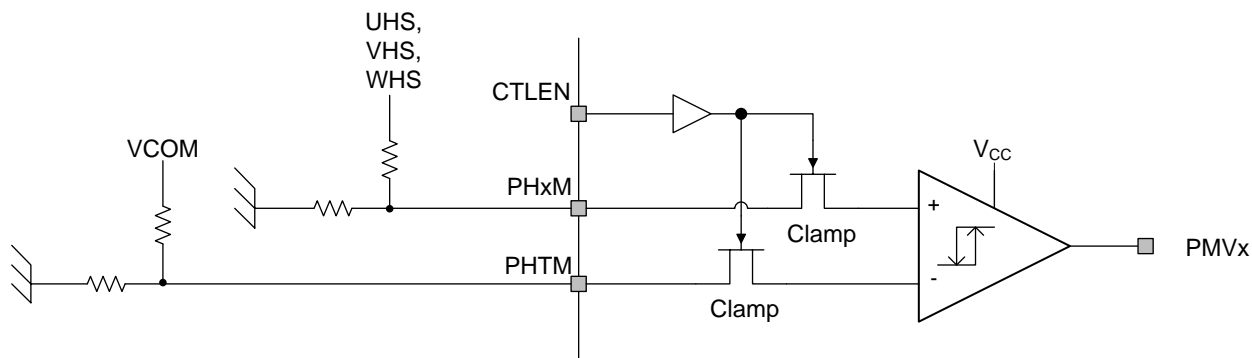


Figure 19. Phase Comparator Block Diagram



## Feature Description (continued)

### 7.2.7 Motor Current Sense

The operational amplifier is operating with an external resistor network for higher flexibility to adjust the current measurement to application requirements. The first stage amplifier is operating with the external resistor and the output voltage up to  $V_B$  at ALFB. The gain of the amplifier is adjustable by external resistors from  $\times 10$  to  $\times 30$ . The second stage amplifier is a buffer to MCU at ALV. Current sense has a comparator for motor overcurrent (OVAD). ADTH is the overcurrent threshold level and sets the value by the external resistor as well. Figure 9 shows the curve of the detection level. ALFB is divided by 2, compare this value with ADTH. In the recommended application, zero-point adjustment is required as a large error offset in the initial condition.

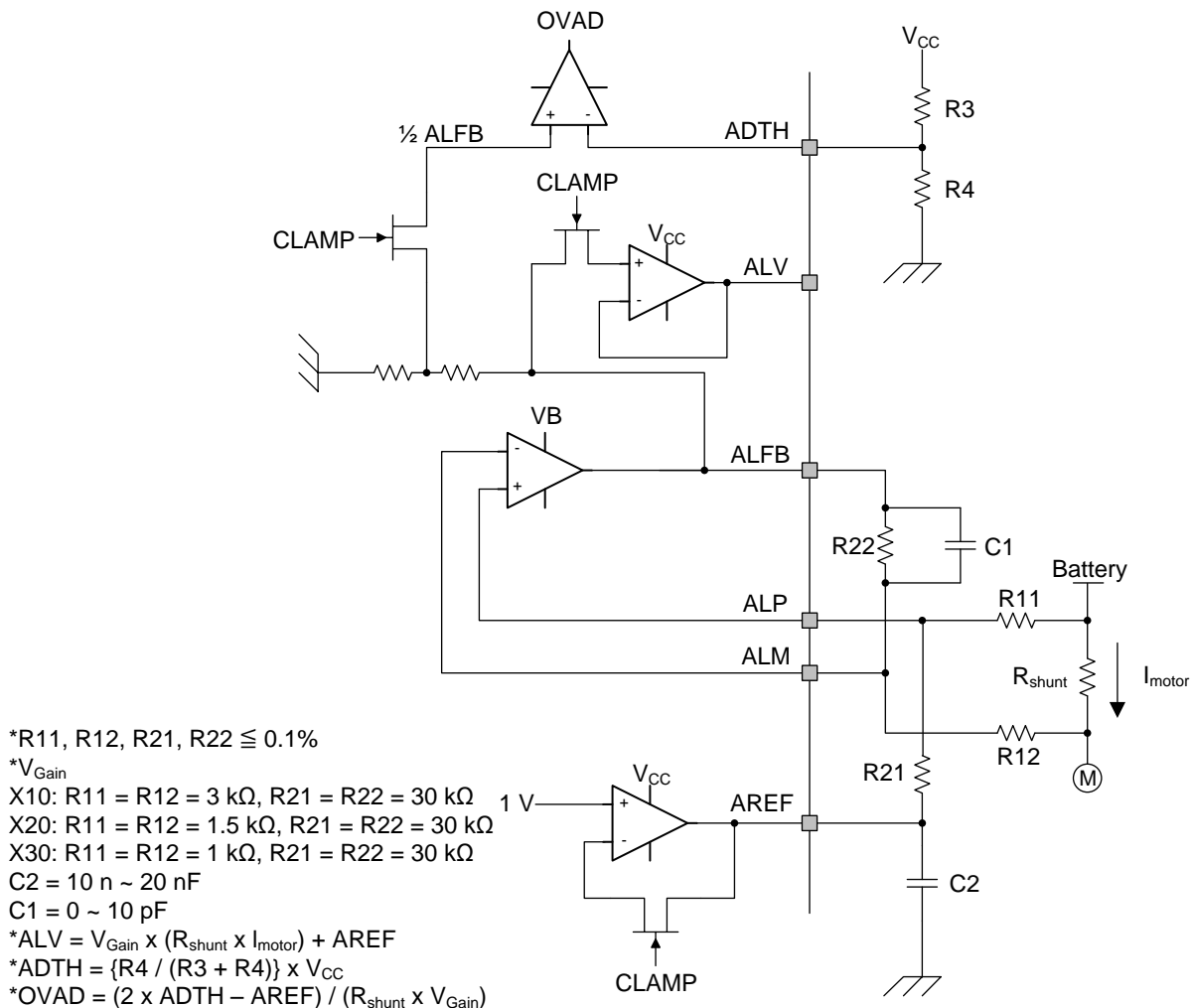


Figure 20. Motor Current Sense Block Diagram

### 7.2.8 Phase Amplifier (Sample and Hold Mode and Through Mode)

The 3-channel amplifier module monitors the drain-source for high-side and low-side FETs. Two modes (selected by the SPI) are provided: sample and hold mode, and through mode. Sample and hold is controlled by PSSx at the external pins and PSCx connects the charging capacitor. Through mode is real-time detection and the amplifier has  $\times 1$ – $\times 4$  gain control.

DRV3202-Q1

SLVSB4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

Feature Description (continued)

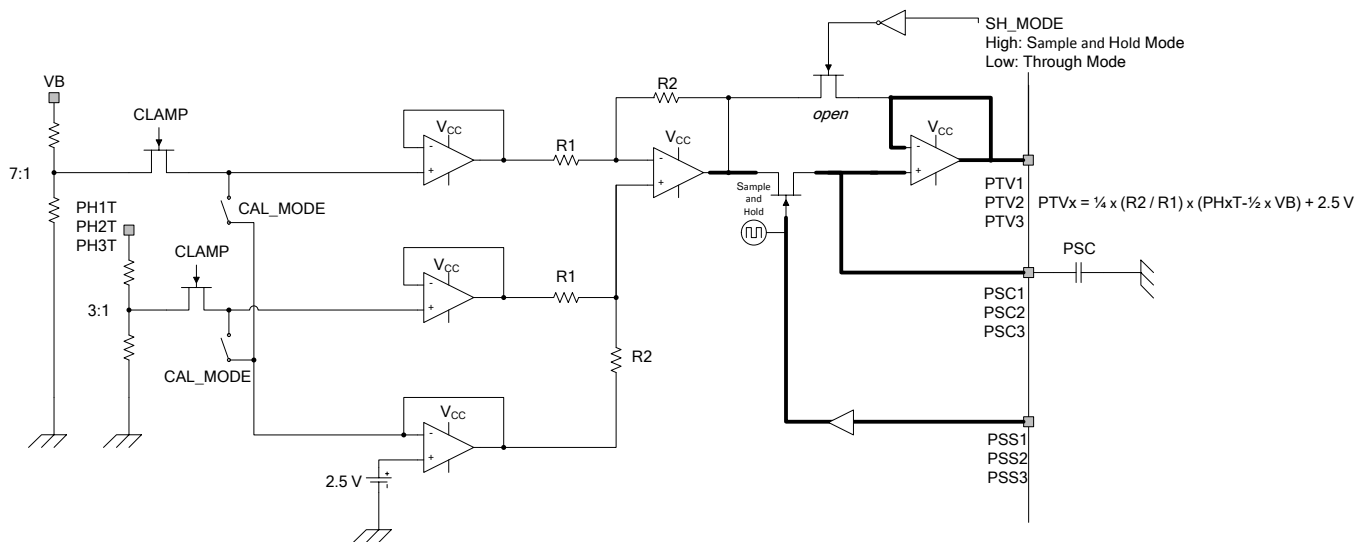


Figure 21. Sample and Hold Mode Block Diagram

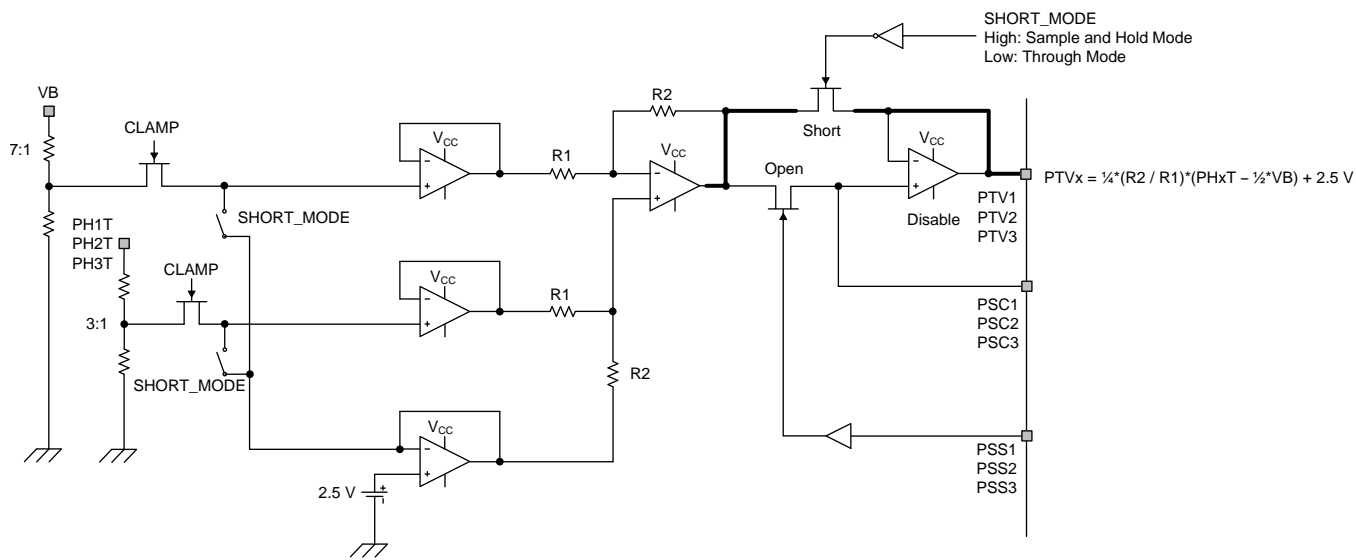


Figure 22. Through Mode Block Diagram

Feature Description (continued)

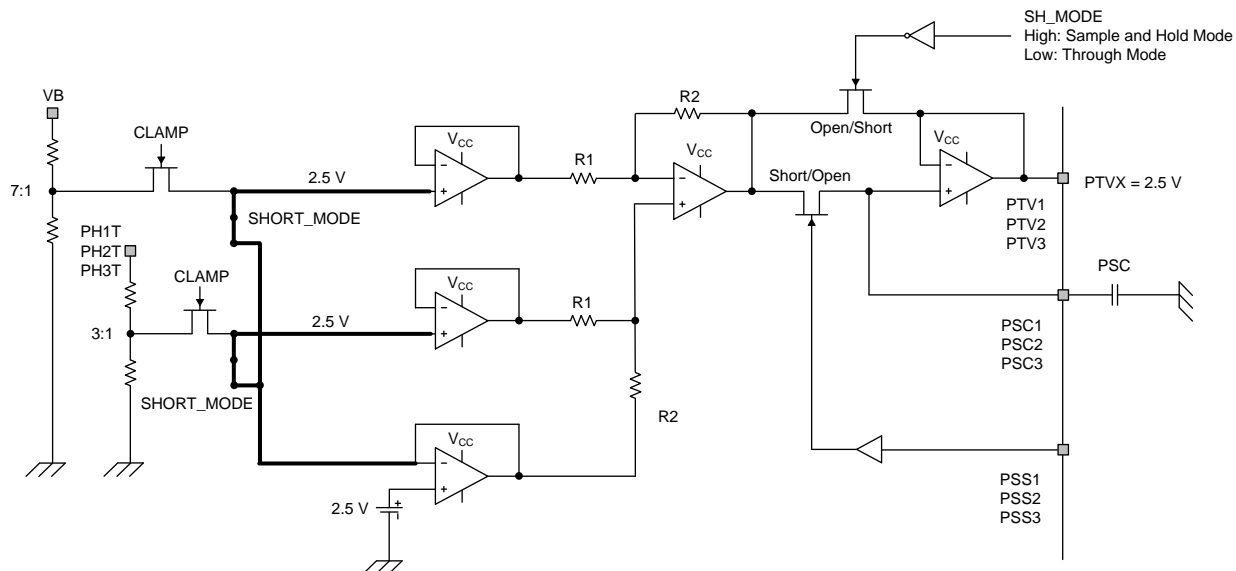


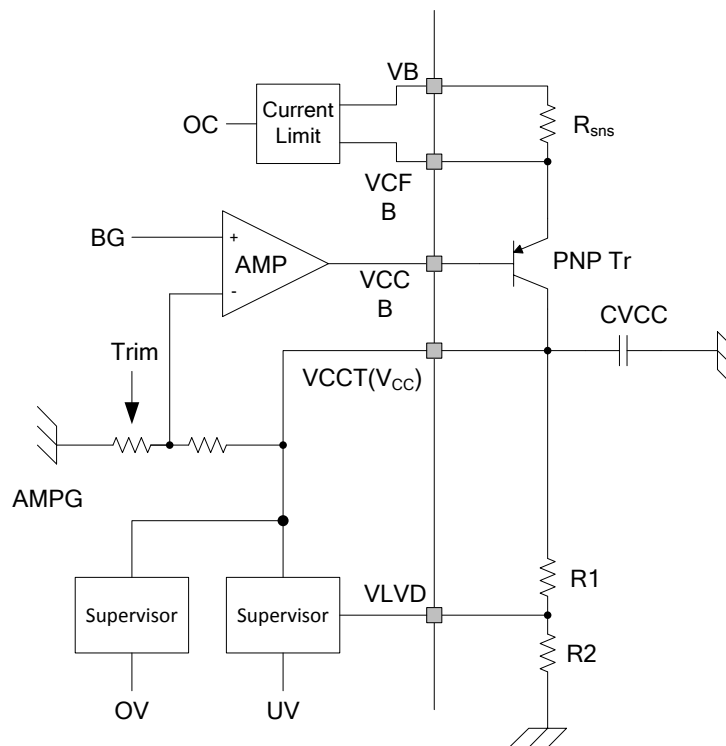
Figure 23. Short Mode (Optional) Block Diagram

7.2.9 Regulators

The regulator block offers a 5-V LDO and a 3.3-V LDO. The  $V_{CC}$  LDO regulates  $V_B$  down to 5 V with an external PNP controlled by the regulator block. The 5-V LDO is supplied to the MCU and other components. The 5-V LDO is protected against a short to GND fault, and the external resistors R1 and R2 set the undervoltage. The  $V_{DD}$  regulator regulates  $V_B$  down to 3.3-V with an internal FET and a controller.

The regulators detect the overvoltage and undervoltage events of both supplies.

Feature Description (continued)



\*  $R_{sns} = 0.2 V / I_{CLVCC}$   
 \*  $V_{CCUV} = 2.325 \times \{(R1+R2) / R2\}$

Figure 24. V<sub>CC</sub> Block Diagram

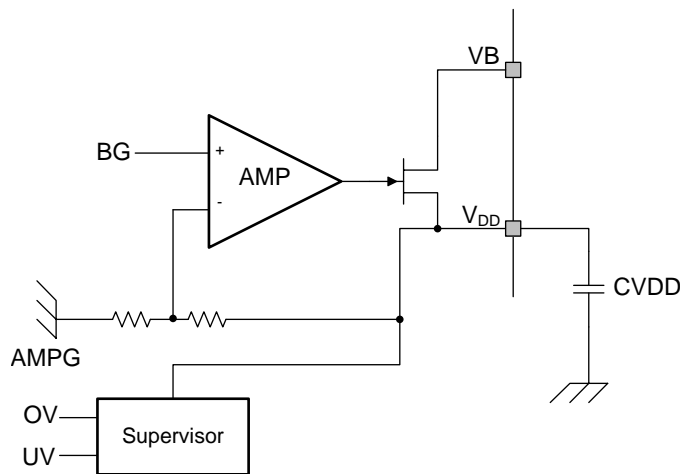
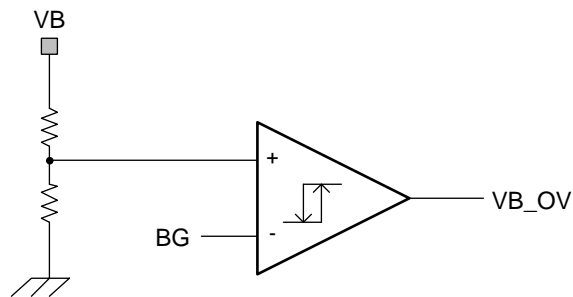


Figure 25. V<sub>DD</sub> Block Diagram

7.2.10 VB Monitor

The block monitors VB overvoltage.

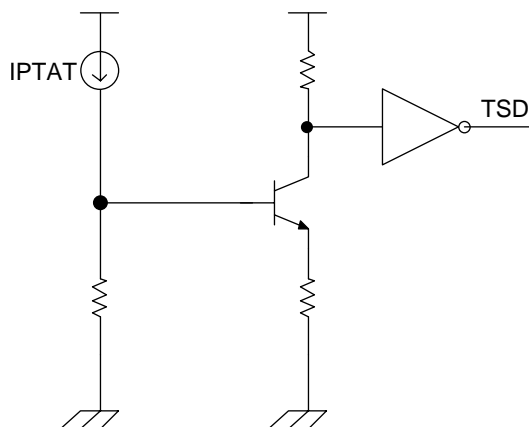
**Feature Description (continued)**



**Figure 26. VB Monitor Block Diagram**

**7.2.11 Thermal Shutdown**

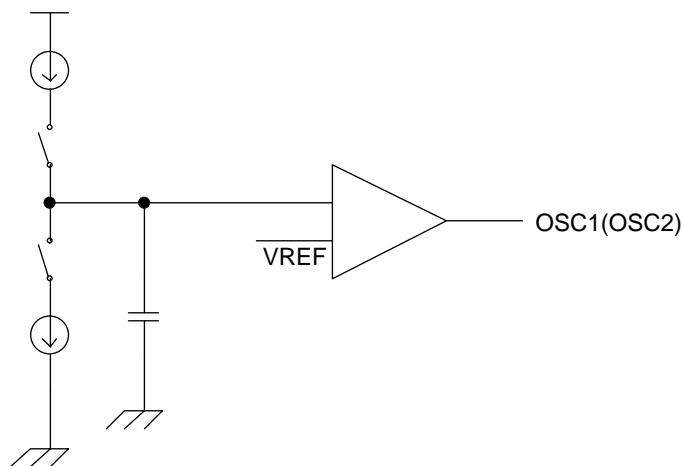
The device has temperature sensors that produce a pre-driver stop condition if the chip temperature exceeds 175°.



**Figure 27. Thermal Shutdown Block Diagram**

**7.2.12 Oscillator**

Oscillator block generates two 10-MHZ clock signals. OSC1 is the main clock used for internal logic synchronization and timing control. OSC2 is the secondary clock which is used to monitor the status of OSC1.



**Figure 28. Oscillator Block Diagram**

DRV3202-Q1

SLVSB4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

Feature Description (continued)

7.2.13 I/O

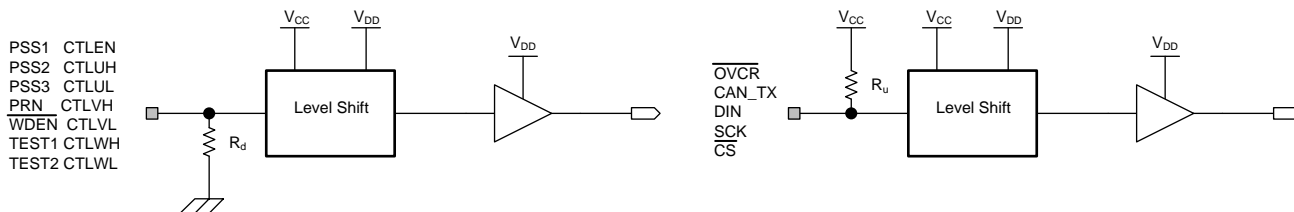


Figure 29. Input Buffer 1 Block Diagram

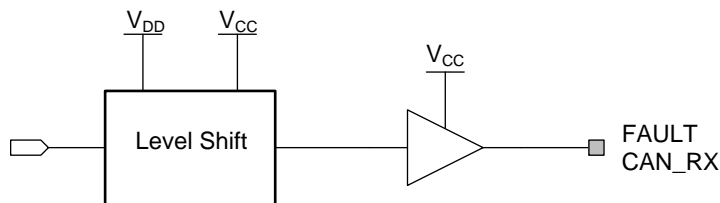


Figure 30. Output Buffer 1 Block Diagram

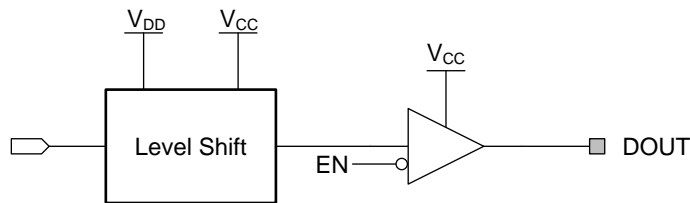


Figure 31. Output Buffer 2 Block Diagram

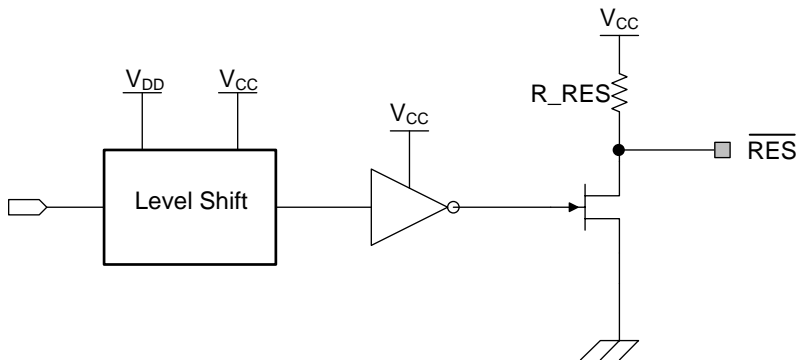


Figure 32. Output Buffer 3 Block Diagram

7.2.14 Error Detection

Table 1. Error Detection

ITEMS	SPI	PRE-DRIVER	FAULT SIGNAL	RES
VB – Overvoltage	–	STOP	L	H
CP – Overvoltage	–	STOP	L	H
CP – Undervoltage	Error Bit (CPLV)	–	L	H
V <sub>CC</sub> – Overvoltage	Error Bit (VCO)	–	L	H
V <sub>CC</sub> – Undervoltage	–	STOP	L	L

Table 1. Error Detection (continued)

ITEMS	SPI	PRE-DRIVER	FAULT SIGNAL	RES
V <sub>CC</sub> – Overcurrent	Error Bit (V <sub>CC</sub> )	–	H	H
Motor – Overcurrent	Error Bit (OVAD)	STOP	H	H
V <sub>DD</sub> – Overvoltage	Error Bit (VDO)	–	L	H
V <sub>DD</sub> – Undervoltage	–	STOP	L	L
Thermal Shut Down	Error Bit (TD)	STOP	H	H
Watchdog	–	–	L	L
EEPROM Data Check	Error Bit (EEP)	–	L	H
Clock Monitor	–	–	L	L
CAN Overcurrent	Error Bit (CCD)	–	L	H
SPI	Error Bit (SPI)	–	L	H

7.3 Device Functional Modes

Table 2. Motor Overcurrent Truth Table

RES	OVCR	MOTOR OVERCURRENT	OVAD	PRE-DRIVER ENABLE OR DISABLE
0	–	–	0 (Clear)	Disable <sup>(1)</sup>
1	0	–	0 (Clear) <sup>(2)(3)</sup>	Enable
	1	0	Keep	Enable
		1	1 (Set)	Disable

- (1) The CTLEN goes to Hi-Z because the external CPU will not drive it when RES = 0, then all the pre-drivers are turned off because CTLEN is internally pulled down.
- (2) The OVAD is not set, even if a motor overcurrent error is generated during OVCR = 0.
- (3) The OVAD is cleared if OVCR = 0 even when the motor overcurrent error is generated.

7.4 Register Maps

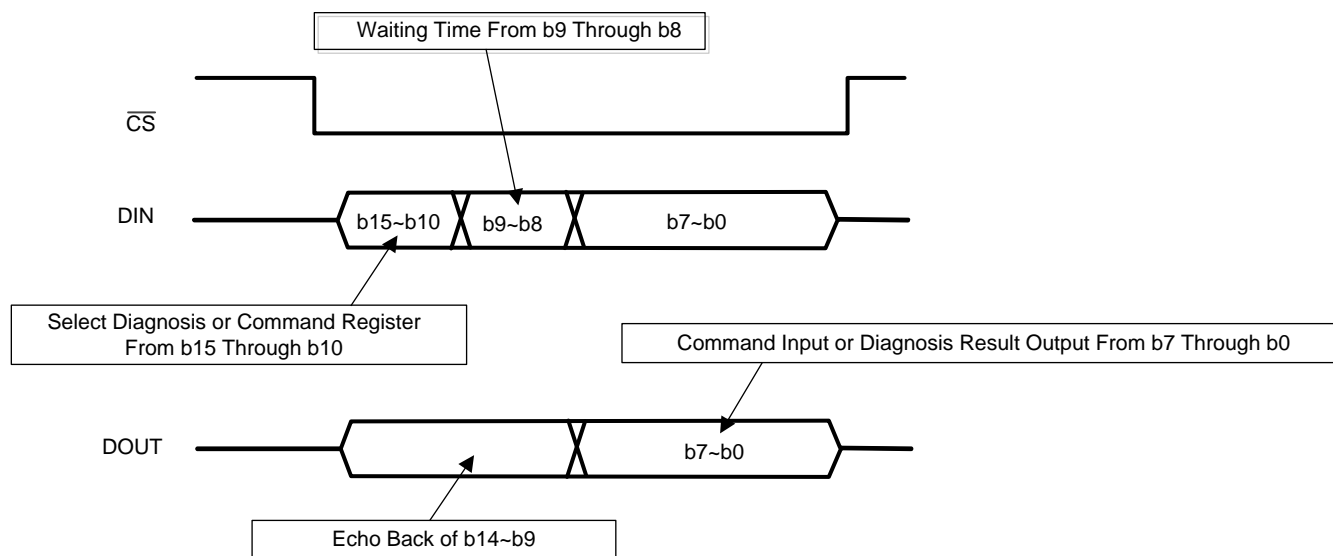


Figure 33. SPI Bit Sequence

Table 3. SPI Bit Map (DIN)

ITEM	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
COMMAND1	0	0	0	0	0	1	–	–	SHM	SRT	–	–	–	–	–	–
COMMAND2	0	0	0	0	1	0	–	–	AG1	AG0	–	–	–	–	–	–
COMMAND3	0	0	0	0	1	1	–	–	–	–	–	–	–	–	–	–

DRV3202-Q1

SLVSB4B – OCTOBER 2012 – REVISED JULY 2016

www.ti.com

Register Maps (continued)

Table 3. SPI Bit Map (DIN) (continued)

ITEM	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DIAG_READ1	0	0	1	0	0	0	–	–	–	–	–	–	–	–	–	–
DIAG_READ2	0	1	0	0	0	0	–	–	–	–	–	–	–	–	–	–
DIAG_READ3	0	1	1	0	0	0	–	–	–	–	–	–	–	–	–	–

In Table 3, the B15–B10 are the control bits, so the each command depends on them (listed below).

1. **B15-B10 = 0 0 0 0 0 1**

These are the commands:

- 1) Phase AMP Sampling Hold Mode (B7 bit)
  - 0: OFF (through) (INITIAL VALUE)
  - 1: ON (use sample hold mode)
- 2) Phase AMP Short Mode [Short\_Mode] (B6 bit)
  - 0: OFF (no calibration) (INITIAL VALUE)
  - 1: ON (use calibration mode)

2. **B15-B10 = 0 0 0 0 1 0**

These are the commands:

- 1) Phase AMP Gain (B7 bit and B6 bit)
  - B7:0 B6:0; Gain x1 (INITIAL VALUE)
  - B7:0 B6:1; Gain x2
  - B7:1 B6:0; Gain x3
  - B7:1 B6:1; Gain x4

3. **B15-B10 = 0 0 0 0 1 1**

Not used

4. **B15-B10 = 0 0 1 0 0 0**

This command is to read the diagnosis of the current regulator, SPI communication, overvoltage detection, and input diagnosis.

5. **B15-B10 = 0 1 0 0 0 0**

This command is to read the diagnosis of SPI communication.

6. **B15-B10 = 0 1 1 0 0 0**

Not used

7. **B15-B10 = Other command**

This command sets the SPI-NG (DOUT, B7) bit.

Table 4. SPI Bit Map (DOUT)

ITEM	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
ON/OFF COMMAND ECHO BACK	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	0	–	–	–	–	–	–	–	–
	0	0	0	0	0	1	1	0	–	–	–	–	–	–	–	–
DIAG_READ1	0	0	0	1	0	0	0	0	VCC	OCD	CCD	VCO	VDO	CPLV	TD	EEP
DIAG_READ2	0	0	1	0	0	0	0	0	SPI	–	–	–	–	–	–	–
DIAG_READ3	0	0	1	1	0	0	0	0	–	–	–	–	–	–	–	–

1. **B14-B9 = 0 0 1 0 0 0**

This flag is cleared after the register is read by the CPU.

- 1) **V<sub>CC</sub> Current Detection (B7)**
  - 0: NORMAL
  - 1: Fail (Short to GND or open)
- 2) **Overcurrent Detection (B6)**
  - 0: NORMAL
  - 1: Fail (Overcurrent)
- 3) **CAN Current Detection (B5)**
  - 0: NORMAL



- 1: Fail (Overcurrent)
  - 4) **V<sub>CC</sub> Overvoltage Detection (B4)**  
0: NORMAL  
1: Fail (V<sub>CC</sub> overvoltage)
  - 5) **V<sub>DD</sub> Overvoltage Detection (B3)**  
0: NORMAL  
1: Fail (V<sub>DD</sub> overvoltage)
  - 6) **CPV Low Voltage Detection (B2)**  
0: NORMAL  
1: Fail (CPV low voltage)
  - 7) **Thermal Detection (B1)**  
0: NORMAL  
1: Fail (Overtemperature)
  - 8) **EEPROM\* Data Consistency Check (B0)**  
0: NORMAL  
1: Fail (EEPROM DATA CRC error)
- \*ASIC calibration EEPROM

**NOTE**

Just after power-on of the IC, some of the bits listed above may be set depending on the apply sequence of VB. It is recommended to issue a DIAG\_READ1 to clear these bits prior to all S/W sequences.

2. **B14-B9 = 0 1 0 0 0 0**

This flag is cleared after the register is read by the CPU.

1) **SPI-NG (B7)**

- 0: NORMAL
- 1: Fail (SPI read and write command is wrong)

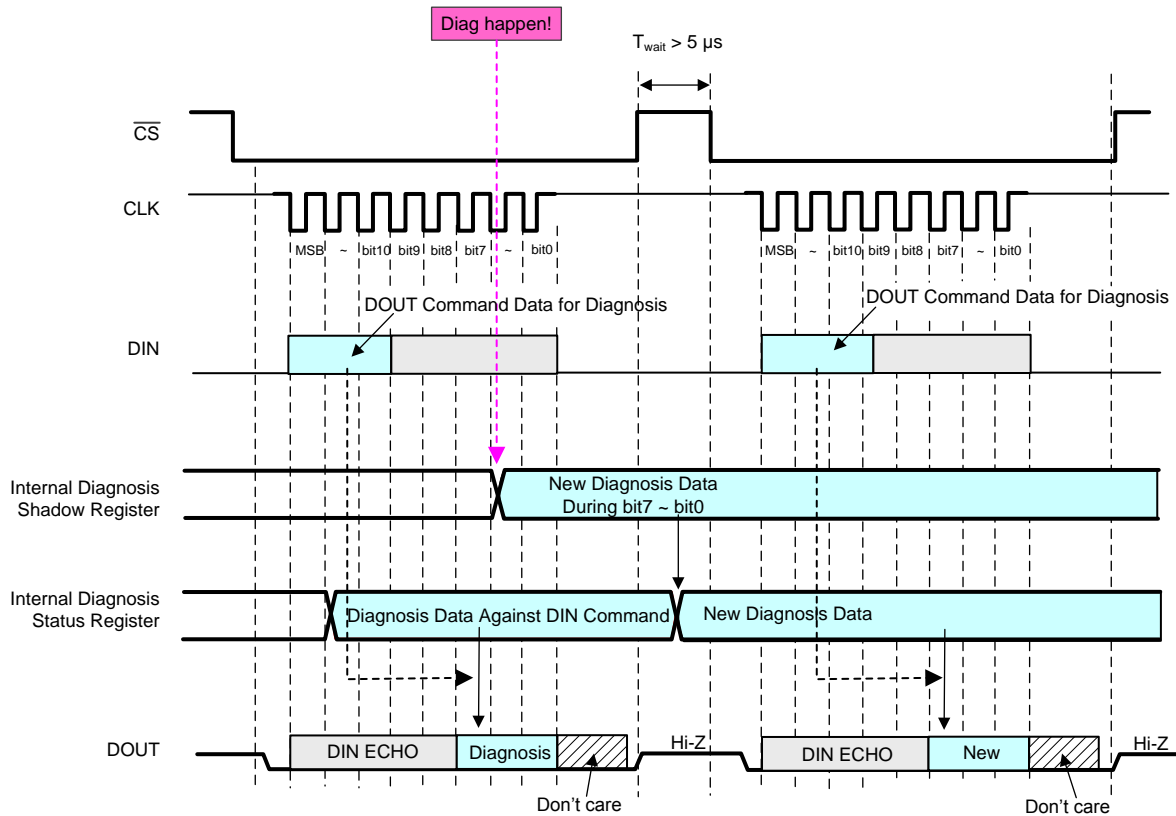


Figure 34. DIAG\_READ

## DRV3202-Q1

SLVSBJ4B –OCTOBER 2012–REVISED JULY 2016

[www.ti.com](http://www.ti.com)

### 7.4.1 Internal Diagnosis Register (Status Register and Shadow Register)

If the diagnosis happens during the SPI communication, the function follows this protocol:

The diagnosis information is stored in the shadow register when the diagnosis happens.

After the output of the previous information a new diagnosis is sent from the shadow to the status register, and both registers are output through the DOUT pin.

In this case, a FAULT signal continues to be output until a new diagnosis is read by the CPU.

All diagnosis bits read by the DIAG\_READ1 command happen before the  $\overline{CS}$  falling edge. So, all the diagnosis events that happen right after the  $\overline{CS}$  falling edge are not read by the current DIAG\_READ1 command, instead they are read by the next DIAG\_READ1 command.

## 8 Device and Documentation Support

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 8.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 8.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV3202QFPFQ1	NRND	HTQFP	FPF	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV3202	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

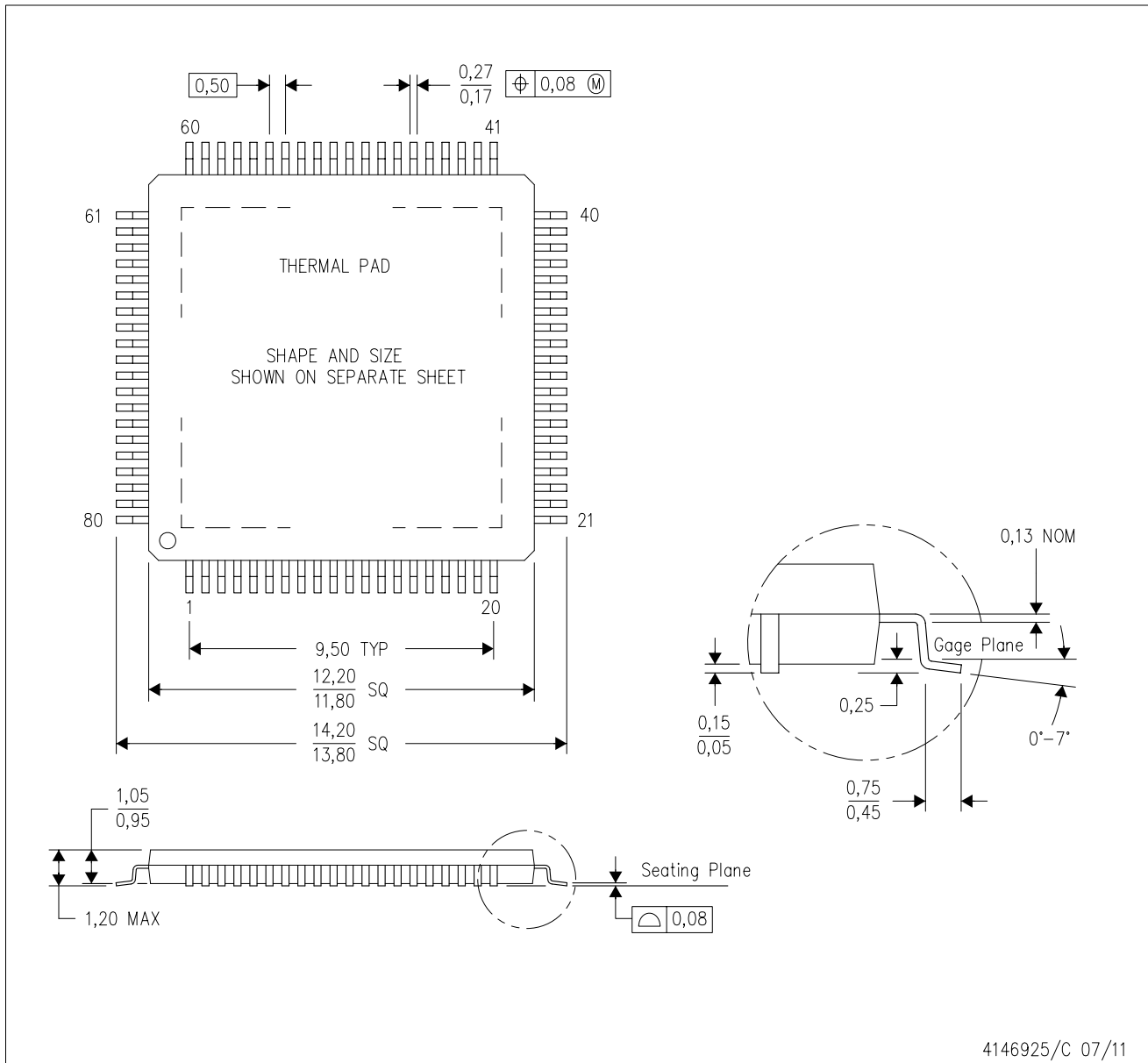
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



# MECHANICAL DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

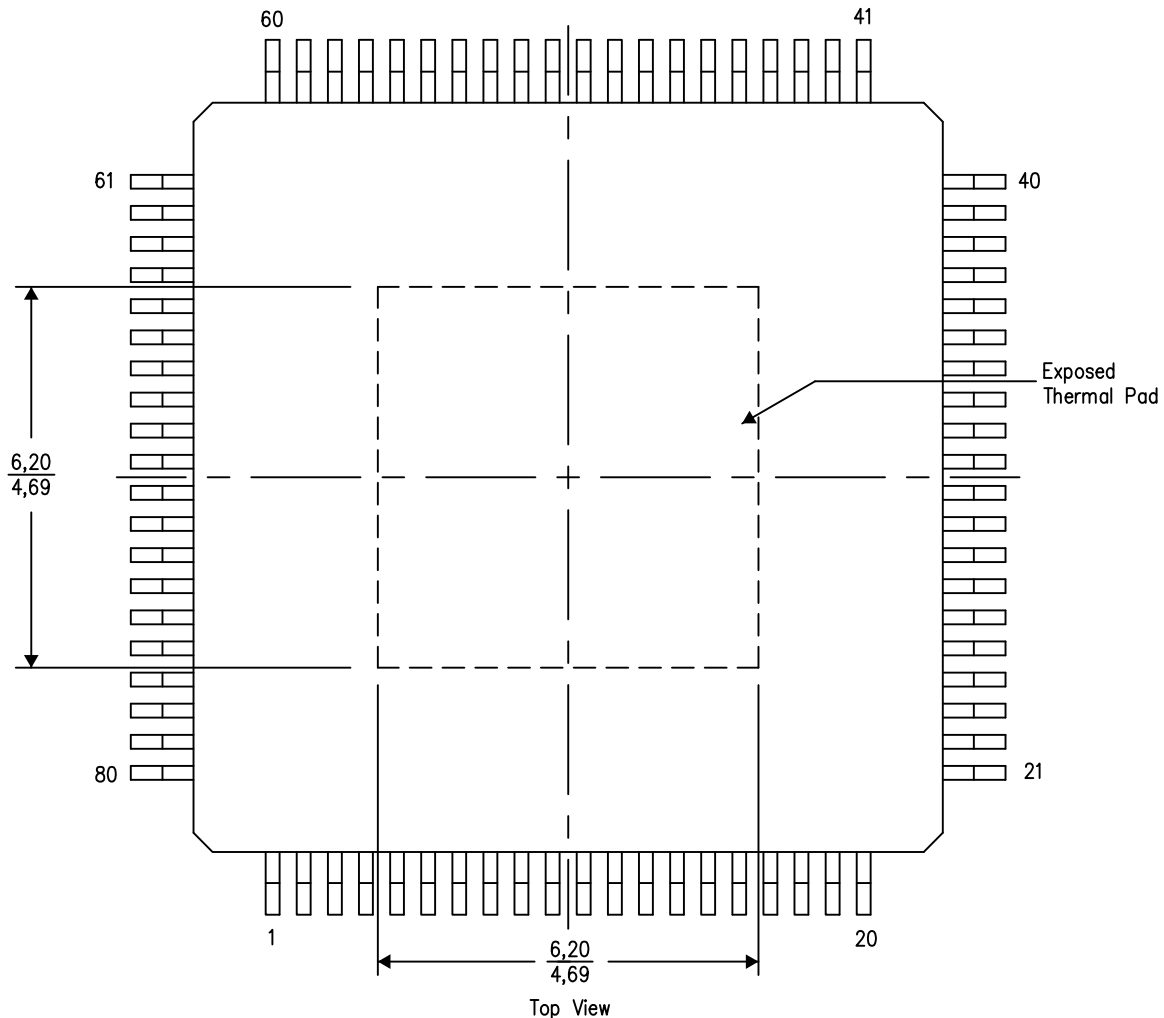
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206327-3/P 05/14

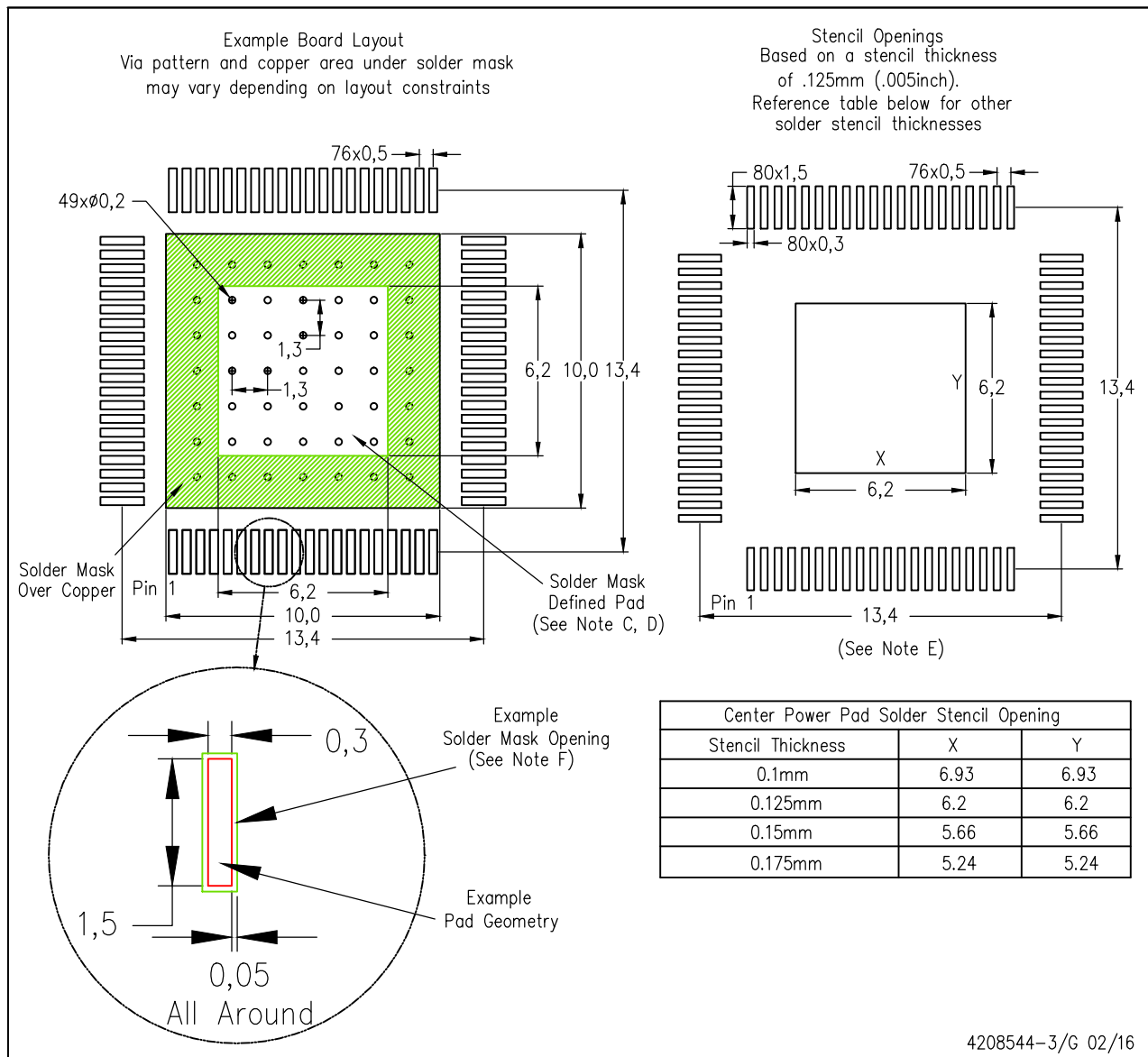
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# LAND PATTERN DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- PowerPAD is a trademark of Texas Instruments.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)