

TPCP8407

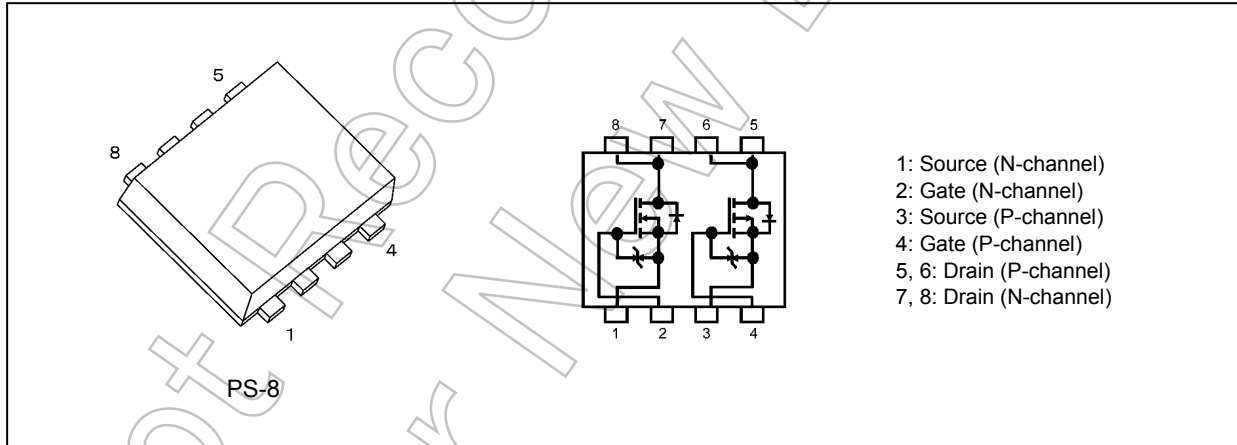
1. Applications

- Motor Drivers
- Mobile Equipment

2. Features

- (1) AEC-Q101 qualified
- (2) Small, thin package
- (3) Low gate charge
 N-channel MOSFET: $Q_{SW} = 4.7 \text{ nC (typ.)}$
 P-channel MOSFET: $Q_{SW} = 5.5 \text{ nC (typ.)}$
- (4) Low drain-source on-resistance
 N-channel MOSFET: $R_{DS(ON)} = 29.1 \text{ m}\Omega \text{ (typ.) (} V_{GS} = 10 \text{ V)}$
 P-channel MOSFET: $R_{DS(ON)} = 43.7 \text{ m}\Omega \text{ (typ.) (} V_{GS} = -10\text{V)}$
- (5) Low leakage current
 N-channel MOSFET: $I_{DSS} = 10 \text{ }\mu\text{A (max) (} V_{DS} = 40 \text{ V)}$
 P-channel MOSFET: $I_{DSS} = -10 \text{ }\mu\text{A (max) (} V_{DS} = -40 \text{ V)}$
- (6) Enhancement mode
 N-channel MOSFET: $V_{th} = 2 \text{ to } 3 \text{ V (} V_{DS} = 10 \text{ V, } I_D = 1 \text{ mA)}$
 P-channel MOSFET: $V_{th} = -2 \text{ to } -3 \text{ V (} V_{DS} = -10 \text{ V, } I_D = -1 \text{ mA)}$

3. Packaging and Internal Circuit



Start of commercial production

2013-05

4. Absolute Maximum Ratings (Note) ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

4.1. N-Channel MOSFET

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	40	V
Gate-source voltage	V_{GSS}	± 20	
Drain current (DC) (Note 1)	I_D	5	A
Drain current (pulsed) (Note 1)	I_{DP}	20	
Power dissipation (single operation) (t = 5 s) (Note 2), (Note 4)	$P_{D(1)}$	1.77	W
Power dissipation (per device for dual operation) (t = 5 s) (Note 2), (Note 5)	$P_{D(2)}$	1.47	
Power dissipation (single operation) (t = 5 s) (Note 3), (Note 4)	$P_{D(1)}$	0.69	
Power dissipation (per device for dual operation) (t = 5 s) (Note 3), (Note 5)	$P_{D(2)}$	0.43	
Single-pulse avalanche energy (Note 6)	E_{AS}	33.2	mJ
Avalanche current	I_{AR}	5	A
Channel temperature (Note 7)	T_{ch}	175	$^\circ\text{C}$
Storage temperature (Note 7)	T_{stg}	-55 to 175	

4.2. P-Channel MOSFET

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	-40	V
Gate-source voltage	V_{GSS}	-20/+10	
Drain current (DC) (Note 1)	I_D	-4	A
Drain current (pulsed) (Note 1)	I_{DP}	-16	
Power dissipation (single operation) (t = 5 s) (Note 2), (Note 4)	$P_{D(1)}$	1.77	W
Power dissipation (per device for dual operation) (t = 5 s) (Note 2), (Note 5)	$P_{D(2)}$	1.47	
Power dissipation (single operation) (t = 5 s) (Note 3), (Note 4)	$P_{D(1)}$	0.69	
Power dissipation (per device for dual operation) (t = 5 s) (Note 3), (Note 5)	$P_{D(2)}$	0.43	
Single-pulse avalanche energy (Note 6)	E_{AS}	46.2	mJ
Avalanche current	I_{AR}	-4	A
Channel temperature (Note 7)	T_{ch}	175	$^\circ\text{C}$
Storage temperature (Note 7)	T_{stg}	-55 to 175	

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics			Symbol	Max	Unit
Channel-to-ambient thermal resistance (single operation)	(t = 5 s)	(Note 2), (Note 4)	$R_{th(ch-a)(1)}$	84.7	°C/W
Channel-to-ambient thermal resistance (per device for dual operation)	(t = 5 s)	(Note 2), (Note 5)	$R_{th(ch-a)(2)}$	102	
Channel-to-ambient thermal resistance (single operation)	(t = 5 s)	(Note 3), (Note 4)	$R_{th(ch-a)(1)}$	217.3	
Channel-to-ambient thermal resistance (per device for dual operation)	(t = 5 s)	(Note 3), (Note 5)	$R_{th(ch-a)(2)}$	348.8	

Note 1: Ensure that the channel temperature does not exceed 175 °C.

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

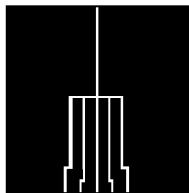
Note 4: Power dissipation and thermal resistance values per device with the other device being off (During single operation, power is supplied to only one of the two devices.)

Note 5: Power dissipation and thermal resistance values per device for dual operation (During dual operation, power is evenly supplied to both devices.)

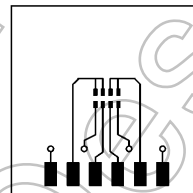
Note 6: N channel: $V_{DD} = 25\text{ V}$, $T_{ch} = 25\text{ °C}$ (initial), $L = 1.379\text{ mH}$, $R_G = 1\text{ }\Omega$, $I_{AR} = 5\text{ A}$

P channel: $V_{DD} = -25\text{ V}$, $T_{ch} = 25\text{ °C}$ (initial), $L = 2.999\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AR} = -4\text{ A}$

Note 7: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Not Recommended for New

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

6.1.1. N-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	40	—	—	V
Drain-source breakdown voltage (Note 8)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	20	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2	2.5	3	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 6\text{ V}, I_D = 2.5\text{ A}$	—	39.3	62.8	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$	—	29.1	36.3	

6.1.2. P-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = -16/+10\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current	I_{DSS}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-40	—	—	V
Drain-source breakdown voltage (Note 8)	$V_{(BR)DSX}$	$I_D = -10\text{ mA}, V_{GS} = 10\text{ V}$	-30	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-2	-2.5	-3	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = -6\text{ V}, I_D = -2\text{ A}$	—	51.4	82.2	$\text{m}\Omega$
		$V_{GS} = -10\text{ V}, I_D = -2\text{ A}$	—	43.7	56.8	

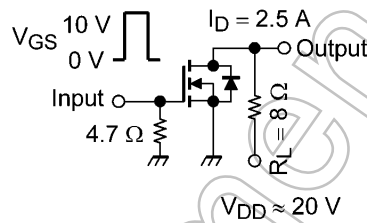
Note 8: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Not Recommended for New

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

6.2.1. N-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	505	—	pF
Reverse transfer capacitance	C_{rss}		—	66	—	
Output capacitance	C_{oss}		—	115	—	
Switching time (rise time)	t_r	See Fig. 6.2.1.1.	—	5	—	ns
Switching time (turn-on time)	t_{on}		—	12	—	
Switching time (fall time)	t_f		—	4	—	
Switching time (turn-off time)	t_{off}		—	17	—	

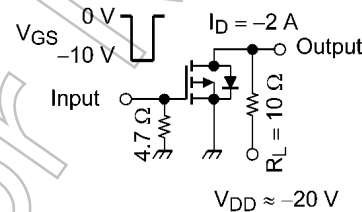


Duty $\leq 1\%$, $t_w = 10\text{ }\mu\text{s}$

Fig. 6.2.1.1 Switching Time Test Circuit

6.2.2. P-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	810	—	pF
Reverse transfer capacitance	C_{rss}		—	85	—	
Output capacitance	C_{oss}		—	130	—	
Switching time (rise time)	t_r	See Fig. 6.2.2.1.	—	8	—	ns
Switching time (turn-on time)	t_{on}		—	25	—	
Switching time (fall time)	t_f		—	33	—	
Switching time (turn-off time)	t_{off}		—	126	—	



Duty $\leq 1\%$, $t_w = 10\text{ }\mu\text{s}$

Fig. 6.2.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

6.3.1. N-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 32\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$	—	11.8	—	nC
Gate-source charge 1	Q_{gs1}		—	2.1	—	
Gate-drain charge	Q_{gd}		—	3.9	—	
Gate switch charge	Q_{SW}		—	4.7	—	

6.3.2. P-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx -32\text{ V}$, $V_{GS} = -10\text{ V}$, $I_D = -4\text{ A}$	—	18	—	nC
Gate-source charge 1	Q_{gs1}		—	2.6	—	
Gate-drain charge	Q_{gd}		—	4.6	—	
Gate switch charge	Q_{SW}		—	5.5	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

6.4.1. N-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 9)	I_{DRP}	—	—	—	20	A
Diode forward voltage	V_{DSF}	$I_{DR} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	—	—	-1.2	V

6.4.2. P-Channel MOSFET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 9)	I_{DRP}	—	—	—	-16	A
Diode forward voltage	V_{DSF}	$I_{DR} = -4\text{ A}$, $V_{GS} = 0\text{ V}$	—	—	1.2	V

Note 9: Ensure that the channel temperature does not exceed $175\text{ }^\circ\text{C}$.

7. Marking

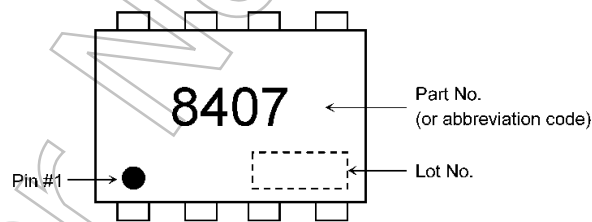


Fig. 7.1 Marking

8. Characteristics Curves (Note)

8.1. N-Channel MOSFET

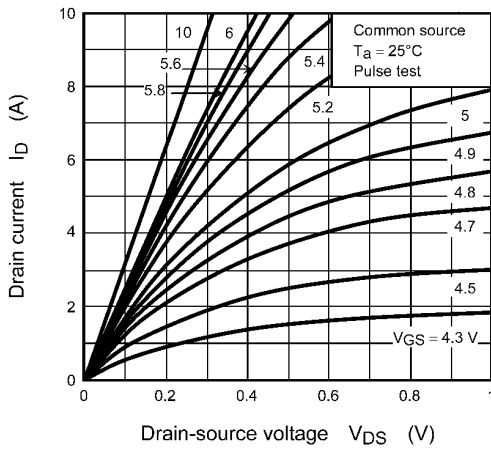


Fig. 8.1.1 ID - VDS

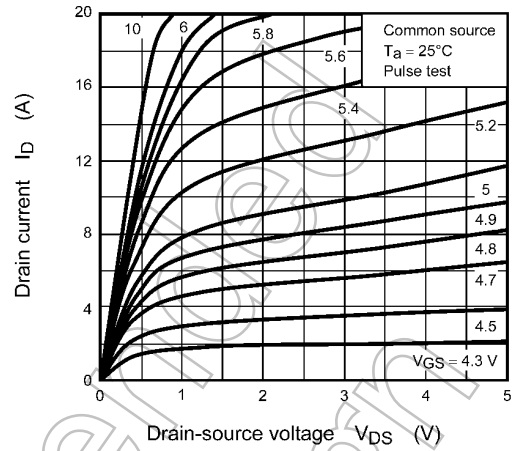


Fig. 8.1.2 ID - VDS

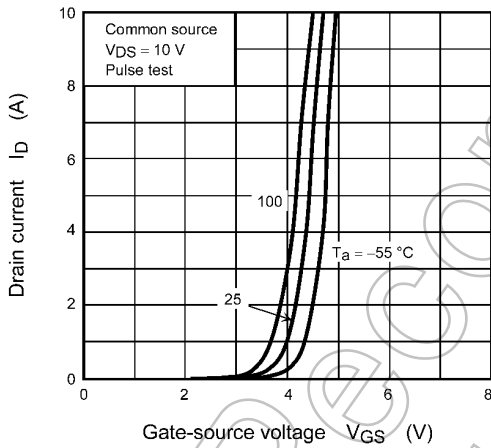


Fig. 8.1.3 ID - VGS

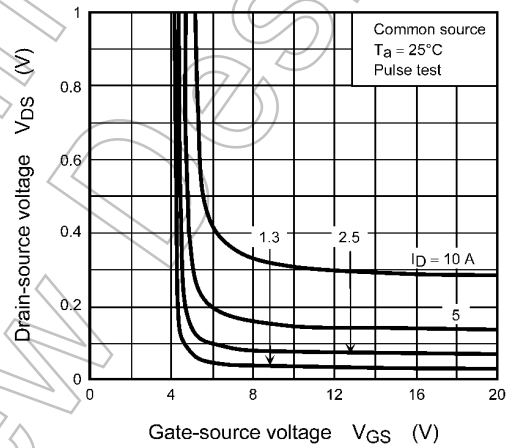


Fig. 8.1.4 VDS - VGS

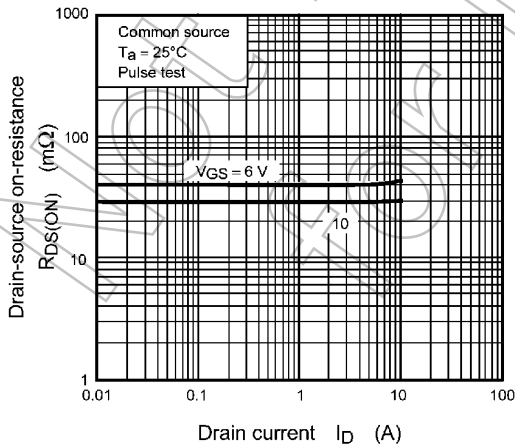


Fig. 8.1.5 RDS(ON) - ID

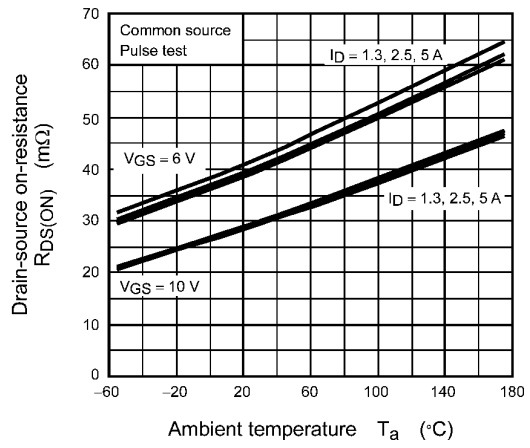


Fig. 8.1.6 RDS(ON) - Ta (Note 10)

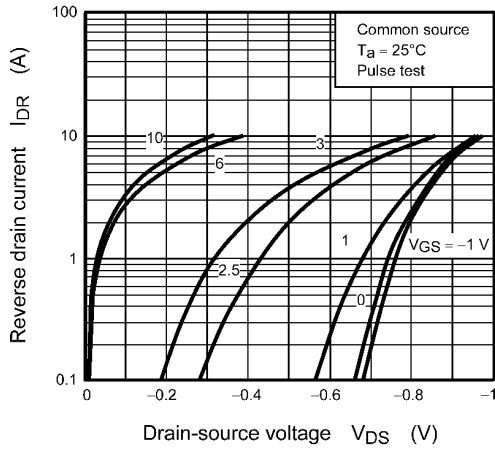


Fig. 8.1.7 $I_{DR} - V_{DS}$

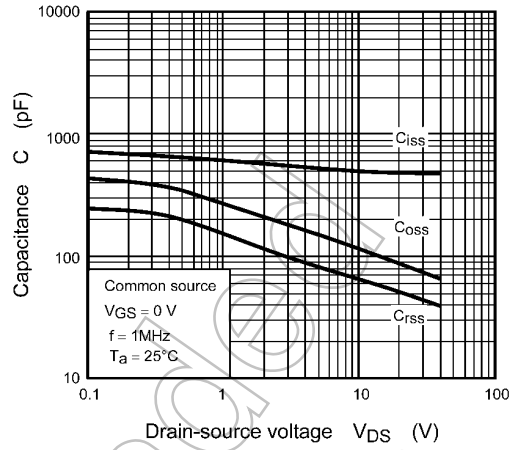


Fig. 8.1.8 Capacitance - V_{DS}

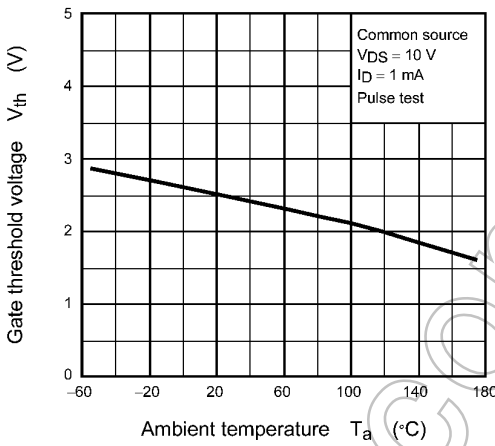


Fig. 8.1.9 $V_{th} - T_a$ (Note 10)

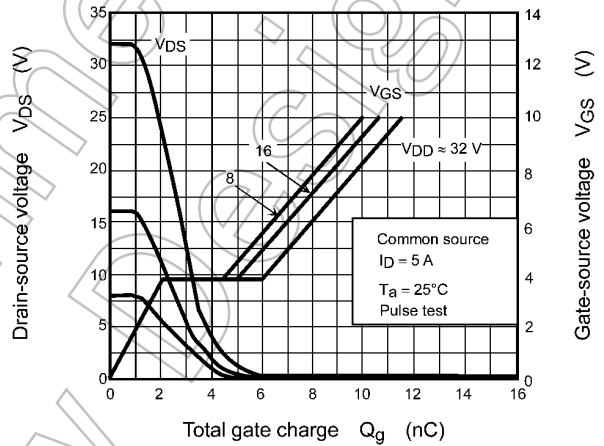


Fig. 8.1.10 Dynamic Input/Output Characteristics

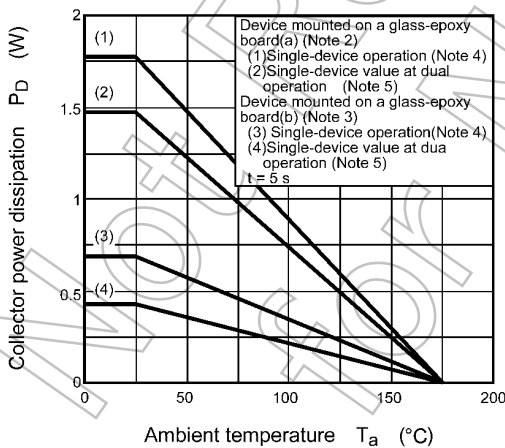


Fig. 8.1.11 $P_D - T_a$
(Guaranteed Maximum) (Note 10)

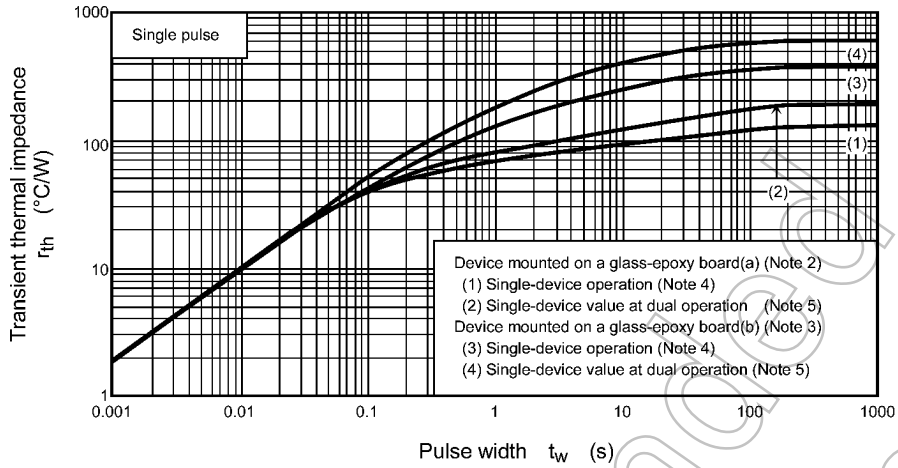


Fig. 8.1.12 $r_{th} - t_w$
(Guaranteed Maximum)

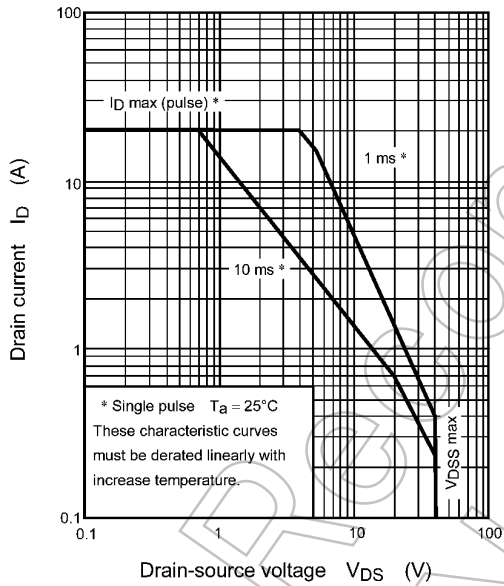


Fig. 8.1.13 Safe Operating Area
(Guaranteed Maximum)

8.2. P-Channel MOSFET

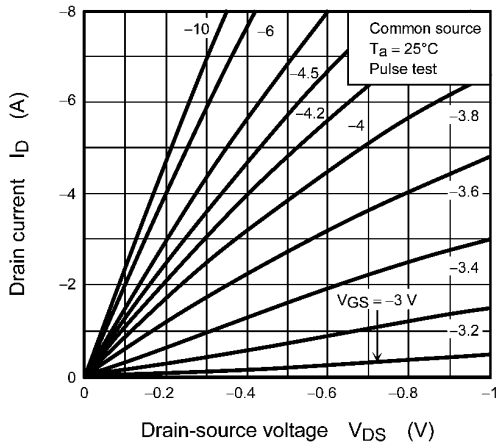


Fig. 8.2.1 $I_D - V_{DS}$

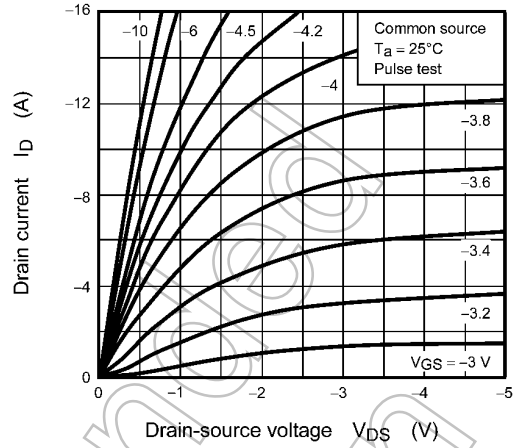


Fig. 8.2.2 $I_D - V_{DS}$

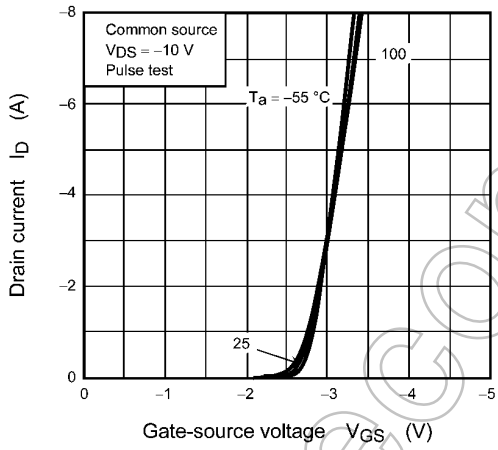


Fig. 8.2.3 $I_D - V_{GS}$

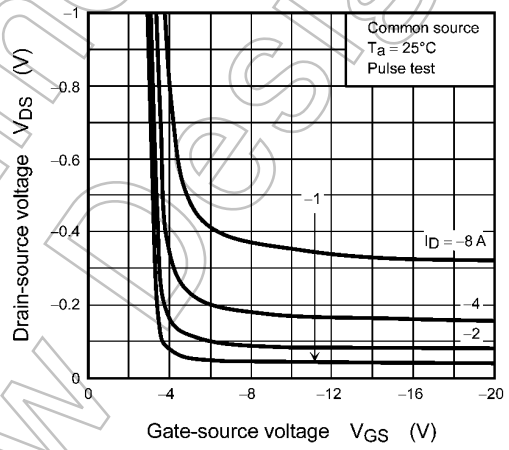


Fig. 8.2.4 $V_{DS} - V_{GS}$

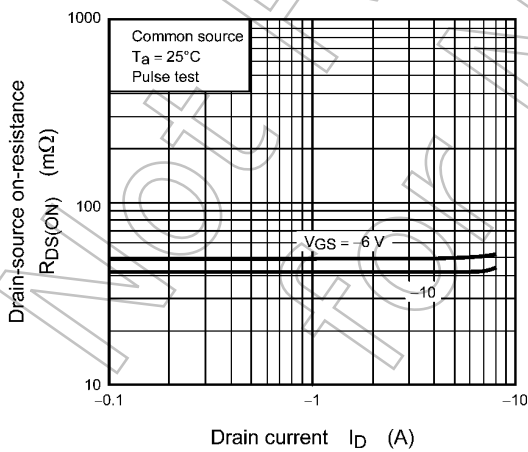


Fig. 8.2.5 $R_{DS(ON)} - I_D$

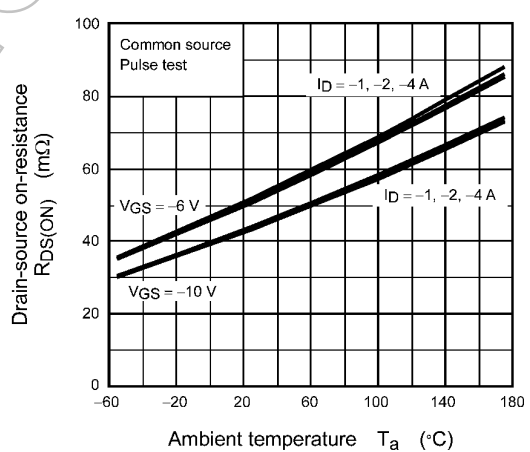


Fig. 8.2.6 $R_{DS(ON)} - T_a$ (Note 10)

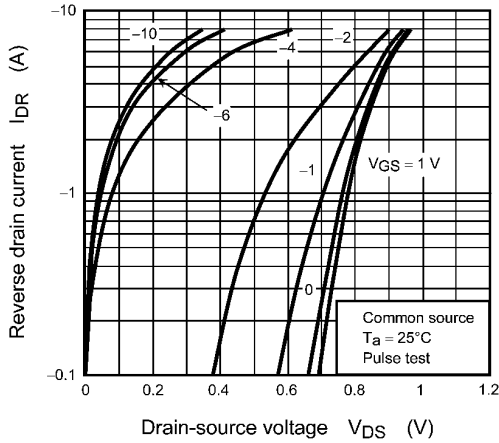


Fig. 8.2.7 $I_{DR} - V_{DS}$

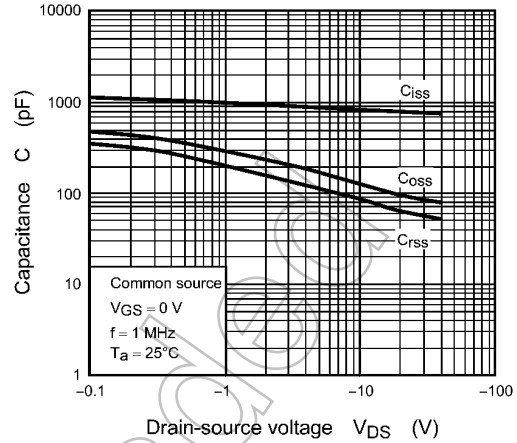


Fig. 8.2.8 Capacitance - V_{DS}

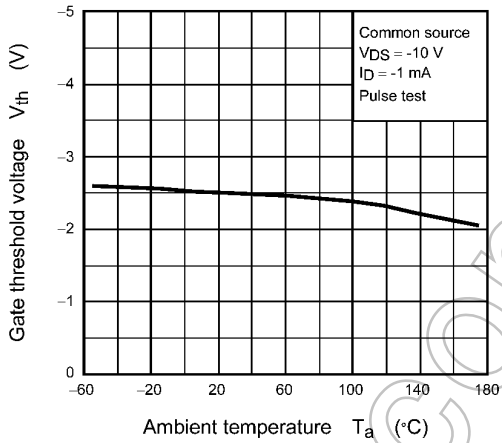


Fig. 8.2.9 $V_{th} - T_a$ (Note 10)

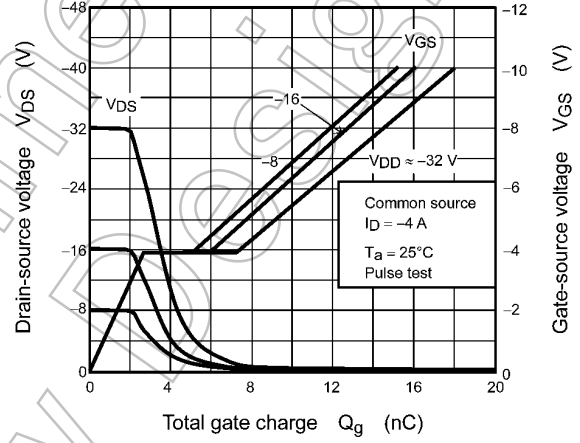


Fig. 8.2.10 Dynamic Input/Output Characteristics

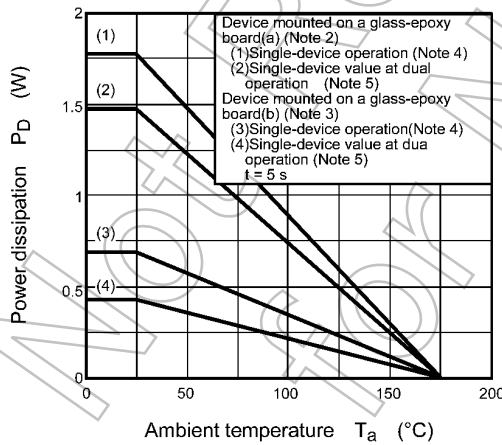


Fig. 8.2.11 $P_D - T_a$
 (Guaranteed Maximum) (Note 10)

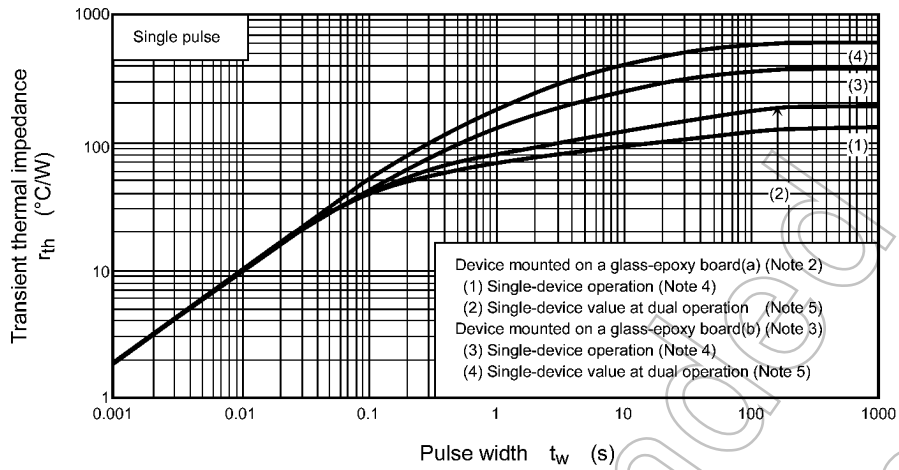


Fig. 8.2.12 $r_{th} - t_w$
(Guaranteed Maximum)

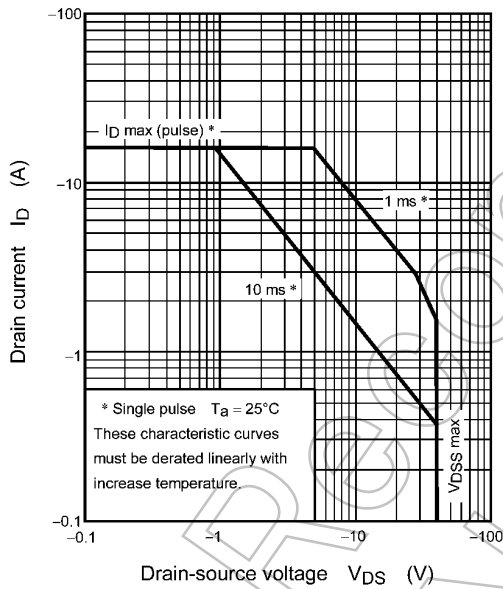


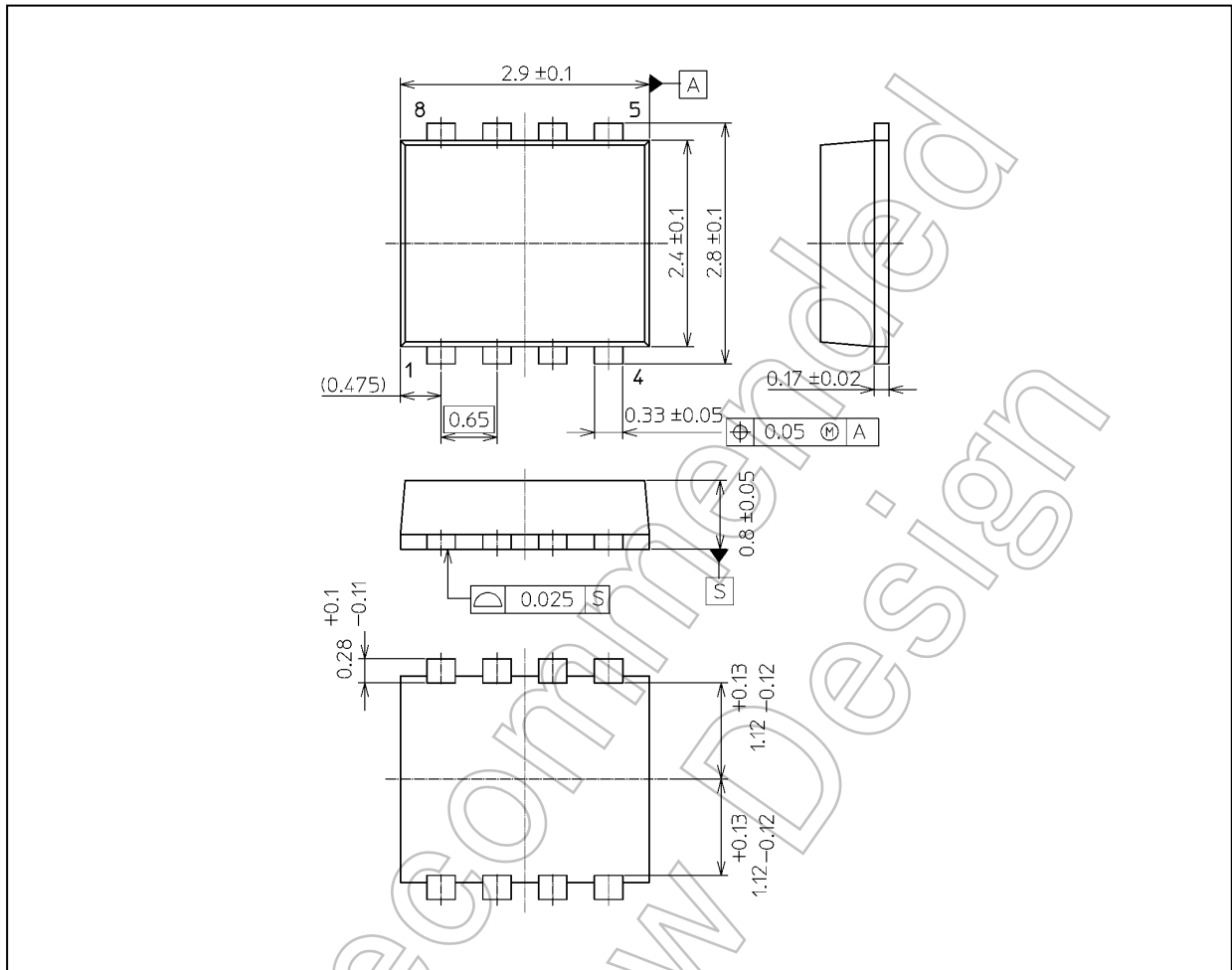
Fig. 8.2.13 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Note 10: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Package Dimensions

Unit: mm



Weight: 0.017 g (typ.)

Package Name(s)
TOSHIBA: 2-3V1S
Nickname: PS-8

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