National Semiconductor

MICROCIRCUIT DATA SHEET

MN100324-X REV 2A0

Original Creation Date: 10/30/95
Last Update Date: 07/30/99
Last Major Revision Date: 03/24/99

HEX TTL-to-ECL TRANSLATOR

General Description

The 100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable Input (E), when LOW, holds all inverting outputs HIGH and holds all true inputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the 100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The VEE and VTTL power may be applied in either order.

Industry Part Number

100324

NS Part Numbers

100324DMQB
100324FMQB
100324J-QMLV
100324W-QMLV

Prime Die

F324

Controlling Document

5962-91530

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 50% power reduction of the 100124
- 2000V ESD protection
- -4.2V to -5.7V operating range

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature (Tstg)	-65 C to +150 C
Maximum Junction Temperature (Tj)	
Ceramic	+175 C
Plastic	+150 C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	-0.5V to +6.0V
Output Current (DC Output HIGH)	-50mA
ESD (Note 2)	$\geq$ 2000V
VTTL Pin Potential to Ground Pin	-0.5V to +6.0V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Military	-55 C to +125 C
Industrial	-40 C to +85 C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, Tc= -55C to +125C, VCC=VCCA=GND, VTTL Range: +4.5V to +5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-4.5V, VTTL=5.5V, VM=2.7V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input Breakdown Current	VEE=-4.5V, VTTL=5.5V, VM=7.0V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input Low Current	VEE=-4.5V, VTTL=5.5V, VM=0.4V	1, 3	Dn		-0.9	mA	1, 2, 3
		VEE= -4.5V, VTTL=5.5V, VM=0.4V	1, 3	E		-5.4	mA	1, 2, 3
VFCD	Input Clamp Diode Voltage	VEE= -4.5V, VTTL= 4.5V, IM= -18mA	1, 3	INPUTS		-1.2	V	1, 2, 3
VOH	Output HIGH Voltage	Vee=-4.2V/-5.7V, VTTL=5.0V, VIH=5.0V, VIL=0.0V LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VTTL=5.0V, VIH=5.0V, VIL=0.0V LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage	Vee=-4.2V/-5.7V, VTTL=5.0V, VIH=2.0V, VIL=0.8V LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage	Vee=-4.2V/-5.7V, VTTL=5.0V, VIH=2.0V, VIL=0.8V LOADING: 50 ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	2.0	5.0	V	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	0.0	0.8	V	1, 2, 3
Cin	Input Capacitance	VEE=Open, VTTL=Open	6	INPUTS		10	pF	4
IEE	Power Supply Current	VEE=-4.2/-5.7V, VTTL=5.0V	1, 3	VEE	-70	-22	mA	1, 2, 3
ITTL	Power Supply Current	VEE=-4.5V, VTTL=5.5V	1, 3	VTTL		38	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vee Range: -4.2V to -5.7V, LOADING: 50 Ohms To -2.0V, VCC=VCCA=GND, VTTL Range: +4.5V to +5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH/tpHL	Propagation Delay	VEE=-4.2/-5.7V VTTL=4.5/5.5V	2, 4	Dn or E to Qn	0.5	2.9	ns	9
			2, 4	Dn or E to Qn	0.3	3.3	ns	10
			2, 4	Dn or E to Qn	0.5	3.0	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V, VTTL=4.5/5.5V	6	Qn	0.45	1.8	ns	9, 10
			6	Qn	0.35	1.8	ns	11

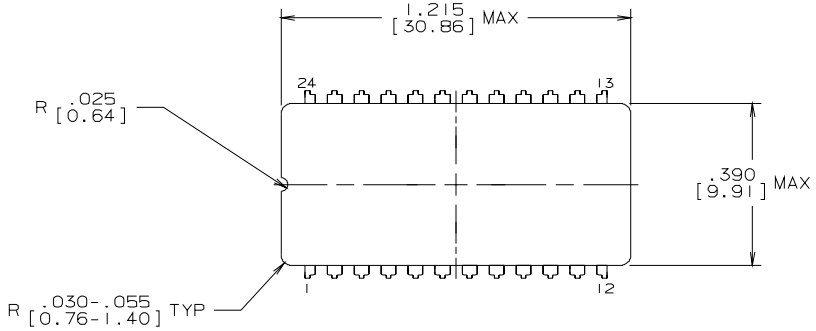
Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

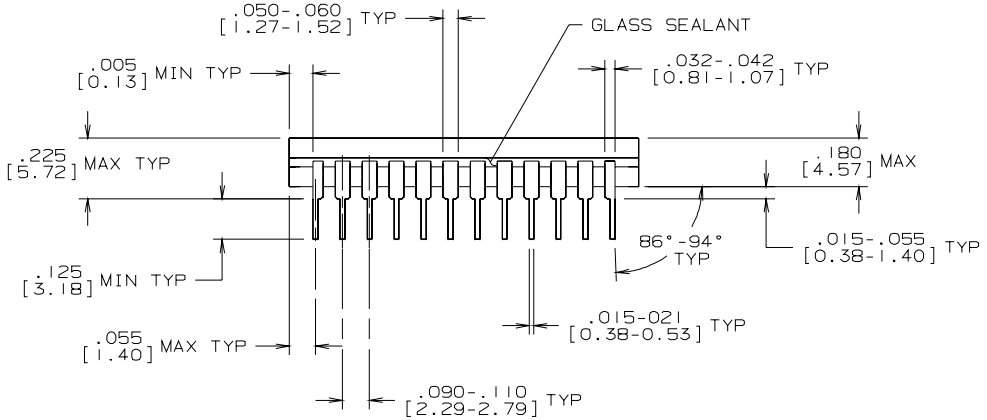
Graphics and Diagrams

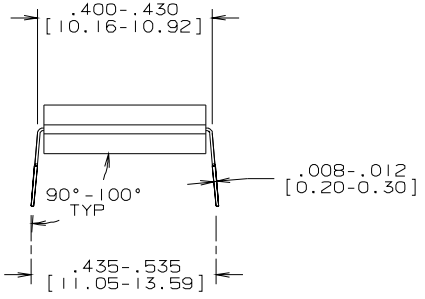
GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP (J), 24LD, .400 CENTERS (P/P DWG)
P000052A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000053A	CERPACK, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPACK, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN D.E.GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH MM

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 24 LEAD, .400 CENTERS

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-J24E	J

FORMERLY: N/A

SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
2A0	M0003420	07/30/99	Donald B. Miller	1) Added the Cin parameter and limits. 2) Added the SMD number. 3) VFCD test - changed VEE from -4.2V to -4.5V, and changed VTTL from -4.5V to 4.5V.