



The Future of Analog IC Technology®

MP6219

5V, 1A – 2A Programmable Current Limit Power Distribution Switch

DESCRIPTION

The MP6219 is a protection device designed to protect circuitry on the output from transients on input. It also protects input from undesired shorts and transients coming from the output.

The MP6219 is an integrated power switch with programmable current limit. The max load at the output is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor.

An internal charge pump drives the gate of the power device. It features a 44mΩ switch for high efficiency and requires minimal external components.

The MP6219 features current protection and thermal shutdown for fault control. It also involves UVLO and output over voltage protection.

The MP6219 is available in an 8-pin SOICE package.

FEATURES

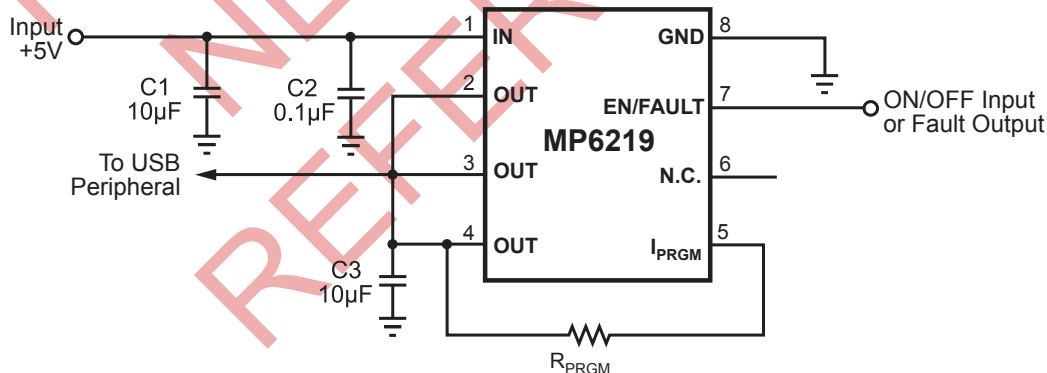
- Integrated 44mΩ FET
- Adjustable Current Limit to 2A
- Optimized for 5V Inputs
- Enable Active High
- 1.1ms Soft-Start Rise Time
- UL File # E322138

APPLICATIONS

- USB Power Distribution
- PCI Bus Power
- Notebook PC
- Inrush Current Limit
- Heavy Capacitive Loads

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TYPICAL APPLICATION



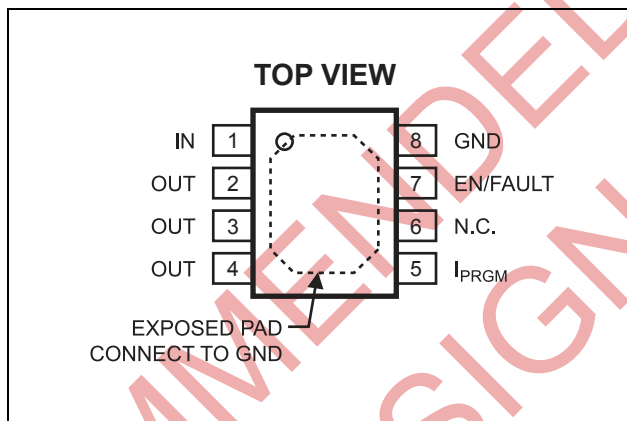
UL Recognized Component

ORDERING INFORMATION

| Part Number* | Package | Top Marking | Free Air Temperature (T _A) |
|--------------|----------------------|-------------|--|
| MP6219DN | SOIC8E (Exposed Pad) | MP6219DN | -40°C to +85°C |

* For Tape & Reel, add suffix -Z (e.g. MP6219DN-Z).
 For RoHS Compliant packaging, add suffix -LF (e.g. MP6219DN-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|--|-----------------|
| IN, OUT, I _{PRGM} | 8V |
| EN/FAULT | 6V |
| Junction Temperature..... | -40°C to +150°C |
| Continuous Power Dissipation (T _A = +25°C) ⁽²⁾ | 2.5W |
| Storage Temperature..... | -65°C to +155°C |

Recommended Operating Conditions

| | |
|----------------------------|-----------------|
| Input Voltage..... | 5V ± 10% |
| Operating Junct.Temp. | -40°C to +125°C |

| Thermal Resistance ⁽³⁾ | θ_{JA} | θ_{JC} |
|--|-----------------------|-----------------------|
| SOIC8E..... | 50 | 10 ... °C/W |

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$, $R_{PRGM} = 24\Omega$, $C_{OUT} = 10\mu F$, $T_J = 25^\circ C$, unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|--------------|---|------|------|----------|------------|
| Power FET | | | | | | |
| Delay Time | t_{DLY} | Enabling of chip to $I_D = 100mA$, 12Ω resistive load | | 0.2 | | ms |
| ON Resistance | R_{DSon} | $T_J = 25^\circ C$ | | 44 | 82 | m Ω |
| | | $T_J = 80^\circ C$, Note 4 | | 95 | | |
| Off State Output Voltage | V_{OFF} | $V_{IN} = 8Vdc$, Enable = $0Vdc$, $R_L = 500\Omega$ | | | 120 | mV |
| Thermal Latch | | | | | | |
| Shutdown Temperature | T_{SD} | | | 175 | | $^\circ C$ |
| Under/Over Voltage Protection | | | | | | |
| Output Clamping Voltage | V_{CLAMP} | Overvoltage Protection $V_{IN} = 8V$ | 5.95 | 6.65 | 7.35 | V |
| Under Voltage Lockout | V_{UVLO} | Turn on, V_{IN} rising | 3.2 | 3.6 | 4.0 | V |
| Under Voltage Lockout (UVLO) Hysteresis | V_{HYST} | | | 0.1 | | V |
| Current Limit | | | | | | |
| Current Limit | I_{LIM-SS} | $R_{PRGM} = 24\Omega$ | 1.4 | 2.0 | 2.7 | A |
| Trip Current | I_{LIM-OL} | $R_{PRGM} = 24\Omega$ | | 3.0 | | A |
| Slew Rate | | | | | | |
| Output Rise Time | T_r | Note 5 | | 1.1 | | ms |
| EN/Fault | | | | | | |
| Low Level Input Voltage | V_{IL} | Output Disabled | | | 0.5 | V |
| Intermediate Level Input Voltage | $V_{I(INT)}$ | Thermal Fault, Output Disabled | 0.80 | 1.6 | 2.0 | V |
| High Level Input Voltage | V_{IH} | Output Enabled | 2.5 | | | V |
| High State Maximum Voltage | $V_{I(MAX)}$ | | | 4.8 | | V |
| Low Level Input Current (Sink) | I_{IL} | $V_{ENABLE} = 0V$ | | -28 | -50 | μA |
| Maximum Fanout for Fault Signal | | Total number of chips that can be connected for simultaneous shutdown | | | 3 | Units |
| Maximum Voltage on Enable Pin | V_{MAX} | Note 6 | | | V_{IN} | V |
| Total Device | | | | | | |
| Supply Current | I_Q | Device Operational, No load | | 1.5 | 2.0 | mA |
| | | Thermal Shutdown | | 0.5 | | |
| Minimum Operating Voltage for UVLO | V_{MIN} | Enable < $0.5V$ | | | 3.0 | V |

Notes:

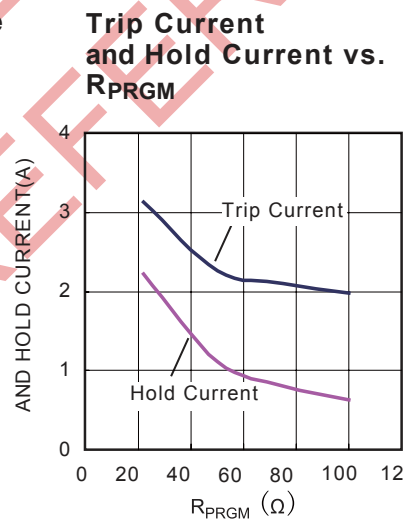
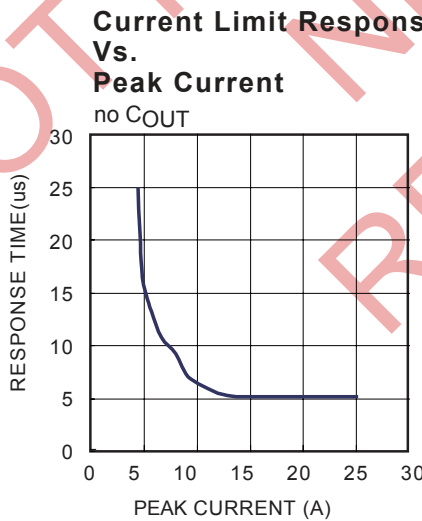
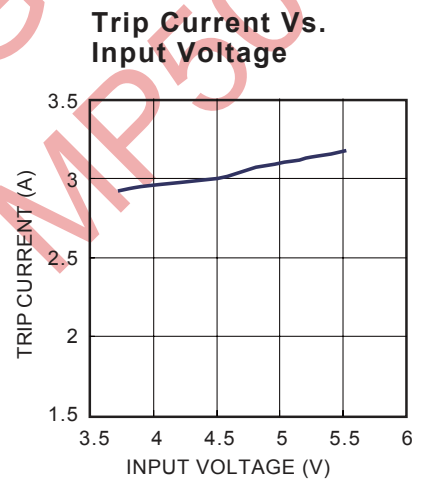
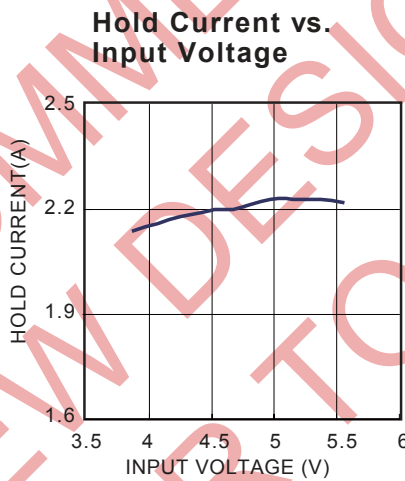
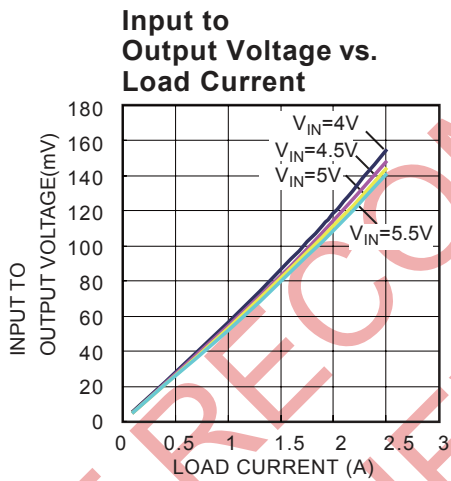
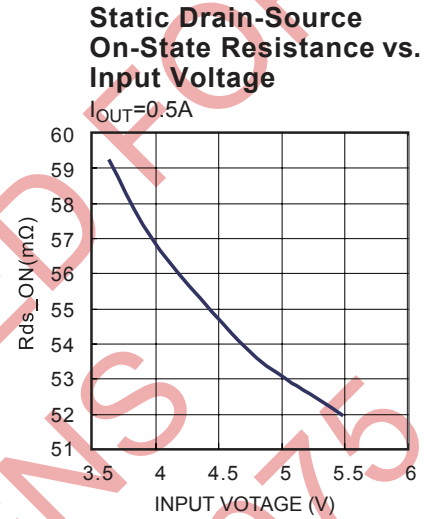
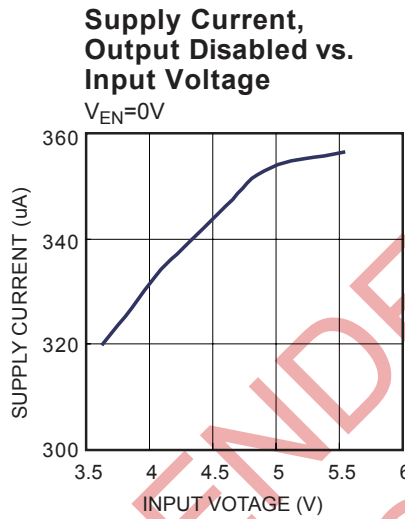
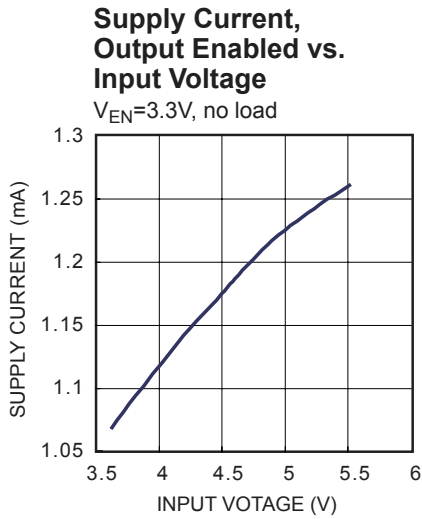
- 4) Guaranteed by design.
- 5) Measured from 10% to 90%.
- 6) Maximum Input Voltage to be $\leq 6.0V$ if $V_{IN} \geq 6.0V$. Maximum Input Voltage to be V_{IN} if $V_{IN} \leq 6.0V$.

PIN FUNCTIONS

| Pin # | Name | Description |
|---------|--------------------|--|
| 1 | IN | Input to the device. 5V nominal Input Voltage |
| 2, 3, 4 | OUT | This pin is the output of the internal power FET. |
| 5 | I _{PRGM} | A resistor between this pin and the OUTPUT pin sets the overload and short circuit current limit levels. |
| 6 | N.C. | No Connect. |
| 7 | EN/FAULT | The EN/Fault pin is a tri-state, bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. |
| 8 | GND Exposed Pad | Negative Input Voltage to the Device. This is used as the internal reference for the IC. Connect Exposed Pad to GND plane proper thermal performance. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$, $V_{EN}=3.3V$, $R_{PRGM}=24\Omega$, $C_{OUT}=10\mu F$, $T_A=25^\circ C$, unless otherwise noted.

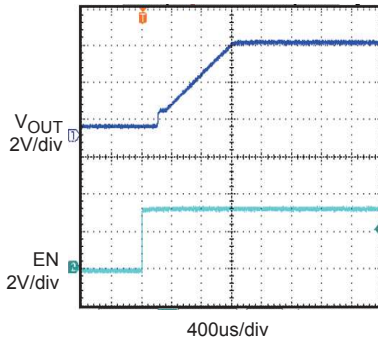


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$, $V_{EN} = 3.3V$, $R_{PRGM} = 24\Omega$, $C_{OUT} = 10\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

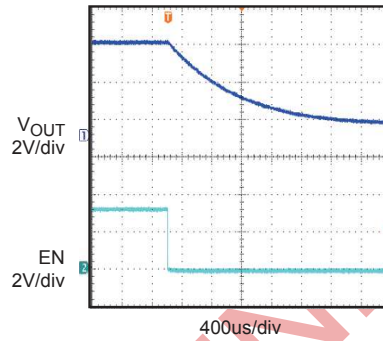
Turn On Delay and Rise Time with 1uF Load

$C_{OUT} = 1\mu F$, no load



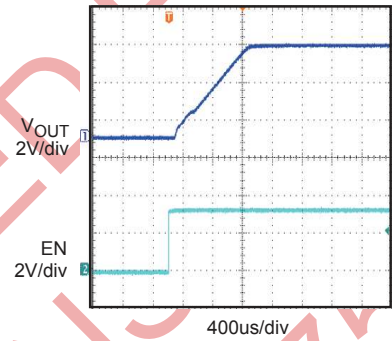
Turn Off Delay and Fall Time with 1uF Load

$C_{OUT} = 1\mu F$, no load



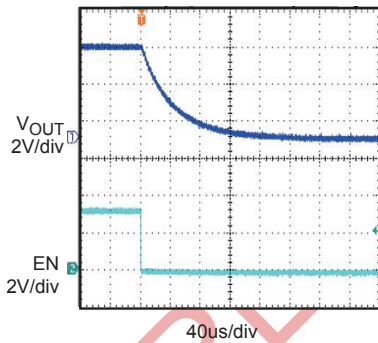
Turn On Delay and Rise Time with 10uF Load

$R_L = 3.9\Omega$, $C_{OUT} = 10\mu F$

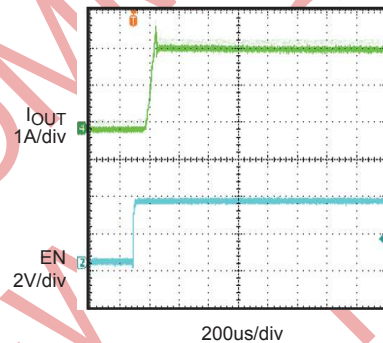


Turn Off Delay and Fall Time with 10uF Load

$R_L = 3.9\Omega$, $C_{OUT} = 10\mu F$

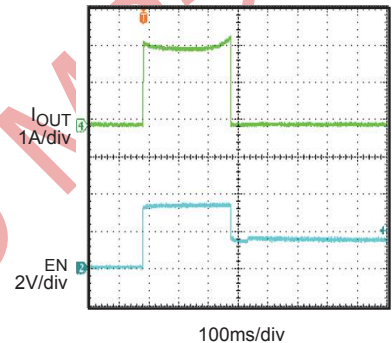


Short Circuit Current Device Enabled into Short

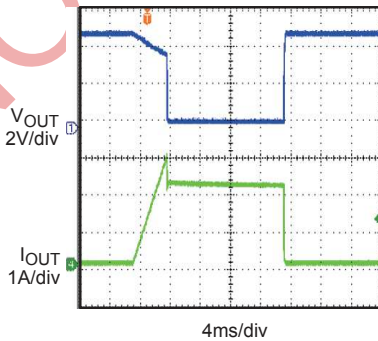


Short Circuit Current Device Enabled into Short and Thermal Shut Down

EN floating

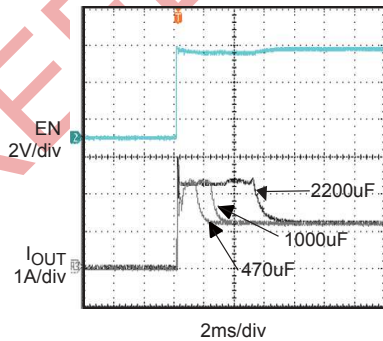


Trip Current with Ramped Load on Enabled Device

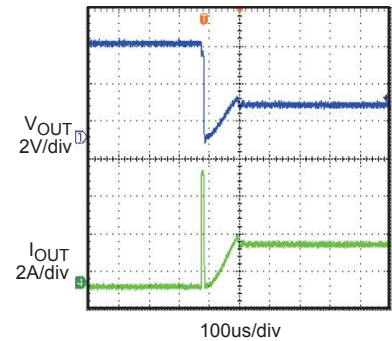


Inrush Current with Different Load Capacitance

$R_L = 3.9\Omega$, EN floating

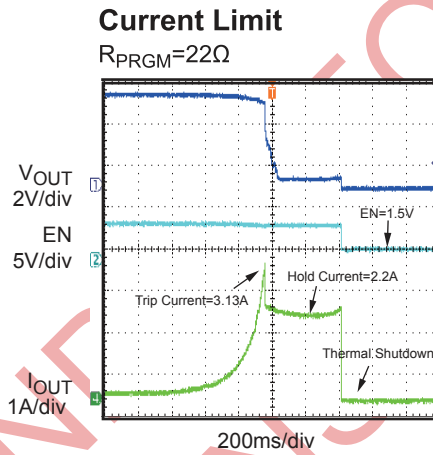
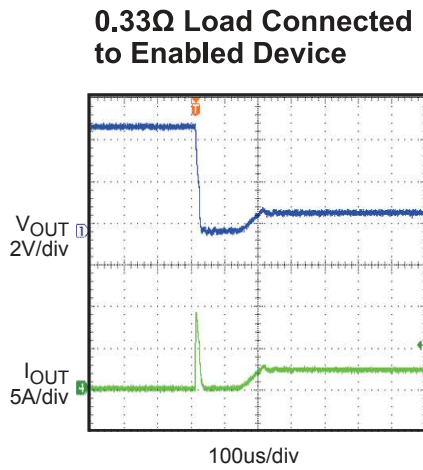


0.66Ω Load Connected to Enabled Device



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$, $V_{EN}=3.3V$, $R_{PRGM}=24\Omega$, $C_{OUT}=10\mu F$, $T_A=25^\circ C$, unless otherwise noted.



NOT RECOMMENDED FOR NEW DESIGNERS REFER TO MP5075

BLOCK DIAGRAM

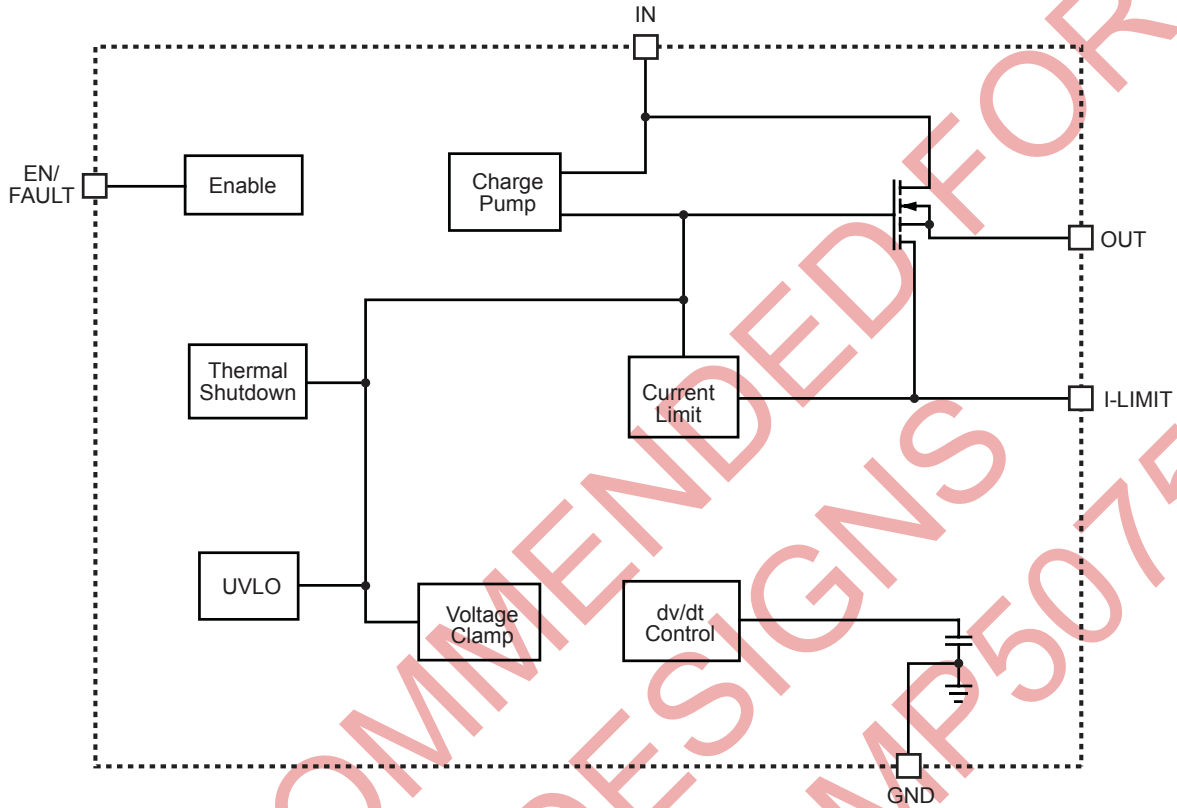


Figure 1—Functional Block Diagram

CURRENT LIMIT

The desired current limit is a function of the external current limit resistor.

Table1-Current Limit vs. Current Limit Resistor
($V_{IN}=5V$)

| | | | |
|-------------------------------|------|-------|------|
| Current Limit Resistor | 24Ω | 50Ω | 100Ω |
| Trip Current | 3.0A | 2.25A | 2.0A |
| Hold Current | 2.0A | 1.1A | 0.6A |

When the part is active, if load reaches trip current (minimum threshold current triggering overcurrent protection) or a short is present, the part switches into to a constant-current (hold current) mode. Part will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

However, when the part is powered up by V_{CC} or EN, the load current should be smaller than hold current. Otherwise, the part can't be fully turned on.

In a typical application using a current limit resistor of 24Ω, the trip current will be 3A and the hold current will be 2A. If the device is in its normal operating state and passing 2A it will need to dissipate only 176mW with the very low on resistance of 44mΩ. For the package dissipation of 50°C/Watt, the temperature rise will only be + 8.8°C. Combined with a 25°C ambient, this is only 33.8°C total package temperature.

During a short circuit condition, the device now has 5V across it and the hold current clamps at 2A and therefore must dissipate 10W. At 50°C/watt, if uncontrolled, the temperature would rise above the thermal protection threshold (+175°C) and the device will shutdown to cause the temperature to drop.

Proper heat sink must be used if the device is intended to supply the hold current and not shutdown. Without a heat sink, hold current should be maintained below 600mA at + 25°C and below 360mA at +85°C to prevent the device from activating the thermal shutdown feature.

EN/FAULT PIN

The EN/Fault Pin is a Bi-Directional three level I/O with a weak pull up current (28uA typical). The three levels are low, mid and high. It functions to enable/disable the part and to relay Fault information.

EN/Fault pin as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

EN/Fault pin as an output:

1. The pull up current may (if not overridden) allow a “wired nor” pull up to enable the part.
2. An under voltage will cause a low on the EN/Fault pin, and will clear the fault flag.
3. A thermal fault will cause a mid level on the EN/Fault pin, and will set the fault flag.

The EN/Fault line must be above the mid level for the output to be turned on.

The fault flag is a internal flip-flop that can be set or reset under various conditions:

1. Thermal Shutdown: set fault flag
2. Under Voltage: reset fault flag
3. Low voltage on EN/Fault pin: reset fault flag
4. Mid voltage on EN/Fault pin: no effect

Under a fault, the EN/Fault pin is driven to the mid level.

There are 4 types of faults, and each fault has a direct and indirect effect on the EN/Fault pin and the internal fault flag.

In a typical application where there are multiple MP6219 chips in a system, the EN/Fault lines are typically connected together.

Table2-Fault Function Influence in Application

| Fault description | Internal action | Effect on Fault Pin | Effect on Flag | Effect on secondary Part |
|--------------------|---|---|----------------|---|
| Short/over current | Limit current | none | none | none |
| Under Voltage | Output is turned off | Internally drives EN/Fault pin to Logic low | Flag is reset | Secondary part output is disabled, and fault flag is reset. |
| Over Voltage | Limit output voltage | None | None | None |
| Thermal Shutdown | Shutdown part. The part is latched off until a UVLO or externally driven to ground. | Internally drives EN/Fault pin to mid level | Flag is Set | Secondary part output is disabled. |

UNDER VOLTAGE LOCK OUT OPERATION

If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

When the supply goes above the UVLO threshold, the output is enabled and the fault line is released. When the fault line is released it will be pulled high by a 28uA current source. No external pull up resistor is required. In addition, the pull up voltage is limited to 5 volts.

THERMAL PROTECTION

When thermal protection is triggered, the output is disabled and the fault line is driven to the mid level. The thermal fault condition is latched

(meaning the fault flag is set), and the part will remain latched off until the fault (enable) line is brought low. Cycling the power below the UVLO threshold will also reset the fault flag.

PCB LAYOUT

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference.

Place R_{PRGM} close to I_{PRGM} pin and input cap close to IN pin. Keep the N/C pin float. Put vias in thermal pad and ensure enough copper area near IN and OUT to achieve better thermal performance.

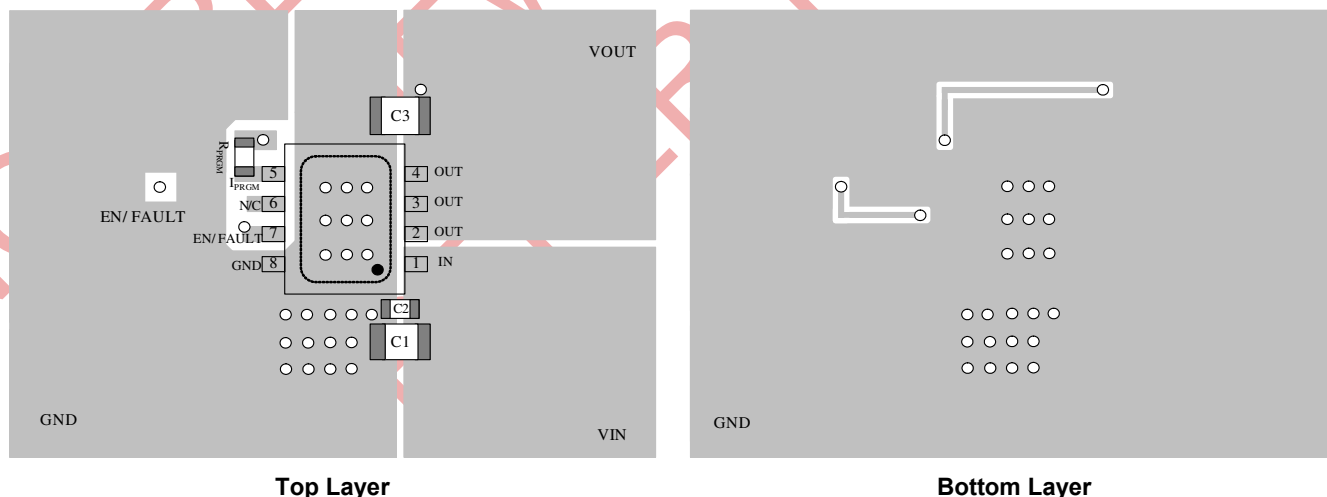
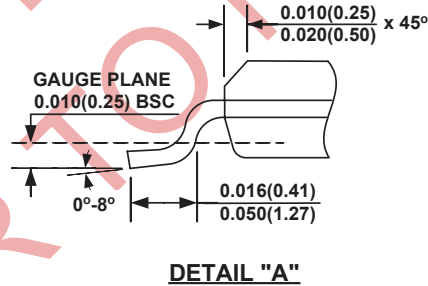
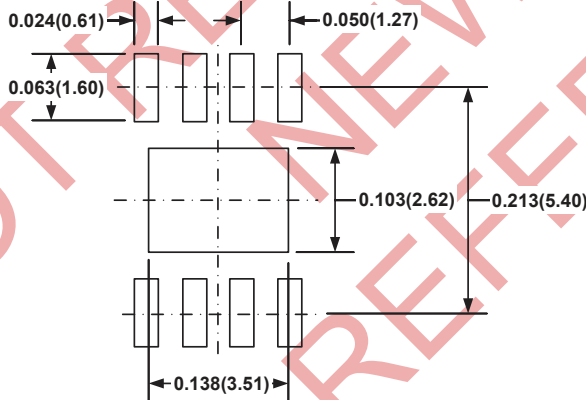
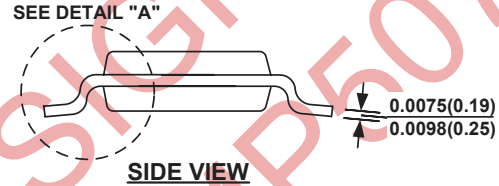
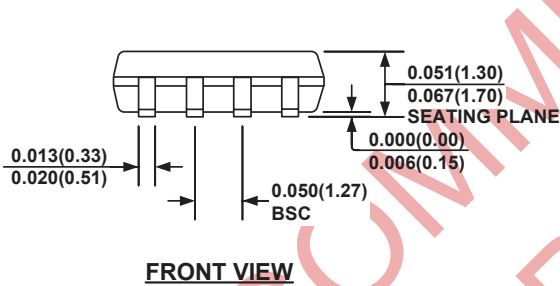
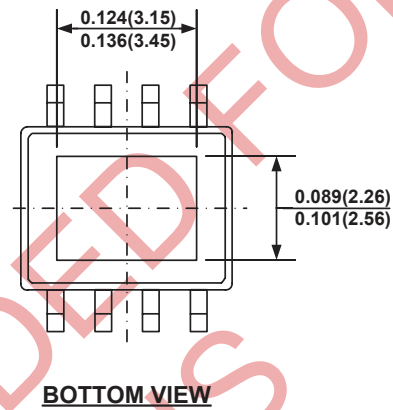
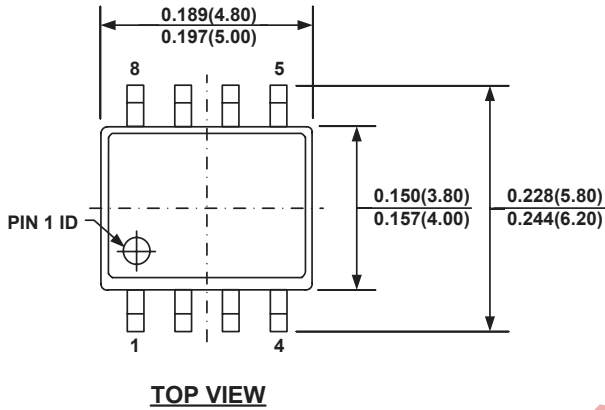


Figure 2—PCB Layout

PACKAGE INFORMATION

SOIC8E (EXPOSED PAD)



NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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