

# NTR4101P, NTRV4101P

## MOSFET – Power, Single P-Channel, Trench, SOT-23 –20 V

### Features

- Leading –20 V Trench for Low  $R_{DS(on)}$
- –1.8 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint
- NTRV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Load/Power Management for Portables
- Load/Power Management for Computing
- Charging Circuits and Battery Protection

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DS}$	–20	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 8.0$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	–2.4	A
			$T_A = 85^\circ\text{C}$	–1.7	
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$	–3.2		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	0.73	W
			$t \leq 10$ s	1.25	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	–1.8	A
		$T_A = 85^\circ\text{C}$	–1.3		
		$T_A = 25^\circ\text{C}$	$P_D$	0.42	
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$	–18	A	
ESD Capability (Note 3)	$C = 100$ pF, $R_S = 1500$ $\Omega$	ESD	225	V	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	–55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	–2.4	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{GS} = -8$ V, $I_L = -1.8$ Apk, $L = 10$ mH, $R_G = 25$ $\Omega$ )		EAS	16	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

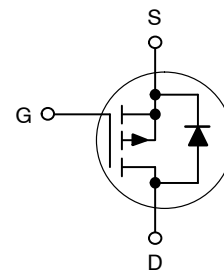


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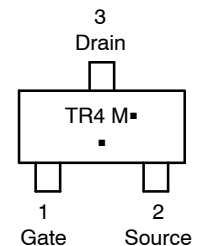
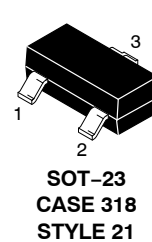
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$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
–20 V	70 m $\Omega$ @ –4.5 V	–3.2 A
	90 m $\Omega$ @ –2.5 V	
	112 m $\Omega$ @ –1.8 V	

### P-Channel MOSFET



### MARKING DIAGRAM & PIN ASSIGNMENT



TR4 = Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTR4101PT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTRV4101PT1G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTR4101P, NTRV4101P

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	170	°C/W
Junction-to-Ambient – $t < 10$ s (Note 1)	$R_{\theta JA}$	100	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	300	

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- Surface-mounted on FR4 board using the minimum recommended pad size.
- ESD Rating Information: HBM Class 0

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4) ( $V_{GS} = 0$ V, $I_D = -250$ $\mu\text{A}$ )	$V_{(BR)DSS}$	-20			V
Zero Gate Voltage Drain Current (Note 4) ( $V_{GS} = 0$ V, $V_{DS} = -16$ V)	$I_{DSS}$			-1.0	$\mu\text{A}$
Gate-to-Source Leakage Current ( $V_{GS} = \pm 8.0$ V, $V_{DS} = 0$ V)	$I_{GSS}$			$\pm 100$	nA

### ON CHARACTERISTICS

Gate Threshold Voltage (Note 4) ( $V_{GS} = V_{DS}$ , $I_D = -250$ $\mu\text{A}$ )	$V_{GS(th)}$	-0.4	-0.72	-1.2	V
Drain-to-Source On-Resistance ( $V_{GS} = -4.5$ V, $I_D = -1.6$ A) ( $V_{GS} = -2.5$ V, $I_D = -1.3$ A) ( $V_{GS} = -1.8$ V, $I_D = -0.9$ A)	$R_{DS(on)}$		70 90 112	85 120 210	m $\Omega$
Forward Transconductance ( $V_{DS} = -5.0$ V, $I_D = -2.3$ A)	$g_{FS}$		7.5		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$(V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -10$ V)	$C_{iss}$	675		pF
Output Capacitance		$C_{oss}$	100		
Reverse Transfer Capacitance		$C_{rss}$	75		
Total Gate Charge	$(V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -1.6$ A)	$Q_{G(tot)}$	7.5	8.5	nC
Gate-to-Source Gate Charge	$(V_{DS} = -10$ V, $I_D = -1.6$ A)	$Q_{GS}$	1.2		nC
Gate-to-Drain "Miller" Charge	$(V_{DS} = -10$ V, $I_D = -1.6$ A)	$Q_{GD}$	2.2		nC
Gate Resistance		$R_G$	6.5		$\Omega$

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$(V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -1.6$ A, $R_G = 6.0$ $\Omega$ )	$t_{d(on)}$	7.5		ns
Rise Time		$t_r$	12.6		
Turn-Off Delay Time		$t_{d(off)}$	30.2		
Fall Time		$t_f$	21.0		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$(V_{GS} = 0$ V, $I_S = -2.4$ A)	$V_{SD}$		-0.82	-1.2	V
Reverse Recovery Time	$(V_{GS} = 0$ V, $dI_{SD}/dt = 100$ A/ $\mu\text{s}$ , $I_S = -1.6$ A)	$t_{rr}$		12.8	15	ns
Charge Time		$t_a$		9.9		ns
Discharge Time		$t_b$		3.0		ns
Reverse Recovery Charge		$Q_{rr}$		1008		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: Pulse Width  $\leq 300$   $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperature.

# NTR4101P, NTRV4101P

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

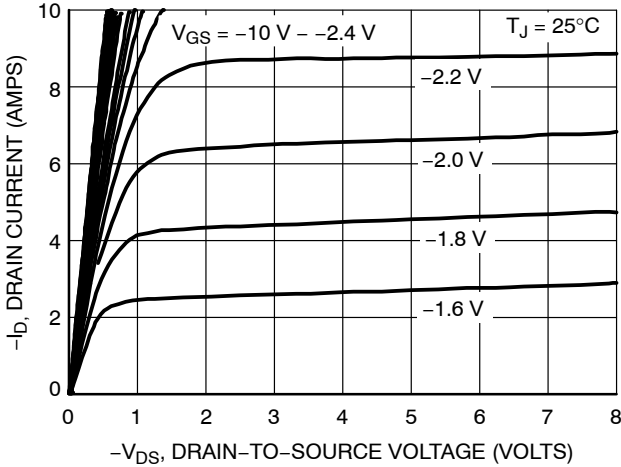


Figure 1. On-Region Characteristics

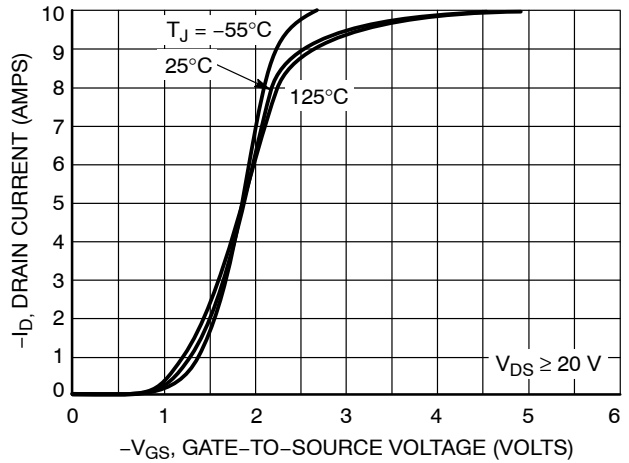


Figure 2. Transfer Characteristics

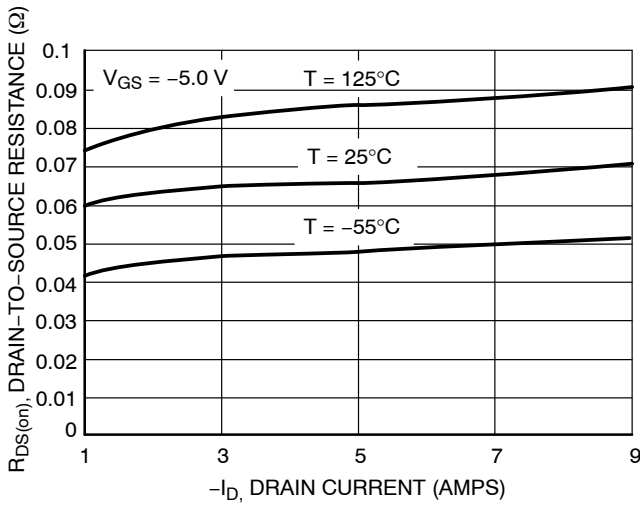


Figure 3. On-Resistance vs. Drain Current and Temperature

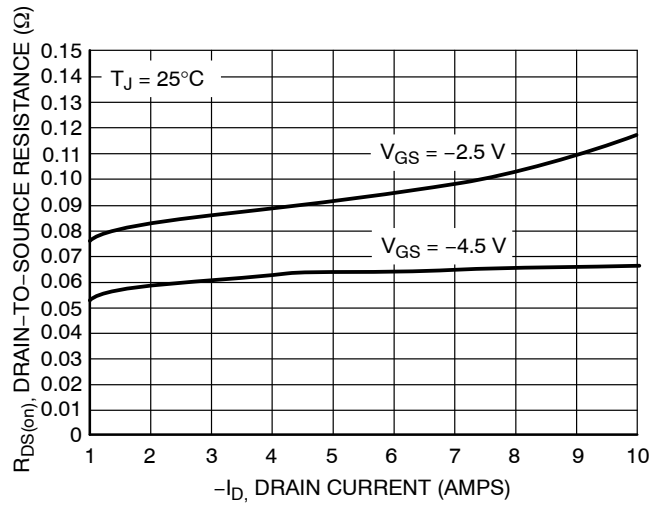


Figure 4. On-Resistance vs. Drain Current and Temperature

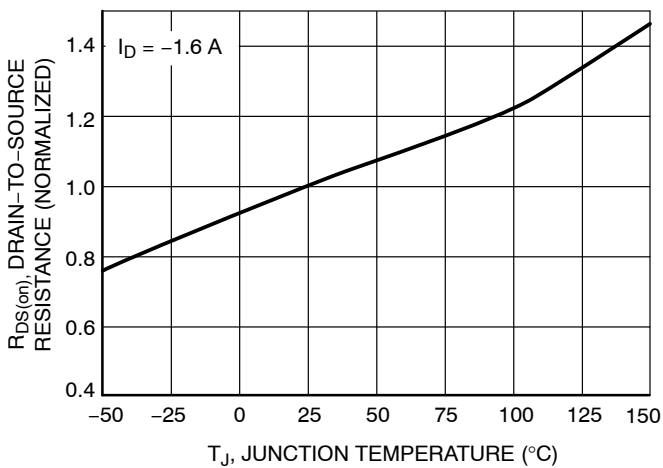


Figure 5. On-Resistance Variation with Temperature

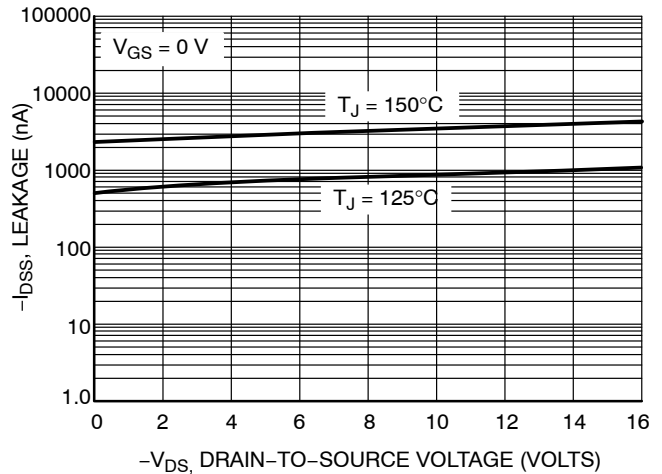


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTR4101P, NTRV4101P

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

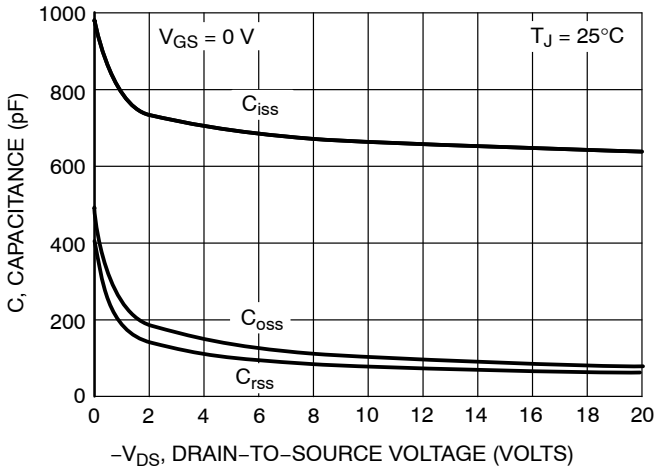


Figure 7. Capacitance Variation

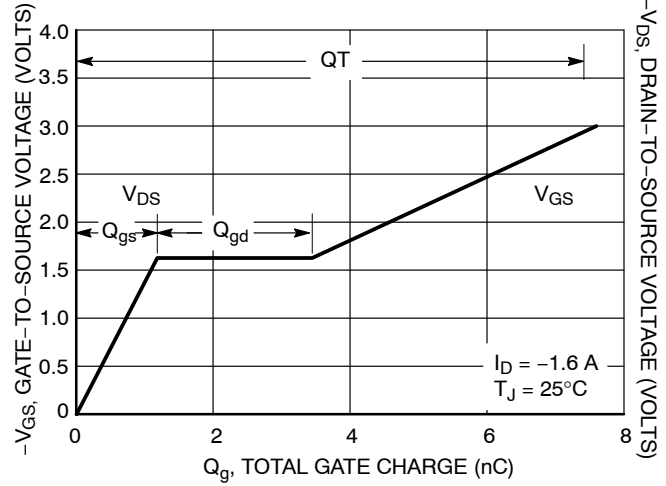


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

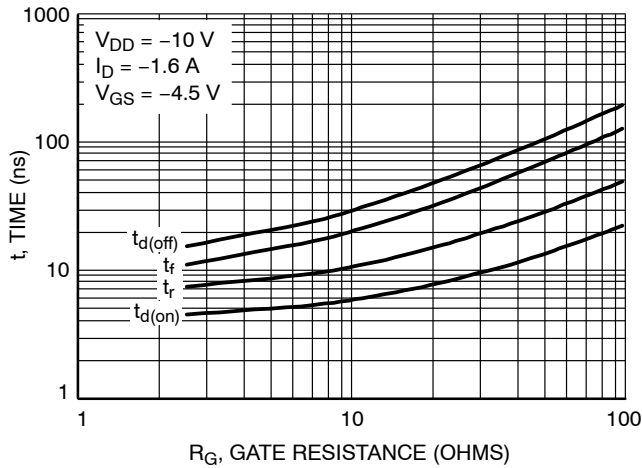


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

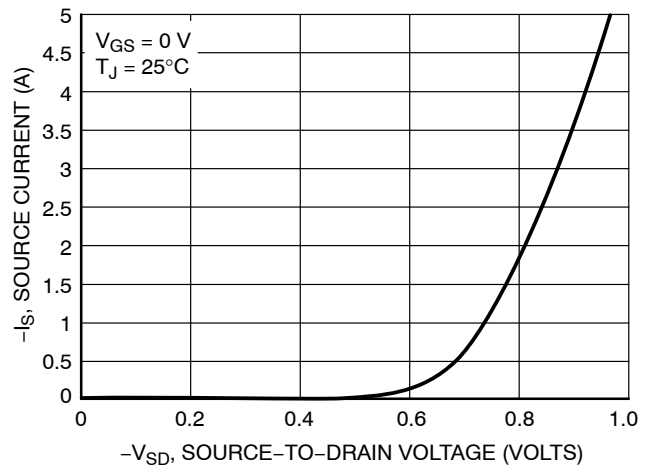


Figure 10. Diode Forward Voltage vs. Current

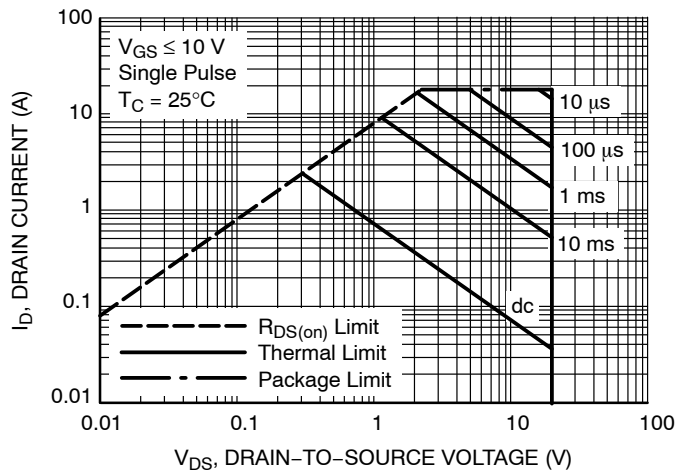
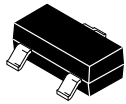


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

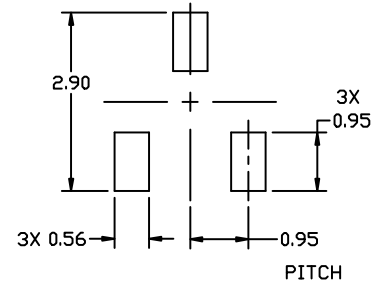
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



### SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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