ESP32 Series

Datasheet

Including:

ESP32-D0WD

ESP32-D0WDQ6

ESP32-D2WD

ESP32-S0WD



About This Guide

This document provides the specifications of ESP32 family of chips.

Revision History

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1. Overview

ESP32 is a single 2.4 GHz Wi-Fi-and-Bluetooth combo chip designed with the TSMC ultra-low-power 40 nm technology. It is designed to achieve the best power and RF performance, showing robustness, versatility and reliability in a wide variety of applications and power scenarios.

The ESP32 series of chips includes ESP32-D0WDQ6, ESP32-D0WD, ESP32-D2WD, and ESP32-S0WD. For details on part numbers and ordering information, please refer to Part Number and Ordering Information.

1.1 Featured Solutions

1.1.1 Ultra-Low-Power Solution

ESP32 is designed for mobile, wearable electronics, and Internet-of-Things (IoT) applications. It features all the state-of-the-art characteristics of low-power chips, including fine-grained clock gating, multiple power modes, and dynamic power scaling. For instance, in a low-power IoT sensor hub application scenario, ESP32 is woken up periodically and only when a specified condition is detected. Low-duty cycle is used to minimize the amount of energy that the chip expends. The output of the power amplifier is also adjustable, thus contributing to an optimal trade-off between communication range, data rate and power consumption.

Note:

For more information, refer to Section 3.7 RTC and Low-Power Management.

1.1.2 Complete Integration Solution

ESP32 is a highly-integrated solution for Wi-Fi-and-Bluetooth IoT applications, with around 20 external components. ESP32 integrates an antenna switch, RF balun, power amplifier, low-noise receive amplifier, filters, and power management modules. As such, the entire solution occupies minimal Printed Circuit Board (PCB) area.

ESP32 uses CMOS for single-chip fully-integrated radio and baseband, while also integrating advanced calibration circuitries that allow the solution to remove external circuit imperfections or adjust to changes in external conditions. As such, the mass production of ESP32 solutions does not require expensive and specialized Wi-Fi testing equipment.

1.2 Wi-Fi Key Features

- 802.11 b/g/n
- 802.11 n (2.4 GHz), up to 150 Mbps
- WMM
- TX/RX A-MPDU, RX A-MSDU
- Immediate Block ACK
- Defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces

- Simultaneous support for Infrastructure Station, SoftAP, and Promiscuous modes
 Note that when ESP32 is in Station mode, performing a scan, the SoftAP channel will be changed.
- · Antenna diversity

Note:

For more information, please refer to Section 3.5 Wi-Fi.

1.3 BT Key Features

- Compliant with Bluetooth v4.2 BR/EDR and BLE specifications
- Class-1, class-2 and class-3 transmitter without external power amplifier
- Enhanced Power Control
- +12 dBm transmitting power
- NZIF receiver with -97 dBm BLE sensitivity
- Adaptive Frequency Hopping (AFH)
- Standard HCI based on SDIO/SPI/UART
- High-speed UART HCI, up to 4 Mbps
- Bluetooth 4.2 BR/EDR BLE dual mode controller
- Synchronous Connection-Oriented/Extended (SCO/eSCO)
- CVSD and SBC for audio codec
- Bluetooth Piconet and Scatternet
- Multi-connections in Classic BT and BLE
- Simultaneous advertising and scanning

1.4 MCU and Advanced Features

1.4.1 CPU and Memory

- Xtensa[®] single-/dual-core 32-bit LX6 microprocessor(s), up to 600 MIPS (200 MIPS for ESP32-S0WD, 400 MIPS for ESP32-D2WD)
- 448 KB ROM
- 520 KB SRAM
- 16 KB SRAM in RTC
- QSPI supports multiple flash/SRAM chips

1.4.2 Clocks and Timers

- Internal 8 MHz oscillator with calibration
- Internal RC oscillator with calibration
- External 2 MHz ~ 60 MHz crystal oscillator (40 MHz only for Wi-Fi/BT functionality)
- External 32 kHz crystal oscillator for RTC with calibration
- Two timer groups, including 2×64 -bit timers and $1 \times main$ watchdog in each group
- One RTC timer
- RTC watchdog

1.4.3 Advanced Peripheral Interfaces

- 34 × programmable GPIOs
- 12-bit SAR ADC up to 18 channels
- 2 × 8-bit DAC
- 10 × touch sensors
- 4 × SPI
- 2 × I²S
- 2 × I²C
- 3 × UART
- 1 host (SD/eMMC/SDIO)
- 1 slave (SDIO/SPI)
- Ethernet MAC interface with dedicated DMA and IEEE 1588 support
- CAN 2.0
- IR (TX/RX)
- Motor PWM
- LED PWM up to 16 channels
- Hall sensor

1.4.4 Security

- Secure boot
- Flash encryption
- 1024-bit OTP, up to 768-bit for customers
- Cryptographic hardware acceleration:
 - AES
 - Hash (SHA-2)
 - RSA
 - ECC

- Random Number Generator (RNG)

1.5 Applications (A Non-exhaustive List)

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
 - Light control
 - Smart plugs
 - Smart door locks
- Smart Building
 - Smart lighting
 - Energy monitoring
- Industrial Automation
 - Industrial wireless control
 - Industrial robotics
- Smart Agriculture
 - Smart greenhouses
 - Smart irrigation

- Agriculture robotics
- Audio Applications
 - Internet music players
 - Live streaming devices
 - Internet radio players
 - Audio headsets
- Health Care Applications
 - Health monitoring
 - Baby monitors
- Wi-Fi-enabled Toys
 - Remote control toys
 - Proximity sensing toys
 - Educational toys
- Wearable Electronics
 - Smart watches
 - Smart bracelets
- Retail & Catering Applications
 - POS machines
 - Service robots

1.6 Block Diagram

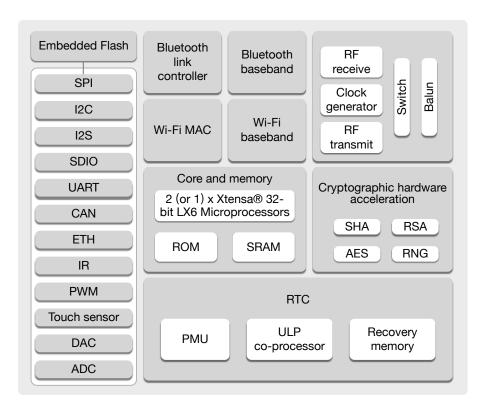


Figure 1: Functional Block Diagram

Note:

Products in the ESP32 series differ from each other in terms of their support for embedded flash and the number of CPUs they have. For details, please refer to Part Number and Ordering Information.

2. Pin Definitions

2.1 Pin Layout

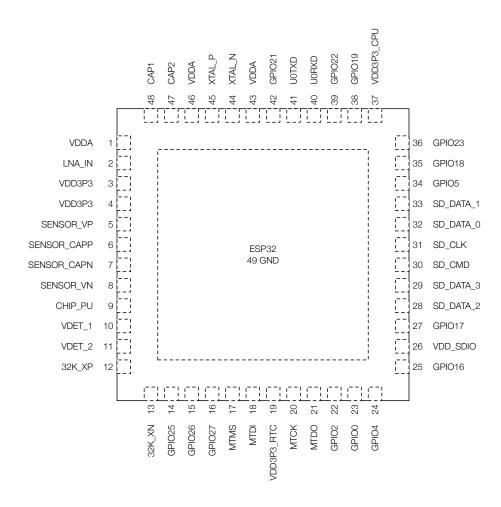


Figure 2: ESP32 Pin Layout (QFN 6*6, Top View)

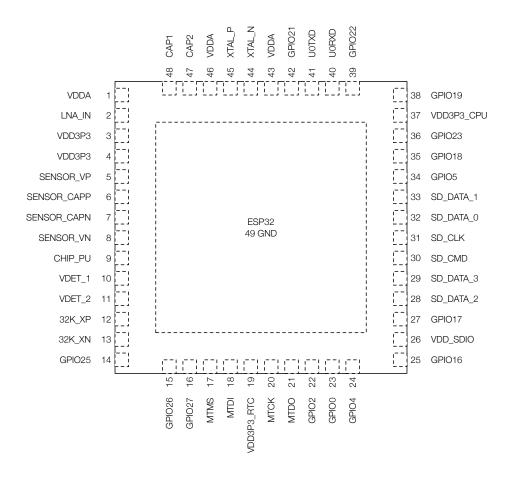


Figure 3: ESP32 Pin Layout (QFN 5*5, Top View)

Note:

For details on ESP32's part numbers and the corresponding packaging, please refer to Part Number and Ordering Information.

2.2 Pin Description

Table 1: Pin Description

Name	No.	Туре	Function					
	Analog							
VDDA	1	Р	Analog power supply (2.3 V – 3.6 V)					
LNA_IN	2	I/O	RF input and output					
VDD3P3	3	Р	Analog power supply (2.3 V – 3.6 V)					
VDD3P3	4	Р	Analog power supply (2.3 V – 3.6 V)					
			VDD3P3_RTC					
SENSOR_VP	5	I	GPIO36, ADC1_CH0, RTC_GPIO0					
SENSOR_CAPP	6	I	GPIO37, ADC1_CH1, RTC_GPIO1					
SENSOR_CAPN	7	I	GPIO38, ADC1_CH2, RTC_GPIO2					
SENSOR_VN	8	I	GPIO39, ADC1_CH3, RTC_GPIO3					
	High: On; enables the chip							
CHIP_PU	CHIP_PU 9 I Low: Off; the chip powers off							
			Note: Do not leave the CHIP_PU pin floating.					

Name	No.	Туре	Function								
VDET_1	10	ı	GPIO34,	ADC1_CH6,	RTC_GPIO4						
VDET_2	11	ı	GPIO35, A	ADC1_CH7,	RTC_GPIO5						
32K_XP	12	1/0	GPIO32, A	ADC1_CH4,	RTC_GPIO9,	TOUCH9,	32K_XP (32.768	3 kHz crystal	oscillator inpu	t)	
32K_XN	13	1/0	GPIO33, A	ADC1_CH5,	RTC_GPIO8,	TOUCH8,	32K_XN (32.768	3 kHz crystal	oscillator outp	out)	
GPIO25	14	I/O	GPI025, /	ADC2_CH8,	RTC_GPIO6,	DAC_1,	EMAC_RXD0				
GPIO26	15	I/O	GPI026, /	ADC2_CH9,	RTC_GPIO7,	DAC_2,	EMAC_RXD1				
GPIO27	16	1/0	GPIO27,	ADC2_CH7,	RTC_GPIO17,	TOUCH7,	EMAC_RX_DV				
MTMS	17	1/0	GPIO14, /	ADC2_CH6,	RTC_GPIO16,	TOUCH6,	EMAC_TXD2,	HSPICLK,	HS2_CLK,	SD_CLK,	MTMS
MTDI	18	I/O	GPIO12,	ADC2_CH5,	RTC_GPIO15,	TOUCH5,	EMAC_TXD3,	HSPIQ,	HS2_DATA2,	SD_DATA2,	MTDI
VDD3P3_RTC	19	Р	Input powe	er supply for R	TC IO (2.3 V – 3.	.6 V)					
MTCK	20	I/O	GPIO13,	ADC2_CH4,	RTC_GPIO14,	TOUCH4,	EMAC_RX_ER,	HSPID,	HS2_DATA3,	SD_DATA3,	MTCK
MTDO	21	1/0	GPIO15, /	ADC2_CH3,	RTC_GPIO13,	TOUCH3,	EMAC_RXD3,	HSPICS0,	HS2_CMD,	SD_CMD,	MTDO
GPIO2	22	1/0	GPIO2,	ADC2_CH2,	RTC_GPIO12,	TOUCH2,		HSPIWP,	HS2_DATA0,	SD_DATA0	
GPIO0	23	1/0	GPIO0,	ADC2_CH1,	RTC_GPIO11,	TOUCH1,	EMAC_TX_CLK	, CLK_OUT1	,		
GPIO4	24	I/O	GPIO4,	ADC2_CH0,	RTC_GPIO10,	TOUCH0,	EMAC_TX_ER,	HSPIHD,	HS2_DATA1,	SD_DATA1	
					VDD	_SDIO					
GPIO16	25	I/O	GPIO16, I	HS1_DATA4,	U2RXD,	EMAC_CLK	_OUT				
VDD_SDIO	26	Р	Output po	wer supply: 1.8	3 V or the same	voltage as V	DD3P3_RTC				
GPIO17	27	I/O	GPIO17, I	HS1_DATA5,	U2TXD,	EMAC_CLK	_OUT_180				
SD_DATA_2	28	I/O	GPIO9, I	HS1_DATA2,	U1RXD,	SD_DATA2,	SPIHD				
SD_DATA_3	29	I/O	GPIO10, I	HS1_DATA3,	U1TXD,	SD_DATA3,	SPIWP				
SD_CMD	30	I/O	GPIO11, I	HS1_CMD,	U1RTS,	SD_CMD,	SPICS0				
SD_CLK	31	I/O	GPIO6, I	HS1_CLK,	U1CTS,	SD_CLK,	SPICLK				
SD_DATA_0	32	I/O	GPIO7, I	HS1_DATA0,	U2RTS,	SD_DATA0,	SPIQ				
SD_DATA_1	33	I/O	GPIO8, I	HS1_DATA1,	U2CTS,	SD_DATA1,	SPID				
					VDD3I	P3_CPU					
GPIO5	34	I/O	GPIO5, I	HS1_DATA6,	VSPICS0,	EMAC_RX_	CLK				
GPIO18	35	I/O	GPIO18, I	HS1_DATA7,	VSPICLK						
GPIO23	36	I/O	GPIO23, I	HS1_STROBE,	VSPID						
VDD3P3_CPU	37	Р	Input powe	er supply for Cl	PU IO (1.8 V – 3	.6 V)					
GPIO19	38	I/O	GPIO19, I	U0CTS,	VSPIQ,	EMAC_TXD	0				
GPIO22	39	I/O	GPIO22, I	U0RTS,	VSPIWP,	EMAC_TXD	1				
U0RXD	40	I/O		U0RXD,	CLK_OUT2						
U0TXD	41	I/O	GPIO1, I	U0TXD,	CLK_OUT3,	EMAC_RXD)2				
GPIO21	42	I/O	GPIO21,		VSPIHD,	EMAC_TX_	EN				
						alog					
VDDA	43	Р		wer supply (2.3	3 V – 3.6 V)						
XTAL_N	44	0		ystal output							
XTAL_P	45	I	External cr	<u> </u>							
VDDA	46	Р		wer supply (2.3							
CAP2	47	I	Connects	to a 3 nF capa	citor and 20 k Ω	resistor in pa	rallel to CAP1				
CAP1	48	I		to a 10 nF serie	es capacitor to g	ground					
GND	49	Р	Ground								

Note:

- The pin-pin mapping between ESP32-D2WD and the embedded flash is as follows: GPIO16 = CS#, GPIO17 = IO1/DO, SD_CMD = IO3/HOLD#, SD_CLK = CLK, SD_DATA_0 = IO2/WP#, SD_DATA_1 = IO0/DI. The pins used for embedded flash are not recommended for other uses.
- In most cases, the data port connection between ESP32 series of chips other than ESP32-D2WD and external flash is as follows: SD_DATA0/SPIQ = IO1/DO, SD_DATA1/SPID = IO0/DI, SD_DATA2/SPIHD = IO3/HOLD#, SD_DATA3/SPIWP = IO2/WP#.
- For a quick reference guide to using the IO_MUX, Ethernet MAC, and GIPO Matrix pins of ESP32, please refer to Appendix ESP32 Pin Lists.

2.3 Power Scheme

ESP32's digital pins are divided into three different power domains:

- VDD3P3_RTC
- VDD3P3_CPU
- VDD_SDIO

VDD3P3_RTC is also the input power supply for RTC and CPU.

VDD3P3_CPU is also the input power supply for CPU.

VDD_SDIO connects to the output of an internal LDO whose input is VDD3P3_RTC. When VDD_SDIO is connected to the same PCB net together with VDD3P3_RTC, the internal LDO is disabled automatically. The power scheme diagram is shown below:

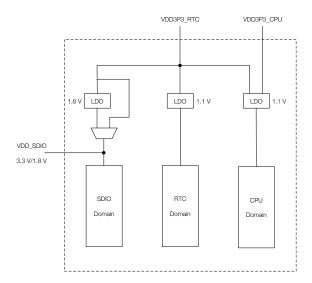


Figure 4: ESP32 Power Scheme

The internal LDO can be configured as having 1.8 V, or the same voltage as VDD3P3_RTC. It can be powered off via software to minimize the current of flash/SRAM during the Deep-sleep mode.

Notes on CHIP_PU:

• The illustration below shows the ESP32 power-up and reset timing. Details about the parameters are listed in Table 2.

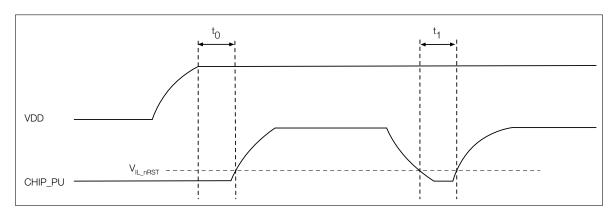


Figure 5: ESP32 Power-up and Reset Timing

Table 2: Description of ESP32 Power-up and Reset Timing Parameters

Parameters	Description	Min.	Unit
+.	Time between the 3.3 V rails being brought up and CHIP_PU being	50	μS
t ₀	activated	30	μ S
+	Duration of CHIP_PU signal level $<$ V_{IL_nRST} (refer to its value in	50	0
L1	Table 13 DC Characteristics) to reset the chip	50	μ S

- In scenarios where ESP32 is powered on and off repeatedly by switching the power rails, while there is a
 large capacitor on the VDD33 rail and CHIP_PU and VDD33 are connected, simply switching off the CHIP_PU
 power rail and immediately switching it back on may cause an incomplete power discharge cycle and failure
 to reset the chip adequately.
 - An additional discharge circuit may be required to accelerate the discharge of the large capacitor on rail VDD33, which will ensure proper power-on-reset when the ESP32 is powered up again. Please find the discharge circuit in Figure ESP32-WROOM-32 Peripheral Schematics, in <u>ESP32-WROOM-32 Datasheet</u>.
- When a battery is used as the power supply for the ESP32 series of chips and modules, a supply voltage supervisor is recommended, so that a boot failure due to low voltage is avoided. Users are recommended to pull CHIP_PU low if the power supply for ESP32 is below 2.3 V. For the reset circuit, please refer to Figure ESP32-WROOM-32 Peripheral Schematics, in ESP32-WROOM-32 Datasheet.

Notes on power supply:

- The operating voltage of ESP32 ranges from 2.3 V to 3.6 V. When using a single-power supply, the recommended voltage of the power supply is 3.3 V, and its recommended output current is 500 mA or more.
- When VDD_SDIO 1.8 V is used as the power supply for external flash/PSRAM, a 2-kohm grounding resistor should be added to VDD_SDIO. For the circuit design, please refer to Figure ESP32-WROVER Schematics, in ESP32-WROVER Datasheet.
- When the three digital power supplies are used to drive peripherals, e.g., 3.3 V flash, they should comply with the peripherals' specifications.

2.4 Strapping Pins

ESP32 has five strapping pins:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPI05

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration by strapping pins.

Table 3: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)									
Pin	Default	3.3	3 V	1.8 V					
MTDI	Pull-down	()	-	1				
			Booting Mode						
Pin	Default	SPL	Boot	Downlo	ad Boot				
GPI00	Pull-up	-	1	()				
GPIO2	Pull-down	Don't	-care	()				
		Enabling/Disabling D	Debugging Log Print over	U0TXD During Booting					
Pin	Default	U0TXD	Toggling	U0TXD Silent					
MTDO	Pull-up	-	1	0					
			Timing of SDIO Slave						
Pin	Default	Falling-edge Sampling	Falling-edge Sampling	Rising-edge Sampling	Rising-edge Sampling				
FIII	Delault	Falling-edge Output	Rising-edge Output	Falling-edge Output	Rising-edge Output				
MTDO	Pull-up	0 0		1	1				
GPIO5	Pull-up	0	1	0	1				

Note:

- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave", after booting.
- For ESP32 chips that contain an embedded flash, users need to note the logic level of MTDI. For example, ESP32-D2WD contains an embedded flash that operates at 1.8 V, therefore, the MTDI should be pulled high.

The illustration below shows the setup and hold times for the strapping pin before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 4.

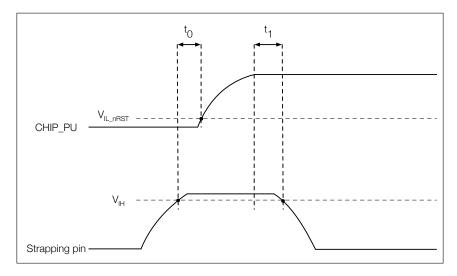


Figure 6: Setup and Hold Times for the Strapping Pin

Table 4: Parameter Descriptions of Setup and Hold Times for the Strapping Pin

Parameters	Description	Min.	Unit
t_0	Setup time before CHIP_PU goes from low to high	0	ms
t_1	Hold time after CHIP_PU goes high	1	ms

3. Functional Description

This chapter describes the functions integrated in ESP32.

3.1 CPU and Memory

3.1.1 CPU

ESP32 contains one or two low-power Xtensa® 32-bit LX6 microprocessor(s) with the following features:

- 7-stage pipeline to support the clock frequency of up to 240 MHz (160 MHz for ESP32-S0WD and ESP32-D2WD)
- 16/24-bit Instruction Set provides high code-density
- Support for Floating Point Unit
- Support for DSP instructions, such as a 32-bit multiplier, a 32-bit divider, and a 40-bit MAC
- Support for 32 interrupt vectors from about 70 interrupt sources

The single-/dual-CPU interfaces include:

- Xtensa RAM/ROM Interface for instructions and data
- Xtensa Local Memory Interface for fast peripheral register access
- External and internal interrupt sources
- JTAG for debugging

3.1.2 Internal Memory

ESP32's internal memory includes:

- 448 KB of ROM for booting and core functions
- 520 KB of on-chip SRAM for data and instructions
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.
- Embedded flash

Note:

- Products in the ESP32 series differ from each other, in terms of their support for embedded flash and the size of it.
 For details, please refer to Part Number and Ordering Information.
- ESP32-D2WD has a 16-Mbit, 40-MHz embedded flash, connected via pins GPIO16, GPIO17, SD_CMD, SD_CLK, SD_DATA_0 and SD_DATA_1.

3.1.3 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the <u>ESP32 Technical Reference Manual</u>. ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- Up to 16 MB of external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
 - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
 - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. SRAM up to 8 MB is supported and up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

Note:

After ESP32 is initialized, firmware can customize the mapping of external SRAM or flash into the CPU address space.

3.1.4 Memory Map

The structure of address mapping is shown in Figure 7. The memory and peripheral mapping of ESP32 is shown in Table 5.

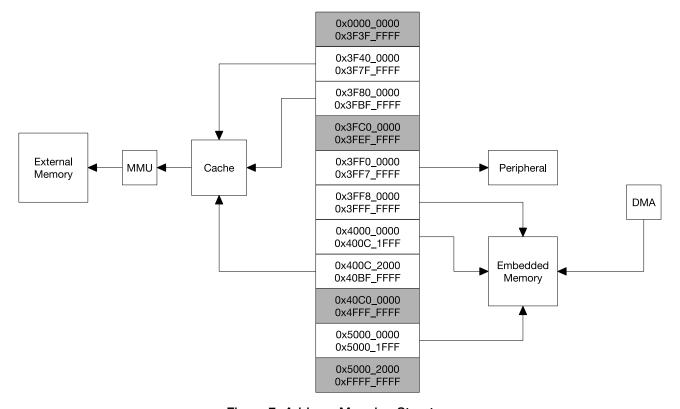


Figure 7: Address Mapping Structure

Table 5: Memory and Peripheral Mapping

Category	Target	Start Address	End Address	Size	
	Internal ROM 0	0x4000_0000	0x4005_FFFF	384 KB	
	Internal ROM 1	0x3FF9_0000	0x3FF9_FFFF	64 KB	
	Internal SRAM 0	0x4007_0000	0x4009_FFFF	192 KB	
Embedded	Internal SRAM 1	0x3FFE_0000	0x3FFF_FFFF	128 KB	
Memory	Internal Shalvi I	0x400A_0000	0x400B_FFFF	120 ND	
Wierriery	Internal SRAM 2	0x3FFA_E000	0x3FFD_FFFF	200 KB	
	DTC EAST Momon/	0x3FF8_0000	0x3FF8_1FFF	- 8 KB	
	RTC FAST Memory	0x400C_0000	0x400C_1FFF		
	RTC SLOW Memory	0x5000_0000	0x5000_1FFF	8 KB	
External	External Flash	0x3F40_0000	0x3F7F_FFFF	4 MB	
Memory	External riasii	0x400C_2000	0x40BF_FFFF	11 MB+248 KB	
Merriory	External SRAM	0x3F80_0000	0x3FBF_FFFF	4 MB	
	DPort Register	0x3FF0_0000	0x3FF0_0FFF	4 KB	
	AES Accelerator	0x3FF0_1000	0x3FF0_1FFF	4 KB	
	RSA Accelerator	0x3FF0_2000	0x3FF0_2FFF	4 KB	
	SHA Accelerator	0x3FF0_3000	0x3FF0_3FFF	4 KB	
	Secure Boot	0x3FF0_4000	0x3FF0_4FFF	4 KB	
	Cache MMU Table	0x3FF1_0000	0x3FF1_3FFF	16 KB	
	PID Controller	0x3FF1_F000	0x3FF1_FFFF	4 KB	
	UARTO	0x3FF4_0000	0x3FF4_0FFF	4 KB	
	SPI1	0x3FF4_2000	0x3FF4_2FFF	4 KB	
	SPI0	0x3FF4_3000	0x3FF4_3FFF	4 KB	
	GPIO	0x3FF4_4000	0x3FF4_4FFF	4 KB	
	RTC	0x3FF4_8000	0x3FF4_8FFF	4 KB	
	IO MUX	0x3FF4_9000	0x3FF4_9FFF	4 KB	
Peripheral	SDIO Slave	0x3FF4_B000	0x3FF4_BFFF	4 KB	
i eriprierai	UDMA1	0x3FF4_C000	0x3FF4_CFFF	4 KB	
	1280	0x3FF4_F000	0x3FF4_FFFF	4 KB	
	UART1	0x3FF5_0000	0x3FF5_0FFF	4 KB	
	I2C0	0x3FF5_3000	0x3FF5_3FFF	4 KB	
	UDMA0	0x3FF5_4000	0x3FF5_4FFF	4 KB	
	SDIO Slave	0x3FF5_5000	0x3FF5_5FFF	4 KB	
	RMT	0x3FF5_6000	0x3FF5_6FFF	4 KB	
	PCNT	0x3FF5_7000	0x3FF5_7FFF	4 KB	
	SDIO Slave	0x3FF5_8000	0x3FF5_8FFF	4 KB	
	LED PWM	0x3FF5_9000	0x3FF5_9FFF	4 KB	
	Efuse Controller	0x3FF5_A000	0x3FF5_AFFF	4 KB	
	Flash Encryption	0x3FF5_B000	0x3FF5_BFFF	4 KB	
	PWM0	0x3FF5_E000	0x3FF5_EFFF	4 KB	
	TIMG0	0x3FF5_F000	0x3FF5_FFFF	4 KB	
	TIMG1	0x3FF6_0000	0x3FF6_0FFF	4 KB	
	SPI2	0x3FF6_4000	0x3FF6_4FFF	4 KB	

Category	Target	Start Address	End Address	Size
	SPI3	0x3FF6_5000	0x3FF6_5FFF	4 KB
	SYSCON	0x3FF6_6000	0x3FF6_6FFF	4 KB
	I2C1	0x3FF6_7000	0x3FF6_7FFF	4 KB
	SDMMC	0x3FF6_8000	0x3FF6_8FFF	4 KB
	EMAC	0x3FF6_9000	0x3FF6_AFFF	8 KB
	PWM1	0x3FF6_C000	0x3FF6_CFFF	4 KB
	I2S1	0x3FF6_D000	0x3FF6_DFFF	4 KB
	UART2	0x3FF6_E000	0x3FF6_EFFF	4 KB
	PWM2	0x3FF6_F000	0x3FF6_FFFF	4 KB
	PWM3	0x3FF7_0000	0x3FF7_0FFF	4 KB
	RNG	0x3FF7_5000	0x3FF7_5FFF	4 KB

3.2 Timers and Watchdogs

3.2.1 64-bit Timers

There are four general-purpose timers embedded in the ESP32. They are all 64-bit generic timers which are based on 16-bit prescalers and 64-bit auto-reload-capable up/down-timers.

The timers feature:

- A 16-bit clock prescaler, from 2 to 65536
- A 64-bit timer
- Configurable up/down timer: incrementing or decrementing
- Halt and resume of time-base counter
- Auto-reload at alarming
- Software-controlled instant reload
- Level and edge interrupt generation

3.2.2 Watchdog Timers

The ESP32 has three watchdog timers: one in each of the two timer modules (called the Main Watchdog Timer, or MWDT) and one in the RTC module (called the RTC Watchdog Timer, or RWDT). These watchdog timers are intended to recover from an unforeseen fault causing the application program to abandon its normal sequence. A watchdog timer has four stages. Each stage may trigger one of three or four possible actions upon the expiry of its programmed time period, unless the watchdog is fed or disabled. The actions are: interrupt, CPU reset, core reset, and system reset. Only the RWDT can trigger the system reset, and is able to reset the entire chip, including the RTC itself. A timeout value can be set for each stage individually.

During flash boot the RWDT and the first MWDT start automatically in order to detect, and recover from, booting problems.

The ESP32 watchdogs have the following features:

- Four stages, each of which can be configured or disabled separately
- A programmable time period for each stage

- One of three or four possible actions (interrupt, CPU reset, core reset, and system reset) upon the expiry of each stage
- 32-bit expiry counter
- Write protection that prevents the RWDT and MWDT configuration from being inadvertently altered
- SPI flash boot protection
 If the boot process from an SPI flash does not complete within a predetermined time period, the watchdog will reboot the entire system.

3.3 System Clocks

3.3.1 CPU Clock

Upon reset, an external crystal clock source is selected as the default CPU clock. The external crystal clock source also connects to a PLL to generate a high-frequency clock (typically 160 MHz).

In addition, ESP32 has an internal 8 MHz oscillator. The application can select the clock source from the external crystal clock source, the PLL clock or the internal 8 MHz oscillator. The selected clock source drives the CPU clock directly, or after division, depending on the application.

3.3.2 RTC Clock

The RTC clock has five possible sources:

- external low-speed (32 kHz) crystal clock
- external crystal clock divided by 4
- internal RC oscillator (typically about 150 kHz, and adjustable)
- internal 8 MHz oscillator
- internal 31.25 kHz clock (derived from the internal 8 MHz oscillator divided by 256)

When the chip is in the normal power mode and needs faster CPU accessing, the application can choose the external high-speed crystal clock divided by 4 or the internal 8 MHz oscillator. When the chip operates in the low-power mode, the application chooses the external low-speed (32 kHz) crystal clock, the internal RC clock or the internal 31.25 kHz clock.

3.3.3 Audio PLL Clock

The audio clock is generated by the ultra-low-noise fractional-N PLL. More details can be found in Chapter Reset and Clock in the *ESP32 Technical Reference Manual*.

3.4 Radio

The ESP32 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch

· clock generator

3.4.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits and baseband filters are integrated with ESP32.

3.4.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered Complementary Metal Oxide Semiconductor (CMOS) power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling state-of-the-art performance in delivering up to +20.5 dBm of power for an 802.11b transmission and +18 dBm for an 802.11n transmission.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- Carrier leakage
- I/Q phase matching
- Baseband nonlinearities
- RF nonlinearities
- · Antenna matching

These built-in calibration routines reduce the amount of time required for product testing, and render the testing equipment unnecessary.

3.4.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including all inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.5 Wi-Fi

ESP32 implements a TCP/IP and full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled with minimal host interaction to minimize the active-duty period.

3.5.1 Wi-Fi Radio and Baseband

The ESP32 Wi-Fi Radio and Baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 in both 20 MHz and 40 MHz bandwidth
- 802.11n MCS32 (RX)

- 802.11n 0.4 μs guard-interval
- up to 150 Mbps of data rate
- Receiving STBC 2×1
- Up to 20.5 dBm of transmitting power
- Adjustable transmitting power
- Antenna diversity

ESP32 supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and selects the best antenna to minimize the effects of channel fading.

3.5.2 Wi-Fi MAC

The ESP32 Wi-Fi MAC applies low-level protocol functions automatically. They are as follows:

- 4 × virtual Wi-Fi interfaces
- Simultaneous Infrastructure BSS Station mode/SoftAP mode/Promiscuous mode
- RTS protection, CTS protection, Immediate Block ACK
- Defragmentation
- TX/RX A-MPDU, RX A-MSDU
- TXOP
- WMM
- CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4) and CRC
- Automatic beacon monitoring (hardware TSF)

3.6 Bluetooth

ESP32 integrates a Bluetooth link controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

3.6.1 Bluetooth Radio and Baseband

The ESP32 Bluetooth Radio and Baseband support the following features:

- Class-1, class-2 and class-3 transmit output powers, and a dynamic control range of up to 24 dB
- $\pi/4$ DQPSK and 8 DPSK modulation
- High performance in NZIF receiver sensitivity with over 97 dB of dynamic range
- Class-1 operation without external PA
- Internal SRAM allows full-speed data-transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- ACL, SCO, eSCO and AFH
- A-law, μ -law and CVSD digital audio CODEC in PCM interface

- SBC audio CODEC
- Power management for low-power applications
- SMP with 128-bit AES

3.6.2 Bluetooth Interface

- Provides UART HCI interface, up to 4 Mbps
- Provides SDIO / SPI HCl interface
- Provides PCM / I2S audio interface

3.6.3 Bluetooth Stack

The Bluetooth stack of ESP32 is compliant with the Bluetooth v4.2 BR / EDR and BLE specifications.

3.6.4 Bluetooth Link Controller

The link controller operates in three major states: standby, connection and sniff. It enables multiple connections, and other operations, such as inquiry, page, and secure simple-pairing, and therefore enables Piconet and Scatternet. Below are the features:

- · Classic Bluetooth
 - Device Discovery (inquiry, and inquiry scan)
 - Connection establishment (page, and page scan)
 - Multi-connections
 - Asynchronous data reception and transmission
 - Synchronous links (SCO/eSCO)
 - Master/Slave Switch
 - Adaptive Frequency Hopping and Channel assessment
 - Broadcast encryption
 - Authentication and encryption
 - Secure Simple-Pairing
 - Multi-point and scatternet management
 - Sniff mode
 - Connectionless Slave Broadcast (transmitter and receiver)
 - Enhanced power control
 - Ping
- Bluetooth Low Energy
 - Advertising
 - Scanning
 - Simultaneous advertising and scanning
 - Multiple connections

- Asynchronous data reception and transmission
- Adaptive Frequency Hopping and Channel assessment
- Connection parameter update
- Data Length Extension
- Link Layer Encryption
- LE Ping

3.7 RTC and Low-Power Management

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

- Power modes
 - Active mode: The chip radio is powered on. The chip can receive, transmit, or listen.
 - Modem-sleep mode: The CPU is operational and the clock is configurable. The Wi-Fi/Bluetooth baseband and radio are disabled.
 - Light-sleep mode: The CPU is paused. The RTC memory and RTC peripherals, as well as the ULP co-processor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.
 - Deep-sleep mode: Only the RTC memory and RTC peripherals are powered on. Wi-Fi and Bluetooth connection data are stored in the RTC memory. The ULP co-processor is functional.
 - Hibernation mode: The internal 8-MHz oscillator and ULP co-processor are disabled. The RTC recovery
 memory is powered down. Only one RTC timer on the slow clock and certain RTC GPIOs are active.
 The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

Table 6: Power Consumption by Power Modes

Power mode	Description			Power consumption	
Active (RF working)	Wi-Fi Tx packet Wi-Fi/BT Tx packet			Please refer to Table 15 for details.	
	Wi-Fi/BT Rx and listening			lable to for detaile.	
Modem-sleep	The CPU is	240 MHz	Dual-core chip(s)	30 mA ~ 68 mA	
			Single-core chip(s)	N/A	
		160 MHz	Dual-core chip(s)	27 mA ~ 44 mA	
	powered on.		Single-core chip(s)	27 mA ~ 34 mA	
		Normal speed: 80 MHz	Dual-core chip(s)	20 mA ~ 31 mA	
			Single-core chip(s)	20 mA ~ 25 mA	
Light-sleep	-			0.8 mA	
	The ULP co-processor is powered on.			150 μΑ	
Deep-sleep	ULP sensor-monitored pattern			100 μA @1% duty	
	RTC timer + RTC memory			10 <i>μ</i> A	
Hibernation	RTC timer only			5 μΑ	
Power off	CHIP_PU is set to low level, the chip is powered off.			0.1 μΑ	

Note:

- * Among the ESP32 series of SoCs, ESP32-D0WDQ6 and ESP32-D0WD have a maximum CPU frequency of 240 MHz, ESP32-D2WD and ESP32-S0WD have a maximum CPU frequency of 160 MHz.
- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, power consumption changes accordingly.
- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I²C are able to operate.
- When the system works in the ULP sensor-monitored pattern, the ULP co-processor works with the ULP sensor periodically and the ADC works with a duty cycle of 1%, so the power consumption is 100 μ A.

4. Peripherals and Sensors

4.1 Descriptions of Peripherals and Sensors

4.1.1 General Purpose Input / Output Interface (GPIO)

ESP32 has 34 GPIO pins which can be assigned various functions by programming the appropriate registers. There are several kinds of GPIOs: digital-only, analog-enabled, capacitive-touch-enabled, etc. Analog-enabled GPIOs and Capacitive-touch-enabled GPIOs can be configured as digital GPIOs.

Most of the digital GPIOs can be configured as internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. Most of the digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the SDIO, UART, SPI, etc. (More details can be found in the Appendix, Table IO_MUX.) For low-power operations, the GPIOs can be set to hold their states.

4.1.2 Analog-to-Digital Converter (ADC)

ESP32 integrates 12-bit SAR ADCs and supports measurements on 18 channels (analog-enabled pins). The ULP-coprocessor in ESP32 is also designed to measure voltage, while operating in the sleep mode, which enables low-power consumption. The CPU can be woken up by a threshold setting and/or via other triggers.

With appropriate settings, the ADCs can be configured to measure voltage on 18 pins maximum.

Table 7 describes the ADC characteristics.

Table 7: ADC Characteristics

Parameter	Description	Min	Max	Unit
DNL (Differential nonlinearity)	RTC controller; ADC connected to an external 100 nF capacitor;		7	LSB
INL (Integral nonlinearity)	DC signal input; ambient temperature at 25 °C; Wi-Fi&BT off		12	LSB
Compling rate	RTC controller		200	ksps
Sampling rate	DIG controller	-	2	Msps

Notes:

- When atten=3 and the measurement result is above 3,000 (voltage at approx. 2,450 mV), the ADC accuracy will be worse than described in the table above.
- To get better DNL results, users can take multiple sampling tests with a filter, or calculate the average value.

By default, there are ±6% differences in measured results between chips. ESP-IDF provides couple of <u>calibration</u> <u>methods</u> for ADC1. Results after calibration using eFuse Vref value are shown in Table 8. For higher accuracy, users may apply other calibration methods provided in ESP-IDF, or implement their own.

Table 8: ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	Atten=0, effective measurement range of 100-950 mV	-23	23	mV
	Atten=1, effective measurement range of 100-1,250 mV	-30	30	mV
	Atten=2, effective measurement range of 150-1,750 mV	-40	40	mV
	Atten=3, effective measurement range of 150-2,450 mV	-60	60	mV

4.1.3 Hall Sensor

ESP32 integrates a Hall sensor based on an N-carrier resistor. When the chip is in the magnetic field, the Hall sensor develops a small voltage laterally on the resistor, which can be directly measured by the ADC.

4.1.4 Digital-to-Analog Converter (DAC)

Two 8-bit DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and a buffer. This dual DAC supports power supply as input voltage reference. The two DAC channels can also support independent conversions.

4.1.5 Touch Sensor

ESP32 has 10 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected. The 10 capacitive-sensing GPIOs are listed in Table 9.

Capacitive-sensing signal name Pin name TO GPIO4 T1 GPI00 T2 GPIO2 T3 MTDO T4 **MTCK** T5 MTDI T6 **MTMS** T7 **GPIO27** T8 32K_XN T9 32K XP

Table 9: Capacitive-Sensing GPIOs Available on ESP32

4.1.6 Ultra-Low-Power Co-processor

The ULP processor and RTC memory remain powered on during the Deep-sleep mode. Hence, the developer can store a program for the ULP processor in the RTC slow memory to access the peripheral devices, internal timers and internal sensors during the Deep-sleep mode. This is useful for designing applications where the CPU needs to be woken up by an external event, or a timer, or a combination of the two, while maintaining minimal power consumption.

4.1.7 Ethernet MAC Interface

An IEEE-802.3-2008-compliant Media Access Controller (MAC) is provided for Ethernet LAN communications. ESP32 requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to ESP32 through 17 signals of MII or nine signals of RMII. The following features are supported on the Ethernet MAC (EMAC) interface:

- 10 Mbps and 100 Mbps rates
- Dedicated DMA controller allowing high-speed transfer between the dedicated SRAM and Ethernet MAC

- Tagged MAC frame (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames)
- · 32-bit CRC generation and removal
- Several address-filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 512 words (32-bit)
- Hardware PTP (Precision Time Protocol) in accordance with IEEE 1588 2008 (PTP V2)
- 25 MHz/50 MHz clock output

4.1.8 SD/SDIO/MMC Host Controller

An SD/SDIO/MMC host controller is available on ESP32, which supports the following features:

- Secure Digital memory (SD mem Version 3.0 and Version 3.01)
- Secure Digital I/O (SDIO Version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA Version 1.1)
- Multimedia Cards (MMC Version 4.41, eMMC Version 4.5 and Version 4.51)

The controller allows up to 80 MHz of clock output in three different data-bus modes: 1-bit, 4-bit and 8-bit. It supports two SD/SDIO/MMC4.41 cards in a 4-bit data-bus mode. It also supports one SD card operating at 1.8V.

4.1.9 SDIO/SPI Slave Controller

ESP32 integrates an SD device interface that conforms to the industry-standard SDIO Card Specification Version 2.0, and allows a host controller to access the SoC, using the SDIO bus interface and protocol. ESP32 acts as the slave on the SDIO bus. The host can access the SDIO-interface registers directly and can access shared memory via a DMA engine, thus maximizing performance without engaging the processor cores.

The SDIO/SPI slave controller supports the following features:

- SPI, 1-bit SDIO, and 4-bit SDIO transfer modes over the full clock range from 0 to 50 MHz
- Configurable sampling and driving clock edge
- Special registers for direct access by host
- Interrupts to host for initiating data transfer
- Automatic loading of SDIO bus data and automatic discarding of padding data
- Block size of up to 512 bytes
- Interrupt vectors between the host and the slave, allowing both to interrupt each other
- Supports DMA for data transfer

4.1.10 Universal Asynchronous Receiver Transmitter (UART)

ESP32 has three UART interfaces, i.e., UART0, UART1 and UART2, which provide asynchronous communication (RS232 and RS485) and IrDA support, communicating at a speed of up to 5 Mbps. UART provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All of the interfaces can be accessed by the DMA controller or directly by the CPU.

4.1.11 I²C Interface

ESP32 has two I²C bus interfaces which can serve as I²C master or slave, depending on the user's configuration. The I²C interfaces support:

- Standard mode (100 Kbit/s)
- Fast mode (400 Kbit/s)
- Up to 5 MHz, yet constrained by SDA pull-up strength
- 7-bit/10-bit addressing mode
- Dual addressing mode

Users can program command registers to control I²C interfaces, so that they have more flexibility.

4.1.12 I²S Interface

Two standard I²S interfaces are available in ESP32. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with an 8-/16-/32-/48-/64-bit resolution as input or output channels. BCK clock frequency, from 10 kHz up to 40 MHz, is supported. When one or both of the I²S interfaces are configured in the master mode, the master clock can be output to the external DAC/CODEC.

Both of the I2S interfaces have dedicated DMA controllers. PDM and BT PCM interfaces are supported.

4.1.13 Infrared Remote Controller

The infrared remote controller supports eight channels of infrared remote transmission and receiving. By programming the pulse waveform, it supports various infrared protocols. Eight channels share a 512 x 32-bit block of memory to store the transmitting or receiving waveform.

4.1.14 Pulse Counter

The pulse counter captures pulse and counts pulse edges through seven modes. It has eight channels, each of which captures four signals at a time. The four input signals include two pulse signals and two control signals. When the counter reaches a defined threshold, an interrupt is generated.

4.1.15 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) controller can be used for driving digital motors and smart lights. The controller consists of PWM timers, the PWM operator and a dedicated capture sub-module. Each timer provides timing in synchronous or independent form, and each PWM operator generates a waveform for one PWM channel. The dedicated capture sub-module can accurately capture events with external timing.

4.1.16 LED PWM

The LED PWM controller can generate 16 independent channels of digital waveforms with configurable periods and duties.

The 16 channels of digital waveforms operate with an APB clock of 80 MHz. Eight of these channels have the option of using the 8 MHz oscillator clock. Each channel can select a 20-bit timer with configurable counting range, while its accuracy of duty can be up to 16 bits within a 1 ms period.

The software can change the duty immediately. Moreover, each channel automatically supports step-by-step duty increase or decrease, which is useful for the LED RGB color-gradient generator.

4.1.17 Serial Peripheral Interface (SPI)

ESP32 features three SPIs (SPI, HSPI and VSPI) in slave and master modes in 1-line full-duplex and 1/2/4-line half-duplex communication modes. These SPIs also support the following general-purpose SPI features:

- Four modes of SPI transfer format, which depend on the polarity (CPOL) and the phase (CPHA) of the SPI clock
- Up to 80 MHz (The actual speed it can reach depends on the selected pads, PCB tracing, peripheral characteristics, etc.)
- up to 64-byte FIFO

All SPIs can also be connected to the external flash/SRAM and LCD. Each SPI can be served by DMA controllers.

4.1.18 Accelerator

ESP32 is equipped with hardware accelerators of general algorithms, such as AES (FIPS PUB 197), SHA (FIPS PUB 180-4), RSA, and ECC, which support independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA, ECC, Big Integer Multiply and Big Integer Modular Multiplication is 4,096 bits.

The hardware accelerators greatly improve operation speed and reduce software complexity. They also support code encryption and dynamic decryption, which ensures that code in the flash will not be hacked.

4.2 Peripheral Pin Configurations

Table 10: Peripheral Pin Configurations

Interface	Signal	Pin	Function	
	ADC1_CH0	SENSOR_VP		
	ADC1_CH1	SENSOR_CAPP		
	ADC1_CH2	SENSOR_CAPN		
	ADC1_CH3	SENSOR_VN		
	ADC1_CH4	32K_XP		
	ADC1_CH5	32K_XN		
	ADC1_CH6	VDET_1		
	ADC1_CH7	VDET_2		
ADC	ADC2_CH0	GPIO4	Two 12-bit SAR ADCs	
	ADC2_CH1	GPIO0		
	ADC2_CH2	GPIO2		
	ADC2_CH3	MTDO		
	ADC2_CH4	MTCK		
	ADC2_CH5	MTDI		
	ADC2_CH6	MTMS		
	ADC2_CH7	GPIO27		
	ADC2_CH8	GPIO25		
	ADC2_CH9	GPIO26		
DAC	DAC_1	GPIO25	Two 8-bit DACs	
DAC	DAC_2	GPIO26	1WO 0-DIL DAGS	
	TOUCH0	GPIO4		
	TOUCH1	GPIO0		
	TOUCH2	GPIO2		
	TOUCH3	MTDO		
Touch Sensor	TOUCH4	MTCK	Capacitive touch sensors	
TOUCH Sensor	TOUCH5	MTDI	Capacitive teach contests	
	TOUCH6	MTMS		
	TOUCH7	GPIO27		
	TOUCH8	32K_XN		
	TOUCH9	32K_XP		
	MTDI	MTDI		
ITAG	MTCK	MTCK	JTAG for software debugging	
JTAG	MTMS	MTMS	TAG for software debugging	
	MTDO	MTDO		

Interface	Signal	Pin	Function	
	HS2_CLK	MTMS		
SD/SDIO/MMC Host Controller	HS2_CMD	MTDO		
	HS2_DATA0	GPIO2	Supports SD memory card V3.01 standard	
	HS2_DATA1	GPIO4	- Supports 3D memory card v3.01 standard	
	HS2_DATA2	MTDI		
	HS2_DATA3			
	PWM0_OUT0~2			
	PWM1_OUT_IN0~2		Three channels of 16-bit timers generate	
	PWM0_FLT_IN0~2		PWM waveforms. Each channel has a pair	
Motor PWM	PWM1_FLT_IN0~2	Any GPIO Pins	of output signals, three fault detection	
IVIOLOI I VVIVI	PWM0_CAP_IN0~2	Any di 10 mis	signals, three event-capture signals, and	
	PWM1_CAP_IN0~2		three sync signals.	
	PWM0_SYNC_IN0~2		tillee Syric Signais.	
	PWM1_SYNC_IN0~2			
	SD_CLK	MTMS		
	SD_CMD	MTDO	CDIO interfece that conforms to the	
SDIO/SPI Slave	SD_DATA0	GPIO2	SDIO interface that conforms to the	
Controller	SD_DATA1	GPIO4	industry standard SDIO 2.0 card specification	
	SD_DATA2	MTDI	Specification	
	SD_DATA3	MTCK		
	U0RXD_in			
	U0CTS_in			
	U0DSR_in			
	U0TXD_out			
	U0RTS_out			
	U0DTR_out			
UART	U1RXD_in	Any GPIO Pins	Two UART devices with hardware	
	U1CTS_in		flow-control and DMA	
	U1TXD_out			
	U1RTS_out			
	U2RXD_in			
	U2CTS_in			
	U2TXD_out			
	U2RTS_out			
I ² C	I2CEXT0_SCL_in			
	I2CEXT0_SDA_in			
	I2CEXT1_SCL_in			
	I2CEXT1_SDA_in	Any GPIO Pins	Two I ² C devices in slave or master mode	
	I2CEXT0_SCL_out	ANY ON TO FINS	TWO LO GEVICES III SIAVE OF ITIASTEL THOUE	
	I2CEXT0_SDA_out			
	I2CEXT1_SCL_out			
	I2CEXT1_SDA_out	1		

Interface	Signal	Pin	Function
	ledc_hs_sig_out0~7	Any CDIO Din-	16 independent channels @80 MHz
LED PWM	ledc_ls_sig_out0~7	Any GPIO Pins	clock/RTC CLK. Duty accuracy: 16 bits.
	I2S0I_DATA_in0~15		
	I2S0O_BCK_in		
	12S0O_WS_in		
	I2S0I_BCK_in		
	12S0I_WS_in		
	I2S0I_H_SYNC		
	I2S0I_V_SYNC		
	I2S0I_H_ENABLE		
	I2S0O_BCK_out		
	I2S0O_WS_out		
	I2S0I_BCK_out		
	I2S0I_WS_out		Stereo input and output from/to the audio
I2S	I2S0O_DATA_out0~23	Any GPIO Pins	codec; parallel LCD data output; parallel
	I2S1I_DATA_in0~15		camera data input
	I2S1O_BCK_in		
	I2S1O_WS_in		
	I2S1I_BCK_in		
	I2S1I_WS_in		
	I2S1I_H_SYNC		
	I2S1I_V_SYNC		
	I2S1I_H_ENABLE		
	I2S1O_BCK_out		
	I2S1O_WS_out		
	I2S1I_BCK_out		
	I2S1I_WS_out		
	I2S1O_DATA_out0~23		
Infrared Remote	RMT_SIG_IN0~7	Any GPIO Pins	Eight channels for an IR transmitter and
Controller	RMT_SIG_OUT0~7	Any di lo i lis	receiver of various waveforms
	HSPIQ_in/_out		Standard SPI consists of clock,
	HSPID_in/_out		chip-select, MOSI and MISO. These SPIs
	HSPICLK_in/_out		can be connected to LCD and other
	HSPI_CS0_in/_out		external devices. They support the
	HSPI_CS1_out		following features:
General Purpose	HSPI_CS2_out	Any GPIO Pins	Both master and slave modes;
SPI	VSPIQ_in/_out	, , ,	Four sub-modes of the SPI transfer
	VSPID_in/_out		format;
	VSPICLK_in/_out		Configurable SPI frequency;
	VSPI_CS0_in/_out		Up to 64 bytes of FIFO and DMA.
	VSPI_CS1_out		
	VSPI_CS2_out		

Interface	Signal	Pin	Function
	SPIHD	SD_DATA_2	
	SPIWP	SD_DATA_3	
	SPICS0	SD_CMD	
	SPICLK	SD_CLK	
	SPIQ	SD_DATA_0	
	SPID	SD_DATA_1	
	HSPICLK	MTMS	
	HSPICS0	MTDO	Supports Standard SPI, Dual SPI, and
Parallel QSPI HSPID MTCK Quad SPI that can be external flash and SF	Quad SPI that can be connected to the		
	HSPID	MTCK	external flash and SRAM
	HSPIHD	GPIO4	
	HSPIWP	GPIO2	
	VSPICLK	GPIO18	
	VSPICS0	GPIO5	
	VSPIQ	GPIO19	
	VSPID	GPIO23	
	VSPIHD	GPIO21	
	VSPIWP	GPIO22	
	EMAC_TX_CLK	GPIO0	
	EMAC_RX_CLK	GPIO5	
	EMAC_TX_EN	GPIO21	
	EMAC_TXD0	GPIO19	
	EMAC_TXD1	GPIO22	
	EMAC_TXD2	MTMS	
	EMAC_TXD3	MTDI	
	EMAC_RX_ER	MTCK	
	EMAC_RX_DV	GPIO27	
FNAAC	EMAC_RXD0	GPIO25	Ethania t NAA Oo with NAII/DNAII intarfara
EMAC	EMAC_RXD1	GPIO26	Ethernet MAC with MII/RMII interface
	EMAC_RXD2	U0TXD	
	EMAC_RXD3	MTDO	
	EMAC_CLK_OUT	GPIO16	
	EMAC_CLK_OUT_180	GPIO17	
	EMAC_TX_ER	GPIO4	
	EMAC_MDC_out	Any GPIO Pins	
	EMAC_MDI_in	Any GPIO Pins	
	EMAC_MDO_out	Any GPIO Pins	
	EMAC_CRS_out	Any GPIO Pins	
	EMAC_COL_out	Any GPIO Pins	

Interface	Signal	Pin	Function
	pcnt_sig_ch0_in0		
	pcnt_sig_ch1_in0		
	pcnt_ctrl_ch0_in0		
	pcnt_ctrl_ch1_in0		
	pcnt_sig_ch0_in1		
	pcnt_sig_ch1_in1		
	pcnt_ctrl_ch0_in1		
	pcnt_ctrl_ch1_in1		
	pcnt_sig_ch0_in2		
	pcnt_sig_ch1_in2		
	pcnt_ctrl_ch0_in2		
	pcnt_ctrl_ch1_in2		
	pcnt_sig_ch0_in3		
	pcnt_sig_ch1_in3		
	pcnt_ctrl_ch0_in3		Operating in seven different modes, the
Pulse Counter	pcnt_ctrl_ch1_in3	Any GPIO Pins	pulse counter captures pulse and counts
	pcnt_sig_ch0_in4		pulse edges.
	pcnt_sig_ch1_in4		
	pcnt_ctrl_ch0_in4		
	pcnt_ctrl_ch1_in4		
	pcnt_sig_ch0_in5		
	pcnt_sig_ch1_in5		
	pcnt_ctrl_ch0_in5		
	pcnt_ctrl_ch1_in5		
	pcnt_sig_ch0_in6		
	pcnt_sig_ch1_in6		
	pcnt_ctrl_ch0_in6		
	pcnt_ctrl_ch1_in6		
	pcnt_sig_ch0_in7		
	pcnt_sig_ch1_in7		
	pcnt_ctrl_ch0_in7		
	pcnt_ctrl_ch1_in7		

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Table 11: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO	Voltage applied to power supply pins per power domain	-0.3	3.6	V
l _{output} *	Cumulative IO output current	-	1,200	mA
T_{store}	Storage temperature	-40	150	°C

^{*} The chip worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground.

5.2 Recommended Operating Conditions

Table 12: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDDA, VDD3P3_RTC ¹	Voltage applied to power supply pins per	2.3	3.3	3.6	\/
VDD3P3, VDD_SDIO (3.3 V mode) ²	power domain	2.3	3.3	3.0	V
VDD3P3_CPU	Voltage applied to power supply pin	1.8	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	А
T 3	Operating temperature	-40	-	125	°C

- 1. When writing eFuse, VDD3P3_RTC should be at least 3.3 V.
- VDD_SDIO works as the power supply for the related IO, and also for an external device. Please refer to the Appendix IO_MUX of this datasheet for more details.
 - VDD_SDIO can be sourced internally by the ESP32 from the VDD3P3_RTC power domain:
 - When VDD_SDIO operates at 3.3 V, it is driven directly by VDD3P3_RTC through a 6 Ω resistor, therefore, there will be some voltage drop from VDD3P3_RTC.
 - When VDD_SDIO operates at 1.8 V, it can be generated from ESP32's internal LDO. The maximum current this LDO can offer is 40 mA, and the output voltage range is 1.65 V ~ 2.0 V.
 - VDD_SDIO can also be driven by an external power supply.
 - Please refer to Power Scheme, section 2.3, for more information.
- 3. The operating temperature of ESP32-D2WD ranges from $-40~^{\circ}\text{C} \sim 105~^{\circ}\text{C}$, due to the flash embedded in it. The other chips in this series have no ebedded flash, so their range of operating temperatures is $-40~^{\circ}\text{C} \sim 125~^{\circ}\text{C}$.

5.3 DC Characteristics (3.3 V, 25 °C)

Table 13: DC Characteristics (3.3 V, 25 °C)

Symbol	Par	ameter	Min	Тур	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		0.75×VDD ¹	-	VDD1+0.3	V
V_{IL}	Low-level input voltage		-0.3	-	0.25×VDD ¹	V
$ I_{IH} $	High-level input current		-	-	50	nA
$ I_{IL} $	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		0.8×VDD ¹	-	-	V
V_{OL}	Low-level output voltage		-	-	0.1×VDD ¹	V
	High-level source current	VDD3P3_CPU power domain 1, 2	-	40	-	mA
$ _{OH}$	$(VDD^1 = 3.3 \text{ V}, V_{OH} >= 2.64 \text{ V},$	VDD3P3_RTC power domain 1, 2	-	40	-	mA
	output drive strength set to the maximum)	VDD_SDIO power domain 1, 3	-	20	-	mA
	Low-level sink current					
I_{OL}	$ (VDD^1 = 3.3 \text{ V}, V_{OL} = 0.495 \text{ V}, $		-	28	-	mA
	output drive strength set to the	maximum)				
R_{PU}	Pull-up resistor		-	45	-	kΩ
R_{PD}	Pull-down resistor		-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP	_PU to power off the chip	-	-	0.6	V

Notes:

- 1. Please see Table IO_MUX for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
- 2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH} >=2.64 V, as the number of current-source pins increases.
- 3. For VDD_SDIO power domain, per-pin current sourced in the same domain is gradually reduced from around 30 mA to around 10 mA, $V_{OH}>=2.64$ V, as the number of current-source pins increases.

5.4 Reliability Qualifications

Table 14: Reliability Qualifications

Reliability tests	Standards	Test conditions	Result
Electro-Static Discharge Sensitivity	JEDEC EIA/JESD22-C101	±500 V, all pins	Pass
(ESD), Charge Device Mode (CDM) $^{\mathrm{1}}$	JLDLO LIAVILODZZ-OTOT	±500 v, all pills	Fa55
Electro-Static Discharge Sensitivity	JEDEC EIA/JESD22-A114	±1500 V, all pins	Pass
(ESD), Human Body Mode (HBM) $^{\mathrm{2}}$	JEDEO LIAVILODZZ-ATT4	±1000 v, all pills	1 055
Latch-up (Over-current test)	JEDEC STANDARD NO.78	±50 mA ~ ±200 mA, room	Pass
Later-up (Over-current test)	temperature, test for IC		1 055
Latch-up (Over-voltage test)	JEDEC STANDARD NO.78	1.5 × Vmax, room tempera-	Pass
Later-up (Over-voitage test)	JEDEC STANDAND NO.76	ture, test for V_{supply}	Fa55
Moisture Sensitivity Level (MSL)	J-STD-020, MSL 3	30 °C, 60% RH, 192 hours, IR	Pass
iviolature defialtivity Level (IVIOL)	0-31D-020, WISE 3	× 3 @260 °C	1 000

- 1. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
- 2. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

5.5 RF Power-Consumption Specifications

The power consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.

Table 15: RF Power-Consumption Specifications

Mode	Min	Тур	Max	Unit
Transmit 802.11b, DSSS 1 Mbps, POUT = +19.5 dBm	-	240	-	mA
Transmit 802.11g, OFDM 54 Mbps, POUT = +16 dBm	-	190	-	mA
Transmit 802.11n, OFDM MCS7, POUT = +14 dBm	-	180	-	mA
Receive 802.11b/g/n	-	95 ~ 100	-	mA
Transmit BT/BLE, POUT = 0 dBm	-	130	-	mA
Receive BT/BLE	-	95 ~ 100	-	mA

5.6 Wi-Fi Radio

Table 16: Wi-Fi Radio Characteristics

Parameter	Condition	Min	Typical	Max	Unit
Operating frequency range note1	-	2412	-	2484	MHz
Output impedance note2	-	-	note 2	-	Ω
TX power ^{note3}	11n, MCS7	13	14	15	dBm
	11b mode	19.5	20	20.5	dBm
Sensitivity	11b, 1 Mbps	-	-98	-	dBm
	11b, 11 Mbps	-	-91	-	dBm
	11g, 6 Mbps	-	-93	-	dBm
	11g, 54 Mbps	-	-75	-	dBm
	11n, HT20, MCS0	-	-93	-	dBm
	11n, HT20, MCS7	-	-73	-	dBm
	11n, HT40, MCS0	-	-90	-	dBm
	11n, HT40, MCS7	-	-70	-	dBm
Adjacent channel rejection	11g, 6 Mbps	-	37	-	dB
	11g, 54 Mbps	-	21	-	dB
	11n, HT20, MCS0	-	37	-	dB
	11n, HT20, MCS7	-	20	-	dB

^{1.} Device should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.

^{2.} The typical value of ESP32's Wi-Fi radio output impedance is different in chips of different QFN packages. For ESP32 chips with a QFN 6×6 package (ESP32-D0WDQ6), the value is 30+j10 Ω . For ESP32 chips with a QFN 5×5 package (ESP32-D0WD, ESP32-D2WD, ESP32-S0WD), the value is 35+j10 Ω .

^{3.} Target TX power is configurable based on device or certification requirements.

5.7 Bluetooth Radio

5.7.1 Receiver - Basic Data Rate

Table 17: Receiver Characteristics - Basic Data Rate

Parameter	Conditions	Min	Тур	Max	Unit
Sensitivity @0.1% BER	-	-	-94	-	dBm
Maximum received signal @0.1% BER	-	0	-	-	dBm
Co-channel C/I	-	-	+7	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-	-6	dB
	F = F0 – 1 MHz	-	-	-6	dB
	F = F0 + 2 MHz	-	-	-25	dB
Adjacent channel selectivity C/1	F = F0 - 2 MHz	-	-	-33	dB
	F = F0 + 3 MHz	-	-94777767677	dB	
	F = F0 - 3 MHz	-	-	-45	dB
	30 MHz ~ 2000 MHz	-10	-	-	dBm
Out-of-band blocking performance	2000 MHz ~ 2400 MHz	-27	-	- -6 -6 -25 -33 -25 -45 -	dBm
Out-of-band blocking performance	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	_	-	dBm

5.7.2 Transmitter - Basic Data Rate

Table 18: Transmitter Characteristics - Basic Data Rate

Parameter	Conditions	Min	Тур	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	-12	-	+9	dBm
+20 dB bandwidth	-	-	0.9	-	MHz
	$F = F0 \pm 2 MHz$	-	-47	-	dBm
Adjacent channel transmit power	$F = F0 \pm 3 \text{ MHz}$	-	-55	-	dBm
,	$F = F0 \pm > 3 MHz$	-	-60	-	dBm
$\Delta f1_{\text{avg}}$	-	-	-	155	kHz
$\Delta f2$ max	-	133.7	-	-	kHz
$\Delta f 2_{\text{avg}}/\Delta f 1_{\text{avg}}$	-	-	0.92	-	-
ICFT	-	-	-7	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μ s
Drift (DH1)	-	-	6	-	kHz
Drift (DH5)	-	-	6	-	kHz

5.7.3 Receiver - Enhanced Data Rate

Table 19: Receiver Characteristics - Enhanced Data Rate

Parameter	Conditions	Min	Тур	Max	Unit
	π/4 DQPSK				
Sensitivity @0.01% BER	-	-	-90	-	dBm
Maximum received signal @0.01% BER	-	-	0	-	dBm
Co-channel C/I	-	-	11	-	dB
	F = F0 + 1 MHz	-	-7	-	dB
Adjacent channel selectivity C/I Sensitivity @0.01% BER Maximum received signal @0.01% BER	F = F0 - 1 MHz	-	-7	-	dB
Adjacent channel coloctivity C/I	F = F0 + 2 MHz25	-25	-	dB	
Adjacent charmer selectivity 6/1	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
	8DPSK				
Sensitivity @0.01% BER	-	-	-84	-	dBm
Maximum received signal @0.01% BER	-	-	-5	-	dBm
C/I c-channel	-	-	18	-	dB
	F = F0 + 1 MHz	-	2	-	dB
	F = F0 - 1 MHz	-	2	-	dB
Adjacent channel coloctivity C/I	F = F0 + 2 MHz	-	-25	-	dB
Adjacent charmer selectivity C/1	F = F0 - 2 MHz	-	-25	-	dB
Maximum received signal @0.01% BER	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-38	-	dB

5.7.4 Transmitter - Enhanced Data Rate

Table 20: Transmitter Characteristics - Enhanced Data Rate

Parameter	Conditions	Min	Тур	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	-12	-	+9	dBm
π /4 DQPSK max w0	-	-	-0.72	-	kHz
π /4 DQPSK max wi	-	-	-6	-	kHz
π /4 DQPSK max lwi + w0l	-	-	-7.42	-	kHz
8DPSK max w0	-	-	0.7	-	kHz
8DPSK max wi	-	-	-9.6	-	kHz
8DPSK max lwi + w0l	-	-	-10	-	kHz
	RMS DEVM	-	4.28	-	%
π /4 DQPSK modulation accuracy	99% DEVM	-	100	-	%
	Peak DEVM	-	13.3	-	%
	RMS DEVM	-	5.8	-	%
8 DPSK modulation accuracy	99% DEVM	-	100	-	%
	Peak DEVM	-	14	-	%
In-band spurious emissions	$F = F0 \pm 1 MHz$	-	-46	-	dBm

Parameter	Conditions	Min	Тур	Max	Unit
	$F = F0 \pm 2 MHz$	-	-40	-	dBm
	$F = F0 \pm 3 MHz$	-	-46	-	dBm
	F = F0 + /- > 3 MHz	-	-	-53	dBm
EDR differential phase coding	-	-	100	-	%

5.8 Bluetooth LE Radio

5.8.1 Receiver

Table 21: Receiver Characteristics - BLE

Parameter	Conditions	Min	Тур	Max	Unit
Sensitivity @30.8% PER	-	-	-97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
	F = F0 + 1 MHz	-	- 5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	-	-25	-	dB
Adjacent charmer selectivity C/1	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
	30 MHz ~ 2000 MHz	-10	-	-	dBm
Out of hand blocking porformance	2000 MHz ~ 2400 MHz	-27	-	-	dBm
Out-of-band blocking performance	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	_	dBm

5.8.2 Transmitter

Table 22: Transmitter Characteristics - BLE

Parameter	Conditions	Min	Тур	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	-12	-	+9	dBm
	$F = F0 \pm 2 MHz$	-	-52	-	dBm
Adjacent channel transmit power	$F = F0 \pm 3 MHz$	-	-58	-	dBm
	$F = F0 \pm > 3 MHz$	-	-60	-	dBm
$\Delta f1_{avg}$	-	-	-	265	kHz
$\Delta f2_{ extsf{max}}$	-	247	-	-	kHz
$\Delta f 2_{\text{avg}}/\Delta f 1_{\text{avg}}$	-	-	-0.92	-	-
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

6. Package Information

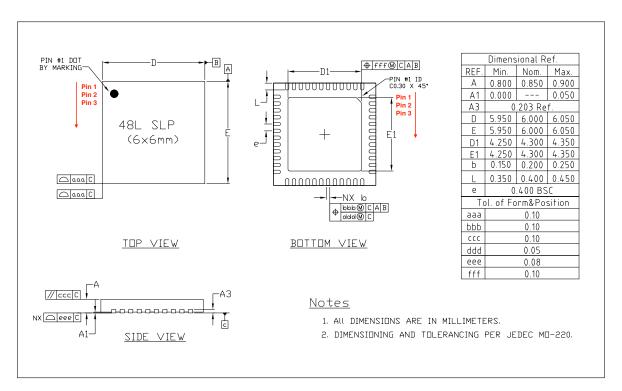


Figure 8: QFN48 (6x6 mm) Package

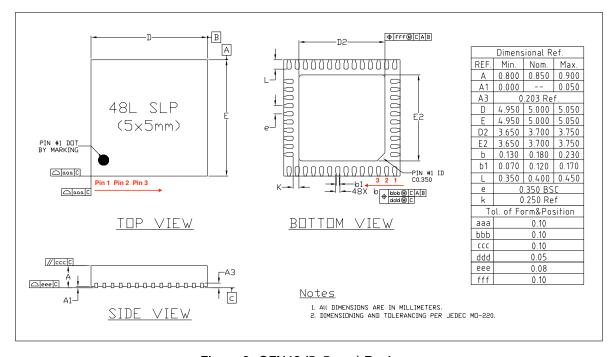


Figure 9: QFN48 (5x5 mm) Package

Note:

The pins of the chip are numbered in an anti-clockwise direction from Pin 1 in the top view.

7. Part Number and Ordering Information

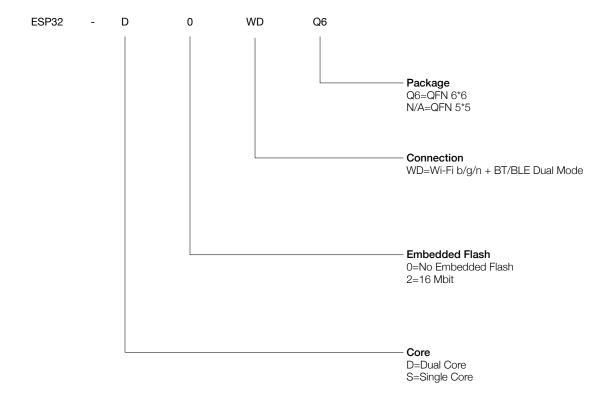


Figure 10: ESP32 Part Number

The table below provides the ordering information of the ESP32 series of chips.

Table 23: ESP32 Ordering Information

Ordering code	Core	Embedded flash	Connection	Package
ESP32-D0WDQ6	Dual core	No embedded flash	Wi-Fi b/g/n + BT/BLE Dual Mode	QFN 6*6
ESP32-D0WD	Dual core	No embedded flash	Wi-Fi b/g/n + BT/BLE Dual Mode	QFN 5*5
ESP32-D2WD	Dual core	16-Mbit embedded flash (40 MHz)	Wi-Fi b/g/n + BT/BLE Dual Mode	QFN 5*5
ESP32-S0WD	Single core	No embedded flash	Wi-Fi b/g/n + BT/BLE Dual Mode	QFN 5*5

8. Learning Resources

8.1 Must-Read Documents

Click on the following links to access documents related to ESP32.

• ESP-IDF Programming Guide

It hosts extensive documentation for ESP-IDF, ranging from hardware guides to API reference.

• ESP32 Technical Reference Manual

The manual provides detailed information on how to use the ESP32 memory and peripherals.

• ESP32 Hardware Resources

The zip files include schematics, PCB layout, Gerber and BOM list.

• ESP32 Hardware Design Guidelines

The guidelines provide recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including the ESP32 chip, the ESP32 modules and development boards.

• ESP32 AT Instruction Set and Examples

This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.

• Espressif Products Ordering Information

8.2 Must-Have Resources

Here are the ESP32-related must-have resources.

• ESP32 BBS

This is an Engineer-to-Engineer (E2E) Community for ESP32, where you can post questions, share knowledge, explore ideas, and solve problems together with fellow engineers.

• ESP32 GitHub

ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. This channel of communication has been established to help developers get started with ESP32 and encourage them to share their knowledge of ESP32-related hardware and software.

• ESP32 Tools

This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".

• ESP-IDF

This webpage links users to the official IoT development framework for ESP32.

• ESP32 Resources

This webpage provides the links to all available ESP32 documents, SDK and tools.

Appendix A – ESP32 Pin Lists

A.1. Notes on ESP32 Pin Lists

Table 24: Notes on ESP32 Pin Lists

No.	Description
4	In Table IO_MUX, the boxes highlighted in yellow indicate the GPIO pins that are input-only.
1	Please see the following note for further details.
	GPIO pins 34-39 are input-only. These pins do not feature an output driver or internal pull-
2	up/pull-down circuitry. The pin names are: SENSOR_VP (GPIO36), SENSOR_CAPP (GPIO37),
	SENSOR_CAPN (GPIO38), SENSOR_VN (GPIO39), VDET_1 (GPIO34), VDET_2 (GPIO35).
	The pins are grouped into four power domains: VDDA (analog power supply), VDD3P3_RTC
	(RTC power supply), VDD3P3_CPU (power supply of digital IOs and CPU cores), VDD_SDIO
3	(power supply of SDIO IOs). VDD_SDIO is the output of the internal SDIO-LDO. The voltage of
	SDIO-LDO can be configured at 1.8 V or be the same as that of VDD3P3_RTC. The strapping
	pin and eFuse bits determine the default voltage of the SDIO-LDO. Software can change the
	voltage of the SDIO-LDO by configuring register bits. For details, please see the column "Power
	Domain" in Table IO_MUX.
	The functional pins in the VDD3P3_RTC domain are those with analog functions, including the
4	32 kHz crystal oscillator, ADC, DAC, and the capacitive touch sensor. Please see columns
	"Analog Function 1~3" in Table IO_MUX.
5	These VDD3P3_RTC pins support the RTC function, and can work during Deep-sleep. For
	example, an RTC-GPIO can be used for waking up the chip from Deep-sleep.
	The GPIO pins support up to six digital functions, as shown in columns "Function 1~6" In Table
	IO_MUX. The function selection registers will be set as "N-1", where N is the function number.
	Below are some definitions:
	SD_* is for signals of the SDIO slave.
	HS1_* is for Port 1 signals of the SDIO host.
	HS2_* is for Port 2 signals of the SDIO host.
6	MT* is for signals of the JTAG.
	• U0* is for signals of the UART0 module.
	U1* is for signals of the UART1 module.
	• U2* is for signals of the UART2 module.
	SPI* is for signals of the SPI01 module.
	HSPI* is for signals of the SPI2 module.
	VSPI* is for signals of the SPI3 module.

No.	Description
	Each column about digital "Function" is accompanied by a column about "Type". Please see
	the following explanations for the meanings of "type" with respect to each "function" they are
	associated with. For each "Function-N", "type" signifies:
	• I: input only. If a function other than "Function-N" is assigned, the input signal of
	"Function-N" is still from this pin.
	• I1: input only. If a function other than "Function-N" is assigned, the input signal of
	"Function-N" is always "1".
	• I0: input only. If a function other than "Function-N" is assigned, the input signal of
7	"Function-N" is always "0".
'	O: output only.
	• T: high-impedance.
	• I/O/T: combinations of input, output, and high-impedance according to the function sig-
	nal.
	• I1/O/T: combinations of input, output, and high-impedance, according to the function signal. If a function is not selected, the input signal of the function is "1".
	For example, pin 30 can function as HS1_CMD or SD_CMD, where HS1_CMD is of an "I1/O/T"
	type. If pin 30 is selected as HS1_CMD, this pin's input and output are controlled by the SDIO
	host. If pin 30 is not selected as HS1_CMD, this pin simput and output are controlled by the 3Dio host.
	Each digital output pin is associated with its configurable drive strength. Column "Drive
	Strength" in Table IO_MUX lists the default values. The drive strength of the digital output
	pins can be configured into one of the following four options:
	• 0: ~5 mA
8	• 1: ~10 mA
	• 2: ~20 mA
	• 3: ~40 mA
	The default value is 2.
	The drive strength of the internal pull-up (wpu) and pull-down (wpd) is \sim 75 μ A.
	Column "At Reset" in Table IO_MUX lists the status of each pin during reset, including input-
9	enable (ie=1), internal pull-up (wpu) and internal pull-down (wpd). During reset, all pins are
	output-disabled.
	Column "After Reset" in Table IO_MUX lists the status of each pin immediately after reset,
10	including input-enable (ie=1), internal pull-up (wpu) and internal pull-down (wpd). After reset,
	each pin is set to "Function 1". The output-enable is controlled by digital Function 1.
	Table Ethernet_MAC is about the signal mapping inside Ethernet MAC. The Ethernet MAC
11	supports MII and RMII interfaces, and supports both the internal PLL clock and the external
' '	clock source. For the MII interface, the Ethernet MAC is with/without the TX_ERR signal. MDC,
	MDIO, CRS and COL are slow signals, and can be mapped onto any GPIO pin through the
	GPIO-Matrix.
	Table GPIO Matrix is for the GPIO-Matrix. The signals of the on-chip functional modules can
12	be mapped onto any GPIO pin. Some signals can be mapped onto a pin by both IO-MUX
	and GPIO-Matrix, as shown in the column tagged as "Same input signal from IO_MUX core"
	in Table GPIO Matrix.

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No.	Description
	*In Table GPIO_Matrix the column "Default Value if unassigned" records the default value of
10	the an input signal if no GPIO is assigned to it. The actual value is determined by register
13	GPIO_FUNCm_IN_INV_SEL and GPIO_FUNCm_IN_SEL. (The value of m ranges from 1 to
	255.)

A.2. GPIO_Matrix

Table 25: GPIO_Matrix

Signal No.	Input signals	Default value if unassigned*	Same input signal from IO_MUX core	Output signals	Output enable of output signals
0	SPICLK_in	0	yes	SPICLK_out	SPICLK_oe
1	SPIQ_in	0	yes	SPIQ_out	SPIQ_oe
2	SPID_in	0	yes	SPID_out	SPID_oe
3	SPIHD_in	0	yes	SPIHD_out	SPIHD_oe
4	SPIWP_in	0	yes	SPIWP_out	SPIWP_oe
5	SPICS0_in	0	yes	SPICS0_out	SPICS0_oe
6	SPICS1_in	0	no	SPICS1_out	SPICS1_oe
7	SPICS2_in	0	no	SPICS2_out	SPICS2_oe
8	HSPICLK_in	0	yes	HSPICLK_out	HSPICLK_oe
9	HSPIQ_in	0	yes	HSPIQ_out	HSPIQ_oe
10	HSPID_in	0	yes	HSPID_out	HSPID_oe
11	HSPICS0_in	0	yes	HSPICS0_out	HSPICS0_oe
12	HSPIHD_in	0	yes	HSPIHD_out	HSPIHD_oe
13	HSPIWP_in	0	yes	HSPIWP_out	HSPIWP_oe
14	U0RXD_in	0	yes	U0TXD_out	1'd1
15	U0CTS_in	0	yes	U0RTS_out	1'd1
16	U0DSR_in	0	no	U0DTR_out	1'd1
17	U1RXD_in	0	yes	U1TXD_out	1'd1
18	U1CTS_in	0	yes	U1RTS_out	1'd1
23	I2S0O_BCK_in	0	no	I2S0O_BCK_out	1'd1
24	I2S1O_BCK_in	0	no	I2S1O_BCK_out	1'd1
25	I2S00_WS_in	0	no	I2S0O_WS_out	1'd1
26	I2S1O_WS_in	0	no	I2S1O_WS_out	1'd1
27	I2S0I_BCK_in	0	no	I2S0I_BCK_out	1'd1
28	I2S0I_WS_in	0	no	I2S0I_WS_out	1'd1
29	I2CEXT0_SCL_in	1	no	I2CEXT0_SCL_out	1'd1
30	I2CEXTO_SDA_in	1	no	I2CEXTO_SDA_out	1'd1
31	pwm0_sync0_in	0	no	sdio_tohost_int_out	1'd1
32	pwm0_sync1_in	0	no	pwm0_out0a	1'd1
33	pwm0_sync2_in	0	no	pwm0_out0b	1'd1
34	pwm0_f0_in	0	no	pwm0_out1a	1'd1
35	pwm0_f1_in	0	no	pwm0_out1b	1'd1

Signal		Default value	Same input signal from		Output enable
No.	Input signals	if unassigned	IO_MUX	Output signals	of output signals
36	pwm0 f0 in	0	core	pwm0_out2a	1'd1
	pwm0_f2_in		no	· _	
37	-	0	no	pwm0_out2b	1'd1
39	pcnt_sig_ch0_in0	0	no	-	1'd1
40	pcnt_sig_ch1_in0	0	no	-	1'd1
41	pcnt_ctrl_ch0_in0	0	no	-	1'd1
42	pcnt_ctrl_ch1_in0	0	no	-	1'd1
43	pcnt_sig_ch0_in1	0	no	-	1'd1
44	pcnt_sig_ch1_in1	0	no	-	1'd1
45	pcnt_ctrl_ch0_in1	0	no	-	1'd1
46	pcnt_ctrl_ch1_in1	0	no	-	1'd1
47	pcnt_sig_ch0_in2	0	no	-	1'd1
48	pcnt_sig_ch1_in2	0	no	-	1'd1
49	pcnt_ctrl_ch0_in2	0	no	-	1'd1
50	pcnt_ctrl_ch1_in2	0	no	-	1'd1
51	pcnt_sig_ch0_in3	0	no	-	1'd1
52	pcnt_sig_ch1_in3	0	no	-	1'd1
53	pcnt_ctrl_ch0_in3	0	no	-	1'd1
54	pcnt_ctrl_ch1_in3	0	no	-	1'd1
55	pcnt_sig_ch0_in4	0	no	-	1'd1
56	pcnt_sig_ch1_in4	0	no	-	1'd1
57	pcnt_ctrl_ch0_in4	0	no	-	1'd1
58	pcnt_ctrl_ch1_in4	0	no	-	1'd1
61	HSPICS1_in	0	no	HSPICS1_out	HSPICS1_oe
62	HSPICS2_in	0	no	HSPICS2_out	HSPICS2_oe
63	VSPICLK_in	0	yes	VSPICLK_out_mux	VSPICLK_oe
64	VSPIQ_in	0	yes	VSPIQ_out	VSPIQ_oe
65	VSPID_in	0	yes	VSPID_out	VSPID_oe
66	VSPIHD_in	0	yes	VSPIHD_out	VSPIHD_oe
67	VSPIWP_in	0	yes	VSPIWP_out	VSPIWP_oe
68	VSPICS0_in	0	yes	VSPICS0_out	VSPICS0_oe
69	VSPICS1 in	0	no	VSPICS1_out	VSPICS1_oe
70	VSPICS2_in	0	no	VSPICS2_out	VSPICS2_oe
71	pcnt_sig_ch0_in5	0	no	ledc_hs_sig_out0	1'd1
72	pcnt_sig_ch1_in5	0	no	ledc_hs_sig_out1	1'd1
73	pcnt_ctrl_ch0_in5	0	no	ledc_hs_sig_out2	1'd1
74	pcnt_ctrl_ch1_in5	0	no	ledc_hs_sig_out3	1'd1
75	pcnt_sig_ch0_in6	0	no	ledc_hs_sig_out4	1'd1
76	pcnt_sig_ch1_in6	0	no	ledc_hs_sig_out5	1'd1
77	pcnt_sig_crrr_in6 pcnt_ctrl_ch0_in6	0	no	ledc_hs_sig_out6	1'd1
78	pcnt_ctrl_ch1_in6	0	no	ledc_hs_sig_out7	1'd1
79	pcnt_ctn_cm_in6 pcnt_sig_ch0_in7	0		ledc_ls_sig_out0	1'd1
19	pont_sig_cno_in/	0	no	leac_is_sig_out0	TUI

			Same input		
Signal		Default value	signal from		Output enable
No.	Input signals	if unassigned	IO_MUX	Output signals	of output signals
1401		ii ariaccigi ica	core		or output signals
80	pcnt_sig_ch1_in7	0	no	ledc_ls_sig_out1	1'd1
81	pcnt_ctrl_ch0_in7	0	no	ledc_ls_sig_out2	1'd1
82	pcnt_ctrl_ch1_in7	0	no	ledc_ls_sig_out3	1'd1
83	rmt_sig_in0	0	no	ledc_ls_sig_out4	1'd1
84	rmt_sig_in1	0	no	ledc_ls_sig_out5	1'd1
85	rmt_sig_in2	0	no	ledc_ls_sig_out6	1'd1
86	rmt_sig_in3	0	no	ledc_ls_sig_out7	1'd1
87	rmt_sig_in4	0	no	rmt_sig_out0	1'd1
88	rmt_sig_in5	0	no	rmt_sig_out1	1'd1
89	rmt_sig_in6	0	no	rmt_sig_out2	1'd1
90	rmt_sig_in7	0	no	rmt_sig_out3	1'd1
91	-	-	-	rmt_sig_out4	1'd1
92	-	-	-	rmt_sig_out6	1'd1
94	-	-	-	rmt_sig_out7	1'd1
95	I2CEXT1_SCL_in	1	no	I2CEXT1_SCL_out	1'd1
96	I2CEXT1_SDA_in	1	no	I2CEXT1_SDA_out	1'd1
97	host_card_detect_n_1	0	no	host_ccmd_od_pullup_en_n	1'd1
98	host_card_detect_n_2	0	no	host_rst_n_1	1'd1
99	host_card_write_prt_1	0	no	host_rst_n_2	1'd1
100	host_card_write_prt_2	0	no	gpio_sd0_out	1'd1
101	host_card_int_n_1	0	no	gpio_sd1_out	1'd1
102	host_card_int_n_2	0	no	gpio_sd2_out	1'd1
103	pwm1_sync0_in	0	no	gpio_sd3_out	1'd1
104	pwm1_sync1_in	0	no	gpio_sd4_out	1'd1
105	pwm1_sync2_in	0	no	gpio_sd5_out	1'd1
106	pwm1_f0_in	0	no	gpio_sd6_out	1'd1
107	pwm1_f1_in	0	no	gpio_sd7_out	1'd1
108	pwm1_f2_in	0	no	pwm1_out0a	1'd1
109	pwm0_cap0_in	0	no	pwm1_out0b	1'd1
110	pwm0_cap1_in	0	no	pwm1_out1a	1'd1
111	pwm0_cap2_in	0	no	pwm1_out1b	1'd1
112	pwm1_cap0_in	0	no	pwm1_out2a	1'd1
113	pwm1_cap1_in	0	no	pwm1_out2b	1'd1
114	pwm1_cap2_in	0	no	pwm2_out1h	1'd1
115	pwm2_flta	1	no	pwm2_out1l	1'd1
116	pwm2_fltb	1	no	pwm2_out2h	1'd1
117	pwm2_cap1_in	0	no	pwm2_out2l	1'd1
118	pwm2_cap2_in	0	no	pwm2_out3h	1'd1
119	pwm2_cap3_in	0	no	pwm2_out3l	1'd1
120	pwm3_flta	1	no	pwm2_out4h	1'd1
121	pwm3_fltb	1	no	pwm2_out4l	1'd1

			Same input		
Signal	Input signals	Default value	signal from	Output signals	Output enable
No.	input signais	if unassigned	IO_MUX	Output signals	of output signals
			core		
122	pwm3_cap1_in	0	no	-	1'd1
123	pwm3_cap2_in	0	no	-	1'd1
124	pwm3_cap3_in	0	no	-	1'd1
140	I2S0I_DATA_in0	0	no	I2S0O_DATA_out0	1'd1
141	I2S0I_DATA_in1	0	no	I2S0O_DATA_out1	1'd1
142	I2S0I_DATA_in2	0	no	I2S0O_DATA_out2	1'd1
143	I2S0I_DATA_in3	0	no	I2S0O_DATA_out3	1'd1
144	I2S0I_DATA_in4	0	no	I2S0O_DATA_out4	1'd1
145	I2S0I_DATA_in5	0	no	I2S0O_DATA_out5	1'd1
146	I2S0I_DATA_in6	0	no	I2S0O_DATA_out6	1'd1
147	I2S0I_DATA_in7	0	no	I2S0O_DATA_out7	1'd1
148	I2S0I_DATA_in8	0	no	I2S0O_DATA_out8	1'd1
149	I2S0I_DATA_in9	0	no	I2S0O_DATA_out9	1'd1
150	I2S0I_DATA_in10	0	no	I2S0O_DATA_out10	1'd1
151	I2S0I_DATA_in11	0	no	I2S0O_DATA_out11	1'd1
152	I2S0I_DATA_in12	0	no	I2S0O_DATA_out12	1'd1
153	I2S0I_DATA_in13	0	no	I2S0O_DATA_out13	1'd1
154	I2S0I_DATA_in14	0	no	I2S0O_DATA_out14	1'd1
155	I2S0I_DATA_in15	0	no	I2S0O_DATA_out15	1'd1
156	-	-	-	I2S0O_DATA_out16	1'd1
157	-	-	-	I2S0O_DATA_out17	1'd1
158	-	-	-	I2S0O_DATA_out18	1'd1
159	-	-	-	I2S0O_DATA_out19	1'd1
160	-	-	-	I2S0O_DATA_out20	1'd1
161	-	-	-	I2S0O_DATA_out21	1'd1
162	-	-	-	I2S0O_DATA_out22	1'd1
163	-	-	-	I2S0O_DATA_out23	1'd1
164	I2S1I_BCK_in	0	no	I2S1I_BCK_out	1'd1
165	I2S1I_WS_in	0	no	I2S1I_WS_out	1'd1
166	I2S1I_DATA_in0	0	no	I2S1O_DATA_out0	1'd1
167	I2S1I_DATA_in1	0	no	I2S1O_DATA_out1	1'd1
168	I2S1I_DATA_in2	0	no	I2S1O_DATA_out2	1'd1
169	I2S1I_DATA_in3	0	no	I2S1O_DATA_out3	1'd1
170	I2S1I_DATA_in4	0	no	I2S1O_DATA_out4	1'd1
171	I2S1I_DATA_in5	0	no	I2S1O_DATA_out5	1'd1
172	I2S1I_DATA_in6	0	no	I2S1O_DATA_out6	1'd1
173	I2S1I_DATA_in7	0	no	I2S1O_DATA_out7	1'd1
174	I2S1I_DATA_in8	0	no	I2S1O_DATA_out8	1'd1
175	I2S1I_DATA_in9	0	no	I2S1O_DATA_out9	1'd1
176	I2S1I_DATA_in10	0	no	I2S1O_DATA_out10	1'd1
177	I2S1I_DATA_in11	0	no	I2S1O_DATA_out11	1'd1

Signal No.	Input signals	Default value if unassigned	Same input signal from IO_MUX core	Output signals	Output enable of output signals
178	I2S1I_DATA_in12	0	no	I2S1O_DATA_out12	1'd1
179	I2S1I_DATA_in13	0	no	I2S1O_DATA_out13	1'd1
180	I2S1I_DATA_in14	0	no	I2S1O_DATA_out14	1'd1
181	I2S1I_DATA_in15	0	no	I2S1O_DATA_out15	1'd1
182	-	-	-	I2S1O_DATA_out16	1'd1
183	-	-	-	I2S1O_DATA_out17	1'd1
184	-	-	-	I2S1O_DATA_out18	1'd1
185	-	-	-	I2S1O_DATA_out19	1'd1
186	-	-	-	I2S1O_DATA_out20	1'd1
187	-	-	-	I2S1O_DATA_out21	1'd1
188	-	-	-	I2S1O_DATA_out22	1'd1
189	-	-	-	I2S1O_DATA_out23	1'd1
190	I2S0I_H_SYNC	0	no	pwm3_out1h	1'd1
191	I2S0I_V_SYNC	0	no	pwm3_out1l	1'd1
192	I2S0I_H_ENABLE	0	no	pwm3_out2h	1'd1
193	I2S1I_H_SYNC	0	no	pwm3_out2l	1'd1
194	I2S1I_V_SYNC	0	no	pwm3_out3h	1'd1
195	I2S1I_H_ENABLE	0	no	pwm3_out3l	1'd1
196	-	-	-	pwm3_out4h	1'd1
197	-	-	-	pwm3_out4l	1'd1
198	U2RXD_in	0	yes	U2TXD_out	1'd1
199	U2CTS_in	0	yes	U2RTS_out	1'd1
200	emac_mdc_i	0	no	emac_mdc_o	emac_mdc_oe
201	emac_mdi_i	0	no	emac_mdo_o	emac_mdo_o_e
202	emac_crs_i	0	no	emac_crs_o	emac_crs_oe
203	emac_col_i	0	no	emac_col_o	emac_col_oe
204	pcmfsync_in	0	no	bt_audio0_irq	1'd1
205	pcmclk_in	0	no	bt_audio1_irq	1'd1
206	pcmdin	0	no	bt_audio2_irq	1'd1
207	-	-	-	ble_audio0_irq	1'd1
208	-	-	-	ble_audio1_irq	1'd1
209	-	-	-	ble_audio2_irq	1'd1
210	-	-	-	pcmfsync_out	pcmfsync_en
211	-	-	-	pcmclk_out	pcmclk_en
212	-	-	-	pcmdout	pcmdout_en
213	-	-	-	ble_audio_sync0_p	1'd1
214	-	-	-	ble_audio_sync1_p	1'd1
215	-	-	-	ble_audio_sync2_p	1'd1
224	-	-	-	sig_in_func224	1'd1
225	-	-	-	sig_in_func225	1'd1
226	-	-	-	sig_in_func226	1'd1

Signal No.	Input signals	Default value if unassigned	Same input signal from IO_MUX core	Output signals	Output enable of output signals
227	-	-	_	sig_in_func227	1'd1
228	-	-	-	sig_in_func228	1'd1

A.3. Ethernet_MAC

Table 26: Ethernet_MAC

PIN Name	Function6	MII (int_osc)	MII (ext_osc)	RMII (int_osc)	RMII (ext_osc)			
GPIO0	EMAC_TX_CLK	TX_CLK (I)	TX_CLK (I)	CLK_OUT(O)	EXT_OSC_CLK(I)			
GPIO5	EMAC_RX_CLK	RX_CLK (I)	RX_CLK (I)	-	-			
GPIO21	EMAC_TX_EN	TX_EN(O)	TX_EN(O)	TX_EN(O)	TX_EN(O)			
GPIO19	EMAC_TXD0	TXD[0](O)	TXD[0](O)	TXD[0](O)	TXD[0](O)			
GPIO22	EMAC_TXD1	TXD[1](O)	TXD[1](O)	TXD[1](O)	TXD[1](O)			
MTMS	EMAC_TXD2	TXD[2](O)	TXD[2](O)	-	-			
MTDI	EMAC_TXD3	TXD[3](O)	TXD[3](O)	-	-			
MTCK	EMAC_RX_ER	RX_ER(I)	RX_ER(I)	-	-			
GPIO27	EMAC_RX_DV	RX_DV(I)	RX_DV(I)	CRS_DV(I)	CRS_DV(I)			
GPIO25	EMAC_RXD0	RXD[0](I)	RXD[0](I)	RXD[0](I)	RXD[0](I)			
GPIO26	EMAC_RXD1	RXD[1](I)	RXD[1](I)	RXD[1](I)	RXD[1](I)			
U0TXD	EMAC_RXD2	RXD[2](I)	RXD[2](I)	-	-			
MTDO	EMAC_RXD3	RXD[3](I)	RXD[3](I)	-	-			
GPIO16	EMAC_CLK_OUT	CLK_OUT(O)	-	CLK_OUT(O)	-			
GPIO17	EMAC_CLK_OUT_180	CLK_OUT_180(O)	-	CLK_OUT_180(O)	-			
GPIO4	EMAC_TX_ER	TX_ERR(O)*	TX_ERR(O)*	-	-			
In GPIO Matrix*	-	MDC(O)	MDC(O)	MDC(O)	MDC(O)			
In GPIO Matrix*	-	MDIO(IO)	MDIO(IO)	MDIO(IO)	MDIO(IO)			
In GPIO Matrix*	-	CRS(I)	CRS(I)	-	-			
In GPIO Matrix*	-	COL(I)	COL(I)	-	-			
*Notes: 1. The GPIO Matrix can be any GPIO. 2. The TX_ERR (O) is optional.								

A.4. IO_MUX

For the list of IO_MUX pins, please see the next page.

IO_MUX

Appendix A

Power Supply Pin	Analog Pin	Digital Pin	Power Domain	Analog Function1	Analog Function2	Analog Function3	RTC Function1	RTC Function2	Function1	Туре	Function2	Туре	Function3	Туре	Function4	Туре	Function5	Туре	Function6	Туре	Drive Strength (2'd2: 20 mA)	At Reset	After Res
VDDA			VDDA supply in																				
	LNA_IN		VDD3P3																				
VDD3P3			VDD3P3 supply in																				
VDD3P3			VDD3P3 supply in																				
	SENSOR_VP		VDD3P3_RTC	ADC_H	ADC1_CH0		RTC_GPIO0		GPIO36	1			GPIO36	1								oe=0, ie=0	oe=0, ie=0
	SENSOR_CAPP		VDD3P3_RTC	ADC_H	ADC1_CH1		RTC_GPIO1		GPI037	1			GPIO37	1								oe=0, ie=0	oe=0, ie=
	SENSOR CAPN		VDD3P3 RTC	ADC H	ADC1 CH2		RTC GPIO2		GPIO38	1			GPIO38	1								oe=0. ie=0	oe=0, ie=
	SENSOR_VN		VDD3P3_RTC	ADC_H	ADC1_CH3		RTC_GPIO3		GPI039	1			GPIO39	1								oe=0, ie=0	oe=0, ie=
	CHIP PU		VDD3P3_RTC																				
	VDET_1		VDD3P3_RTC		ADC1_CH6		RTC_GPIO4		GPI034	1			GPIO34	1								oe=0, ie=0	oe=0, ie
	VDET_2		VDD3P3_RTC		ADC1 CH7		RTC_GPIO5		GPIO35	1			GPIO35	1								oe=0, ie=0	oe=0, ie
	32K XP		VDD3P3 RTC	XTAL 32K P		TOLICHO	RTC GPIO9		GPI032	I/O/T			GPIO32	I/O/T							2'd2	oe=0, ie=0	oe=0, ie
	ULI CA		VDD01 0_1110	ADAL DETC	74501_0114	1000115	1110_01100		GI IOUL	1/0/1			GI IOUL	0071							L GL	00-0,10-0	00-0, id
	32K_XN		VDD3P3_RTC	XTAL_32K_N	ADC1_CH5	TOUGUE	RTC_GPIO8		GPIO33	I/O/T			GPIO33	I/O/T							2°d2	oe=0, ie=0	oe=0, ie
	JEN_AN	GPIO25	VDD3P3_HTC VDD3P3_RTC	DAC 1	ADC1_CH5 ADC2 CH8	IUUUUNS	RTC GPIO6		GPIO33	I/O/T			GPIO33 GPIO25	I/O/T					EMAC RXD0	1	2'd2	oe=0, ie=0 oe=0, ie=0	oe=0, ie
		GPI025 GPI026	VDD3P3_RTC VDD3P3_RTC	DAC 2	ADC2_CH6 ADC2_CH9		RTC_GPIO6		GPI025	I/O/T			GPIO25 GPIO26	I/O/T					EMAC_RXD1	1	2'd2	oe=0, ie=0	oe=0, ie
				DAG_2		-																	
		GPIO27	VDD3P3_RTC		ADC2_CH7		RTC_GPIO17		GPI027	I/O/T			GPIO27	I/O/T					EMAC_RX_DV	1	2'd2	oe=0, ie=0	oe=0, is
		MTMS	VDD3P3_RTC		ADC2_CH6	TOUCH6	RTC_GPIO16		MTMS	10	HSPICLK	I/O/T	GPIO14		HS2_CLK	0	SD_CLK	10	EMAC_TXD2	0	2'd2	oe=0, ie=0	oe=0, is
		MTDI	VDD3P3_RTC		ADC2_CH5	TOUCH5	RTC_GPIO15		MTDI	11	HSPIQ	I/O/T	GPIO12	I/O/T	HS2_DATA2	11/O/T	SD_DATA2	11/O/T	EMAC_TXD3	0	2'd2	oe=0, ie=1, wpd	oe=0, i
VDD3P3_RTC			VDD3P3_RTC supply in																				
		MTCK	VDD3P3_RTC		ADC2_CH4		RTC_GPIO14		MTCK	11	HSPID		GPIO13		HS2_DATA3		SD_DATA3		EMAC_RX_ER	1	2'd2	oe=0, ie=0	oe=0, i
		MTDO	VDD3P3_RTC		ADC2_CH3	TOUCH3	RTC_GPIO13	I2C_SDA	MTDO	O/T	HSPICS0	I/O/T	GPIO15	I/O/T	HS2_CMD	I1/O/T	SD_CMD	11/O/T	EMAC_RXD3	1	2'd2	oe=0, ie=1, wpu	oe=0, i
		GPIO2	VDD3P3_RTC		ADC2_CH2	TOUCH2	RTC_GPIO12	I2C_SCL	GPIO2	I/O/T	HSPIWP	I/O/T	GPIO2	I/O/T	HS2_DATA0	I1/O/T	SD_DATA0	11/O/T			2'd2	oe=0, ie=1, wpd	oe=0, is
		GPI00	VDD3P3_RTC		ADC2_CH1	TOUCH1	RTC_GPIO11	I2C_SDA	GPI00	I/O/T	CLK_OUT1	0	GPI00	I/O/T					EMAC_TX_CLK	1	2'd2	oe=0, ie=1, wpu	oe=0, i
		GPIO4	VDD3P3_RTC		ADC2_CH0	TOUCH0	RTC_GPIO10	I2C_SCL	GPIO4	I/O/T	HSPIHD	I/O/T	GPIO4	I/O/T	HS2_DATA1	11/O/T	SD_DATA1	I1/O/T	EMAC_TX_ER	0	2°d2	oe=0, ie=1, wpd	oe=0, is
		GPIO16	VDD_SDIO						GPIO16	I/O/T			GPIO16	I/O/T	HS1_DATA4	11/O/T	U2RXD	l1	EMAC_CLK_OUT	0	2°d2	oe=0, ie=0	oe=0, is
VDD SDIO			VDD_SDIO supply out/in																				
		GPIO17	VDD_SDIO						GPIO17	I/O/T			GPIO17	I/O/T	HS1_DATA5	11/O/T	U2TXD	0	EMAC_CLK_OUT_180	0	2°d2	oe=0, ie=0	oe=0, is
		SD_DATA_2	VDD_SDIO						SD_DATA2	11/O/T	SPIHD	I/O/T	GPIO9		HS1_DATA2	11/O/T		11			2'd2	oe=0, ie=1, wpu	oe=0, i
		SD DATA 3	VDD SDIO						SD DATA3	10/O/T	SPIWP	I/O/T	GPIO10			11/O/T		0			2'd2	oe=0, ie=1, wpu	oe=0, i
		SD CMD	VDD_SDIO		_				SD CMD	I1/O/T	SPICS0	I/O/T			HS1_CMD		U1RTS	0			2'd2	oe=0, ie=1, wpu	oe=0, i
		SD_CIK	VDD_SDIO						SD_CLK	10	SPICLK	I/O/T	GPI06			0	U1CTS	11			2'd2	oe=0, ie=1, wpu	oe=0, i
			VDD_SDIO		_				SD DATAO	11/O/T			GPIO7		HS1_DATAD		U2RTS	0			2'd2	oe=0, ie=1, wpu	oe=0, i
		SD_DATA_1	VDD_SDIO						SD_DATA1	I1/O/T	SPID		GPI08		HS1_DATA1		U2CTS	11			2'd2	oe=0, ie=1, wpu	oe=0, i
		GPIO5	VDD3P3_CPU						GPI05	I/O/T	VSPICS0	I/O/T			HS1_DATA6	11/O/T			EMAC_RX_CLK	1	2'd2	oe=0, ie=1, wpu	oe=0, i
		GPIO18	VDD3P3_CPU						GPIO18	I/O/T	VSPICLK		GPIO18		HS1_DATA7	11/O/T					2'd2	oe=0, ie=0	oe=0, i
		GPIO23	VDD3P3_CPU						GPIO23	I/O/T	VSPID	I/O/T	GPIO23	I/O/T	HS1_STROBE	10					2°d2	oe=0, ie=0	oe=0, i
VDD3P3_CPU			VDD3P3_CPU supply in																				
		GPIO19	VDD3P3_CPU						GPIO19	I/O/T	VSPIQ	I/O/T	GPIO19	I/O/T	UOCTS	11			EMAC_TXD0	0	2'd2	oe=0, ie=0	oe=0, i
		GPI022	VDD3P3_CPU						GPI022	I/O/T	VSPIWP	I/O/T	GPIO22	I/O/T	UORTS	0			EMAC_TXD1	0	2'd2	oe=0, ie=0	oe=0, is
		UORXD	VDD3P3_CPU						UORXD	11	CLK_OUT2	0	GPIO3	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, is
		UOTXD	VDD3P3_CPU						UOTXD	0	CLK_OUT3	0	GPIO1	I/O/T					EMAC_RXD2	1	2°d2	oe=0, ie=1, wpu	oe=0, is
		GPIO21	VDD3P3 CPU						GPI021	I/O/T	VSPIHD	I/O/T		I/O/T					EMAC TX EN	0	2'd2	oe=0, ie=0	oe=0, is
VDDA			VDDA supply in																	-	-		J, K
	XTAL N		VDDA																				
	XTAL P		VDDA	-			_																_
VDDA	AU L		VDDA supply in				_		-														+
VUUN	CAP2		VDDA supply in	-			-		-		-												_
	CAP2 CAP1		VDDA	-			-		-														_
			YDUN																				+
8	14	26																					

Notes:

- wpu: weak pull-up;
- wpd: weak pull-dowr
- ne: input enable
 ne: output ena
- Please see Table: Notes on ESP32 Pin Lists for more information. (请参考表: 管脚清单说明。

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Revision History

Date	Version	Release notes
		Added pin-pin mapping between ESP32-D2WD and the embedded flash under
2019.07	V3.1	Table 1 Pin Description;
		Updated Figure 10 ESP32 Part Number.
2019.04	V3.0	Added information about the setup and hold times for the strapping pins in Section
2019.04	V3.0	2.4: Strapping Pins.
		Applied new formatting to Table 1: Pin Description;
2019.02	V2.9	Fixed typos with respect to the ADC1 channel mappings in Table 10: Peripheral
		Pin Configurations.
		Changed the RF power control range in Table 18, Table 20 and Table 22 from -12
2019.01	V2.8	~ +12 to −12 ~ +9 dBm;
		Small text changes.
2018.11	V2.7	Updated Section 1.5;
2010.11		Updated pin statuses at reset and after reset in Table IO_MUX.
2018.10	V2.6	Updated QFN package drawings in Chapter 6: Package Information.
		Added "Cumulative IO output current" entry to Table 11: Absolute Maximum
	V2.5	Ratings;
2018.08		Added more parameters to Table 13: DC Characteristics;
		Changed the power domain names in Table IO_MUX to be consistent with
		the pin names.
		Deleted information on Packet Traffic Arbitration (PTA);
		Added Figure 5: ESP32 Power-up and Reset Timing in Section 2.3: Power
2018.07	V2.4	Scheme;
2010.07	V 2.4	Added the power consumption of dual-core SoCs in Table 6: Power Con-
		sumption by Power Modes;
		Updated section 4.1.2: Analog-to-Digital Converter (ADC).
2018.06	V2.3	Added the power consumption at CPU frequency of 160 MHz in Table 6: Power
2010.00	٧٤.٥	Consumption by Power Modes.

Date	Version	Release notes
2018.05	V2.2	 Changed the voltage range of VDD3P3_RTC from 1.8-3.6V to 2.3-3.6V in Table 1: Pin Description; Updated Section 2.3: Power Scheme; Updated Section 3.1.3: External Flash and SRAM; Updated Table 6: Power Consumption by Power Modes; Deleted content about temperature sensor; Changes to electrical characteristics: Updated Table 11: Absolute Maximum Ratings; Added Table 12: Recommended Operating Conditions; Added Table 13: DC Characteristics; Added Table 14: Reliability Qualifications; Updated the values of "Gain control step" and "Adjacent channel transmit power" in Table 18: Transmitter Characteristics - Basic Data Rate; Updated the values of "Gain control step", "π/4 DQPSK modulation accuracy", "8 DPSK modulation accuracy" and "In-band spurious emissions" in Table 20: Transmitter Characteristics - Enhanced Data Rate; Updated the values of "Gain control step", "Adjacent channel transmit power" in Table 22: Transmitter Characteristics - BLE.
2018.01	V2.1	 Deleted software-specific features; Deleted information on LNA pre-amplifier; Specified the CPU speed and flash speed of ESP32-D2WD; Added notes to Section 2.3: Power Scheme.
2017.12	V2.0	Added a note on the sequence of pin number in Chapter 6.
2017.10	V1.9	 Updated the description of the pin CHIP_PU in Table 1; Added a note to Section 2.3: Power Scheme; Updated the description of the chip's system reset in Section 2.4: Strapping Pins; Added a description of antenna diversity and selection to Section 3.5.1; Deleted "Association sleep pattern" in Table 6 and added notes to Active sleep and Modem-sleep.
2017.08	V1.8	Added Table 4.2 in Section 4;Corrected a typo in Figure 1.

Date	Version	Release notes
2017.08	V1.7	 Changed the transmitting power to +12 dBm; the sensitivity of NZIF receiver to -97 dBm in Section 1.3; Added a note to Table 1 Pin Description; Added 160 MHz clock frequency in section 3.1.1; Changed the transmitting power from 21 dBm to 20.5 dBm in Section 3.5.1; Changed the dynamic control range of class-1, class-2 and class-3 transmit output powers to "up to 24 dBm"; and changed the dynamic range of NZIF receiver sensitivity to "over 97 dB" in Section 3.6.1; Updated Table 6: Power Consumption by Power Modes, and added two notes to it; Updated sections 4.1.1, 4.1.9; Updated Table 11: Absolute Maximum Ratings; Updated Table 15: RF Power Consumption Specifications, and changed the duty cycle on which the transmitters' measurements are based by 50%. Updated Table 16: Wi-Fi Radio Characteristics and added a note on "Output impedance" to it; Updated parameter "Sensitivity" in Table 17, 19, 21; Updated parameters "RF transmit power" and "RF power control range", and added parameter "Gain control step" in Table 18, 20, 22; Deleted Chapters: "Touch Sensor" and "Code Examples"; Added a link to certification download.
2017.06	V1.6	 Corrected two typos: Changed the number of external components to 20 in Section 1.1.2; Changed the number of GPIO pins to 34 in Section 4.1.1.
2017.06	V1.5	 Changed the power supply range in Section: 1.4.1 CPU and Memory; Updated the note in Section 2.3: Power Scheme; Updated Table 11: Absolute Maximum Ratings; Changed the drive strength values of the digital output pins in Note 8, in Table 24: Notes on ESP32 Pin Lists; Added the option to subscribe for notifications of documentation changes.
2017.05	V1.4	 Added a note to the frequency of the external crystal oscillator in Section 1.4.2: Clocks and Timers; Added a note to Section 2.4: Strapping Pins; Updated Section 3.7: RTC and Low-Power Management; Changed the maximum driving capability from 12 mA to 80 mA, in Table 11: Absolute Maximum Ratings; Changed the input impedance value of 50Ω, in Table 16: Wi-Fi Radio Characteristics, to output impedance value of 30+j10 Ω; Added a note to No.8 in Table 24: Notes on ESP32 Pin Lists; Deleted GPIO20 in Table IO_MUX.
2017.04	V1.3	 Added Appendix: ESP32 Pin Lists; Updated Table: Wi-Fi Radio Characteristics; Updated Figure: ESP32 Pin Layout (for QFN 5*5).
2017.03	V1.2	 Added a note to Table: Pin Description; Updated the note in Section: Internal Memory.

Date	Version	Release notes
		Added Chapter: Part Number and Ordering Information;
		Updated Section: MCU and Advanced Features;
		Updated Section: Block Diagram;
		Updated Chapter: Pin Definitions;
2017.02	V1.1	Updated Section: CPU and Memory;
		Updated Section: Audio PLL Clock;
		Updated Section: Absolute Maximum Ratings;
		Updated Chapter: Package Information;
		Updated Chapter: Learning Resources.
2016.08	V1.0	First release.