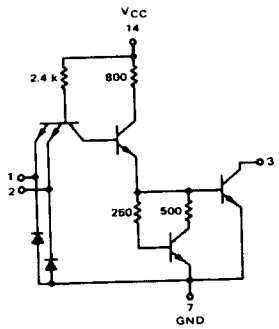
QUAD 2-INPUT "NAND" GATE
(Open Collector)

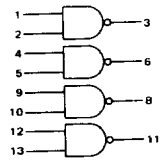
MC3104F • MC3004F
MC3104L • MC3004L,P

(54H01J) (74H01J,N)

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR-function is required or for driving discrete components.



Positive Logic: $3 = \overline{1 \cdot 2}$

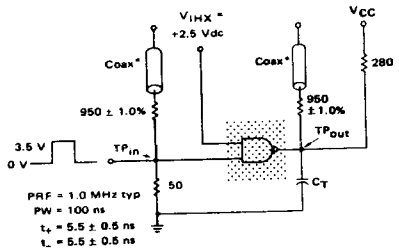
Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 88 mW typ/pkg

Propagation Delay Time = 8.0 ns typ

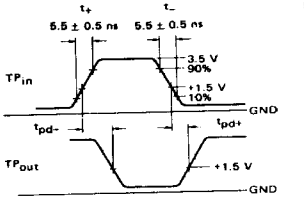
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

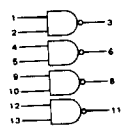
VOLTAGE WAVEFORMS AND DEFINITIONS



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



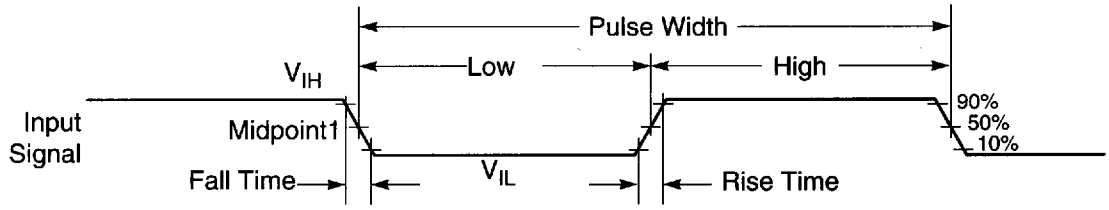
Characteristic	Symbol	Pin Under Test	MC3104 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3004 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_R	V_{IH}	V_F	V_R	V_{BH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{MIX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	2	-	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	6.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	-	7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1	-	-	2	-	3	-	14	-	-	7*
Output Leakage Current	I_{CEX}	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	2	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	25	-	-	-	-	-	25	-	-	mAdc	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	14	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	36	-	36	-	36	-	36	-	36	-	36	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{PDL}	14	-	17.5	-	17.5	-	17.5	-	17.5	-	12	-	17.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Switching Parameters Turn-On Delay	t_{pd-}	1, 3	-	-	-	14	-	-	-	-	-	14	-	-	ns	Pulse In 1	Pulse Out 3	-	-	-	-	-	-	-	-	14	-	-	2	7*
Turn-Off Delay	t_{pd+}	1, 3	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2	7*

@ Test Temperature	TEST CURRENT / VOLTAGE VALUES mA I_{OL}	I_{in}	I_D	Volts V_R	V_{IH}	V_F	V_R	V_{BH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{MIX}
MC3104 −55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
MC3104 +25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5
MC3104 +125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
MC3004 0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-
MC3004 +25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5
MC3004 +75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-

* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference