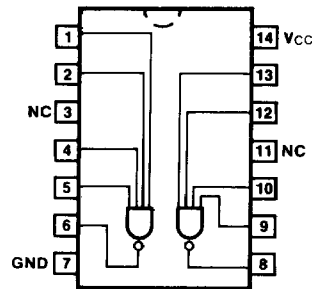


✓ 54/7422 611049
 ✓ 54H/74H22 011051
 ✓ 54S/74S22 011052
 ✓ 54LS/74LS22 611050

DUAL 4-INPUT NAND GATE
(With Open-Collector Output)

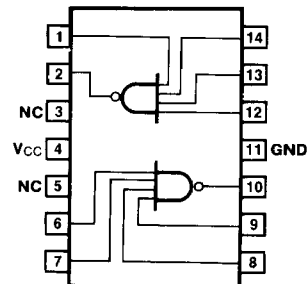
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7422PC, 74H22PC 74S22PC, 74LS22PC		9A
Ceramic DIP (D)	A	7422DC, 74H22DC 74S22DC, 74LS22DC	5422DM, 54H22DM 54S22DM, 54LS22DM	6A
Flatpak (F)	A	7422FC, 74S22FC 74LS22FC	5422FM, 54S22FM 54LS22FM	3I
	B	74H22FC	54H22FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.)	54/74H (U.L.)	54/74S (U.L.)	54/74LS (U.L.)
	HIGH/LOW	HIGH/LOW	HIGH/LOW	HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74	54/74H	54/74S	54/74LS	UNITS	CONDITIONS	
		Min	Max	Min	Max			
I_{CCH}	Power Supply	4.0	5.0	6.6	0.8	mA	$V_{IN} = \text{Gnd}$	$V_{CC} = \text{Max}$
I_{CCL}	Current	11	20	18	2.2			
t_{PLH}	Propagation Delay	45	15	2.0	7.5	ns	Figs. 3-2, 3-4	
t_{PHL}		15	12	2.0	7.0			

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{ V}$.
**OC — Open Collector

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