

# 5.0x7.0mm Surface Mount CMOS Clock Oscillator Series



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## Description

The Connor-Winfield CWX8xx - series is a RoHS compliant 5.0x7.0mm Surface Mount, Fixed Frequency Crystal Controlled Oscillator (XO). Designed for use in applications requiring tight frequency stability and low jitter. The surface mount package is designed for high-density mounting and is optimum for mass production.



## Features

### Model CWX8xx - Series

5.0 x7.0mm Surface Mount Package  
3.3V or 5.0V Operation  
CMOS Output Logic  
Frequency Stabilities Available:  
+/-25ppm or +/-50ppm  
Temperature Range: -20 to 70°C  
Low Jitter <1pS RMS  
Tri-State Enable/Disable  
Tape and Reel Packaging ✓RoHS

## Absolute Maximum Rating

Parameter	Units	Minimum	Nominal	Maximum	Units	Note
Storage Temperature		-55	-	125	°C	
Supply Voltage	(V <sub>cc</sub> =3.3Vdc)	(V <sub>cc</sub> )	-0.5	-	5.0	Vdc
Supply Voltage	(V <sub>cc</sub> =5.0Vdc)	(V <sub>cc</sub> )	-0.5	-	7.0	Vdc
Input Voltage		-0.5	-	V <sub>cc</sub> +0.5	Vdc	

## Operating Specifications

Parameter	Units	Minimum	Nominal	Maximum	Units	Note
Frequency Range	(F <sub>o</sub> )	1.0	-	156.25	MHz	
Total Frequency Tolerance						
Models CWX813-CWX815		-25	-	25	ppm	1
Models CWX823-CWX825		-50	-	50	ppm	1
Operating Temperature Range		-20	-	70	°C	
Supply Voltage	(V <sub>cc</sub> )					
Models CWX813-CWX823		3.135	3.3	3.465	Vdc	
Models CWX815-CWX825		4.5	5.0	5.5	Vdc	
Supply Current	(I <sub>cc</sub> )					
Models CWX813-CWX823 (V <sub>cc</sub> = 3.3Vdc)		-	-	30	mA	
Models CWX815-CWX825 (V <sub>cc</sub> = 5.0Vdc)		-	-	45	mA	

## Input Characteristics

Parameter	Units	Minimum	Nominal	Maximum	Units	Note
Enable Voltage	(High)	(V <sub>ih</sub> )	≥70%V <sub>cc</sub>	-	Vdc	2
Disable Voltage	(Low)	(V <sub>il</sub> )	-	≤30%V <sub>cc</sub>	Vdc	2

## Output Characteristics

Parameter	Units	Minimum	Nominal	Maximum	Units	Note
Load						
Models CWX813-CWX823 (LVCMOS)		-	15	-	pF	
Models CWX815-CWX825 (HCMOS)		-	-	50	pF	
Voltage (High)	(V <sub>oh</sub> )	V <sub>cc</sub> -0.4	-	-	Vdc	
(Low)	(V <sub>ol</sub> )	-	-	0.4	Vdc	
Duty Cycle at 50% of V <sub>cc</sub>		40	50	60	%	
Rise / Fall Time 10% to 90%		-	2	6	ns	
Start-Up Time		-	-	10	ms	
Period Jitter		-	3	5	ps RMS	
Integrated Phase Jitter (BW=12kHz to 20MHz)		-	0.5	1	ps RMS	
SSB Phase Noise at 10Hz offset		-	-60	-	dBc/Hz	
SSB Phase Noise at 100Hz offset		-	-90	-	dBc/Hz	
SSB Phase Noise at 1KHz offset		-	-125	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-140	-	dBc/Hz	
SSB Phase Noise at 100KHz offset		-	-145	-	dBc/Hz	

## Package Characteristics

Package	Hermetically sealed ceramic package
Soldering Process	RoHS compliant, lead free. See solder profile on page 2.

## Notes

- Inclusive of calibration @ 25°C, frequency vs. temperature stability, supply voltage change, load change, shock and vibration, 10 years aging.
- When the oscillator is disabled, the outputs are at high impedance. Output is enabled with no connection on pad 1.



## Ordering Information

<b>CWX</b>	<b>8</b>	<b>1</b>	<b>3</b>	-	<b>16.384M</b>
<b>Type:</b> Clock Series 5x7mm	<b>Temperature Range:</b> 8 = -20 to 70° C	<b>Frequency Stability:</b> 1 = +/-25 ppm 2 = +/-50 ppm	<b>Supply Voltage:</b> 3 = 3.3Vdc. 5 = 5.0Vdc.		<b>Output Frequency:</b> Frequency Format -xxx.xM Min.* -xxx.xxxxxM Max.* *Amount of numbers after the decimal point. M = MHz

Example: CWX813-016.384M = LVCMOS Clock, -20 to 70°C, ±25ppm, 3.3V @ 16.384 MHz

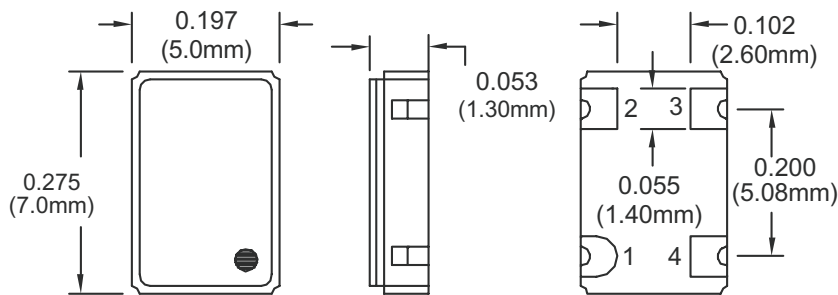
## Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering:	SMD product suitable for Convection Reflow soldering. Peak temperature 260°C. Maximum time above 220°C, 60 seconds.
Solderability	Solderability per Mil Std 883E Method 2003

## Pad Connections and Enable / Disable Function

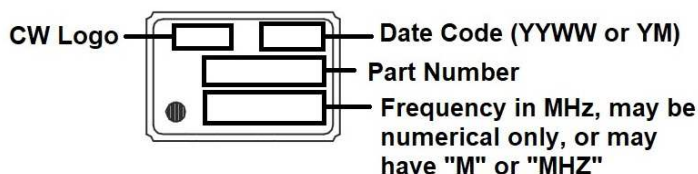
Pad	Connection	Enable / Disable Function (Pad 1)	Output
1	Enable/Disable	High or Open	Enable
2	Ground	Low	Disable (High Impedance)
3	Output		
4	Vcc		

## Package Outline

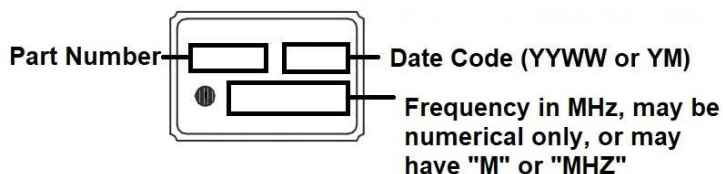


Dimensional Tolerance: ± .008" (±0.2mm)

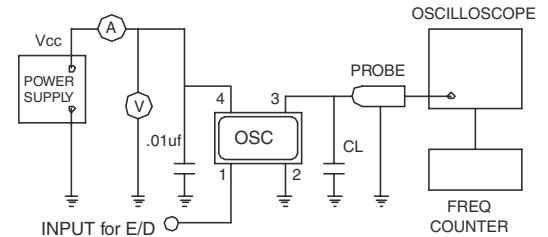
## CWX-Series Marking Configuration



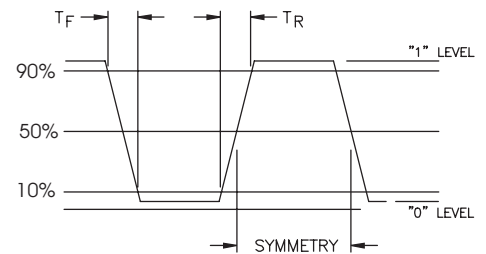
## Alternate Marking Configuration



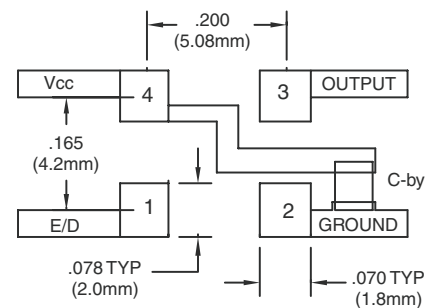
## Test Circuit



## Output Waveform

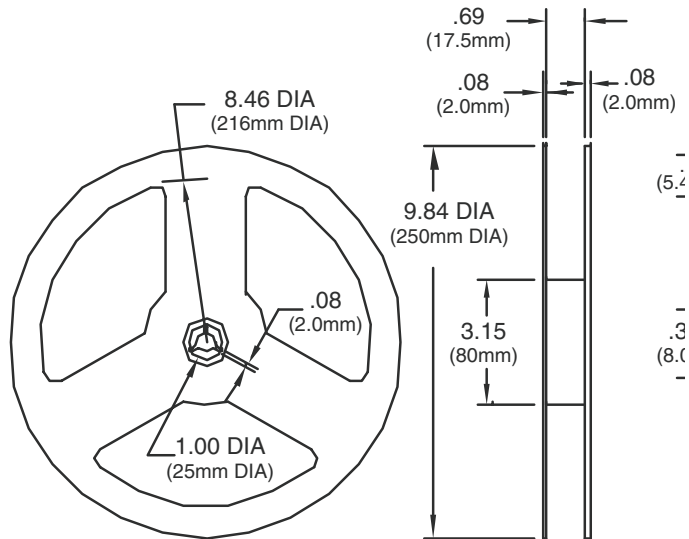


## Suggested Pad Layout



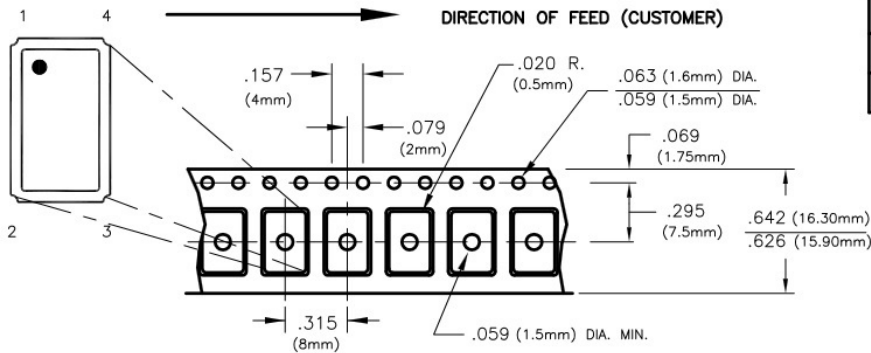
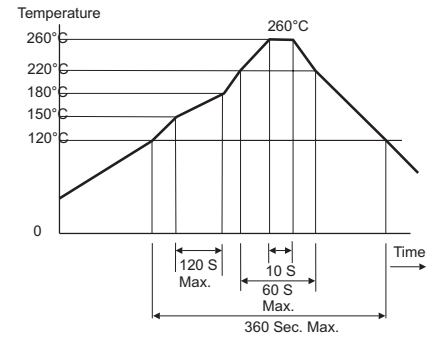
Bypass capacitor, C-by, should be ceramic capacitor ≥.01uF.

## Tape and Reel Dimensions



MEETS EIA-481A and EIAJ-1009B  
2,000 pc/reel Max

## Solder Profile



POCKET SIZE	
(Ao)	5.33mm (.21")
(Bo)	7.87mm (.31")
(Ko)	1.96mm (.077")

16mm (.630") WIDTH  
8mm (.315") PITCH