User's Guide

TPS563201 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS563201 as well as support documentation for the TPS563201EVM-715 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS563201EVM-715.

Table of Contents

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1 Introduction

The TPS563201 is a single, adaptive on-time, D-CAP2™ mode, synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 580 kHz and enters plus skip mode in light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS563201 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS563201 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS563201 dc/dc synchronous converter is designed to provide up to a 3-A output from an input voltage source of 4.5 V to 17 V. The output voltage range is from 0.768V to 7 V. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

The TPS563201EVM-715 evaluation module (EVM) is a single, synchronous buck converter providing 1.05 V at 3 A from 4.5-V to 17-V input. This user's guide describes the TPS563201EVM-715 performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage (V_{IN}) Range	Output Current (I_{OUT}) Range
TPS563201EVM-715	4.5 V to 17 V	0 A to 3 A

2 Performance Specification Summary

A summary of the TPS563201EVM-715 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of 12 V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS563201EVM-715 Performance Specifications Summary

SPECIFICATIONS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5	12	17	V
CH1	Output voltage			1.05		V
	Operating frequency	V_{IN} = 12 V, I_{OUT} = 3 A		580		kHz
	Output current range		0		3	A
	Overcurrent limit	V_{IN} = 12 V, L_{OUT} = 2.2 µH		4.2		A
	Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 3 A		20		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS563201. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.768 V. The value of R1 for a specific output voltage can be calculated using Equation 1.

$$R1 = \frac{R2 \times (V_{OUT} - 0.768\ V)}{0.768\ V} \quad (1)$$

Table 3-1 lists the R5 values for some common output voltages. Note that the values given in Table 3-1 are standard values and not the exact value calculated using Table 3-1.

Table 3-1. TPS563201EVM-715 Output Voltages

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C5 + C6 +C7 (µF)
			MIN	TYP	MAX	
1.0	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	2.2	4.7	20 - 68
3.3	33.2	10.0	2.2	2.2	4.7	20 - 68
5.0	54.9	10.0	3.3	3.3	4.7	20 - 68
6.5	75.0	10.0	3.3	3.3	4.7	20 - 68

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS563201EVM-715. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS563201EVM-715 is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 3 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 1.05 V at 3-A maximum
JP1	EN control. Shunt EN to GND to disable, shunt EN to V_{IN} to enable.
TP1	V_{IN} positive monitor point
TP2	GND monitor test point
TP3	EN test point
TP4	Switch node test point
TP5	Test point for loop response measurements
TP6	V_{OUT} positive monitor point
TP7	GND monitor test point
TP8	GND monitor test point

4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate input voltage to VIN (J1-2) and GND (J1-1).
3. Move the jumper at JP1 (Enable control) from pins 1 and 2 (EN and GND), to pins 2 and 3 (EN and V_{IN}) enabling the output.

4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS563201EVM-715 at an ambient temperature of 25°C.

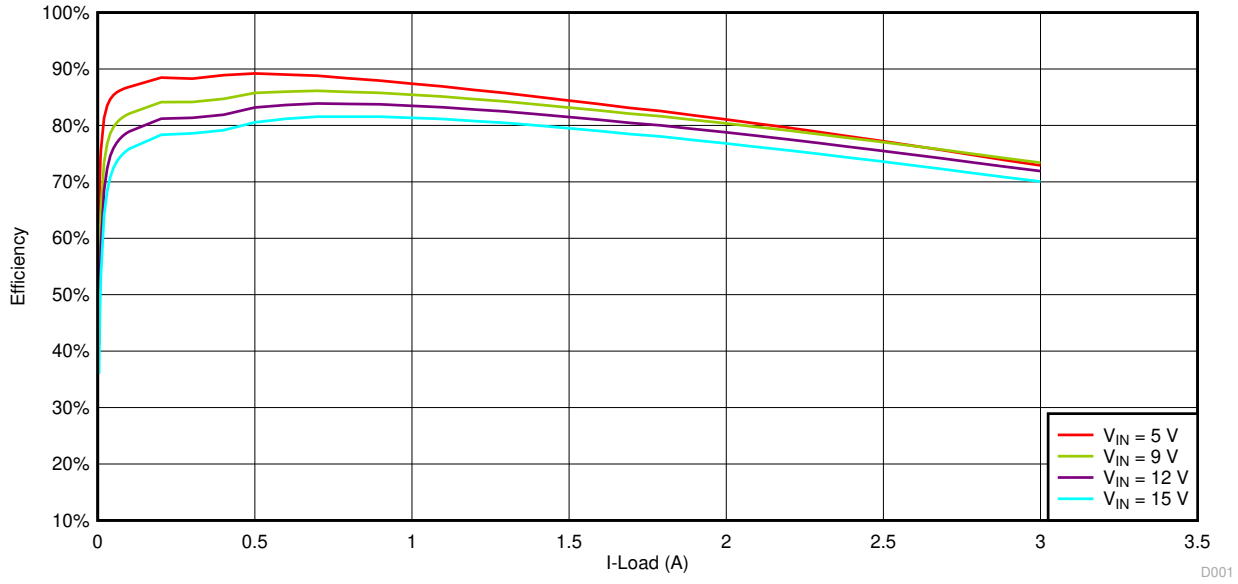

Figure 4-1. Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS563201EVM-715 at an ambient temperature of 25°C.

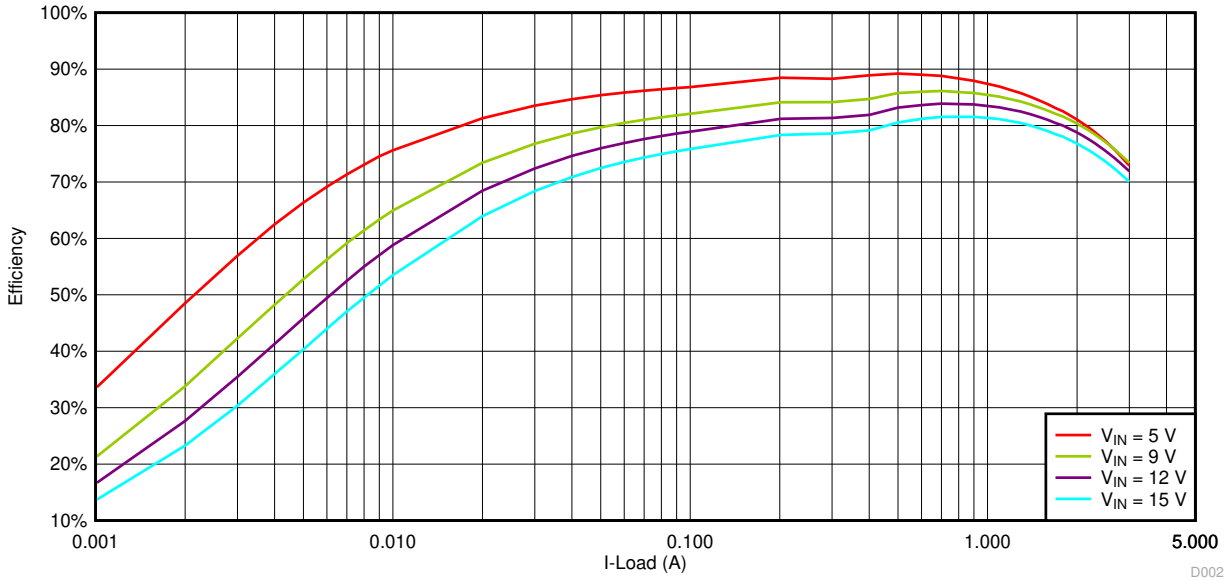

Figure 4-2. Light Load Efficiency

4.4 Load Regulation

The load regulation for the TPS563201EVM-715 is shown in Figure 4-3.

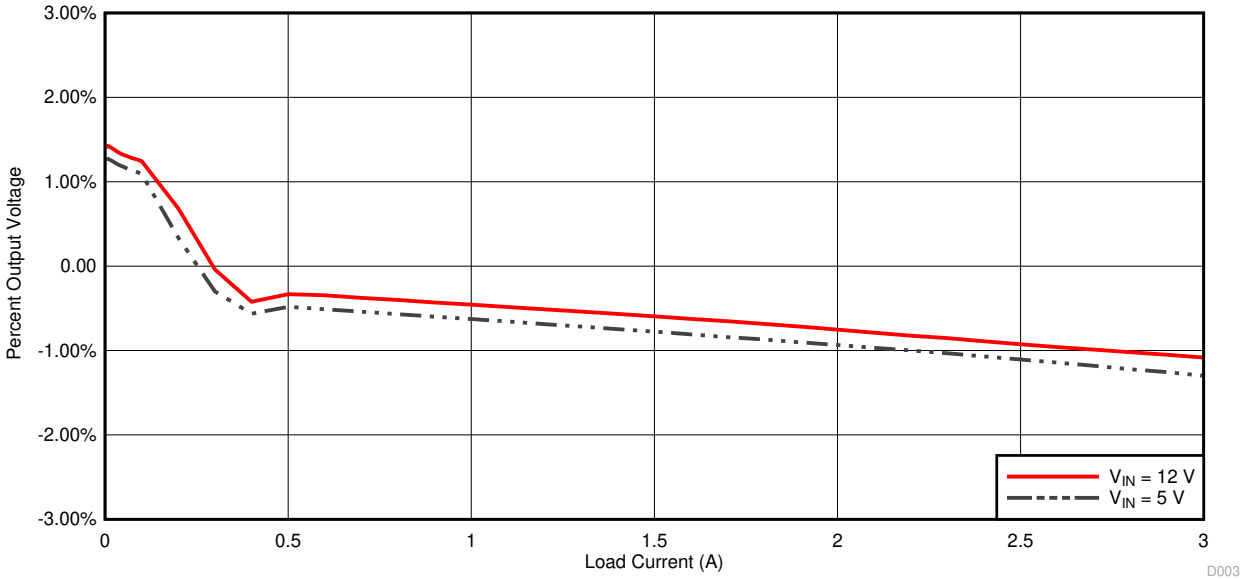

Figure 4-3. Load Regulation

4.5 Line Regulation

The line regulation for the TPS563201EVM-715 is shown in Figure 4-4.

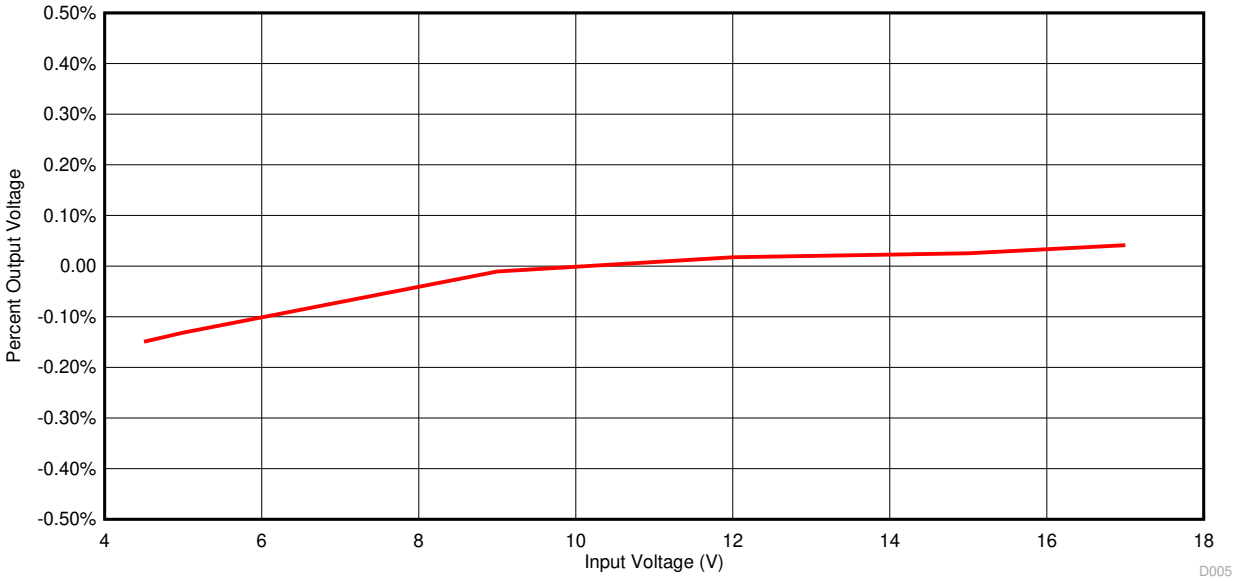

Figure 4-4. Line Regulation

4.6 Load Transient Response

The TPS563201EVM-715 response to load transient is shown in Figure 4-5. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown.

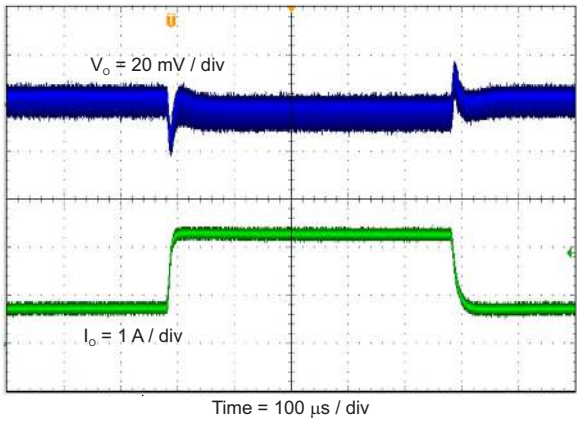

Figure 4-5. Load Transient Response, 25% to 75% Load Step

4.7 Output Voltage Ripple

The TPS563201EVM-715 output voltage ripple is shown in Figure 4-6, Figure 4-7, and Figure 4-8. The output currents are as indicated.

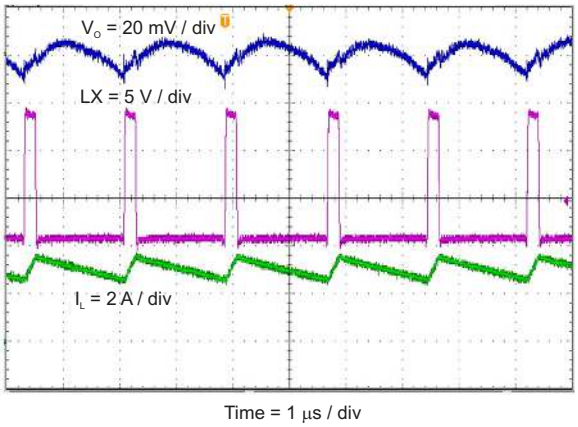

Figure 4-6. Output Voltage Ripple, I_{OUT} = 3 A

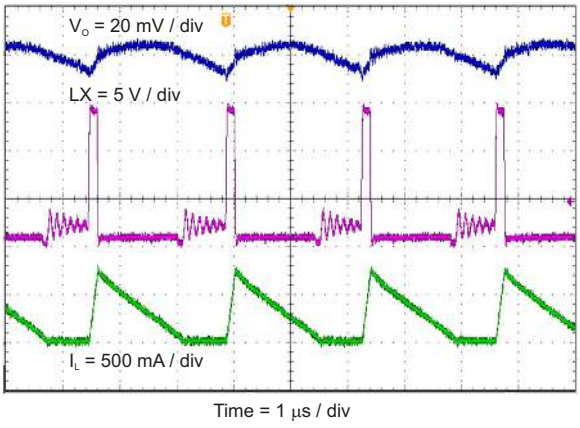

Figure 4-7. Output Voltage Ripple, I_{OUT} = 250 mA

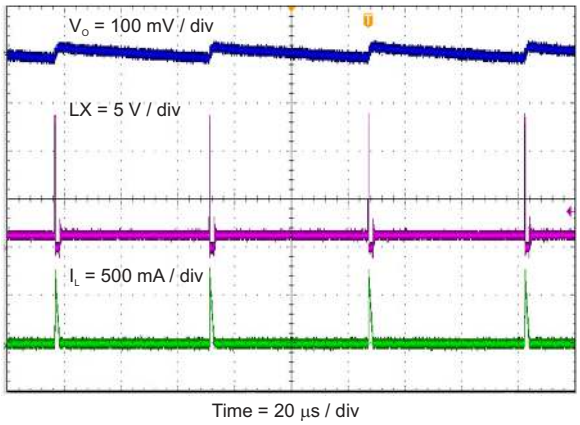

Figure 4-8. Output Voltage Ripple, I_{OUT} = 10 mA

4.8 Input Voltage Ripple

The TPS563201EVM-715 input voltage ripple is shown in Figure 4-9. The output current is as indicated.

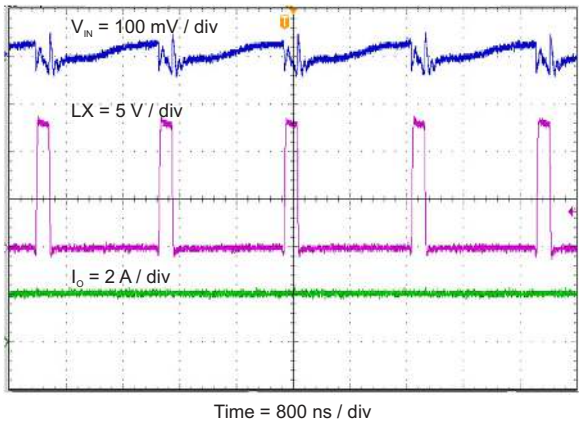

Figure 4-9. Input Voltage Ripple, I_{OUT} = 3 A

4.9 Start-Up

The TPS563201EVM-715 start-up waveform relative to V_{IN} is shown in Figure 4-10. Load = 1 Ω resistive.

The TPS563201EVM-715 start-up waveform relative to enable (EN) is shown in Figure 4-11. Load = 1 Ω resistive.

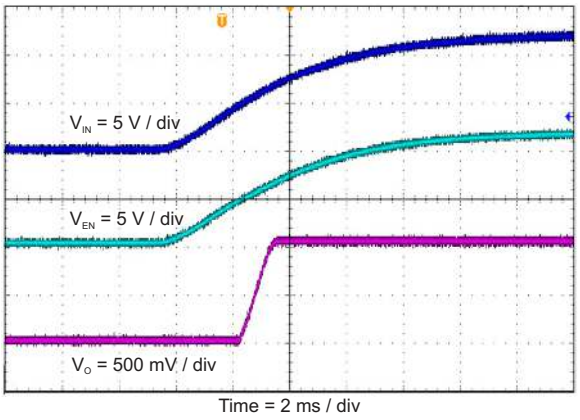

Figure 4-10. Start-Up Relative to V_{IN}

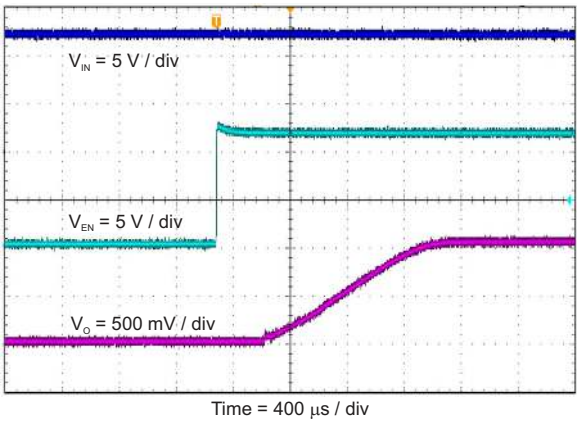

Figure 4-11. Start-Up Relative to EN

4.10 Shut-Down

The TPS563201EVM-715 shut-down waveform relative to V_{IN} is shown in Figure 4-12. Load = 1 Ω resistive.

The TPS563201EVM-715 shut-down waveform relative to EN is shown in Figure 4-13. Load = 1 Ω resistive.

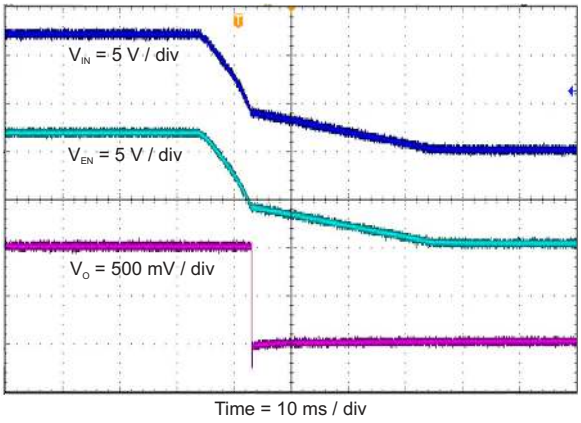

Figure 4-12. Shut-Down Relative to V_{IN}

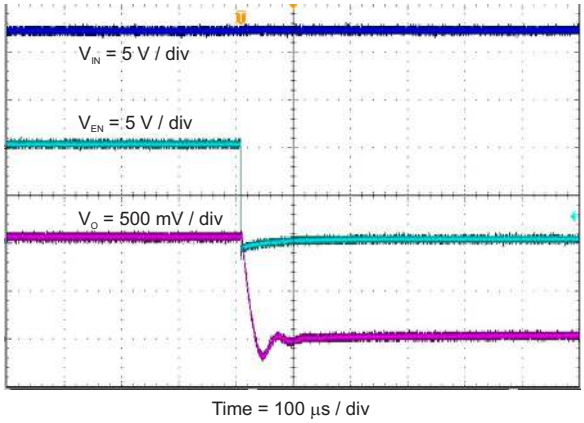

Figure 4-13. Shut-Down Relative to EN

5 Board Layout

This section provides a description of the TPS563201EVM-715, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS563201EVM-715 is shown in Figure 5-1, Figure 5-2 and Figure 5-3. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS563201 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, and C3 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill and the feed back trace from the point of regulation to the top of the resistor divider network.

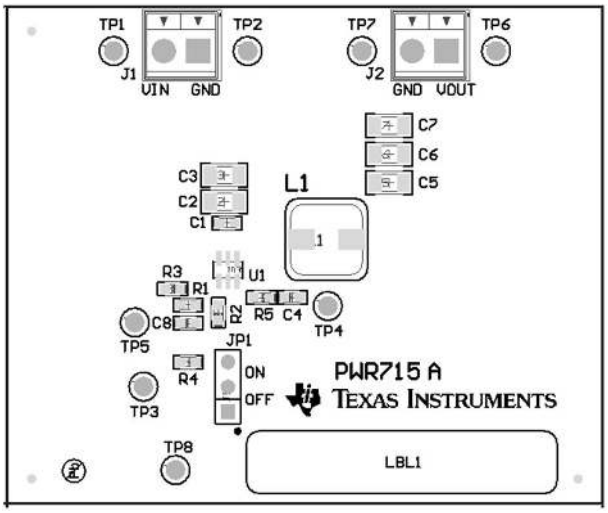

Figure 5-1. Top Assembly

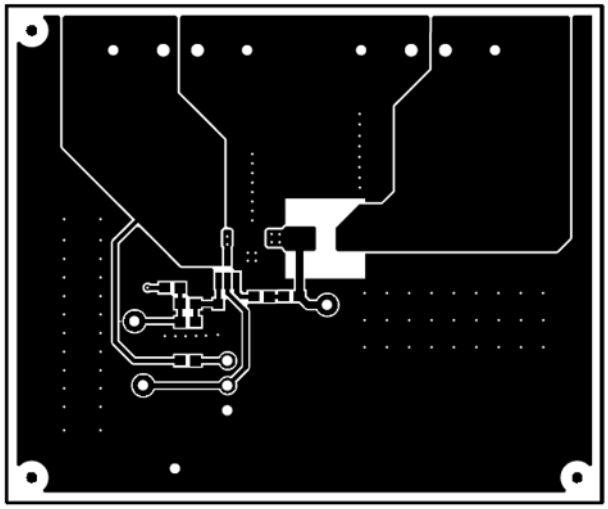

Figure 5-2. Top Layer

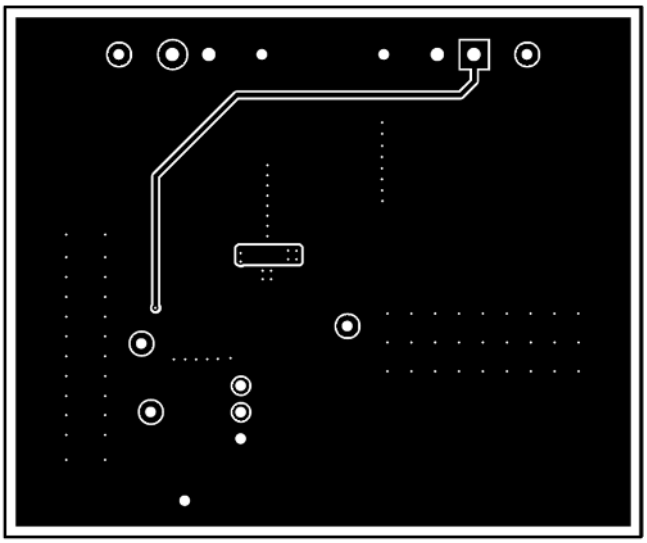

Figure 5-3. Bottom Layer

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS563201EVM-715.

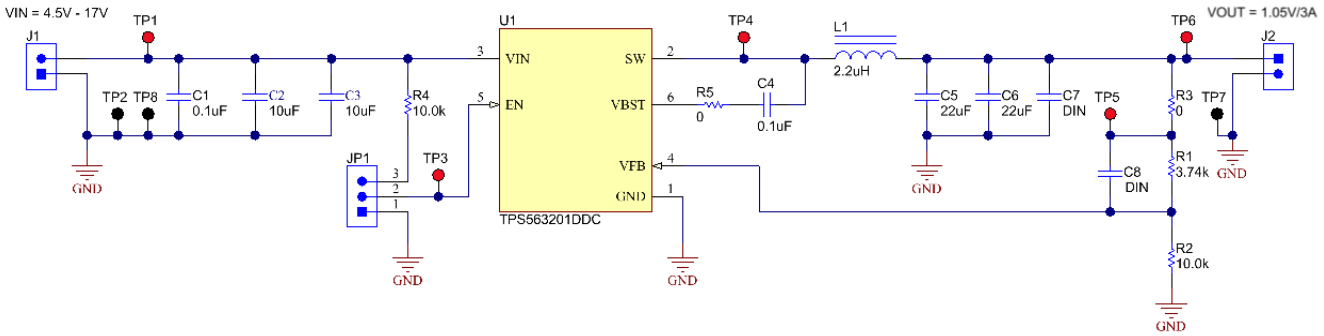

Figure 6-1. TPS563201EVM-715 Schematic Diagram

6.2 Bill of Materials

Table 6-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PWR715	Any
C1, C4	2	0.1 µF	Capacitor, ceramic, 0.1µF, 25 V, ±10%, X5R, 0603	0603	GRM188R61E104KA01D	Murata
C2, C3	2	10 µF	Capacitor, ceramic, 10µF, 25 V, ±10%, X5R, 1206	1206	GRM31CR61E106KA12L	Murata
C5, C6	2	22 µF	Capacitor, ceramic, 22µF, 10 V, ±10%, X7R, 1206	1206	GRM31CR71A226KE15L	Murata
C8	0	10 pF	Capacitor, ceramic, 10 pF, 100 V, ±5%, C0G/NP0, 0603	0603	GRM1885C2A100JA01D	Murata
J1, J2	2		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
JP1	1		Header, 100 mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
L1	1	2.2 µH	Inductor, Shielded Drum Core, Superflux, 2.2 µH, 9 A, 0.0115 Ω, SMD	WE-HC4	744311220	Wurth Elektronik eiSos
LBL1	1		Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R1	1	3.74 kΩ	Resistor, 3.74 kΩ, 1%, 0.1 W, 0603	0603	CRCW06033K74FKEA	Vishay-Dale
R2, R4	2	10.0 kΩ	Resistor, 10.0 kΩ, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R3, R5	2	0	Resistor, 0 Ω, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic
SH-JP1	1	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP3, TP4, TP5, TP6	5	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP2, TP7, TP8	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U1	1		4.5 V to 17 V Input, 3-A Synchronous Step-Down Voltage Regulator	DDC0006A	TPS563201DDC	Texas Instruments
C8	0	10 pF	Capacitor, ceramic, 10 pF, 100 V, ± 5%, C0G/NP0, 0603	0603	GRM1885C2A100JA01D	Murata
C7	0	22 µF	Capacitor, ceramic, 22µF, 10 V, ±10%, X7R, 1206	1206	GRM31CR71A226KE15L	Murata

6.3 Reference

1. *TPS56320x 4.5 V to 17 V Input, 3-A Synchronous Step-Down Voltage Regulator in SOT-23* data sheet (SLVSD90)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2015) to Revision A (July 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated user's guide title	2

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