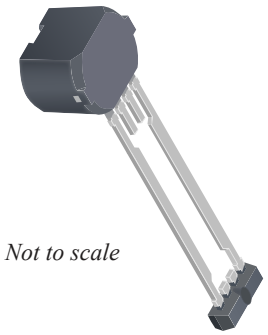
ATS685LSH

Two-Wire, Zero Speed, Differential Gear Tooth Sensor IC

FEATURES AND BENEFITS

- Fully optimized differential digital gear tooth sensor IC
- Running mode lockout
- Unique algorithms for increased vibration immunity
- AGC and reference adjust circuit
- Air gap independent switch points
- Digital output representing gear profile
- Precise duty cycle throughout operating temperature range
- Large operating air gap range
- Short power-on time
- True zero-speed operation
- Undervoltage lockout (UVLO)
- Wide operating voltage range
- Internal current regulator for two-wire operation
- Single-chip sensing IC for high reliability
- Robust test coverage capability using Scan Path and IDDQ measurement

PACKAGE: 4-pin SIP (suffix SH)



Not to scale

DESCRIPTION

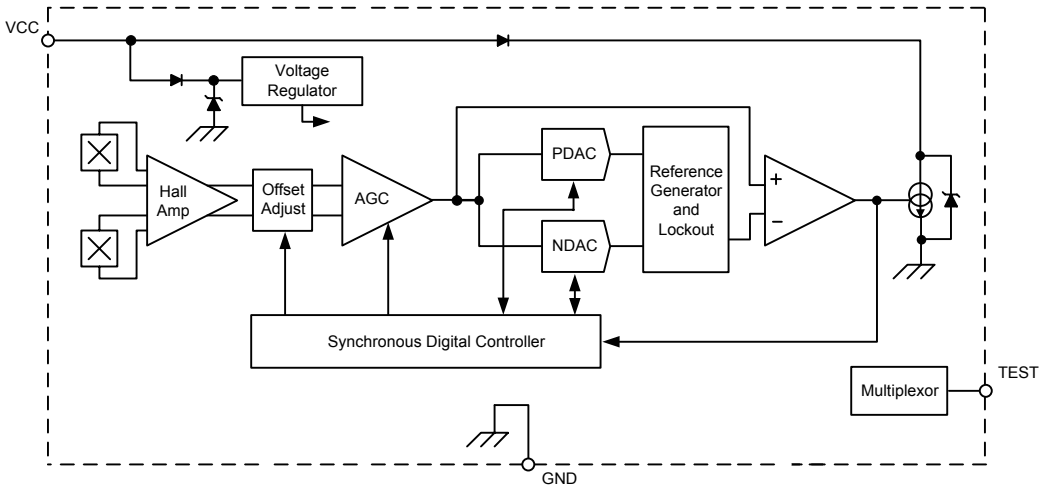
The ATS685LSH is an optimized Hall-effect sensing integrated circuit and rare-earth pellet combination that provides a user-friendly solution for true zero-speed digital gear-tooth sensing in two-wire applications. The sensor IC consists of a single-shot molded plastic package that includes a samarium-cobalt pellet, a pole piece, and a Hall-effect IC that has been optimized to the magnetic circuit. This small package can be easily assembled and used in conjunction with a wide variety of gear shapes and sizes.

The single integrated circuit incorporates a dual element Hall-effect sensor IC and signal processing circuitry that switches in response to differential magnetic signals created by ferromagnetic targets. The device contains a sophisticated compensating circuit to eliminate magnetic and system offsets. Digital tracking of the analog signal is used to achieve true zero speed operation. Advanced calibration algorithms are used to adjust the device gain and offset at power-up, resulting in air gap independent switch points, which greatly improves output accuracy. In addition, advanced algorithms mitigate the effect of system anomalies such as target vibration and sudden changes in air gap.

The regulated current output is configured for two-wire operation. This sensor IC is ideal for obtaining edge and duty cycle information in gear-tooth–based applications such as transmission speed.

The ATS685 is provided in a 4-pin SIP package that is lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

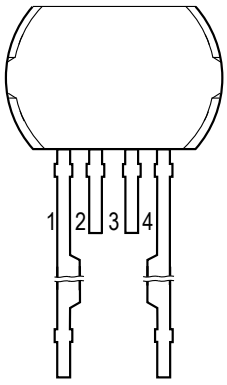
Part Number	Packing*
ATS685LSHTN-T	13-in. reel, 800 pieces per reel

*Contact Allegro™ for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	Range L, refer to Power Derating Curve	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Supply voltage
2	NC	No connection (float or tie to GND)
3	TEST	Test (float or tie to GND)
4	GND	Ground

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OPERATING CHARACTERISTICS V_{CC} and T_A within specification, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit[2]
Electrical Characteristics						
Supply Voltage[3]	V_{CC}	Operating, $T_J < T_J(max)$, I_{CC} within specification	4.0	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 → 5 V or 5 → 0 V	–	3.5	3.95	V
Reverse Supply Current[4]	I_{RCC}	V_{CC} = –18 V	–	–	–10	mA
Supply Zener Clamp Voltage	V_Z	$I_{CC} = I_{CC}(max) + 3$ mA, T_A = 25°C	28	–	–	V
Supply Zener Current	I_Z	T_A = 25°C, V_{CC} = 28 V	–	–	19	mA
Supply Current	$I_{CC(Low)}$	Low-current state	4	6	8	mA
	$I_{CC(High)}$	High-current state	12	14	16	mA
Supply Current Ratio	$I_{CC(High)} / I_{CC(Low)}$	Ratio of high current to low current	1.85	–	3.05	–
Test Pin Zener Clamp Voltage[5]	V_{ZTEST}		–	6	–	V
Power-On State Characteristics						
Power-On Time[6]	t_{PO}	$V_{CC} > V_{CC}(min)$, f_{OP} < 100 Hz	–	1	2	ms
Power-On State[7]	POS	$t > t_{PO}$	–	$I_{CC(High)}$	–	A
Output Stage						
Output Slew Rate[8,9]	di/dt	$\Delta i/\Delta t$ from 90% to 10% I_{CC} level R_{SENSE} = 100 Ω, C_{LOAD} = 10 pF, no C_{BYPASS}	7	14	–	mA/µs
Performance Characteristics						
Operating Frequency	f_{OP}		0	–	12	kHz
Analog Signal Bandwidth	BW		16	20	–	kHz
Operate Point	B_{OP}	% of peak-to-peak B_{SIG}, AG_{OP} within specification	–	70	–	%
Release Point	B_{RP}	% of peak-to-peak B_{SIG}, AG_{OP} within specification	–	30	–	%
Running Mode Lockout Enable Threshold	$V_{LOE(RM)}$	At peak-to-peak $V_{PROC} < V_{LOE(RM)}$, output switching disables	–	170	–	mV
Running Mode Lockout Release Threshold	$V_{LOR(RM)}$	At peak-to-peak $V_{PROC} > V_{LOR(RM)}$, output switching enables	–	200	–	mV
Calibration						
Start Mode Hysteresis	PO_{HYS}		–	$V_{LOR(RM)}$	–	mV
Initial Calibration[10]	CAL_I	Rising output (current) edges, f_{OP} < 200 Hz	–	–	3	edges

Continued on the next page…

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OPERATING CHARACTERISTICS (continued) V_{CC} and T_A within specification, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit[2]
Functional Characteristics						
Operating Signal Range[11]	B_{SIG}	Differential magnetic signal, duty cycle within specification	50	–	1500	G_{PK-PK}
Extended Operating Signal Range	B_{SIGEXT}	Differential magnetic signal, output switching (no missed edges), duty cycle not guaranteed	30	–	–	G_{PK-PK}
Operational Air Gap Range	AG_{OP}	Using Allegro Reference Target 60-0, duty cycle within specification	0.5	–	2.5	mm
Extended Operational Air Gap Range	AG_{EXT}	Using Allegro Reference Target 60-0, output switching (no missed edges), duty cycle not guaranteed	–	–	3.0	mm
Allowable User-Induced Differential Offset	$B_{DIFFEXT}$	Operation within specification	±60	–	–	G
Duty Cycle Variation[12]	ΔD	Wobble < 0.5 mm, AG within specification	–	–	±10	%
Maximum Sudden Signal Amplitude Change	$B_{SIG(INST)}$	Instantaneous symmetric magnetic signal amplitude change, measured as a percentage of peak-to-peak B_{SIG}, f_{OP} < 500 Hz	–	45	–	%

[1]Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]1 G (gauss) = 0.1 mT (millitesla).
[3]Maximum voltage must be adjusted for power dissipation and junction temperature; see Power Derating section.
[4]Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[5]Sustained voltages beyond the clamp voltage may cause permanent damage to the IC.
[6]Measured from $V_{CC} \geq V_{CC}$(min) to the time when the device is able to switch the output signal in response to a magnetic stimulus.
[7]Please refer to the Functional Description, Power-On section.
[8]di is the difference between 10% of $I_{CC(Low)}$ and 90% of $I_{CC(High)}$. dt is the time period between those two points.
[9]C_{LOAD} is the probe capacitance of the oscilloscope used to make the measurement.
[10]For power-on frequency, f_{OP} < 200 Hz. Higher power-on frequencies may result in more input magnetic cycles until full output edge accuracy is achieved, including the possibility of missed output edges.
[11]AG_{OP} is dependent on the available magnetic field. The available field is dependent on target geometry and material and should be independently characterized. The field available from the reference target is given in the Reference Target table.
[12]Target rotation from pin 4 to pin 1.

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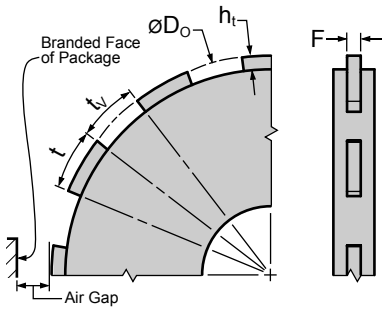
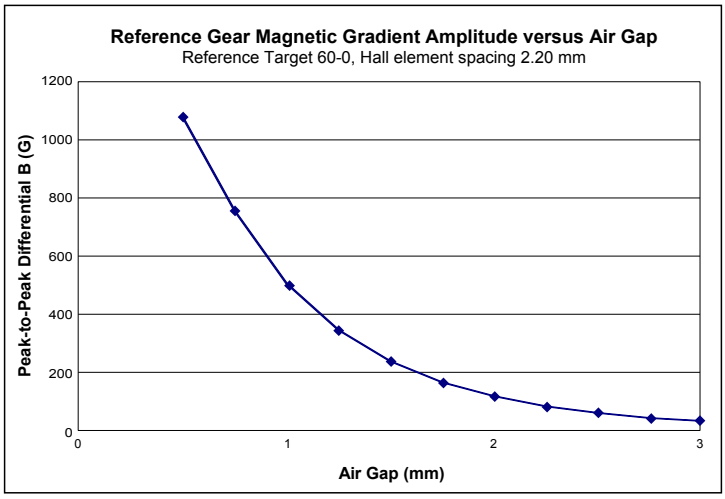
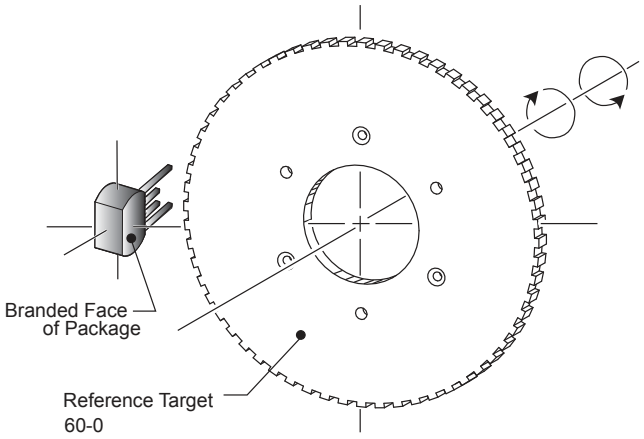
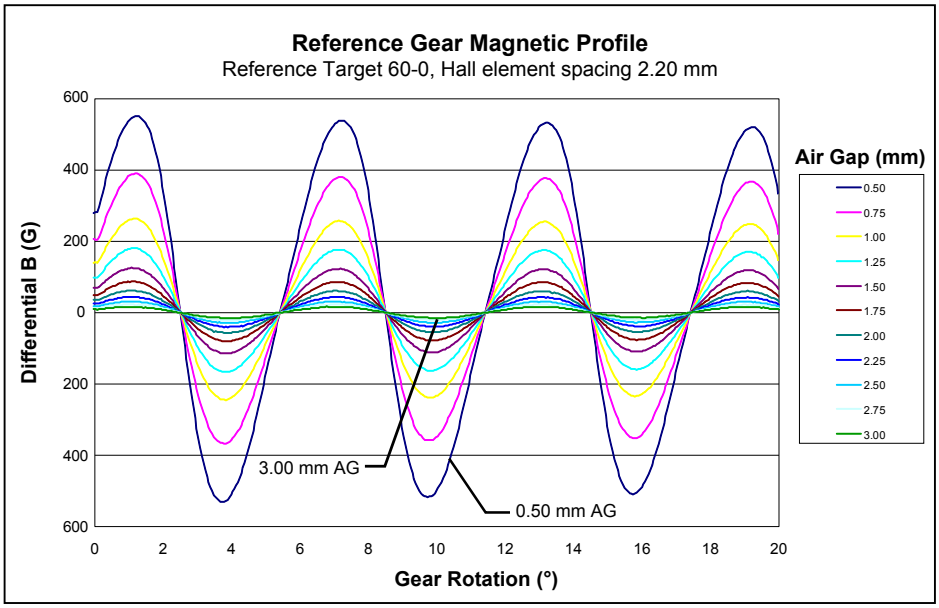
Reference Target 60-0 (60 Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Angular Tooth Thickness	t	Length of tooth, with respect to branded face	3	deg.	
Angular Valley Thickness	t_v	Length of valley, with respect to branded face	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	







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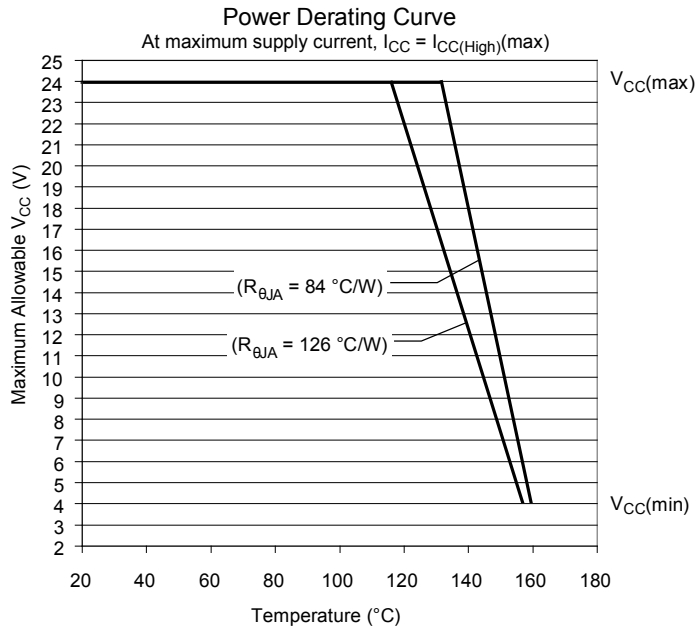
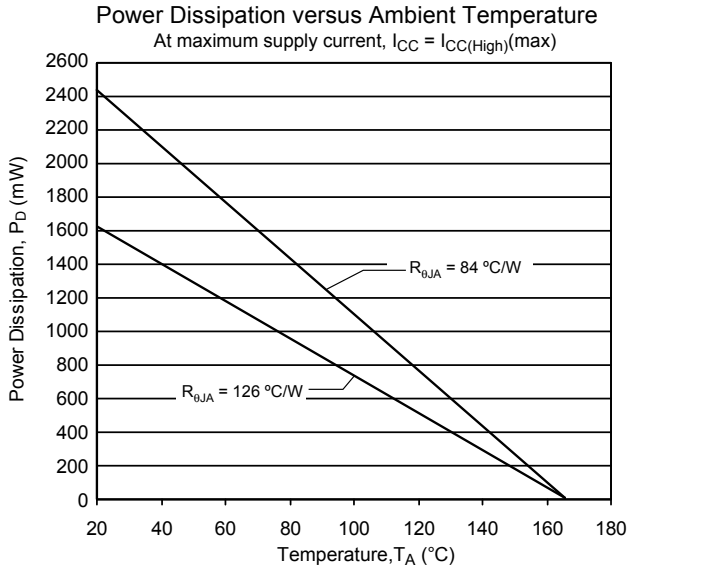
Thermal Characteristics may require derating at maximum conditions, see Power Derating section

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single layer PCB, with copper limited to solder pads	126	°C/W
		Single layer PCB, with copper limited to solder pads and 3.57 in.^{2} (23.03 cm^2) copper area each side	84	°C/W

*Additional thermal information available on the Allegro website





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Functional Description

Sensing Technology

The ATS685 sensor IC contains a single-chip differential Hall-effect circuit, a samarium cobalt pellet, and a flat ferrous pole piece (a precisely mounted magnetic field concentrator that homogenizes the flux passing through the Hall chip). As shown in figure 1, the circuit supports two Hall elements, which sense the magnetic profile of the ferromagnetic gear target simultaneously, but at different points (spaced at a 2.2 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

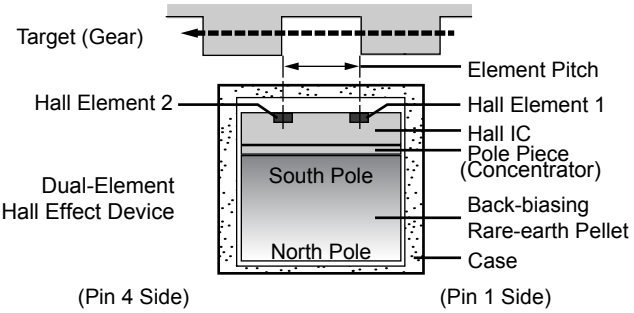

Figure 1. Relative motion of the target is detected by the dual Hall elements mounted on the Hall IC.

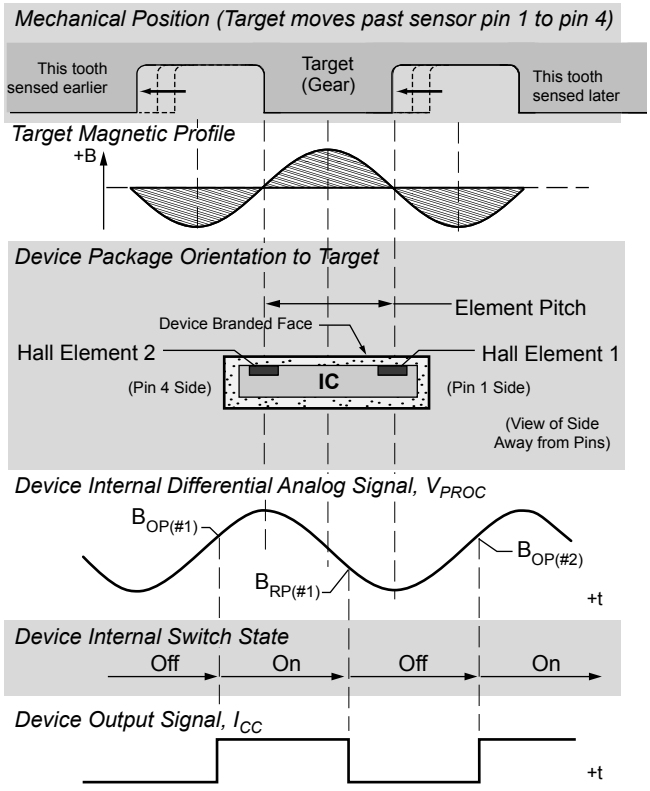

Figure 2. The magnetic profile reflects the geometry of the target, allowing the ATS685 to present an accurate digital output response.

Sensing Technology (continued)

The Hall IC is self-calibrating and integrates a temperature compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset rejection circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling During Operation

Under normal operating conditions, the IC is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in figure 2 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the ATS685. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

Diagnostics

The regulated current output is configured for two-wire applications, requiring one less wire for operation than do switches with the traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges, shown in figure 3 as $I_{CC(HIGH)}$ and $I_{CC(LOW)}$. Any current level not within these ranges indicates a fault condition. If $I_{CC} > I_{CC(HIGH)}$(max), then a short condition exists, and if $I_{CC} < I_{CC(LOW)}$(min), then an open condition exists. Any value of I_{CC} between the allowed ranges for $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ indicates a general fault condition.

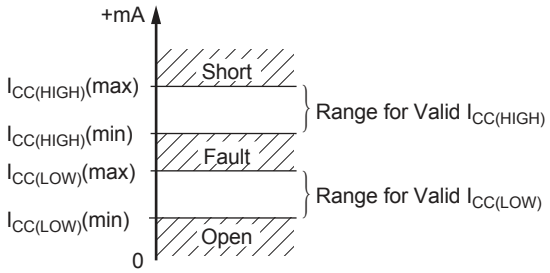

Figure 3. Diagnostic characteristics of supply current values.

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Determining Output Signal Polarity

In figure 2, the top panel, labeled *Mechanical Position*, represents the mechanical features of the target gear and orientation to the device. The bottom panel, labeled *Device Output Signal*, displays the square waveform corresponding to the digital output signal (current amplitude) that results from a rotating gear configured as shown in figure 3. Referring to the target side nearest the face of the sensor IC, the direction of rotation is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side.

In order to read the output signal as a voltage, V_{SENSE}, a sense resistor, R_{SENSE}, can be placed on either the VCC signal or on the GND signal. As shown in figure 4, when R_{SENSE} is placed on the GND signal, the output signal voltage, $V_{SENSE(LowSide)}$, is in phase with I_{CC}. When R_{SENSE} is placed on the VCC signal, the output signal voltage, $V_{SENSE(HighSide)}$, is inverted relative to I_{CC}.

Output Polarity States

R_{SENSE} Location	I_{CC} State	V_{SENSE} State
High side (VCC pin side)	High	Low
	Low	High
Low side (GND pin side)	High	High
	Low	Low

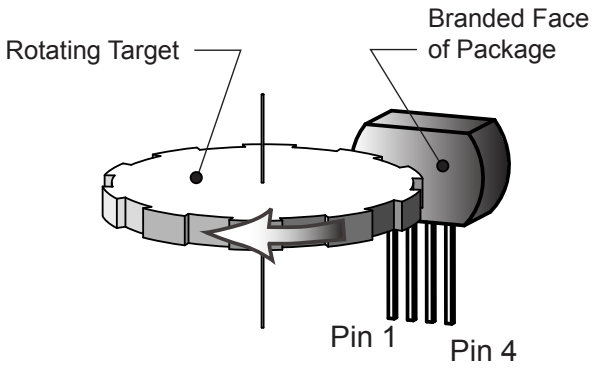

Figure 3. This figure depicts left-to-right (pin 1 to pin 4) direction of target rotation.

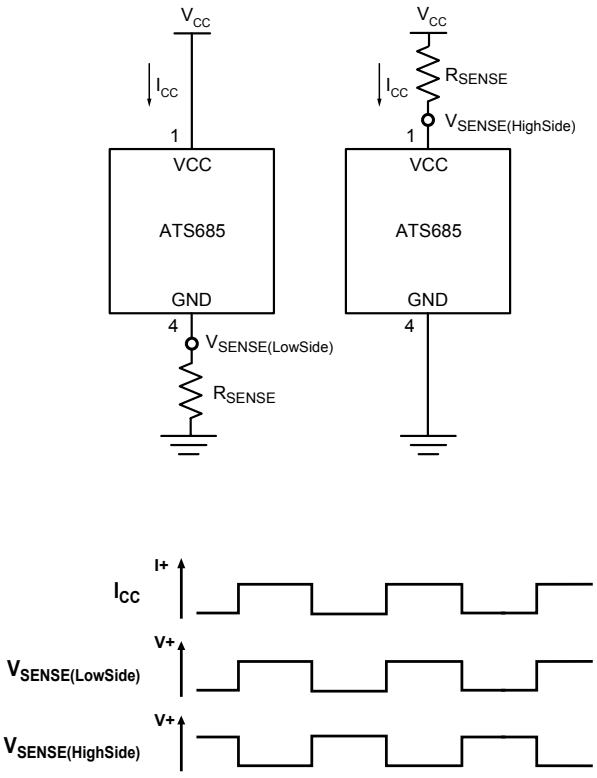

Figure 4. Alternative Polarity Configurations Using Two-Wire Sensing. The Output Polarity States table provides the permutations of output voltage relative to I_{CC}, given alternative locations for R_{SENSE}. Panel A shows the low-side, $V_{SENSE(LowSide)}$, sensing configuration, and panel B shows the high-side, $V_{SENSE(HighSide)}$, configuration. As shown in panel C, $V_{SENSE(LowSide)}$ is in phase with I_{CC}, and $V_{SENSE(HighSide)}$, is inverted.

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Continuous Update of Switch Points

Switch points are the threshold levels of the differential internal analog signal, V_{PROC}, at which the device changes output signal state. The value of V_{PROC} is directly proportional to the magnetic flux density, B, induced by the target and sensed by the Hall elements. As V_{PROC} rises through a certain limit, referred to as the *operate point*, B_{OP}, the output state changes from high to low. As V_{PROC} falls below B_{OP} to a certain limit, the *release point*, B_{RP}, the output state changes from low to high.

As shown in figure 5, threshold levels for the switch points are established as a function of the peak input signal levels. The device incorporates an algorithm that continuously monitors the input signal and updates the switching thresholds accordingly with limited inward movement of V_{PROC}. The switch point for each edge is determined by the detection of the previous two signal edges. In this manner, variations are tracked in real time.

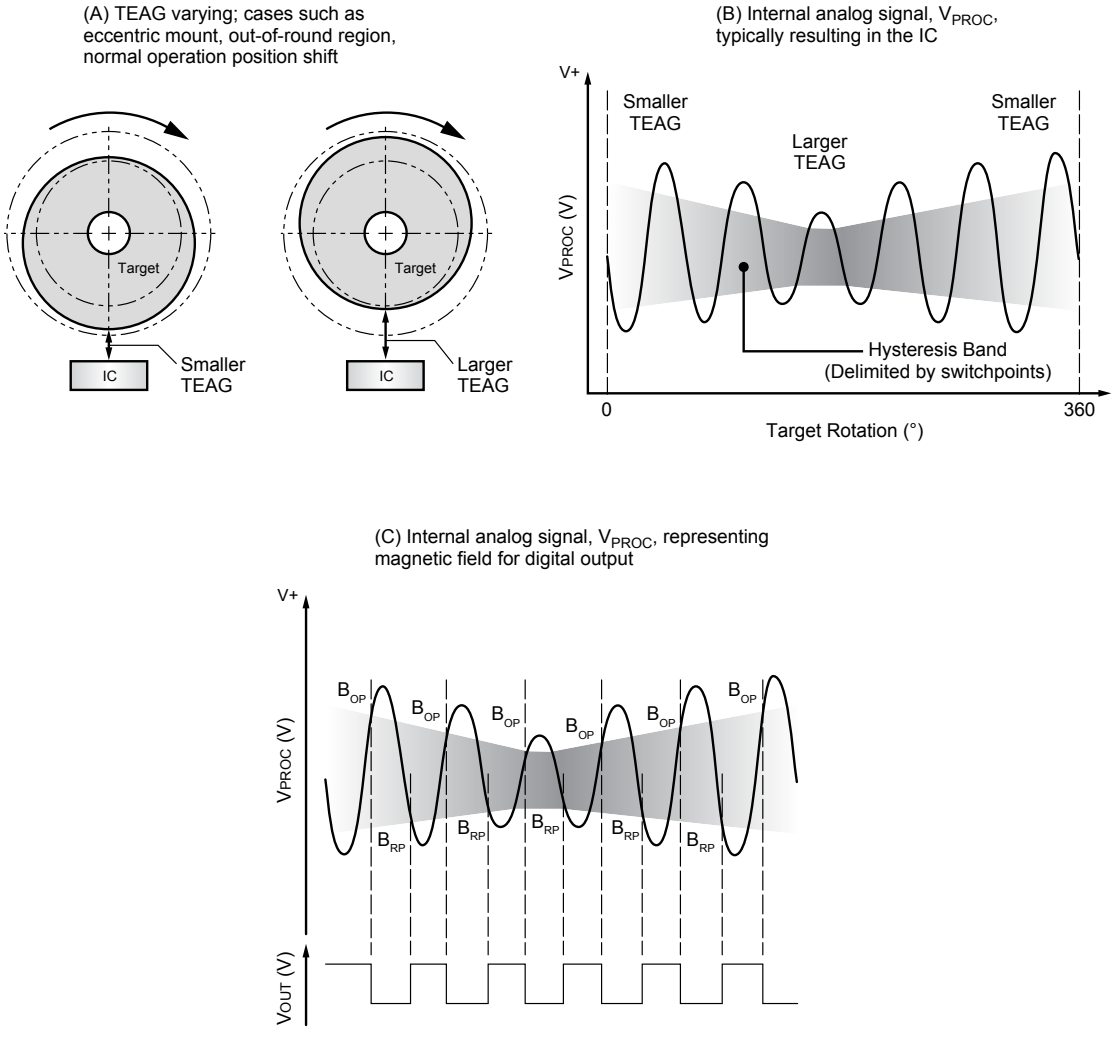

Figure 5. The Continuous Update algorithm allows the Allegro IC to interpret and adapt to variances in the magnetic field generated by the target as a result of eccentric mounting of the target, out-of-round target shape, and similar dynamic application problems that affect the TEAG (Total Effective Air Gap). As shown in panel A, the variance in the target position results in a change in the TEAG. This affects the IC as a varying magnetic field, which results in proportional changes in the internal analog signal, V_{PROC}, shown in panel B. The Continuous Update algorithm is used to establish switch points based on the fluctuation of V_{PROC}, as shown in panel C.

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Power-On

The ATS685 is guaranteed to power-on in the high current state, $I_{CC(High)}$. When power ($V_{CC} > V_{CC}$ (min)) is applied to the device, a short period of time is required to power the various portions of the circuit. During this period, the ATS685 will power-on in the high current state, $I_{CC(High)}$.

Initial Edge Detection

The device self-calibrates using the initial teeth sensed, and then enters running mode. This results in reduced accuracy for a brief period, CAL_I. However, this period allows the device to optimize for running mode operation. As shown in figure 6, the first three high peak signals corresponding to rising output edges are used to calibrate AGC (Automatic Gain Control). There is a slight variance in the duration of initialization, depending on what target feature is opposite the sensor IC when power-on occurs. Also, a high speed of target rotation at power-on may increase the quantity required in the CAL_I period.

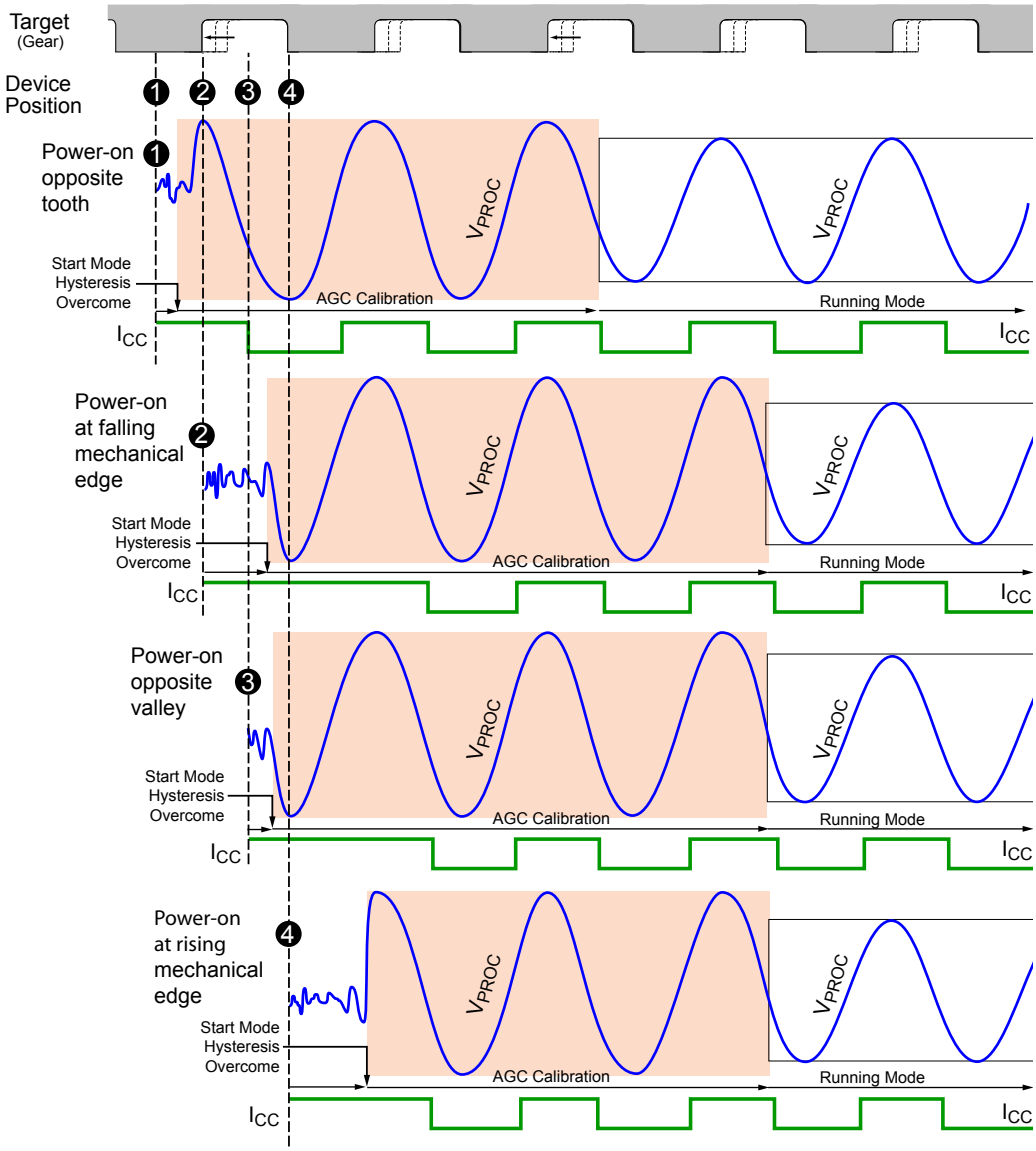

Figure 6. Power-On Initial Edge Detection. This figure demonstrates four typical power-on scenarios. All these examples assume that the target is moving relative to the sensor IC in the direction indicated (from pin 1 to pin 4) and the voltage output is configured for low-side sensing, $V_{OUT(Low)}$. The length of time required to overcome Start Mode Hysteresis, as well as the combined effect of whether it is overcome in a positive or negative direction plus whether the next edge is in that same or opposite polarity, affect the point in time when AGC calibration begins. Three high peaks are always required for AGC calibration when $f_{OP} \leq 200$ Hz, and more may be required at greater speeds.

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Start Mode Hysteresis

This feature helps to ensure optimal self-calibration by rejecting electrical noise and low-amplitude target vibration during initialization. This prevents AGC from calibrating the device on such spurious signals. Calibration can be performed using the actual target features.

A typical scenario is shown in figure 7. The hysteresis, PO_{HYS}, is a minimum level of the peak-to-peak amplitude of the internal analog electrical signal, V_{PROC}, that must be exceeded before the ATS685 starts to compute switch points.

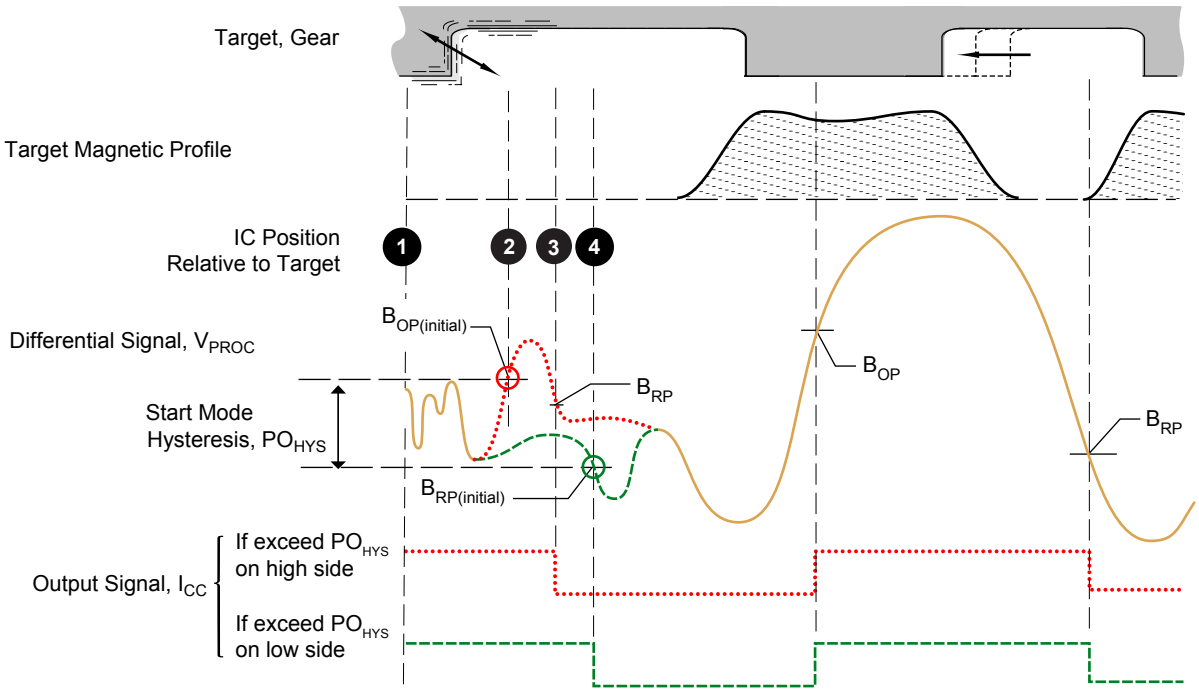

Figure 7. Operation of Start Mode Hysteresis

- At power-on (position 1), the ATS685 begins sampling V_{PROC}.
- At the point where the Start Mode Hysteresis, PO_{HYS}, is exceeded, the device establishes an initial switching threshold, by using the Continuous Update algorithm. If V_{PROC} is rising through the limit on the high side (position 2), the switch point is B_{OP}, and if V_{PROC} is falling through the limit on the low side (position 4), it is B_{RP}. After this point, Start Mode Hysteresis is no longer a consideration. Note that a valid V_{PROC} value exceeding the Start Mode Hysteresis can be generated either by a legitimate target feature or by excessive vibration.
- In either case (B_{OP} or B_{RP}), because the switch point is immediately passed as soon as it is established, the ATS685 enables switching:
  - If on the high side, at B_{OP} (position 2) the output would switch from low to high. However, because output is already high, no output switching occurs.
    At the next switch point, where B_{RP} is passed (position 3), the output switches from high to low.
  - If on the low side, at B_{RP} (position 4) the output switches from high to low.

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Undervoltage Lockout

When the supply voltage falls below the minimum operating voltage, $V_{CC(UV)}$, I_{CC} goes high and remains high regardless of the state of the magnetic gradient from the target. This lockout feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the device. Because V_{CC} is below the V_{CC}(min) specification during lockout, the I_{CC} levels may not be within specification.

Power Supply Protection

The device contains an on-chip regulator and can operate over a wide V_{CC} range. For devices that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 8 for an example of a basic application circuit.

Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). At power-on, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain is then automatically adjusted. Figure 9 illustrates the effect of this feature.

Running Mode Gain Adjust

The ATS685 has a feature during Running mode to compensate for dynamic air gap variation. If the system increases the magnetic input drastically, the device will gradually readjust the gain downwards, allowing the chip to regain the optimum internal electrical signal with the new, larger, magnetic signal.

Dynamic Offset Cancellation (DOC)

The offset circuitry when combined with AGC automatically reduces the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including both Power-on mode and Running mode, compensating for any offset drift (within Allowable User-Induced Differential Offset). Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

Running Mode Lockout

The ATS685 has a Running mode lockout feature to prevent switching on small signals that are characteristic of vibration signals. The internal logic of the chip evaluates small signal amplitudes below a certain level to be vibration. In that event, the output is blanked (locked-out) until the amplitude of the signal returns to normal operating levels.

Watchdog

The ATS685 employs a watchdog circuit to prevent extended loss of output switching during sudden impulses and vibration in the system. If the system changes the magnetic input drastically such that target feature detection is terminated, the device will fully reset itself, allowing the chip to recalibrate properly on the new magnetic input signal.

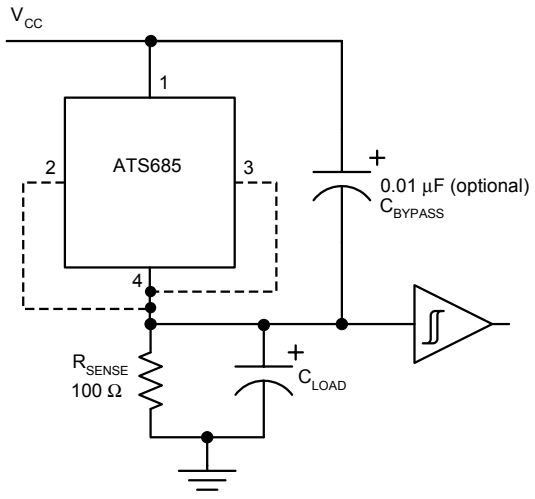

Figure 8. Typical circuit for proper device operation.

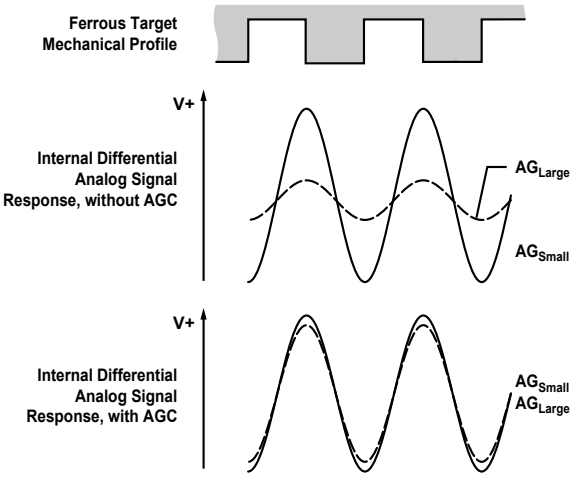

Figure 9. Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap cause differences in the magnetic field at the device, but AGC prevents that from affecting device performance, as shown in the lowest panel.

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Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 6 mA, and $R_{\theta JA}$ = 126 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 6\ mA = 72\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 72\ mW \times 126\ °C/W = 9.1°C$$

$$T_J = T_A + \Delta T = 25°C + 9.1°C = 34.1°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level ($V_{CC}(max)$, $I_{CC}(max)$), without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package SH, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=126 °C/W, $T_J(max)$=165°C, $V_{CC}(max)$ =28 V, and $I_{CC}(max)$ = 16 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 126\ °C/W = 119\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 119\ mW \div 16\ mA = 7.4\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤V_{CC}(est).

Compare V_{CC}(est) to V_{CC}(max). If $V_{CC}(est) \le V_{CC}(max)$, then reliable operation between V_{CC}(est) and V_{CC}(max) requires enhanced $R_{\theta JA}$. If $V_{CC}(est) \ge V_{CC}(max)$, then operation between V_{CC}(est) and V_{CC}(max) is reliable under these conditions.

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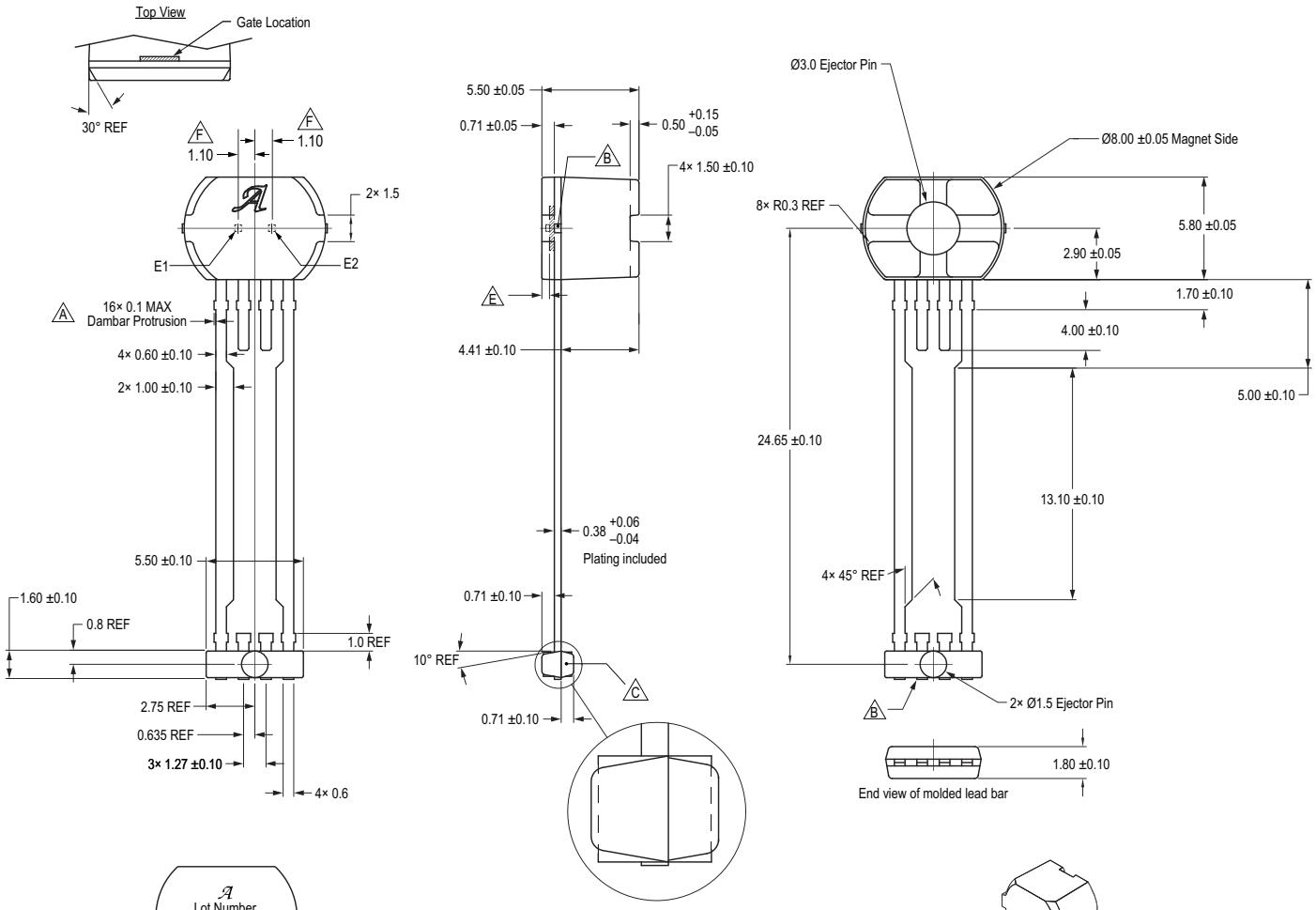
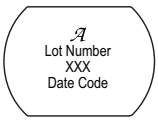
Package SH, 4-Pin SIP

For Reference Only – Not for Tooling Use

(Reference DWG-0000393)
Dimensions in millimeters. NOT TO SCALE.
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

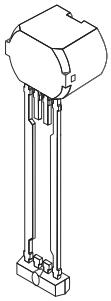




D **Standard Branding Reference View**

Line 1: Logo A molded in
Line 2: 7-digit alpha numeric Lot Number
Line 3: Last 3 digits of Part Number.
Line 4: 4-digit Date Code
Center align

A Dambar removal protrusion (16×)
B Metallic protrusion, electrically connected to pin 4 and substrate (both sides)
C Molded Lead Bar for alignment during shipment
D Branding scale and appearance at supplier discretion
E Active Area Depth 0.43 mm REF
F Hall elements (E1, E2); not to scale



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Revision History

Number	Date	Description
–	March 30, 2011	Initial release
1	May 5, 2020	Minor editorial updates
2	May 1, 2023	Updated package drawing (page 14)

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