April 2005

RMPA2265
Dual Band WCDMA Power Edge™ Power Amplifier Module 1850 to 1910 MHz and 1920 to 1980 MHz

Features

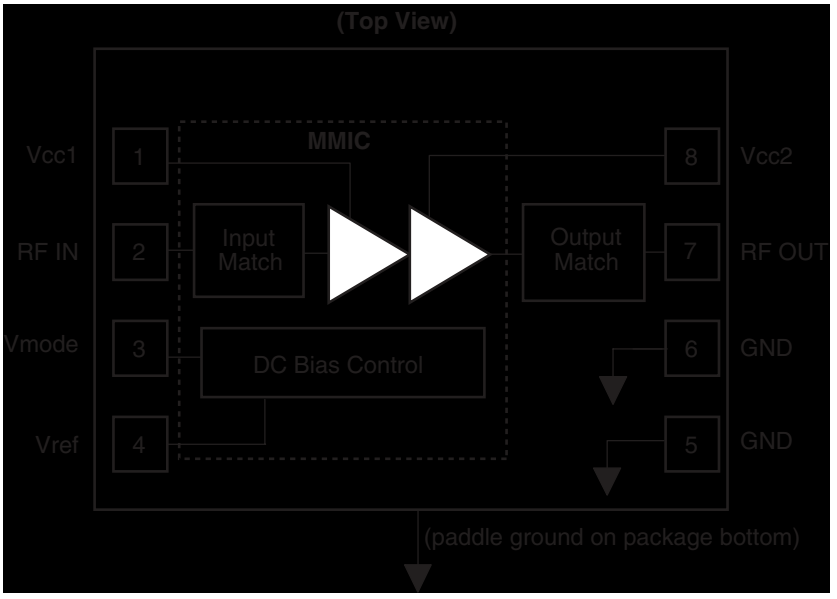
- Single positive-supply operation and low power and shut-down modes
- 42% WCDMA efficiency at +28 dBm average output power 1920–1980 MHz
- 39% WCDMA efficiency at 27.5 dBm average output power 1850–1910 MHz
- Meets UMTS/WCDMA performance requirements in both UMTS bands
- Meets HSDPA performance requirements
- Compact Lead-free compliant LCC package– (3.0 x 3.0 x 1.0 mm nominal)
- Internally matched to 50 Ohms and DC blocked RF input/output

General Description

The RMPA2265 power amplifier module (PAM) is designed for WCDMA/HSDPA applications in both the 1850–1910 and 1920–1980 MHz bands. The 2 stage PAM is internally matched to 50 Ohms to minimize the use of external components and features a low-power mode to reduce standby current and DC power consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using Fairchild's InGaP/GaAs Heterojunction Bipolar Transistor (HBT) process.

Device

Functional Block Diagram



Absolute Ratings [1]

Symbol	Parameter	Ratings	Units
V_{CC1}, V_{CC2}	Supply Voltages	5.0	V
V_{ref}	Reference Voltage	2.6 to 3.5	V
V_{mode}	Power Control Voltage	3.5	V
P_{IN}	RF Input Power	+10	dBm
T_{STG}	Storage Temperature	-55 to +150	°C

Note:

1. No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Electrical Characteristics (1920 to 1980 MHz)[1]

Symbol	Parameter	Min	Typ	Max	Units	Comments
f	Operating Frequency	1920		1980	MHz	
WCDMA Operation						
Gp	Power Gain	26	28		dB	Po = +28dBm, Vmode = 0V
			26		dB	Po = +16dBm, Vmode ≥ 2.0V
Po	Linear Output Power	28			dBm	Vmode = 0V
		16			dBm	Vmode ≥ 2.0V
PAEd	PAEd (digital) @ +28dBm		42		%	Vmode = 0V
	PAEd (digital) @ +16dBm		9		%	Vmode ≥ 2.0V
	PAEd (digital) @ +16dBm		25		%	Vmode ≥ 2.0V, Vcc = 1.4V
Itot	High Power Total Current		440		mA	Po = +28dBm, Vmode = 0V
	Low Power Total Current		120		mA	Po = +16dBm, Vmode ≥ 2.0V
	Adjacent Channel Leakage Ratio					WCDMA Modulation 3GPP 3.2 03-00 DPCCH+1 DCDCH
ACLR1	±5.00MHz Offset 1920–1980MHz		-40		dBc	Po = +28dBm, Vmode = 0V
			-42		dBc	Po = +16dBm, Vmode ≥ 2.0V
ACLR2	±10.00MHz Offset 1920–1980MHz		-54		dBc	Po = +28dBm, Vmode = 0V
			-66		dBc	Po = +16dBm, Vmode ≥ 2.0V
General Characteristics						
VSWR	Input Impedance		2.0:1			
NF	Noise Figure		4		dB	
Rx No	Receive Band Noise Power		-142		dBm/ Hz	Po ≤ +28dBm, 2110 to 2170MHz
2fo – 5fo	Harmonic Suppression[3]			-50	dBc	Po ≤ +28dBm
S	Spurious Outputs[2, 3]			-60	dBc	Load VSWR ≤ 5.0:1
	Ruggedness with Load Mismatch[3]			10:1		No permanent damage
Tc	Case Operating Temperature	-30		85	°C	
DC Characteristics						
Iccq	Quiescent Current		45		mA	Vmode ≥ 2.0V
Iref	Reference Current		5		mA	Po ≤ +28dBm
Icc(off)	Shutdown Leakage Current		1	5	µA	No applied RF signal

Notes:

1. All parameters met at T_C = +25°C, V_{CC} = +3.4V, V_{ref} = 2.85V and load VSWR ≤ 1.2:1, unless otherwise noted.
2. All phase angles.
3. Guaranteed by design.

Electrical Characteristics (1850 to 1910 MHz)[1]

Symbol	Parameter	Min	Typ	Max	Units	Comments
f	Operating Frequency	1850		1910	MHz	
WCDMA Operation						
Gp	Power Gain	26	28		dB	Po = +27.5dBm, Vmode = 0V
			26		dB	Po = +16dBm, Vmode ≥ 2.0V
Po	Linear Output Power	27.5			dBm	Vmode = 0V
		16			dBm	Vmode ≥ 2.0V
PAEd	PAEd (digital) @ +27.5dBm		39		%	Vmode = 0V
	PAEd (digital) @ +16dBm		9		%	Vmode ≥ 2.0V
	PAEd (digital) @ +16dBm		25		%	Vmode ≥ 2.0V, Vcc = 1.4V
Itot	High Power Total Current		420		mA	Po = +27.5dBm, Vmode = 0V
	Low Power Total Current		120		mA	Po = +16dBm, Vmode ≥ 2.0V
	Adjacent Channel Leakage Ratio					WCDMA Modulation 3GPP 3.2 03-00 DPCCH+1 DCDCH
ACLR1	±5.00MHz Offset 1850–1910MHz		-40		dBc	Po = +27.5dBm, Vmode = 0V
			-42		dBc	Po = +16dBm, Vmode ≥ 2.0V
ACLR2	±10.00MHz Offset 1850–1910MHz		-54		dBc	Po = +27.5dBm, Vmode = 0V
			-66		dBc	Po = +16dBm, Vmode ≥ 2.0V
General Characteristics						
VSWR	Input Impedance		2.0:1			
NF	Noise Figure		4		dB	
Rx No	Receive Band Noise Power		-139		dBm/Hz	Po ≤ +27.5dBm, 1930 to 1990MHz
2fo – 5fo	Harmonic Suppression[3]			-50	dBc	Po ≤ +27.5dBm
S	Spurious Outputs[2, 3]			-60	dBc	Load VSWR ≤ 5.0:1
	Ruggedness with Load Mismatch[3]			10:1		No permanent damage
Tc	Case Operating Temperature	-30		85	°C	
DC Characteristics						
Iccq	Quiescent Current		45		mA	Vmode ≥ 2.0V
Iref	Reference Current		5		mA	Po ≤ +27.5dBm
Icc(off)	Shutdown Leakage Current		1	5	µA	No applied RF signal

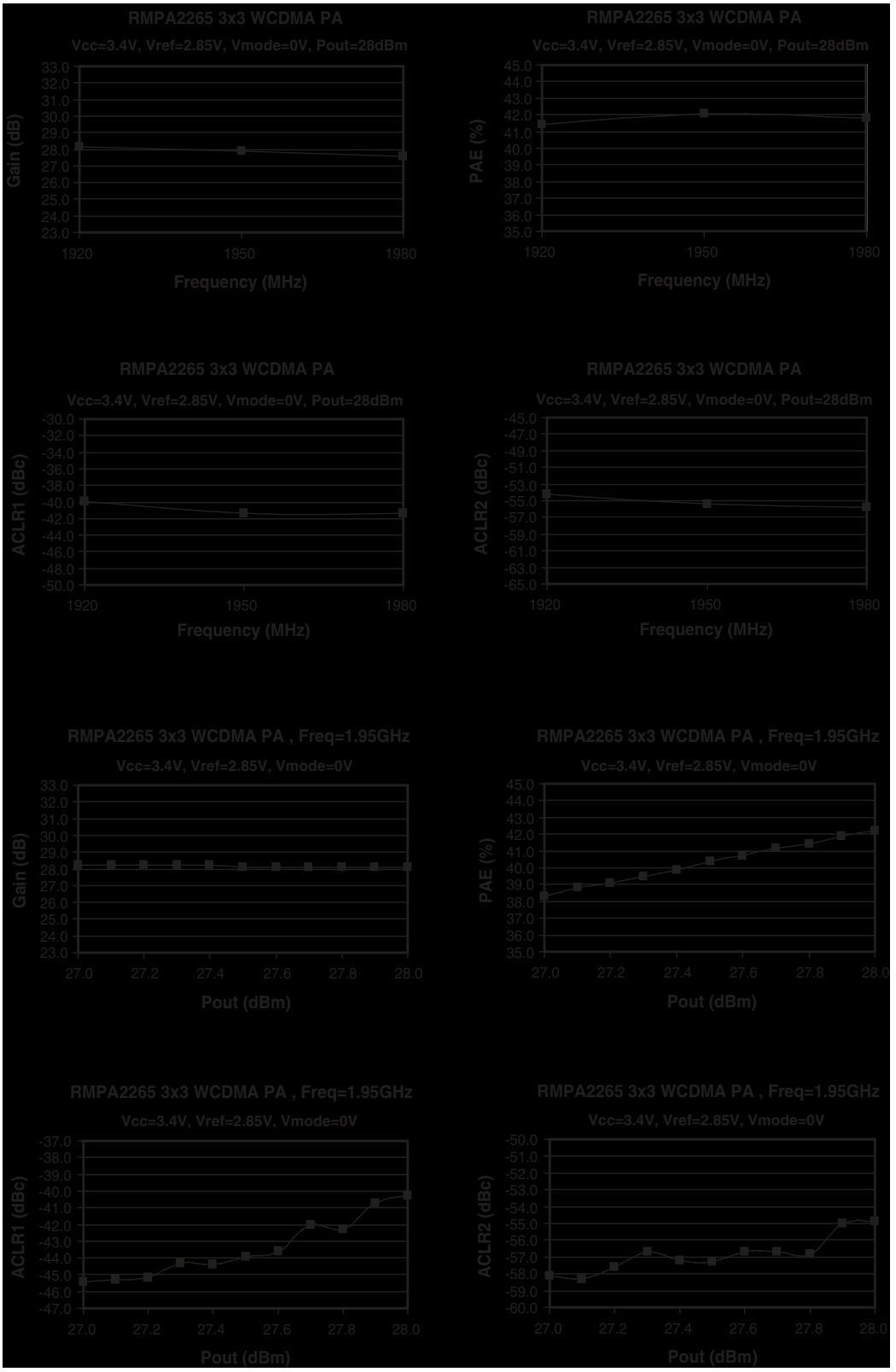
Notes:

1. All parameters met at T_C = +25°C, V_{CC} = +3.4V, V_{ref} = 2.85V and load VSWR ≤ 1.2:1, unless otherwise noted.
2. All phase angles
3. Guaranteed by design

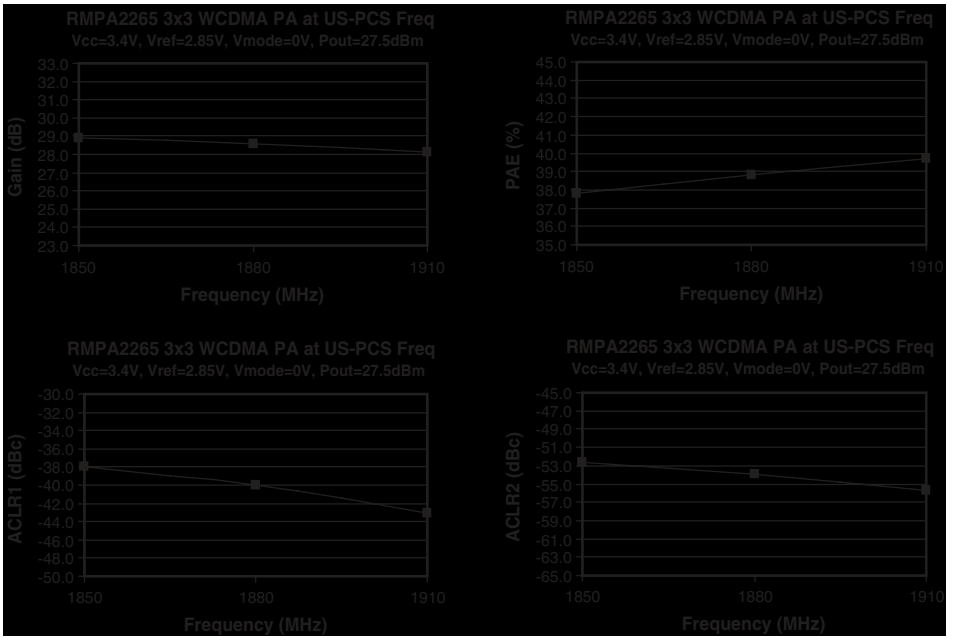
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
f	Operating Frequency	1850		1980	MHz
V_{CC1}, V_{CC2}	Supply Voltage	3.0	3.4	4.2	V
V_{ref}	Reference Voltage Operating Shutdown	 2.7 0	 2.85	 3.1 0.5	 V V
V_{mode}	Bias Control Voltage Low-Power High-Power	 1.8 0	 2.0	 3.0 0.5	 V V
P_{OUT}	Linear Output Power (low-power) 1920–1980 MHz (high power) 1850–1910 MHz (high power)			+16 +28 +27.5	dBm dBm dBm
T_C	Case Operating Temperature	-30		+85	°C

Performance Data: 1920 to 1980 MHz



Performance Data: 1850 to 1910 MHz



Efficiency Improvement Applications

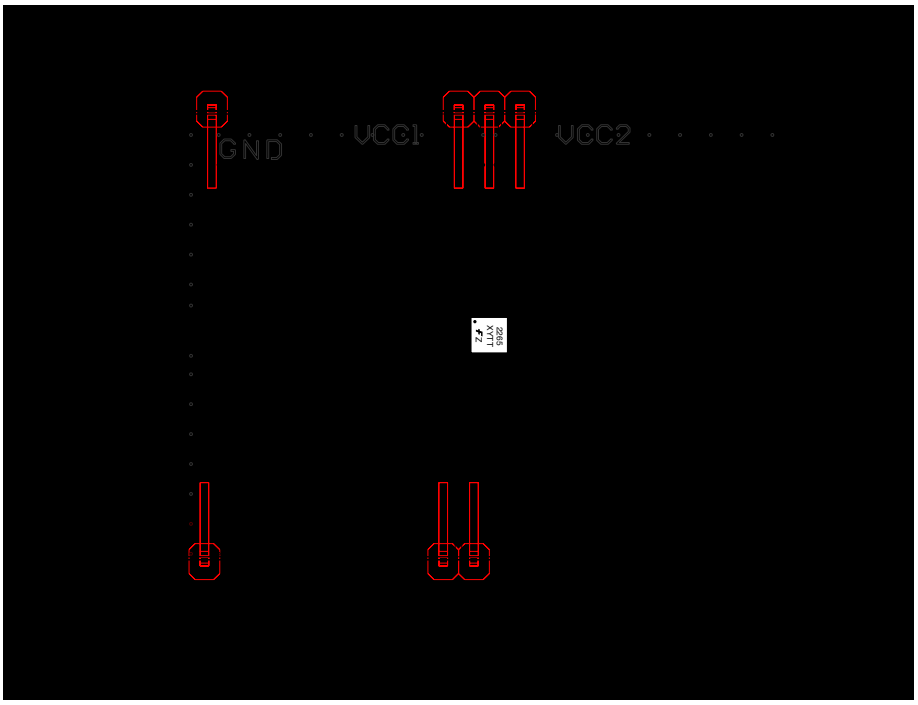
In addition to high-power/low-power bias modes, the efficiency of the PA module can be significantly increased at backed-off RF power levels by dynamically varying the supply voltage (Vcc) applied to the amplifier. Since mobile handsets and power amplifiers frequently operate at 10–20 dB back-off, or more, from maximum rated linear power, battery life is highly dependent on the DC power consumed at antenna power levels in the range of 0 to +16dBm. The reduced demand on transmitted RF power allows the PA supply voltage to be reduced for improved efficiency, while still meeting linearity requirements for WCDMA modulation with excellent margin. High-efficiency DC-DC converters are now available to implement switched-voltage operation.

With the PA module in low-power mode (Vmode = 2.0V) at +16dBm output power and supply voltages reduced from 3.4V nominal down to 1.2V, power-added efficiency is more than doubled from 9 percent to 25 percent (Vcc = 1.2V) while maintaining a typical ACLR1 of -40dBc and ACLR2 of less than -54 dBc. Operation at even lower levels of Vcc supply voltage are possible with a further restriction on the maximum RF output power.

DC Turn On Sequence:

1. Vcc1 = Vcc2 = 3.4V (typical)
2. Vref = 2.85V (typical)
3. High-Power: Vmode = 0V (Pout > 16dBm)
   Low-Power: Vmode = 2.0V (Pout < 16dBm)

Evaluation Board Layout

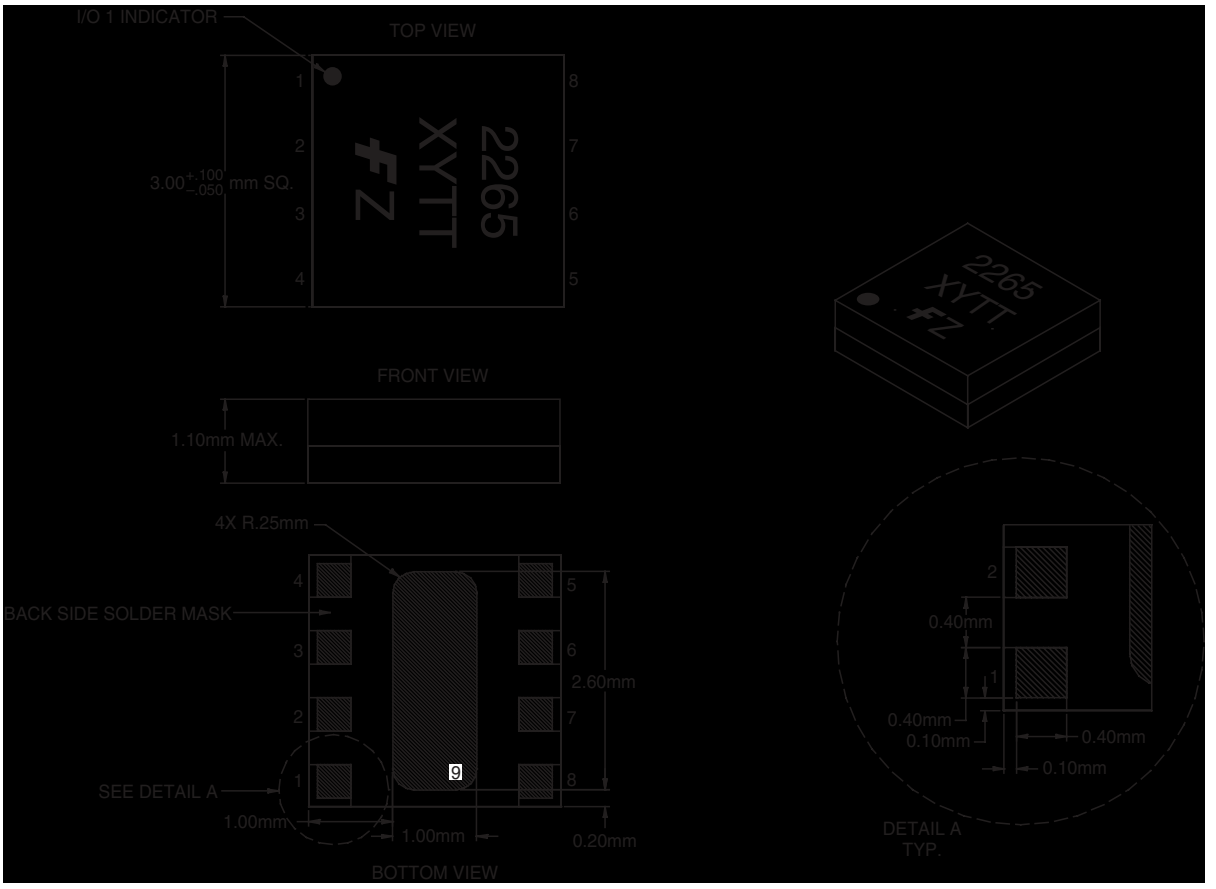


Materials List

Qty	Item No.	Part Number	Description	Vendor
1	1	G657691-1 V1	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
7	3	#2340-5211TN	Terminals	3M
Ref	4	F100003	Assembly, RMPA2265	Fairchild
3	5	GRM39X7R102K50V	1000pF Capacitor (0603)	Murata
3	5 (Alt)	ECJ-1VB1H102K	1000pF Capacitor (0603)	Panasonic
2	6	C3216X5R1A335M	3.3µF Capacitor (1206)	TDK
1	7	GRM39Y5V104Z16V	0.1µF Capacitor (0603)	Murata
1	7 (Alt)	ECJ-1VB1C104K	0.1µF Capacitor (0603)	Panasonic
A/R	8	SN63	Solder Paste	Indium Corp.
A/R	9	SN96	Solder Paste	Indium Corp.

Evaluation Board Schematic

Package Outline



Signal Description

Pin #	Signal Name	Description
1	Vcc1	Supply Voltage to Input Stage
2	RF In	RF Input Signal
3	Vmode	High Power/Low Power Switch
4	Vref	Reference Voltage
5	GND	Ground
6	GND	Ground
7	RF Out	RF Output Signal
8	Vcc2	Supply Voltage to Output Stage
9	GND	Ground

Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
- Assemble the dry-baked devices within 7 days of removal from the oven.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

Solder Materials & Temperature Profile:
Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1-2°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120–150 seconds at 150°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215–220°C, with a maximum limit of 225°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile