ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

www.onsemi.com

ON Semiconductor®

FDMS003N08C

N-Channel Shielded Gate PowerTrench® MOSFET

80 V, 147 A, 3.1 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 3.1 mΩ at V_{GS} = 10 V, I_D = 56 A
- Max $r_{DS(on)}$ = 8.1 mΩ at V_{GS} = 6 V, I_D = 28 A
- 50% lower Qrr than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar
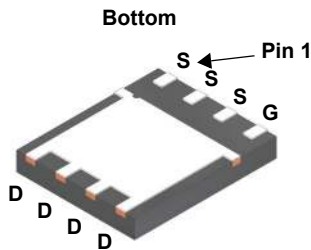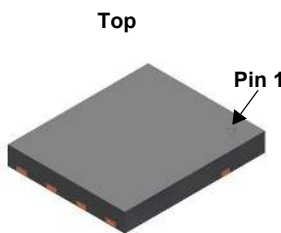
Power 56
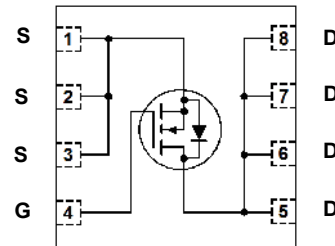
MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C	(Note 5)	147	A
	-Continuous	T_C = 100 °C	(Note 5)	92	
	-Continuous	T_A = 25 °C	(Note 1a)	22	
	-Pulsed		(Note 4)	658	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	486	mJ
P_D	Power Dissipation	T_C = 25 °C		125	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case			1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		(Note 1a)	45	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS003N08C	FDMS003N08C	Power 56	13 ''	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		60		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 310 µA	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 310 µA, referenced to 25 °C		-8.2		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 56 A		2.6	3.1	mΩ
		V_{GS} = 6 V, I_D = 28 A		3.8	8.1	
		V_{GS} = 10 V, I_D = 56 A, T_J = 125 °C		4.3	5.2	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 56 A		123		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		3820	5350	pF
C_{oss}	Output Capacitance			1335	1870	pF
C_{rss}	Reverse Transfer Capacitance			44	80	pF
R_g	Gate Resistance		0.1	0.6	1.3	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 56 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		20	36	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			40	64	ns
t_f	Fall Time			12	23	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	V_{DD} = 40 V, I_D = 56 A		52	73	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V		33	46	nC
Q_{gs}	Gate to Source Charge			17		nC
Q_{gd}	Gate to Drain "Miller" Charge			10		nC
Q_{oss}	Output Charge	V_{DD} = 40 V, V_{GS} = 0 V		77		nC
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, I_D = 56 A		44		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.2 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 56 A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 28 A, di/dt = 300 A/µs		28	45	ns
Q_{rr}	Reverse Recovery Charge			53	84	nC
t_{rr}	Reverse Recovery Time	I_F = 28 A, di/dt = 1000 A/µs		23	36	ns
Q_{rr}	Reverse Recovery Charge			121	194	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.
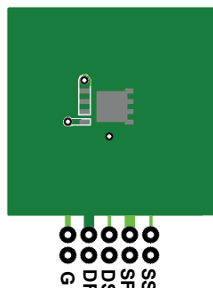
a. 45 °C/W when mounted on a 1 in^2 pad of 2 oz copper.
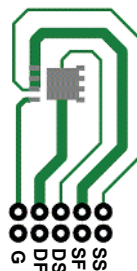
b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. E_{AS} of 486 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 18 A, V_{DD} = 80 V, V_{GS} =10 V. 100% test at L = 0.1 mH, I_{AS} = 57 A.
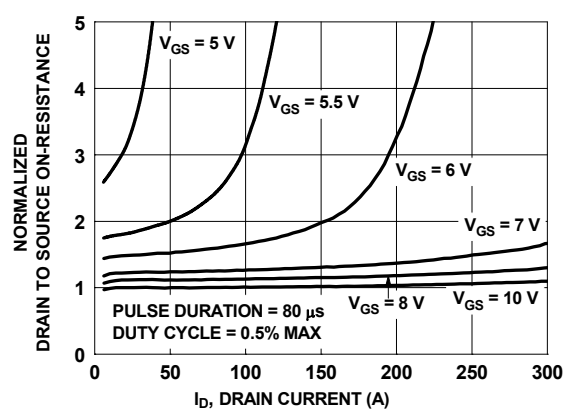4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
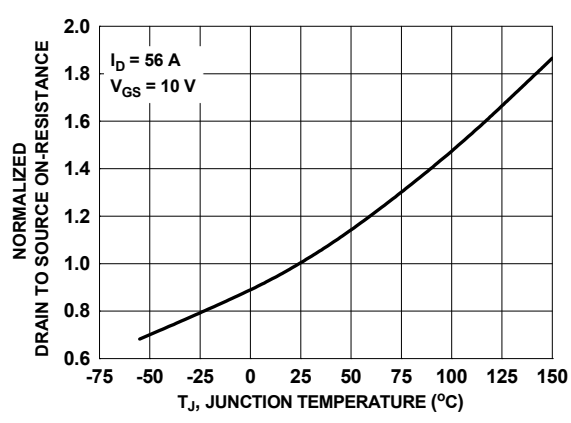
Typical Characteristics T_J = 25 °C unless otherwise noted.
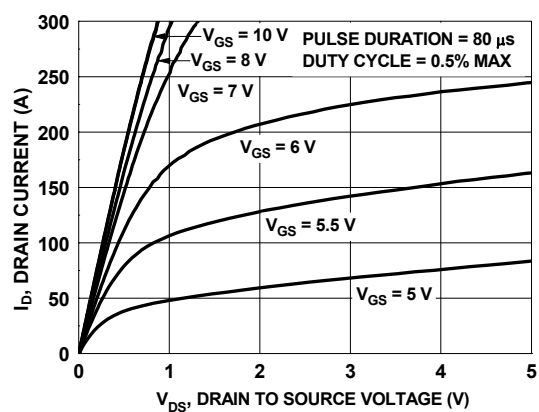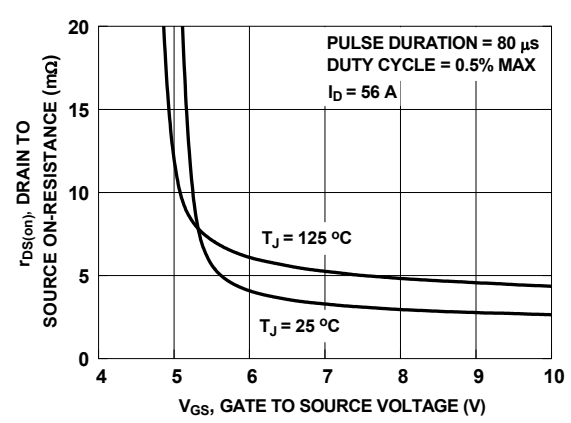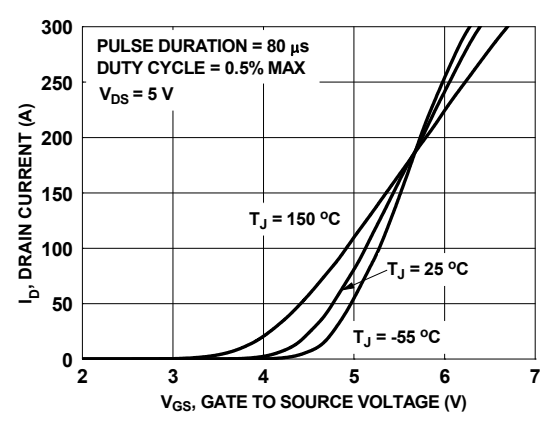

Figure 1. On Region Characteristics

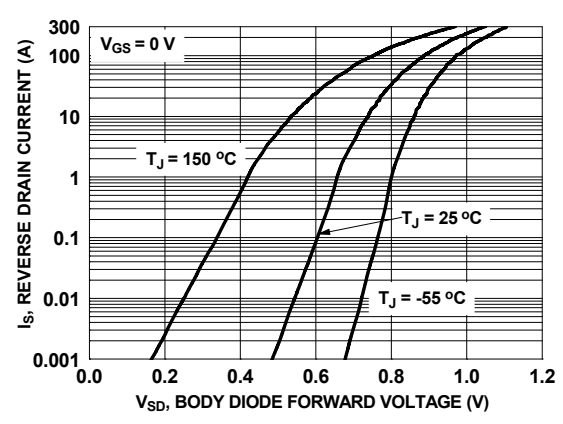Figure 2. Normalized On-Resistance
vs. Drain Current and Gate Voltage

Figure 3. Normalized On Resistance
vs. Junction Temperature
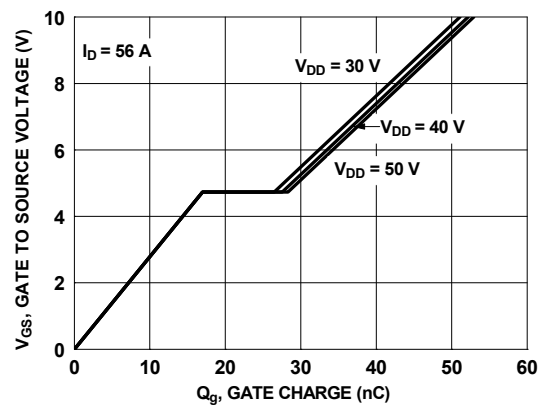

Figure 4. On-Resistance vs. Gate to
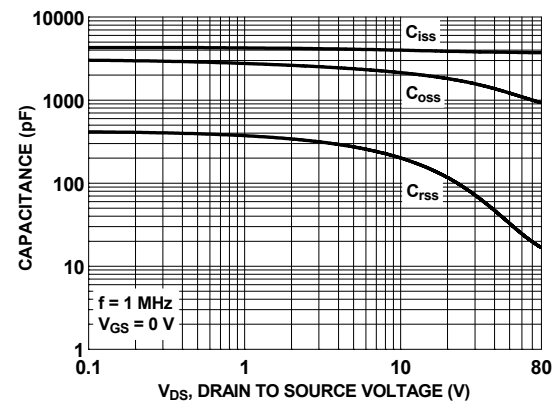Source Voltage

Figure 5. Transfer Characteristics

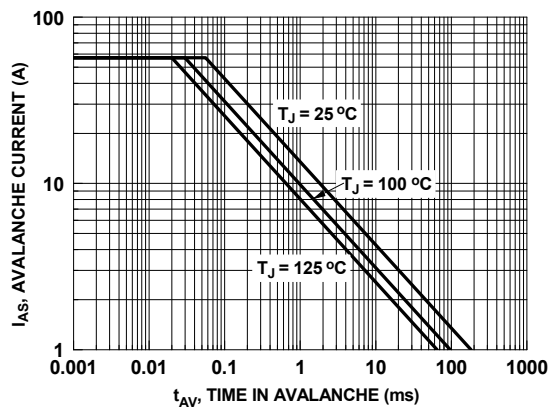Figure 6. Source to Drain Diode
Forward Voltage vs. Source Current

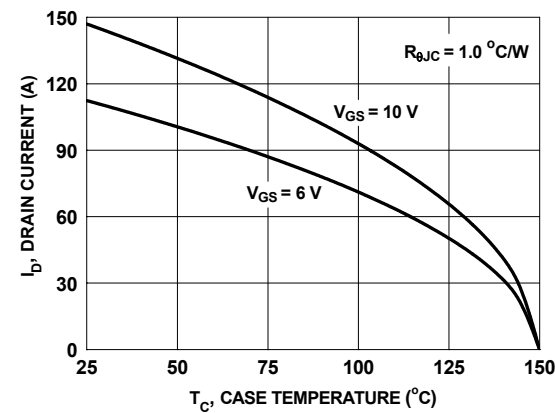## Typical Characteristics T_J = 25 °C unless otherwise noted.
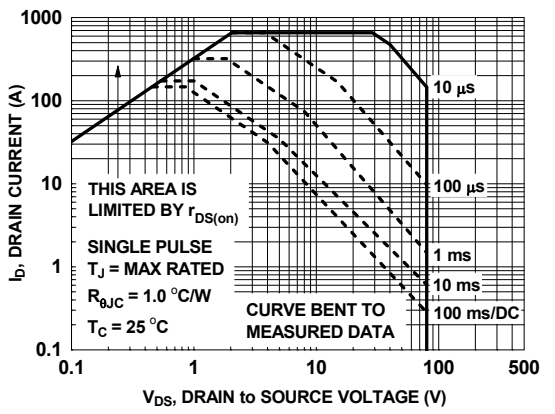

Figure 7. Gate Charge Characteristics
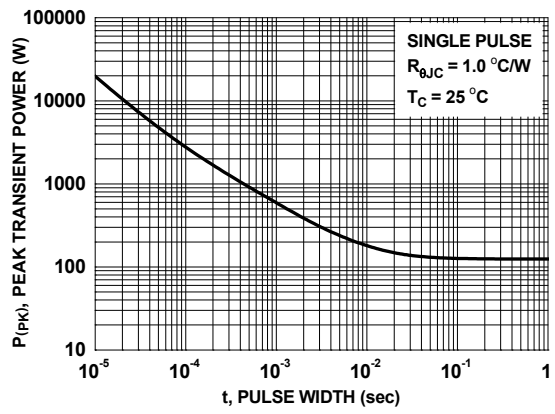

Figure 8. Capacitance vs. Drain to Source Voltage

Figure 9. Unclamped Inductive Switching Capability

Figure 10. Maximum Continuous Drain Current vs. Case Temperature

Figure 11. Forward Bias Safe Operating Area

Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

DUTY CYCLE-DESCENDING ORDER
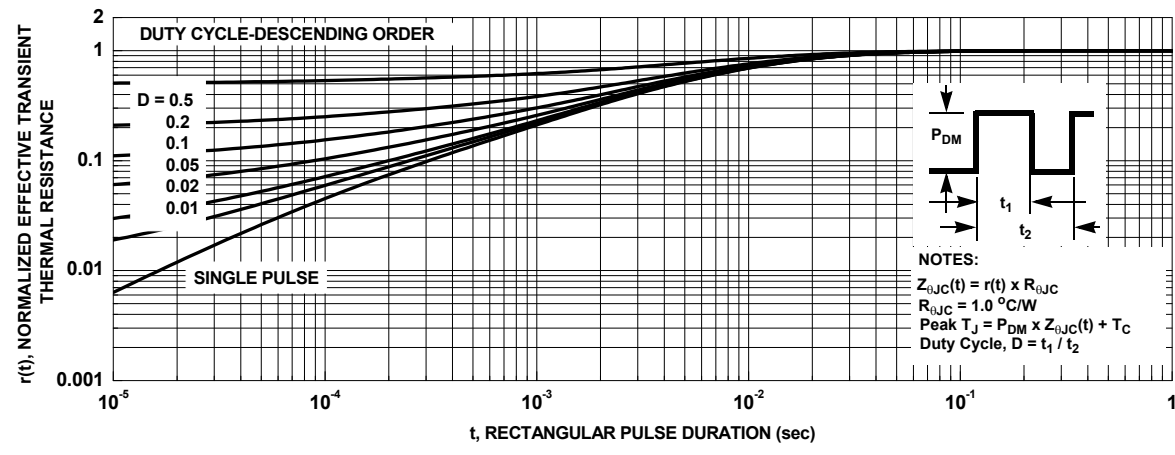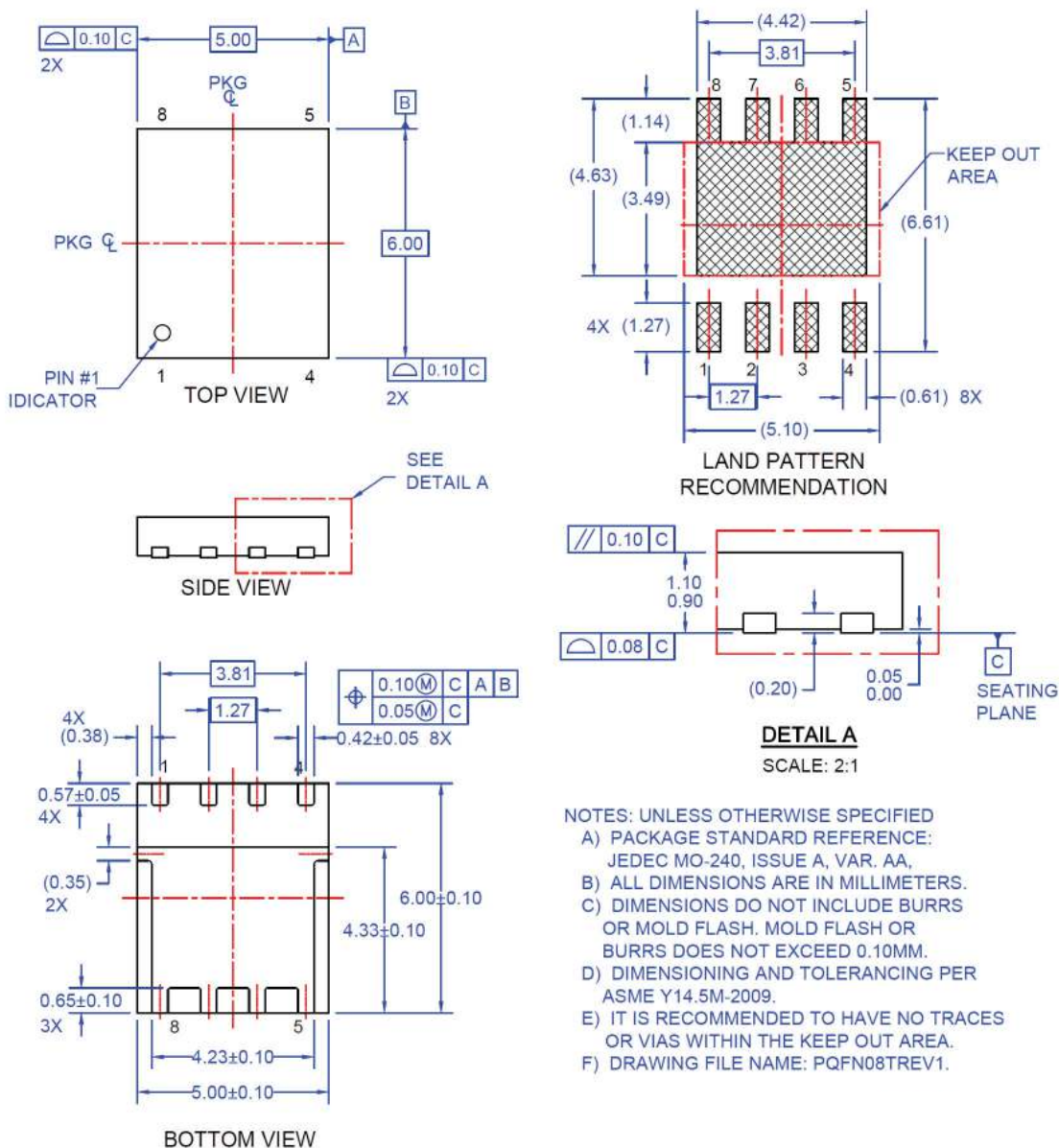
D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE

t, RECTANGULAR PULSE DURATION (sec)

NOTES:
$Z_{\theta JC}(t) = r(t) \times R_{\theta JC}$
$R_{\theta JC} = 1.0\ °C/W$
Peak $T_J = P_{DM} \times Z_{\theta JC}(t) + T_C$
Duty Cycle, $D = t_1 / t_2$

Figure 13. Junction-to-Case Transient Thermal Response Curve

Dimensional Outline and Pad Layout

TOP VIEW

2X | 0.10 | C | 5.00 | A
PKG ℄
8 | 5 | B
PKG ℄ | 6.00
PIN #1 IDICATOR | 1 | 4
2X | 0.10 | C

SIDE VIEW

SEE DETAIL A

BOTTOM VIEW

| 0.10 (M) | C | A | B
| 0.05 (M) | C
3.81
1.27
4X (0.38)
0.42±0.05 8X
0.57±0.05 4X
(0.35) 2X
6.00±0.10
4.33±0.10
0.65±0.10 3X
8 | 5
4.23±0.10
5.00±0.10

LAND PATTERN RECOMMENDATION

(4.42)
3.81
8 7 6 5
(1.14)
(4.63)
(3.49)
KEEP OUT AREA
(6.61)
4X (1.27)
1 2 3 4
1.27
(0.61) 8X
(5.10)

DETAIL A
SCALE: 2:1

| // | 0.10 | C
1.10
0.90
| ⌒ | 0.08 | C
(0.20)
0.05
0.00
| C
SEATING PLANE

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F) DRAWING FILE NAME: PQFN08TREV1.