# SN74AXC4T774 Evaluation Module User Guide

This user's guide describes the characteristics, operation, and use of the SN74AXC4T774EVM Evaluation Module (EVM). A complete printed-circuit board layout, schematic diagrams, and bill of materials are included in this document.

**Contents**



**List of Figures**



**List of Tables**



## Trademarks

All trademarks are the property of their respective owners.

# 1 Introduction

The AXC devices are a new family of direction controlled level translators from Texas Instruments. AXC devices have dual-supply pins enabling configurable voltage translation between 0.65 V and 3.6 V and any intermediate voltage ranges. The SN74AXC4T774EVM can be used to evaluate SN74AXC4T774 translator device in the PW or the RSV packages. Refer to the competitive advantages of the AXC Family in the application report *Power sequencing for the AXC family of devices* (SCEA058). Watch Introduction to the AXC family of direction controlled translation device.

## 1.1 Features

The AXC family of direction controlled translation devices are dual-supply with configurable voltage translation and an operating range from 0.65 V to 3.6 V. The A port is designed to track $V_{CCA}$. $V_{CCA}$ accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track $V_{CCB}$. $V_{CCB}$ accepts any supply voltage from 0.65 V to 3.60 V. The SN74AXC4T774 device is fully specified for partial-power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the outputs, thus preventing damaging current backflow through the device when the device is powered down. The $V_{CC}$ isolation feature ensures that if either $V_{CC}$ input is at ground, both A and B data I/O ports are in the high-impedance state.

The eight channel SN74AXC8T245 device has two direction control pins, each controlling 4 data I/Os enabling independent and simultaneous up and down translation. Refer to SN74AXC8T245EVM for testing SN74AXC8T245PW package.

The four channel SN74AXC4T774 device has individual direction control pins for each of it's IO(A and B) ports to allow configurable up and down translation.

The functional table of the SN74AXC4T774 is listed in Table 1.This EVM is pre-configured to support translation for Serial Peripheral Interface (SPI) and Joint Test Action Group (JTAG) interface as shown in Table 2.Refer to the low voltage translation for standard interfaces in the application report *Low voltage translation for SPI, UART, RGMII, and JTAG interfaces*(SCEA065).

**Table 1. SN74AXC4T774 Functional Table(Each 1-bit section)**

| OE | DIRx | Signal Direction |
|---|---|---|
| H | X | Hi-Z |
| L | L | B data to A bus |
| L | H | A data to B bus |

**Table 2. SPI, JTAG Interface EVM setup**

| PINS | PULL-UP (PW AND RSV) | PULL-DOWN (PW AND RSV) | DEFAULT STATE | STATUS |
|---|---|---|---|---|
| $\overline{OE}$ | R1, R6 | R13, R14 | 10kΩ to GND | DEVICE ENABLED |
| DIR1 | R2, R7 | NO | 10kΩ to Vcca | A1(Input) TO B1(Output) |
| DIR2 | R3, R8 | NO | 10kΩ to Vcca | A2(Input) TO B2(Output) |
| DIR3 | R4, R9 | NO | 10kΩ to Vcca | A3(Input) TO B3(Output) |
| DIR4 | R5, R10 | R15, R16 | 10kΩ to GND | B4(Input) TO A4(Output) |

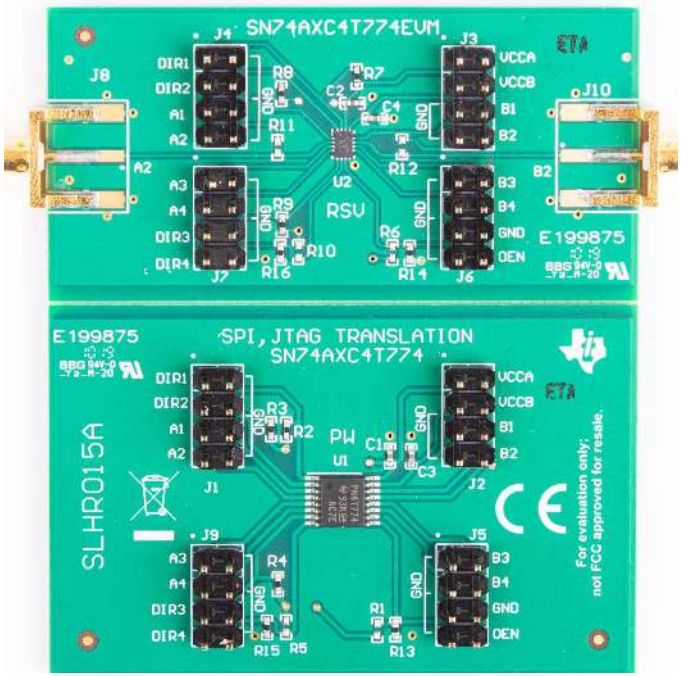


**Figure 1. SPI/JTAG Translation using SN74AXC4T774EVM**

## *1.2 Hardware Description*

### 1.2.1 Headers

The EVM has standard 100-mil headers with the side closer to the device connected to ground. The side farther away from the device is mapped to the device pinout for easier connection as seen in Figure 1. The silkscreen indicates the pin name.

### 1.2.2 Bypass Capacitors

C1, and C2 are the bypass capacitors for $V_{CCA}$ while C3, and C4 are the bypass capacitors for $V_{CCB}$ with a value of 0.1 µF.

### 1.2.3 Pull-up and Pull-down Resistors

The direction control and output enable pins are the inputs for the devices and should never be left floating. The CMOS inputs must be held at a known state, either $V_{CC}$ or ground, to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Table 2 lists the pull-up and pull-down resistors and their default states.

### 1.2.4 SMB Connectors

The edge-mounted SMB connector pair for supporting high-speed operation are provided on data I/O pins of A2 and B2, while the corresponding header pin has an uninstalled R11 and R12 resistor.

## 2 Board Layout

Figure 2 illustrates the SN74AXC4T774EVM layout.

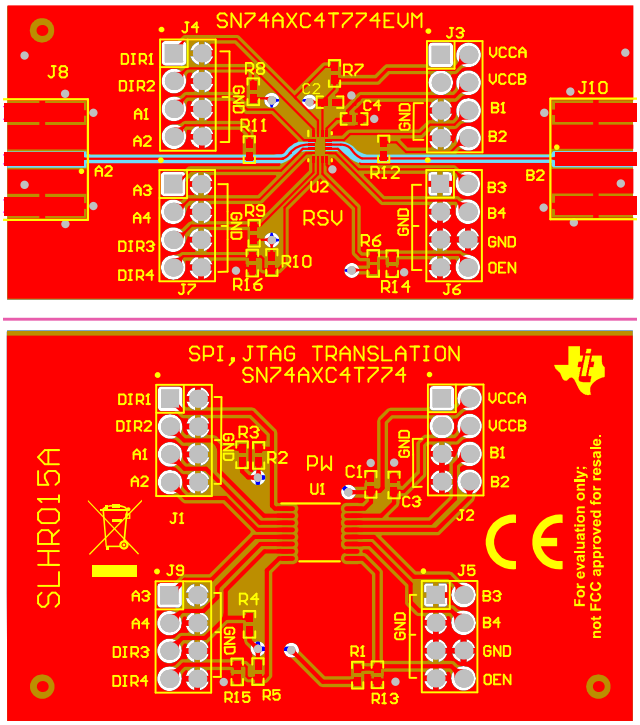


**Figure 2. SN74AXC4T774EVM Layout**

# 3 Schematic and Bill of Materials

## 3.1 Schematic

Figure 3 andFigure 4 illustrates the SN74AXC4T774EVM schematic.

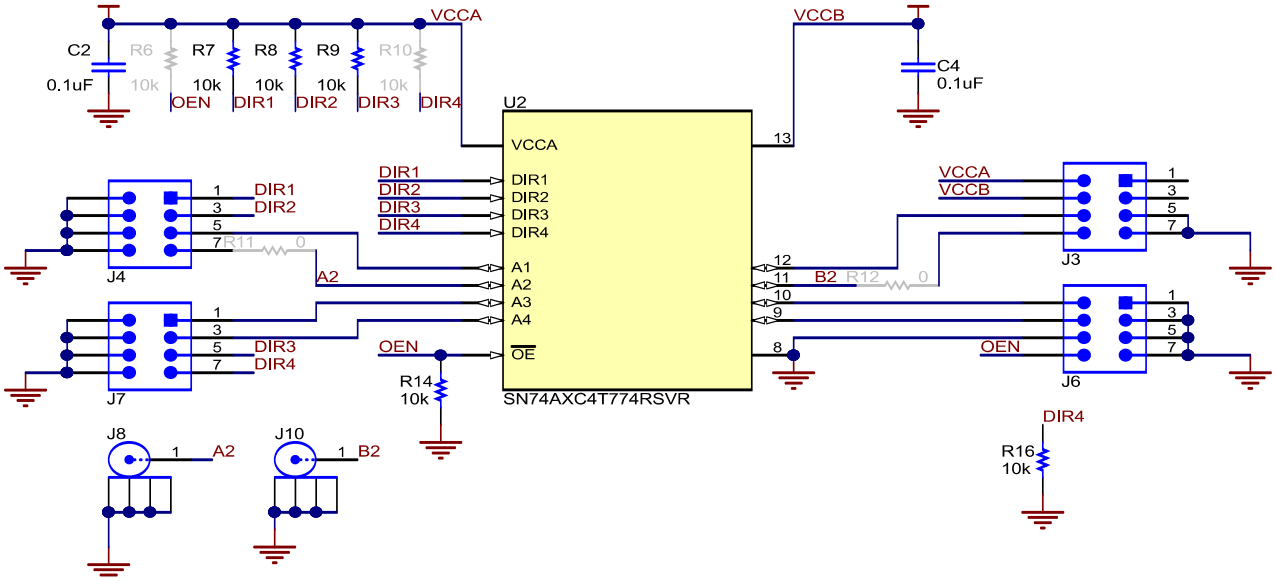


**Figure 3. SN74AXC4T774EVM RSV Schematic**

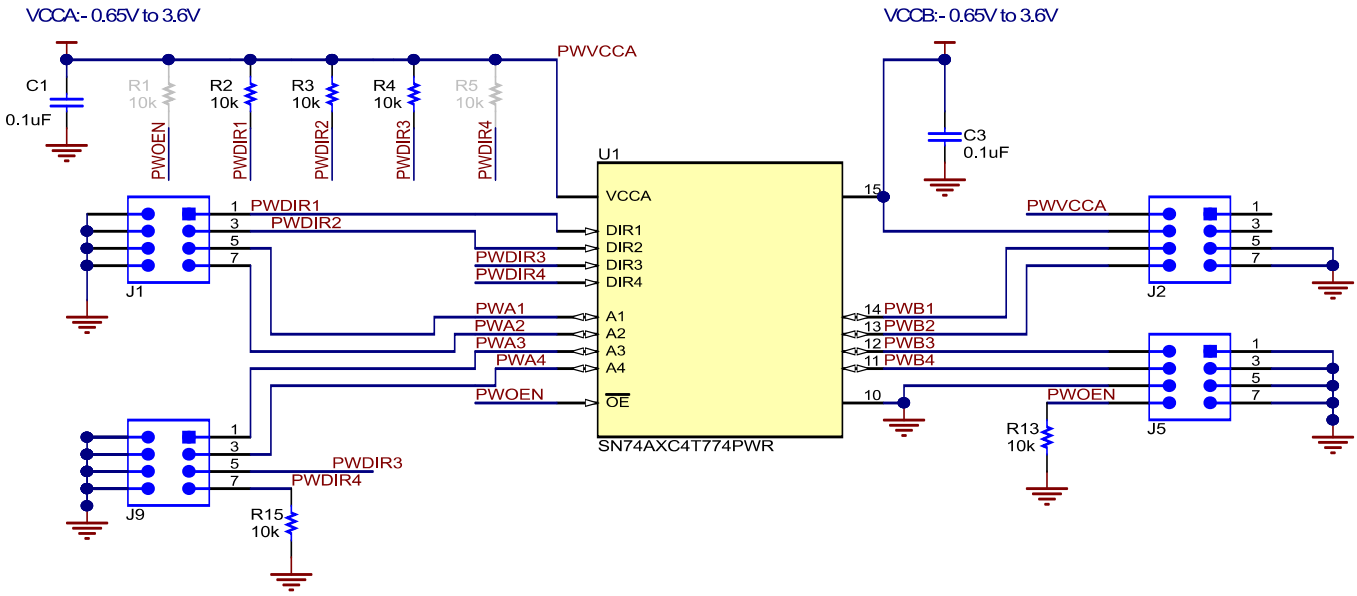


**Figure 4. SN74AXC4T774EVM PW Schematic**

## 3.2 Bill of Materials

Table 3 lists the SN74AXC4T774EVM bill of materials.

**Table 3. SN74AXC4T774EVM Bill of Materials**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| C1, C2, C3, C4 | 4 | 0.1uF | CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402 | 0402 | 0402YC104KAT2A | AVX |
| J1, J2, J3, J4, J5, J6, J7, J9 | 8 | | Header, 100mil, 4x2, Gold, TH | 4x2 Header | TSW-104-07-G-D | Samtec |
| J8, J10 | 2 | | Connector, SMB Jack, End launch, SMT | SMB End launch Jack, SMT | 131-3701-801 | Cinch Connectivity |
| R2, R3, R4, R7, R8, R9, R13, R14, R15, R16 | 10 | 10k | RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040210K0JNED | Vishay-Dale |
| U1 | 1 | | 4 Bit Direction Controlled Level Translator, PW0016A (TSSOP-16) | PW0016A | SN74AXC4T774PWR | Texas Instruments |
| U2 | 1 | | 4 Bit Direction Controlled Level Translator, RSV0016A (UQFN-16) | RSV0016A | SN74AXC4T774RSVR | Texas Instruments |
| FID1, FID2, FID3 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A |
| R1, R5, R6, R10 | 0 | 10k | RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040210K0JNED | Vishay-Dale |
| R11, R12 | 0 | 0 | RES, 0, 5%, 0.063 W, 0402 | 0402 | ERJ-2GE0R00X | Panasonic |

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265