TEXAS INSTRUMENTS

SN74LV4051A

SCLS428I – MAY 1999 – REVISED SEPTEMBER 2015

SN74LV4051A 8-Channel Analog Multiplexers and Demultiplexers

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100-mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Telecommunications
- eCall
- Infotainment

3 Description

The SN74LV4051A 8-channel CMOS analog multiplexers and demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV4051A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5-V (peak) to be transmitted in either direction.
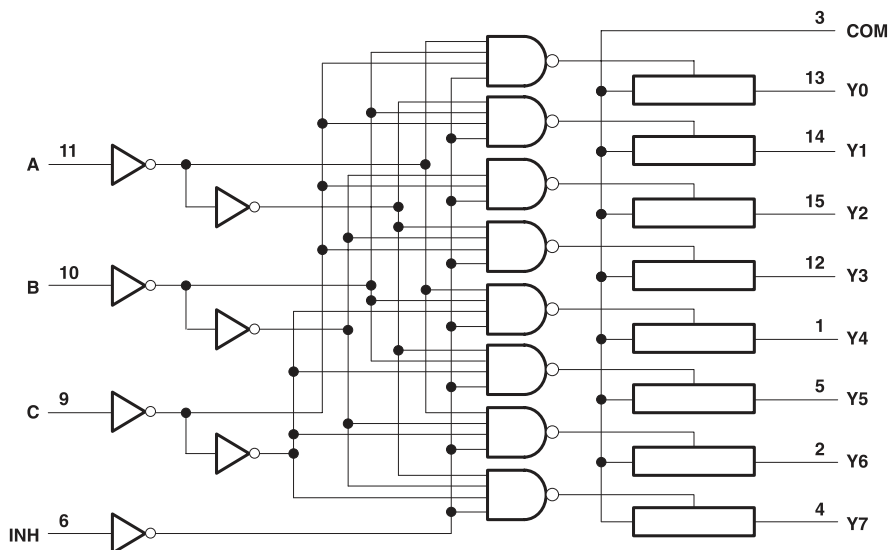
Applications include: signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4051A	TSSOP (16)	5.00 mm × 6.30 mm
	SOIC (16)	9.90 mm × 6.00 mm
	SSOP (16)	6.20 mm × 7.80 mm
	TVSOP (16)	3.60 mm × 6.40 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SO (16)	3.60 mm × 6.40 mm
	VQFN (16)	3.50 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)
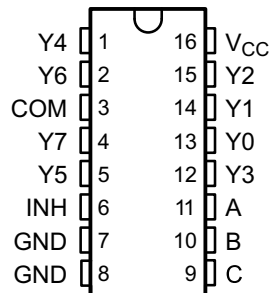
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

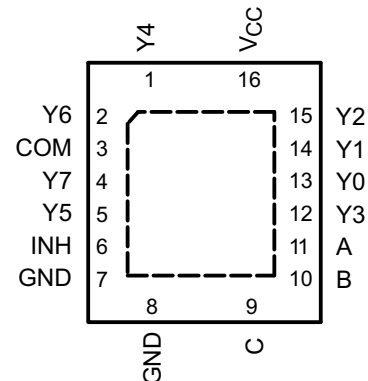**Changes from Revision H (April 2005) to Revision I**   **Page**

5 Pin Configuration and Functions

D, DB, DGB, N, NS, PW Package
16-Pin SOIC, SSOP, TVSOP, PDIP, SO, TSSOP
Top View

Y4	1	16	V_{CC}
Y6	2	15	Y2
COM	3	14	Y1
Y7	4	13	Y0
Y5	5	12	Y3
INH	6	11	A
GND	7	10	B
GND	8	9	C

RGY Package
16-Pin VQFN With Exposed Thermal Pad
Top View

Y4 V_{CC}
1   16

Y6	2	15	Y2
COM	3	14	Y1
Y7	4	13	Y0
Y5	5	12	Y3
INH	6	11	A
GND	7	10	B

8   9
GND C

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	11	I	Selector line A for outputs (see *Device Functional Modes* for specific information)
B	10	I	Selector line B for outputs (see *Device Functional Modes* for specific information)
C	9	I	Selector line C for outputs (see *Device Functional Modes* for specific information)
COM	3	O/I[(1)]	Output/Input of mux
GND	7, 8	—	Ground
INH	6	I[(1)]	Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off.
Y0	13	I/O[(1)]	Input/Output to mux
Y1	14	I/O[(1)]	Input/Output to mux
Y2	15	I/O[(1)]	Input/Output to mux
Y3	12	I/O[(1)]	Input/Output to mux
Y4	1	I/O[(1)]	Input/Output of mux
Y5	5	I/O[(1)]	Input/Output to mux
Y6	2	I/O[(1)]	Input/Output to mux
Y7	4	I/O[(1)]	Input/Output to mux
V_{CC}	16	—	Device power

(1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7.0	V
V_I	Input voltage range[2]		−0.5	7.0	V
V_{IO}	Switch I/O voltage range[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{IOK}	I/O diode current	$V_{IO} < 0$		−50	mA
I_T	Switch through current	$V_{IO} = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Max Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2[2]		5.5	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5			V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} × 0.7$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} × 0.7$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} × 0.7$			
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V			0.5	V
		$V_{CC} = 2.3$ V to 2.7 V			$V_{CC} × 0.3$	
		$V_{CC} = 3$ V to 3.6 V			$V_{CC} × 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V			$V_{CC} × 0.3$	
V_I	Control input voltage		0		5.5	V
V_{IO}	Input or output voltage		0		V_{CC}	V
$Δt/Δv$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V			200	ns/V
		$V_{CC} = 3$ V to 3.6 V			100	
		$V_{CC} = 4.5$ V to 5.5 V			20	
T_A	Operating free-air temperature		−40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) With supply voltages at or near 2 V, the analog switch ON-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LV4051A		UNIT
		N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.8	111.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.1	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.8	56.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.9	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.7	56.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
r_{on}	ON-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 2)	T_A = 25°C	2.3 V		38	180	Ω
			T_A = −40°C to 85°C				225	
			T_A = 25°C	3 V		30	150	
			T_A = −40°C to 85°C				190	
			T_A = 25°C	4.5 V		22	75	
			T_A = −40°C to 85°C				100	
$r_{on(p)}$	Peak ON-state resistance	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	T_A = 25°C	2.3 V		113	500	Ω
			T_A = −40°C to 85°C				600	
			T_A = 25°C	3 V		54	180	
			T_A = −40°C to 85°C				225	
			T_A = 25°C	4.5 V		31	100	
			T_A = −40°C to 85°C				125	
Δr_{on}	Difference in ON-state resistance between switches	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	T_A = 25°C	2.3 V		2.1	30	Ω
			T_A = −40°C to 85°C				40	
			T_A = 25°C	3 V		1.4	20	
			T_A = −40°C to 85°C				30	
			T_A = 25°C	4.5 V		1.3	15	
			T_A = −40°C to 85°C				20	
I_I	Control input current	V_I = 5.5 V or GND	T_A = 25°C	0 to 5.5 V			±0.1	µA
			T_A = −40°C to 85°C				±1	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH} (see Figure 3)	T_A = 25°C	5.5 V			±0.1	µA
			T_A = −40°C to 85°C				±1	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 4)	T_A = 25°C	5.5 V			±0.1	µA
			T_A = −40°C to 85°C				±1	
I_{CC}	Supply current	V_I = V_{CC} or GND	T_A = −40°C to 85°C	5.5 V			20	µA
C_{IC}	Control input capacitance	f = 10 MHz	T_A = 25°C	3.3 V		2		pF
C_{IS}	Common terminal capacitance	T_A = 25°C		3.3 V		23.4		pF
C_{OS}	Switch terminal capacitance	T_A = 25°C		3.3 V		5.7		pF
C_F	Feedthrough capacitance	T_A = 25°C		3.3 V		0.5		pF

Product Folder Links: SN74LV4051A

6.6 Operating Characteristics

V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	5.9	pF

6.7 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		1.9	10	ns
					T_A = −40°C to 85°C			16	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 6)	T_A = 25°C		6.6	18	ns
					T_A = −40°C to 85°C			23	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 6)	T_A = 25°C		7.4	18	ns
					T_A = −40°C to 85°C			23	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF (see Figure 6)	T_A = 25°C		3.8	12	ns
					T_A = −40°C to 85°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 6)	T_A = 25°C		7.8	28	ns
					T_A = −40°C to 85°C			35	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 6)	T_A = 25°C		11.5	28	ns
					T_A = −40°C to 85°C			35	

6.8 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		1.2	6	ns
					T_A = −40°C to 85°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 6)	T_A = 25°C		4.7	12	ns
					T_A = −40°C to 85°C			15	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 6)	T_A = 25°C		5.7	12	ns
					T_A = −40°C to 85°C			15	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		2.5	9	ns
					T_A = −40°C to 85°C			12	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 6)	T_A = 25°C		5.5	20	ns
					T_A = −40°C to 85°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 6)	T_A = 25°C		8.8	20	ns
					T_A = −40°C to 85°C			25	

Product Folder Links: *SN74LV4051A*

6.9 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		0.6	4	ns
					T_A = −40°C to 85°C			7	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 6)	T_A = 25°C		3.5	8	ns
					T_A = −40°C to 85°C			10	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 6)	T_A = 25°C		4.4	8	ns
					T_A = −40°C to 85°C			10	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		1.5	6	ns
					T_A = −40°C to 85°C			8	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 6)	T_A = 25°C		4	14	ns
					T_A = −40°C to 85°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 6)	T_A = 25°C		6.2	14	ns
					T_A = −40°C to 85°C			18	

6.10 Analog Switch Characteristics

over recommended operating free-air temperature range (unless otherwise noted), T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see[1] and Figure 7)		2.3 V		20		MHz
					3 V		25		
					4.5 V		35		
Crosstalk (control input to signal output)	INH	COM or Yn	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		20		mV
					3 V		35		
					4.5 V		60		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see[2] and Figure 9)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Sine-wave distortion	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 $V_{p\text{-}p}$	2.3 V		0.1%		
				V_I = 2.5 $V_{p\text{-}p}$	3 V		0.1%		
				V_I = 4 $V_{p\text{-}p}$	4.5 V		0.1%		

(1) Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads −3 dB.
(2) Adjust f_{in} voltage to obtain 0-dBm input.

Product Folder Links: SN74LV4051A

6.11 Typical Characteristics
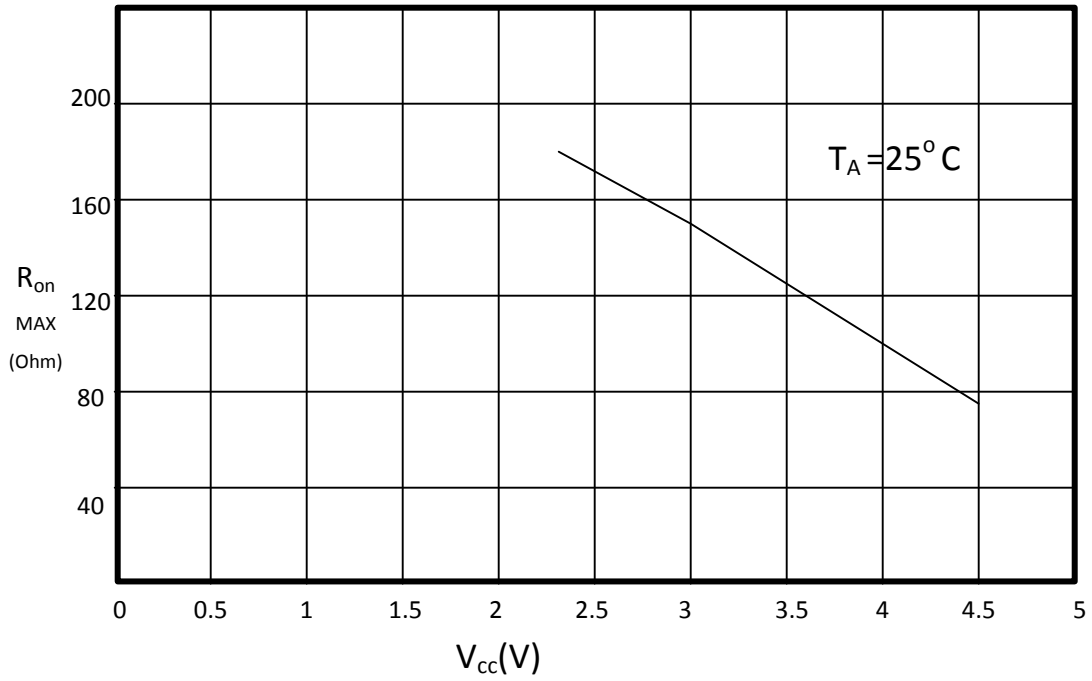
Figure 1. Plot at 25°C for V_{CC} vs Max R_{ON}

Product Folder Links: *SN74LV4051A*

7 Parameter Measurement Information
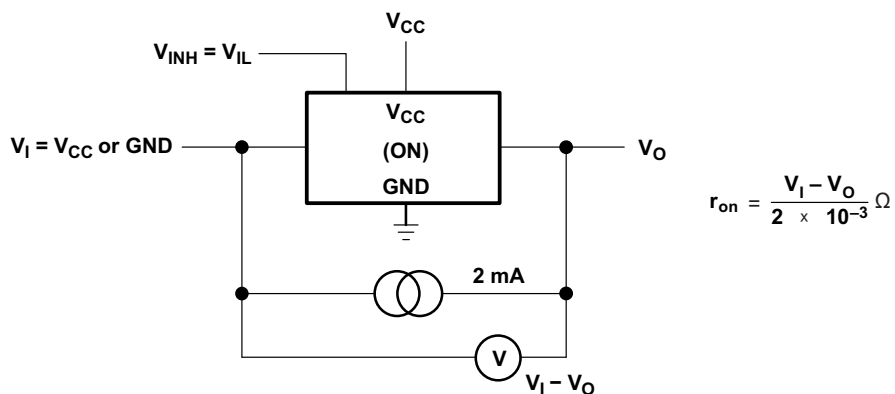
Figure 2. On-State Resistance Test Circuit

$$r_{on} = \frac{V_I - V_O}{2 \times 10^{-3}} \Omega$$

Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$
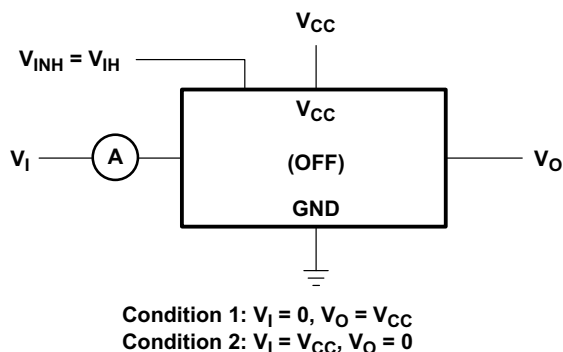
Figure 3. Off-State Switch Leakage-Current Test Circuit

$V_I = V_{CC}$ or GND
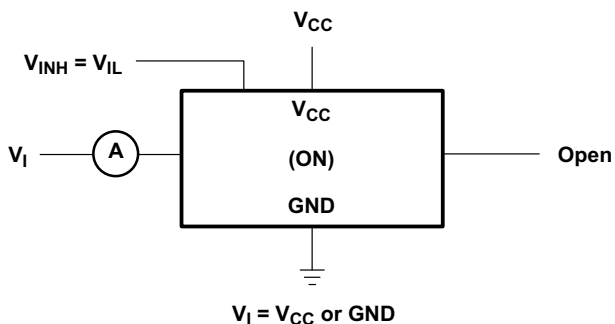
Figure 4. On-State Switch Leakage-Current Test Circuit
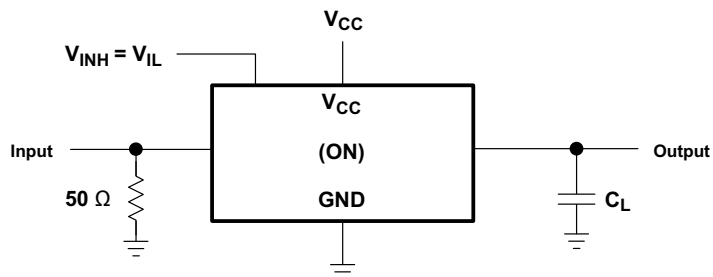
Figure 5. Propagation Delay Time, Signal Input to Signal Output

Product Folder Links: *SN74LV4051A*

Parameter Measurement Information (continued)
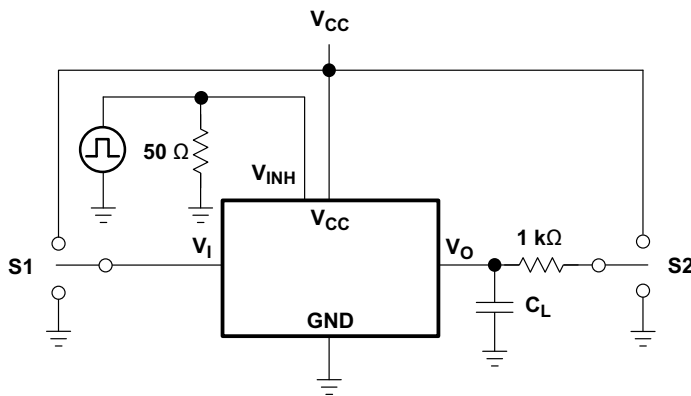
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT
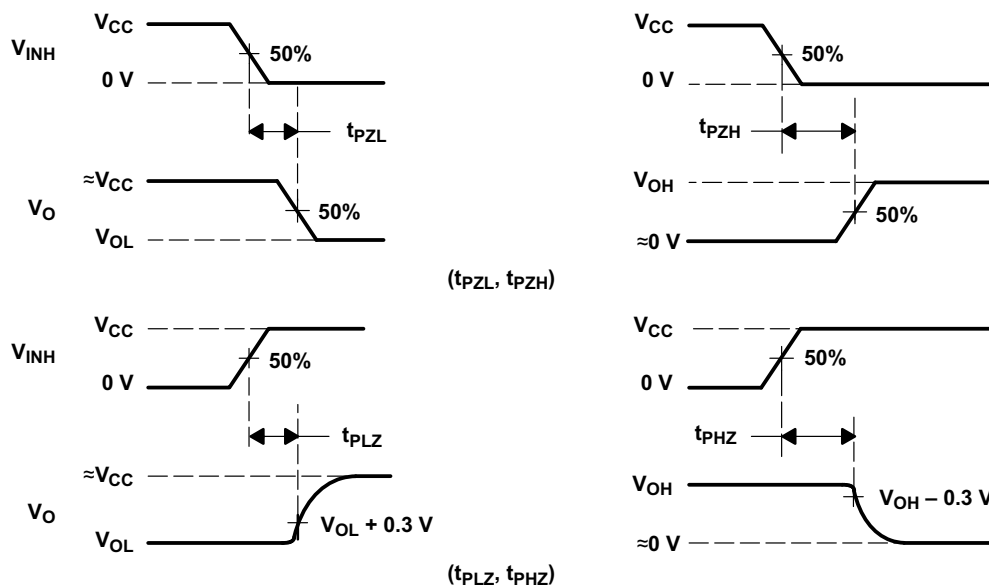
VOLTAGE WAVEFORMS

Figure 6. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output
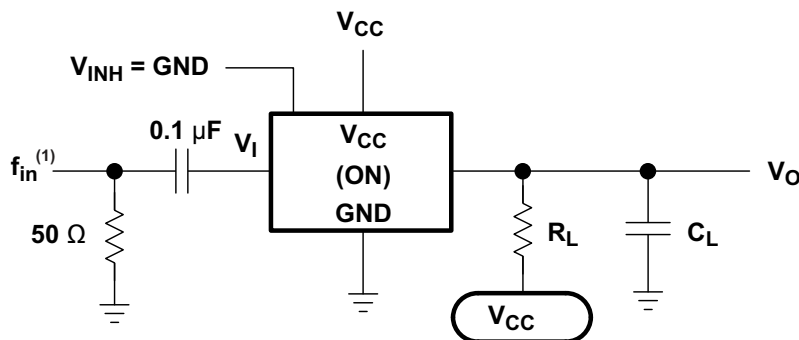
(1) f_{in} is a sine wave.

Figure 7. Frequency Response (Switch On)

Parameter Measurement Information (continued)
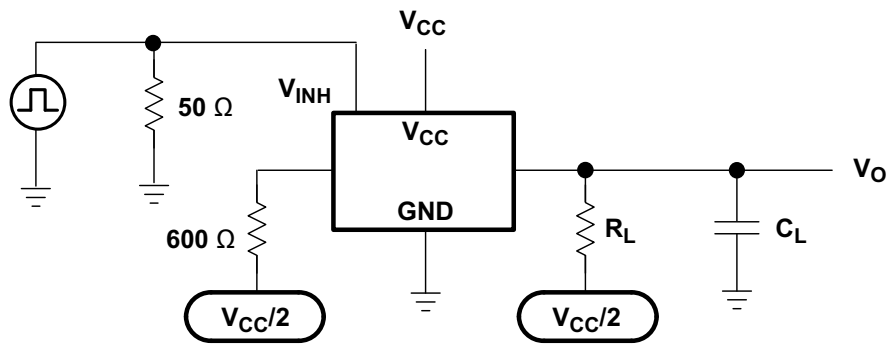
Figure 8. Crosstalk (Control Input, Switch Output)
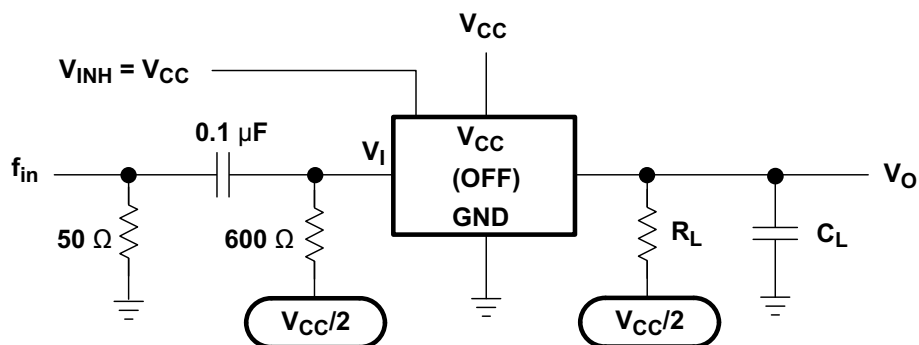
Figure 9. Feedthrough Attenuation (Switch Off)
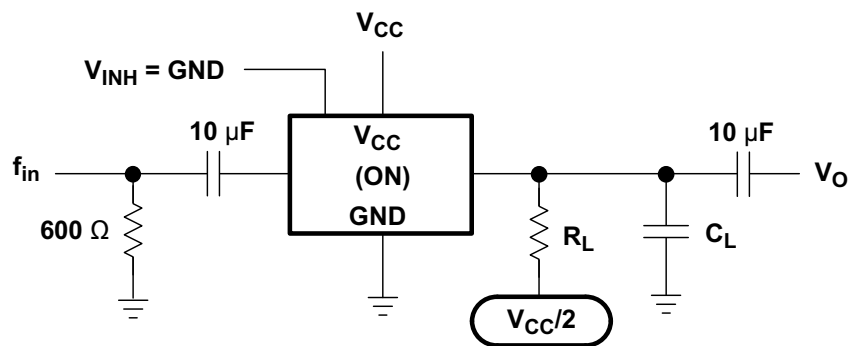
Figure 10. Sine-Wave Distortion

8 Detailed Description

8.1 Overview

The SN74LV4051A device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows for the selection of one of these signals at a time for analysis or propagation.

8.2 Functional Block Diagram
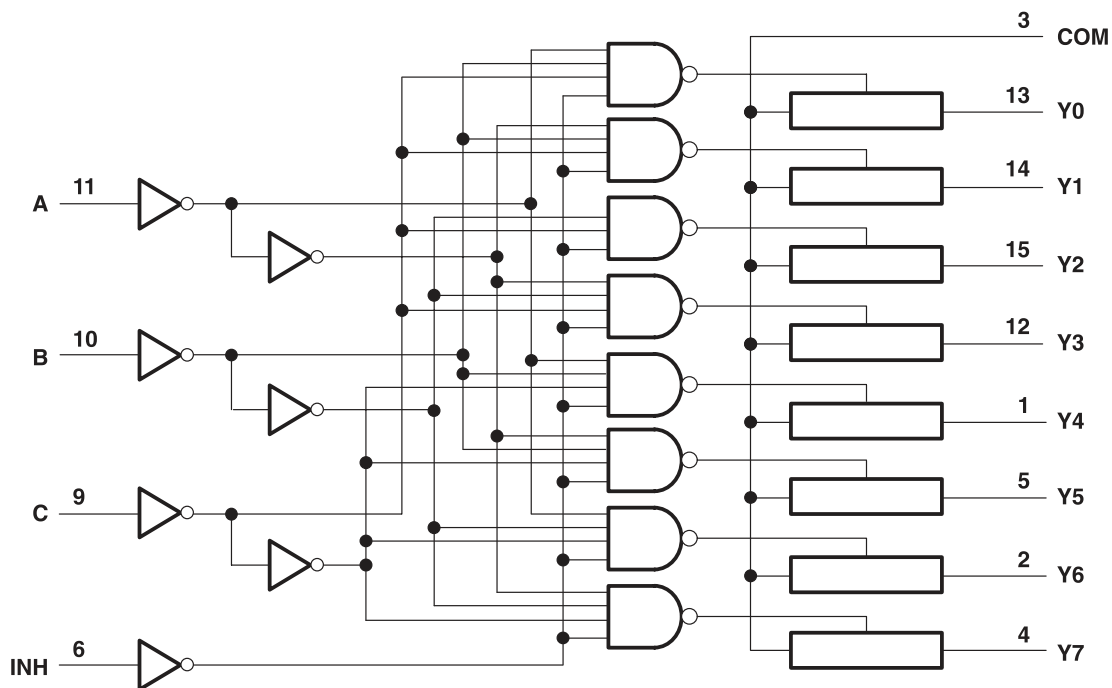
8.3 Feature Description

The SN74LV4051A device contains one 8-channel multiplexer for use in a variety of applications and can also be configured as demultiplexer by using the COM pin as an input and the Yn pins as outputs. This device is qualified to operate in the temperature range –40°C to +85°C (maximum depends on package type).

8.4 Device Functional Modes

Table 1. Function Table

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

Product Folder Links: *SN74LV4051A*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In Figure 11, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller unit (MCU).

9.2 Typical Application
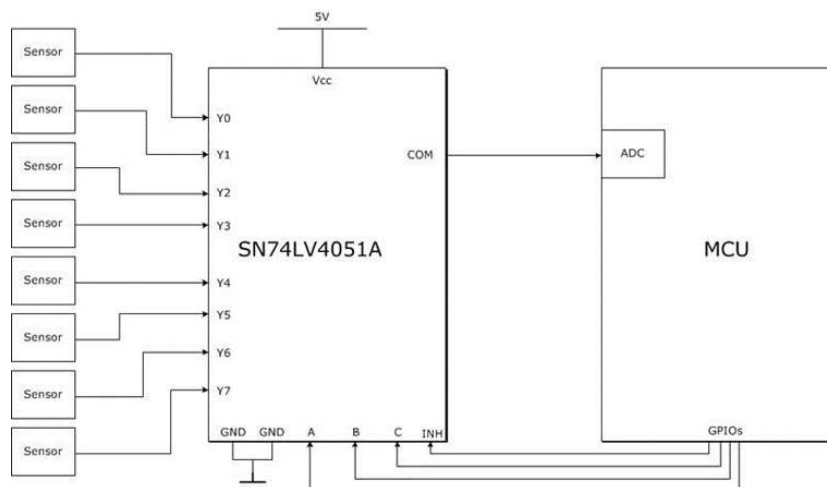
Figure 11. Example of Multiplexer Use With Analog Sensors and the ADC of an MCU

9.2.1 Design Requirements

Designing with the SN74LV4051A device requires a stable input voltage between 2 V (see *Recommended Operating Conditions* for details) and 5.5 V. Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

9.2.2 Detailed Design Procedure

Normally, processing eight different analog signals requires eight separate ADCs, but Figure 11 shows how to achieve this using only one ADC and four GPIOs (general-purpose input/outputs).

Typical Application (continued)

9.2.3 Application Curve
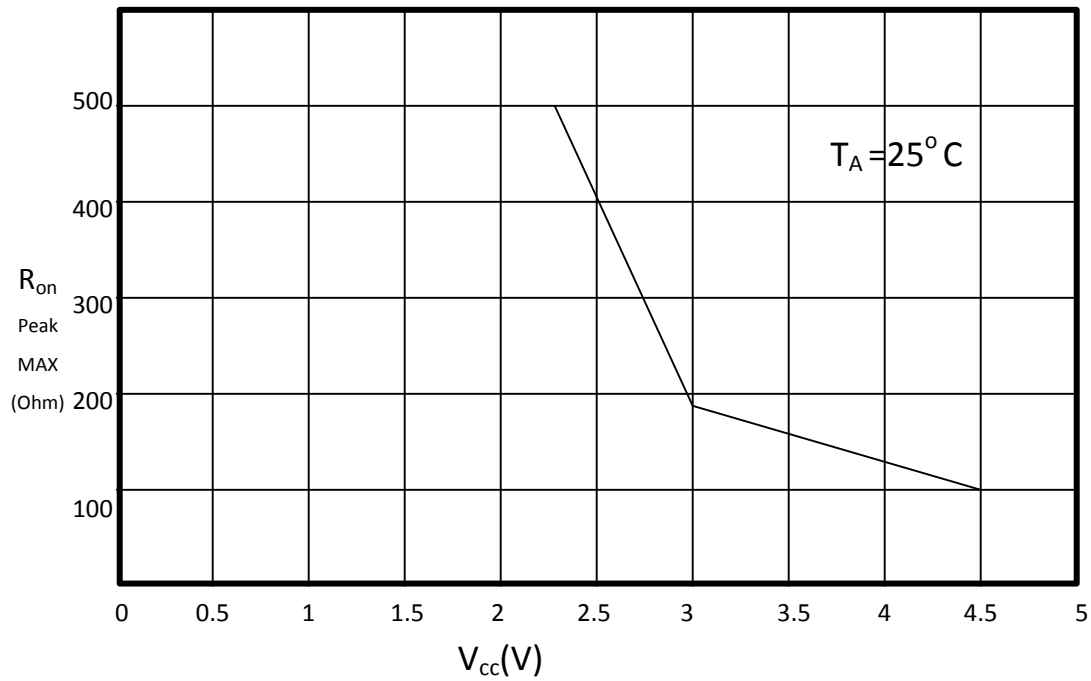
Figure 12. Plot at 25°C for V$_{CC}$ vs Max R$_{ON(peak)}$

Product Folder Links: *SN74LV4051A*

10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

11 Layout

11.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible (see Figure 13). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1" long. These traces must be designed with a characteristic impedance of either 50-Ω or 75-Ω as required by the application. Do **not** place this device too close to high-voltage switching components because they may cause interference.

11.2 Layout Example
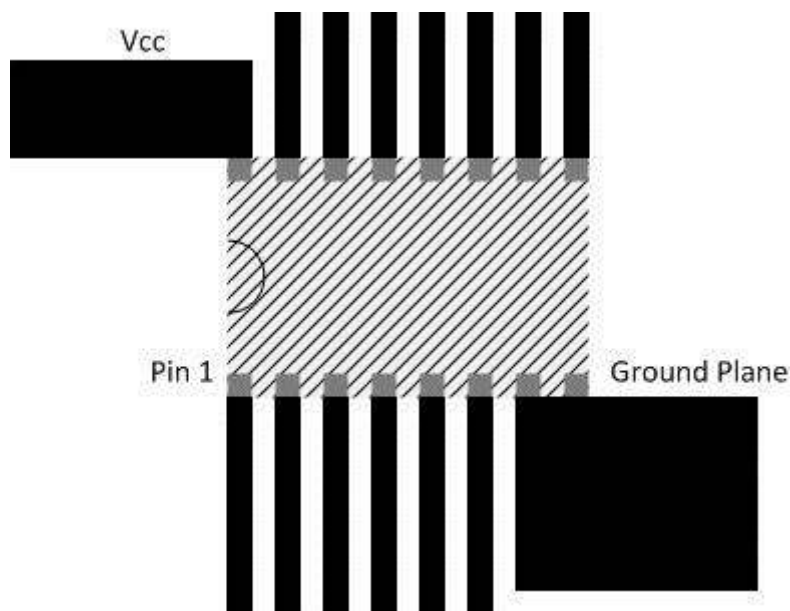
Figure 13. Layout Schematic

Product Folder Links: *SN74LV4051A*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4051AD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4051A	
SN74LV4051ADBR	LIFEBUY	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051ADGVR	LIFEBUY	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051ADGVRG4	LIFEBUY	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV4051A	Samples
SN74LV4051AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4051AN	
SN74LV4051ANSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4051A	
SN74LV4051APW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051APWG4	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LW051A	Samples
SN74LV4051APWRE4	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051APWRG4	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051APWT	LIFEBUY	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	
SN74LV4051ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW051A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4051A :

• Automotive : SN74LV4051A-Q1

• Enhanced Product : SN74LV4051A-EP

NOTE: Qualified Version Definitions:

  • Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

  • Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4051ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4051ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4051ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4051ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4051ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LV4051ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV4051ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV4051ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LV4051APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV4051APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4051APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4051APWT	TSSOP	PW	16	250	356.0	356.0	35.0
SN74LV4051ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
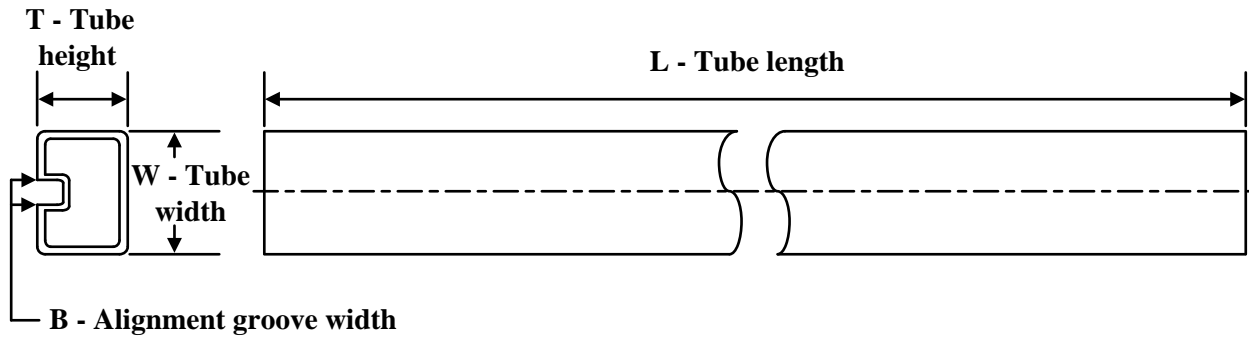
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4051AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV4051AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4051AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4051APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4051APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

8.2 / 7.4 TYP

A

PIN 1 ID AREA

14X 1.27

1   16

10.4 / 10.0 NOTE 3

2X 8.89

8   9

B

5.4 / 5.2 NOTE 4

16X 0.51 / 0.35

⊕ 0.25Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.00 MAX

SEE DETAIL A

0.15 TYP

GAGE PLANE

0.25

0° - 10°

1.05 / 0.55

(1.25)

0.3 / 0.1

DETAIL A
TYPICAL
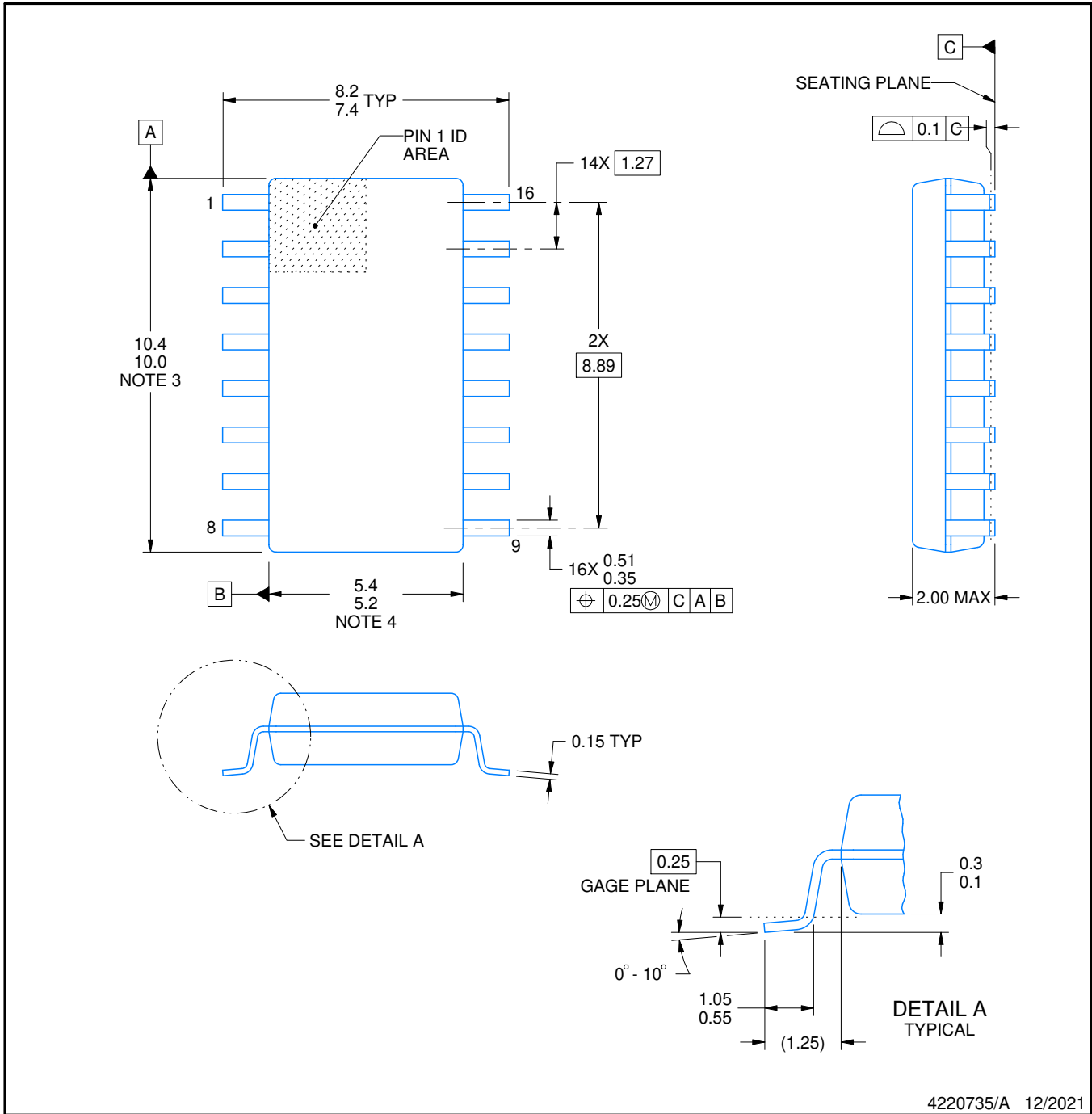
4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
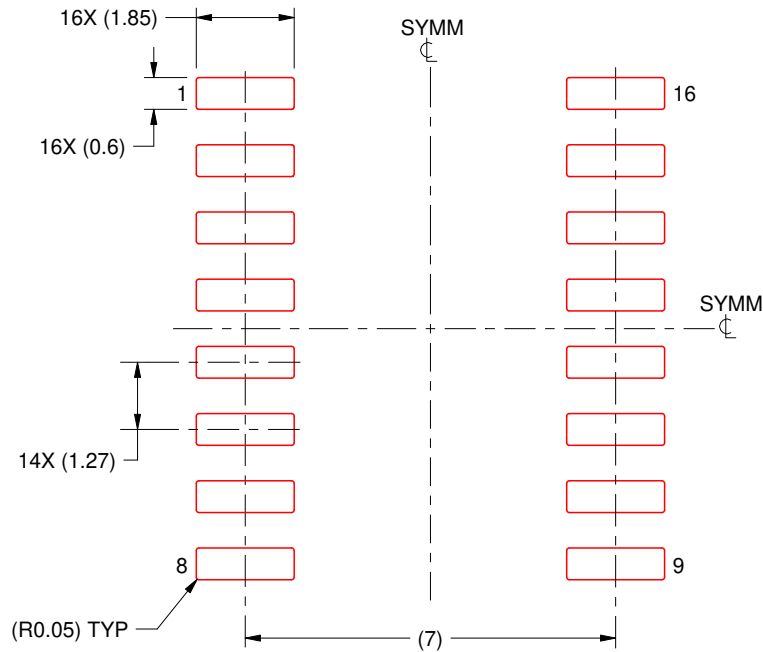
TEXAS INSTRUMENTS
www.ti.com

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX ALL AROUND

0.07 MIN ALL AROUND

NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
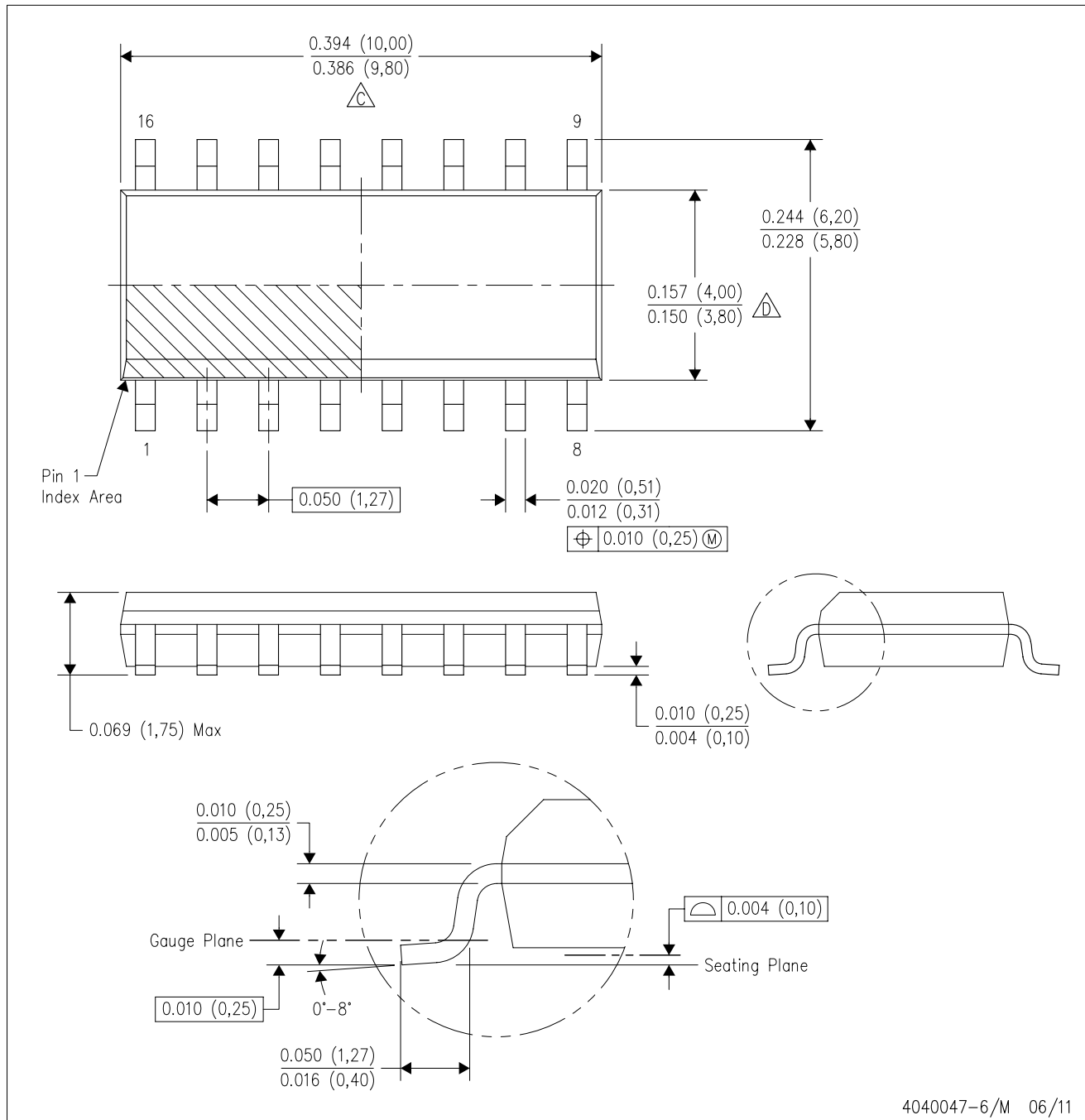BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
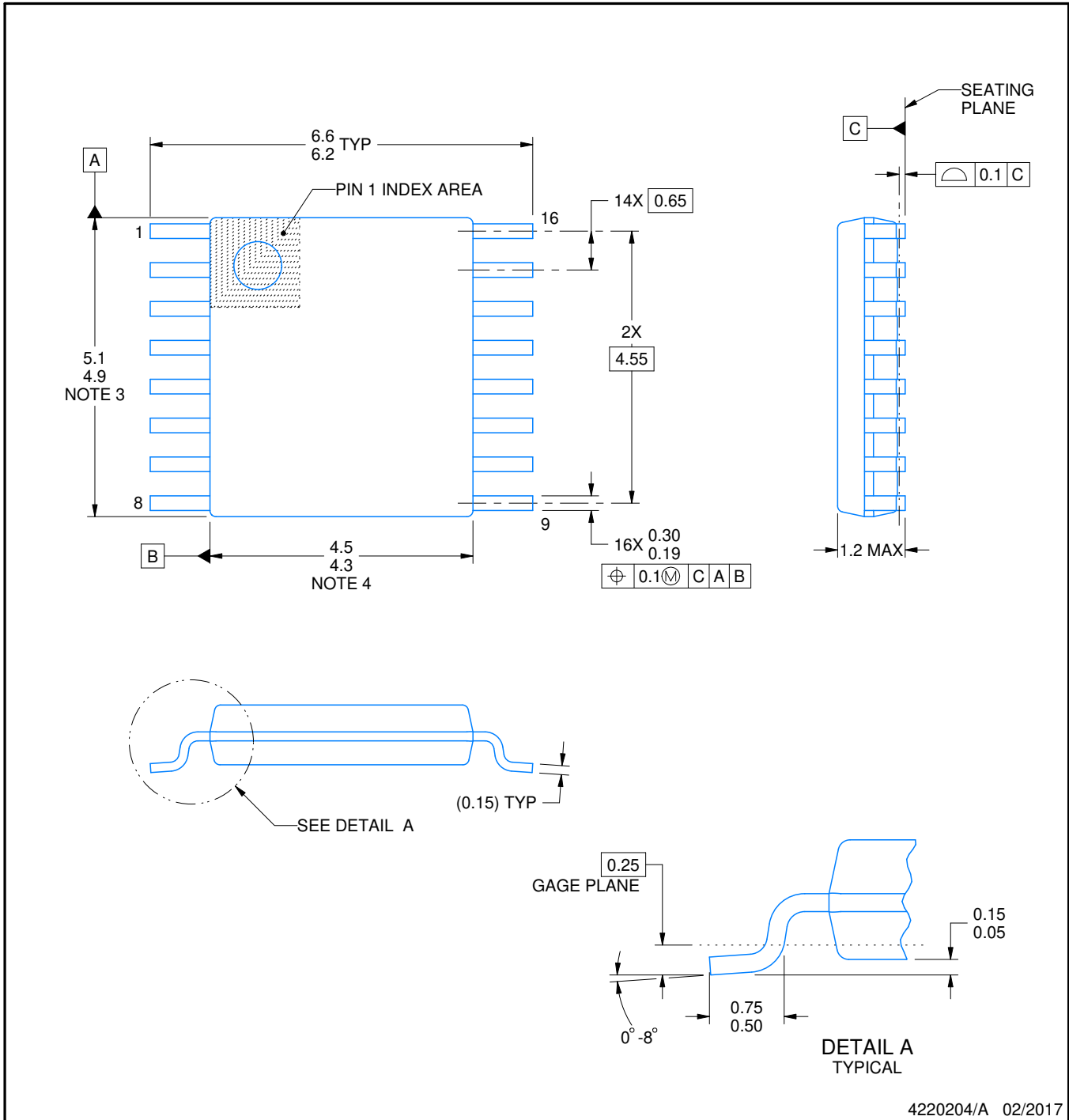
D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047-6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       ⚠C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
       ⚠D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

TEXAS
INSTRUMENTS
www.ti.com

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°
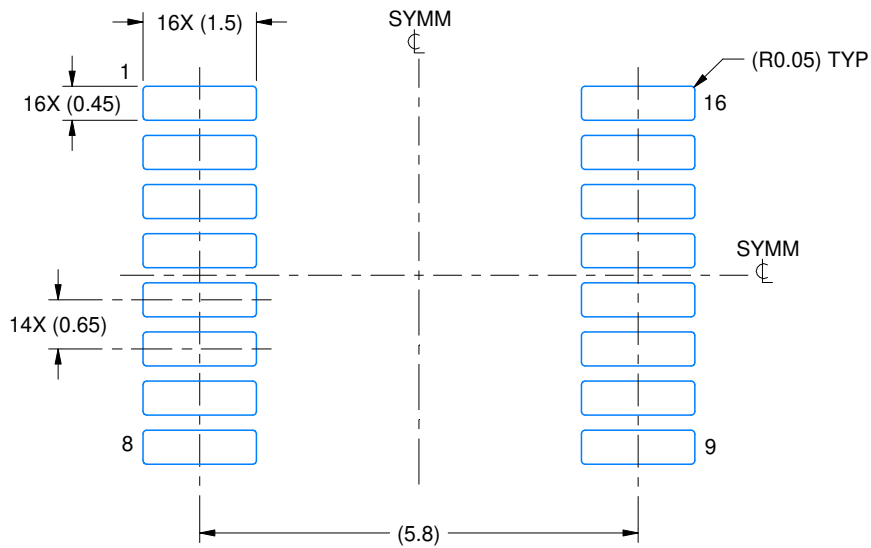
0.75
0.50

DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

(R0.05) TYP

1

16X (0.45)

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
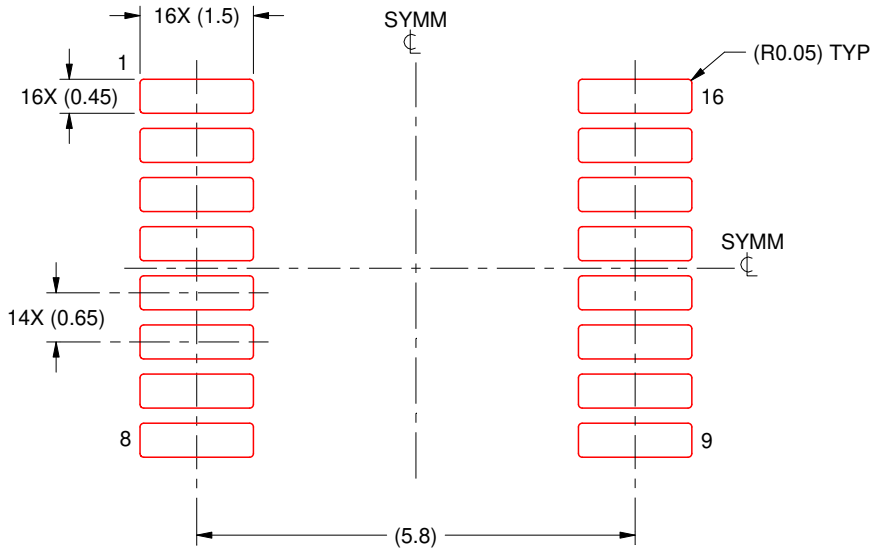
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
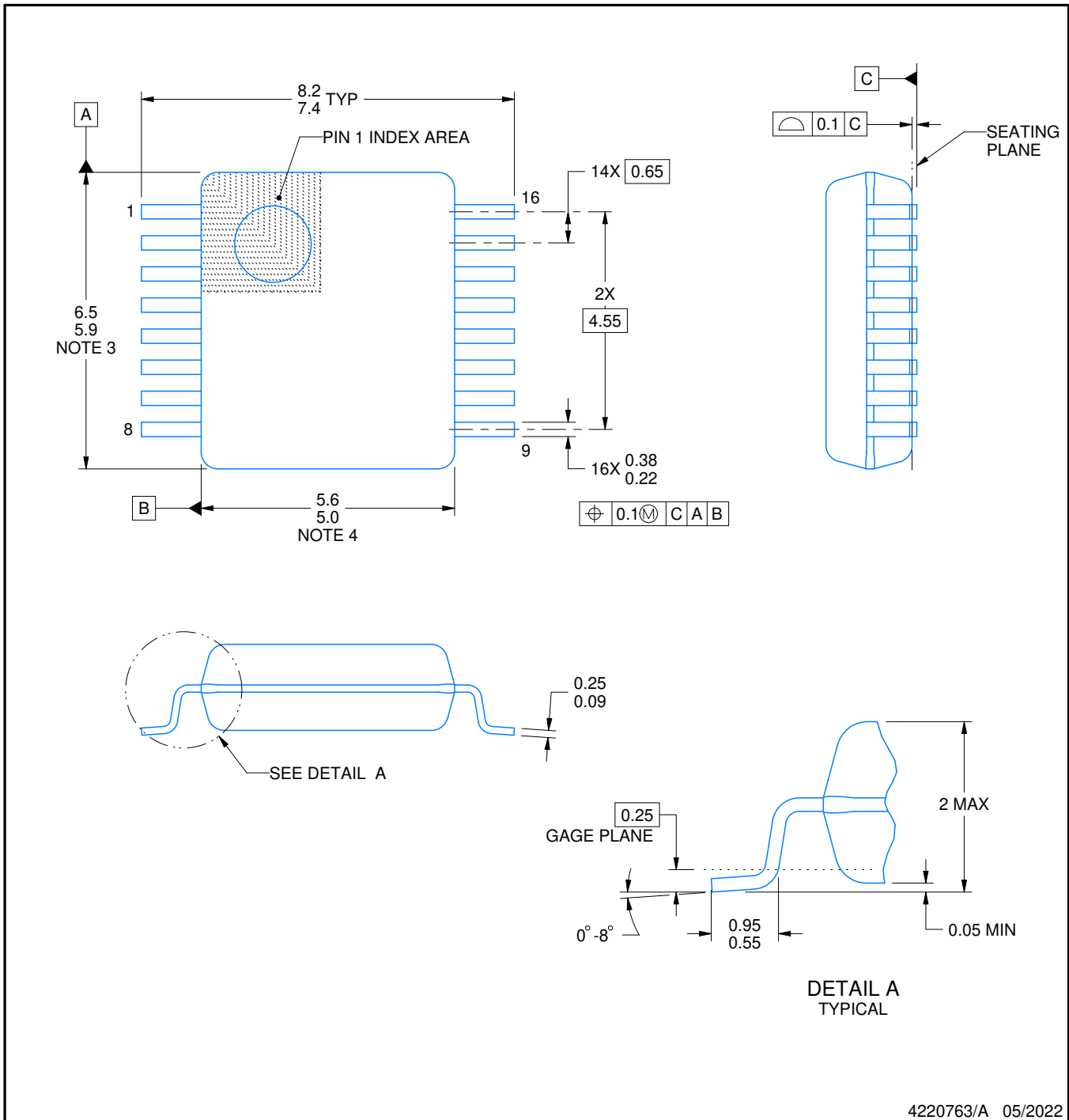9. Board assembly site may have different recommendations for stencil design.

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

16

14X 0.65

2X

4.55

6.5 / 5.9 NOTE 3

8

9

16X 0.38 / 0.22

B

5.6 / 5.0 NOTE 4

⊕ 0.1 Ⓜ C A B

C

◠ 0.1 C

SEATING PLANE

0.25 / 0.09

SEE DETAIL A

0.25 GAGE PLANE

2 MAX

0.95 / 0.55

0°-8°

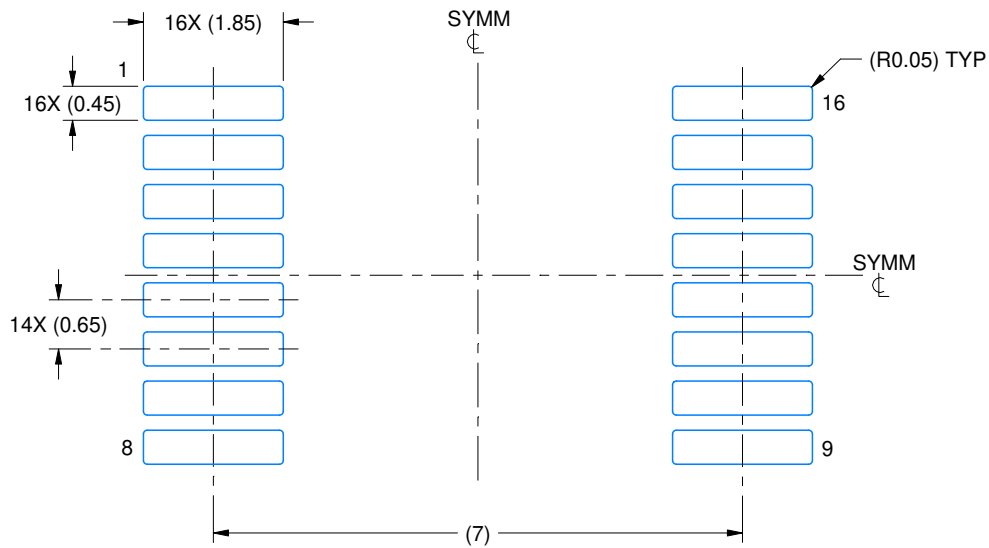0.05 MIN

DETAIL A
TYPICAL

4220763/A   05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

TEXAS INSTRUMENTS
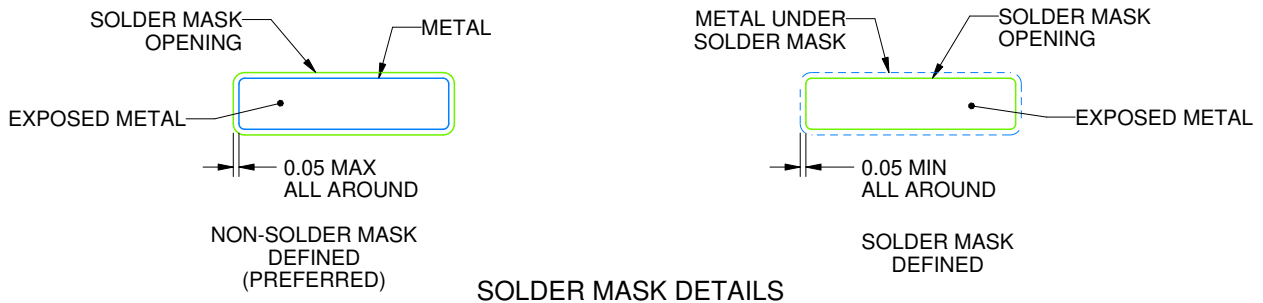www.ti.com

16X (1.85)

1

16X (0.45)

SYMM

16

(R0.05) TYP

SYMM

14X (0.65)

8   9

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING   METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK   SOLDER MASK
                     OPENING

                                   EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
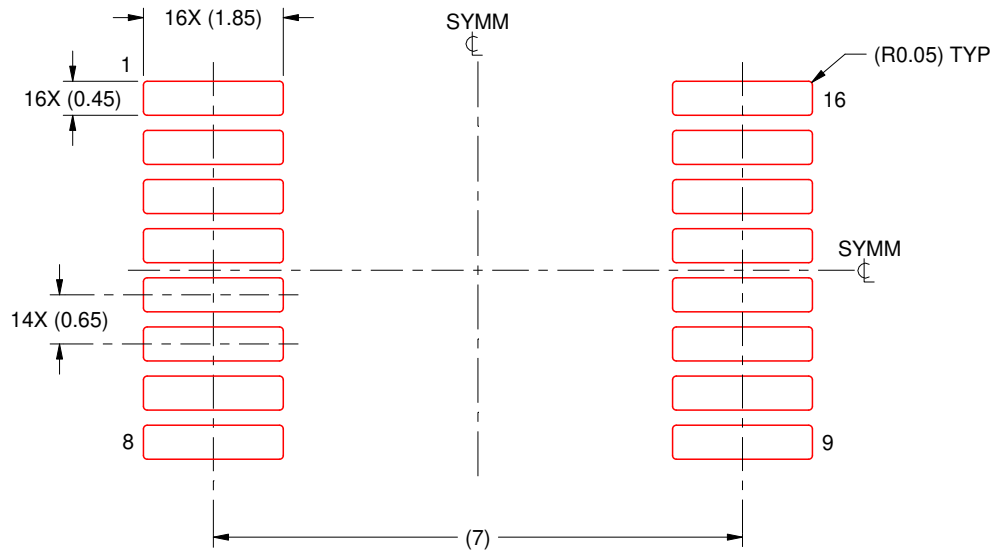
SOLDER MASK DETAILS

4220763/A   05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DB0016A

SSOP - 2 mm max height

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X
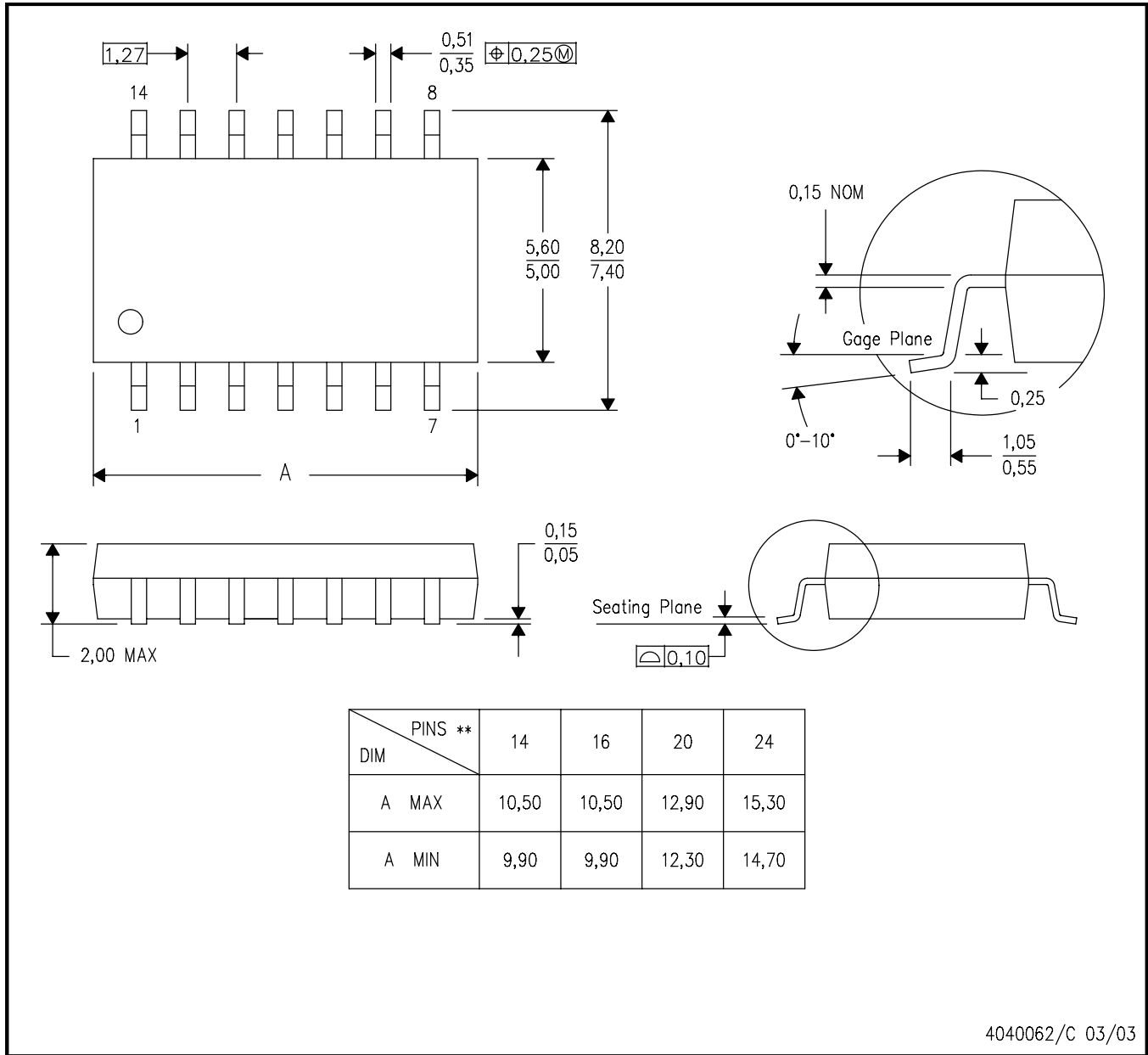
4220763/A   05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

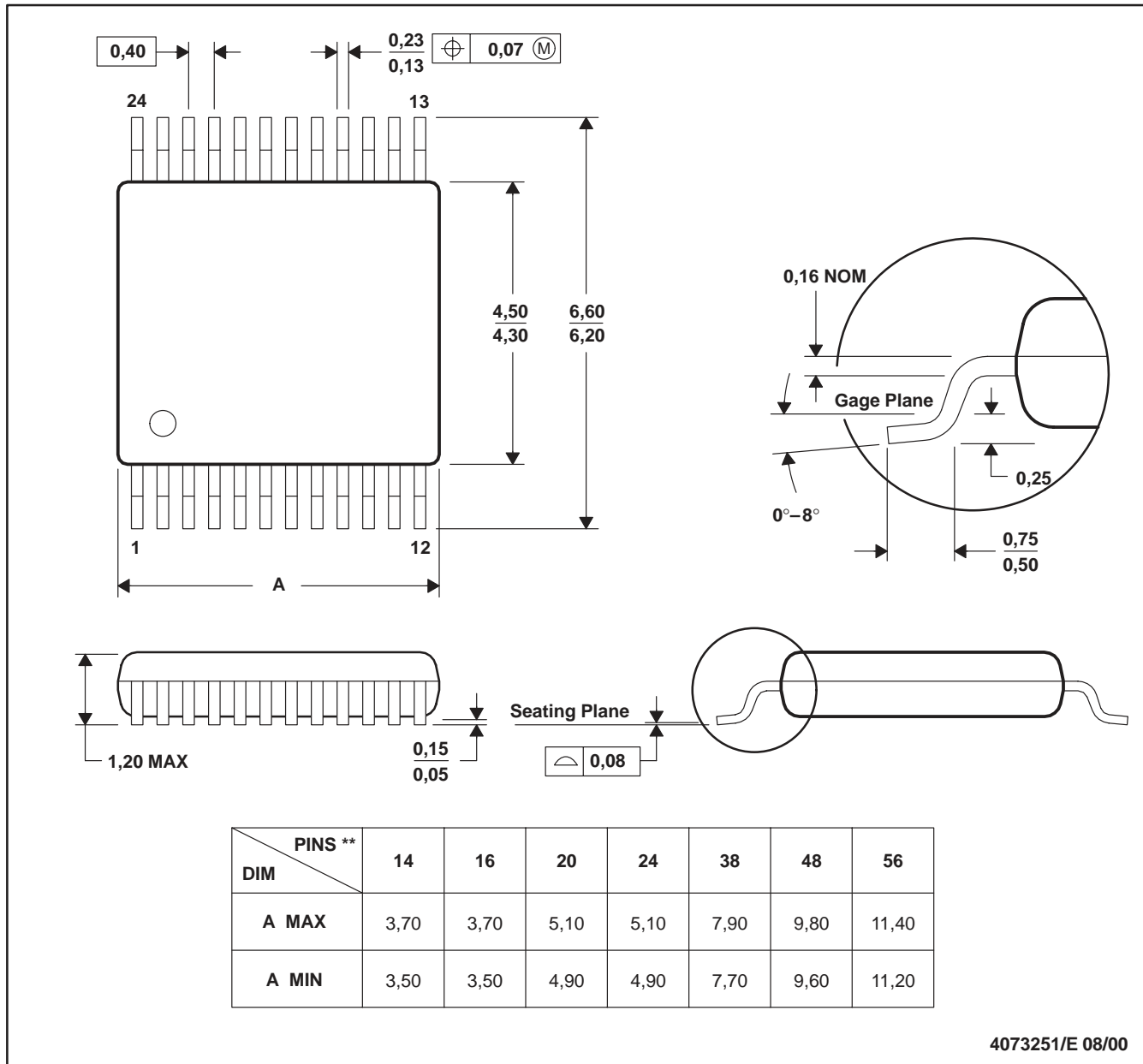| DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
        B.   This drawing is subject to change without notice.
        C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194
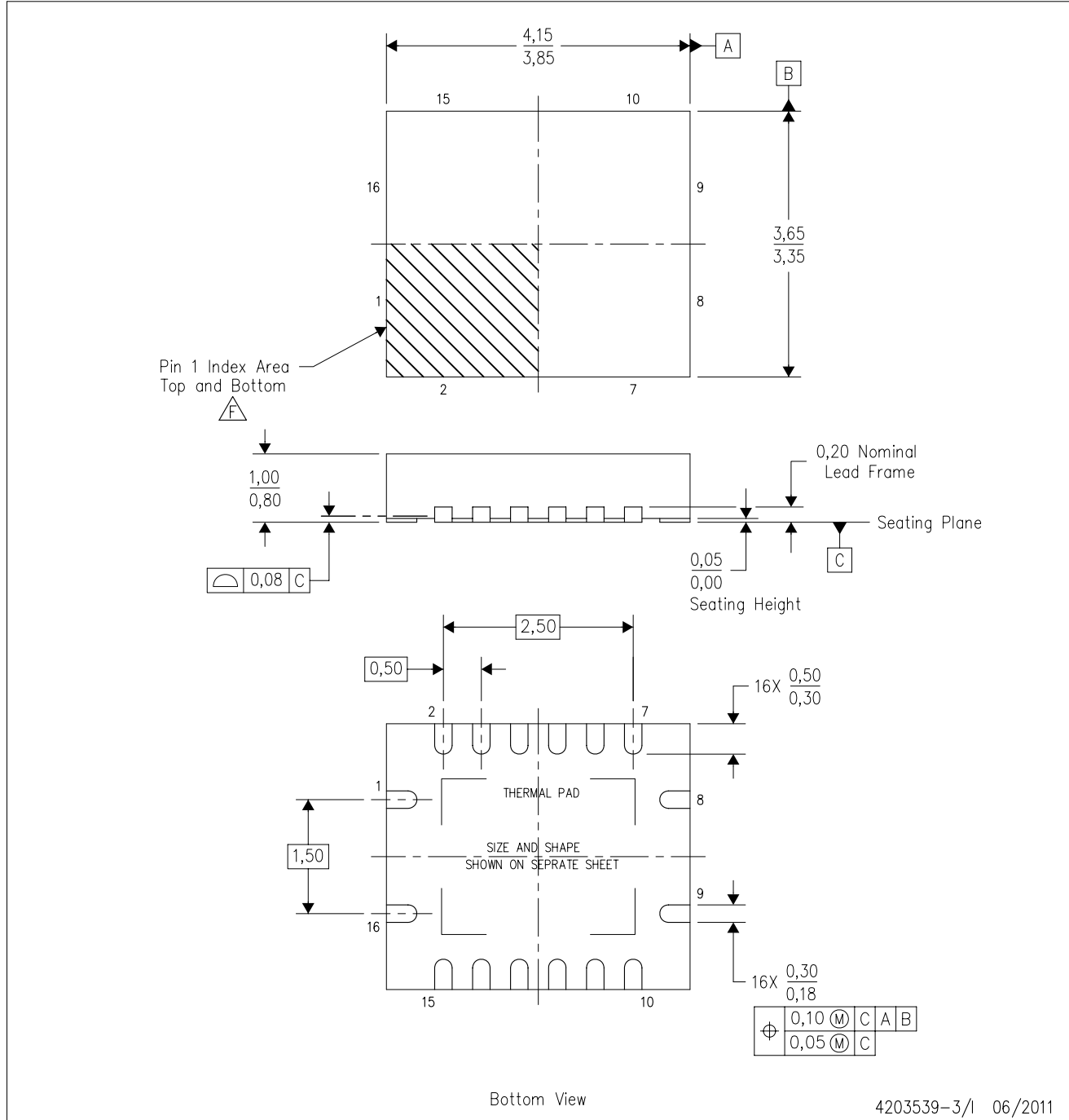
N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD

$\frac{4,15}{3,85}$ A

B

15   10

16   9

8

$\frac{3,65}{3,35}$

1

2   7

Pin 1 Index Area
Top and Bottom

F

0,20 Nominal
Lead Frame

$\frac{1,00}{0,80}$

Seating Plane

0,08 C

$\frac{0,05}{0,00}$
Seating Height

C

2,50

0,50

2   7

16X $\frac{0,50}{0,30}$

1   THERMAL PAD   8

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

1,50

16   9

15   10

16X $\frac{0,30}{0,18}$

0,10 Ⓜ C A B
0,05 Ⓜ C

Bottom View   4203539-3/I   06/2011

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
          B. This drawing is subject to change without notice.
          C. QFN (Quad Flatpack No-Lead) package configuration.
          D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
          E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
          F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
              The Pin 1 identifiers are either a molded, marked, or metal feature.
          G. Package complies to JEDEC MO-241 variation BA.

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RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
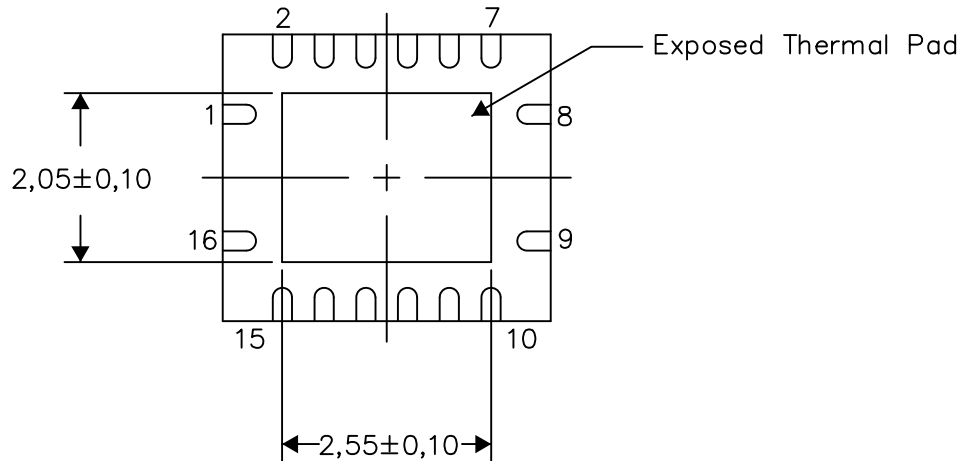
Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P   03/14

NOTE: All linear dimensions are in millimeters

RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

Example
Pad Geometry
(Note C)

All Around

Example Via Layout Design
may vary depending on constraints
(Note D, F)
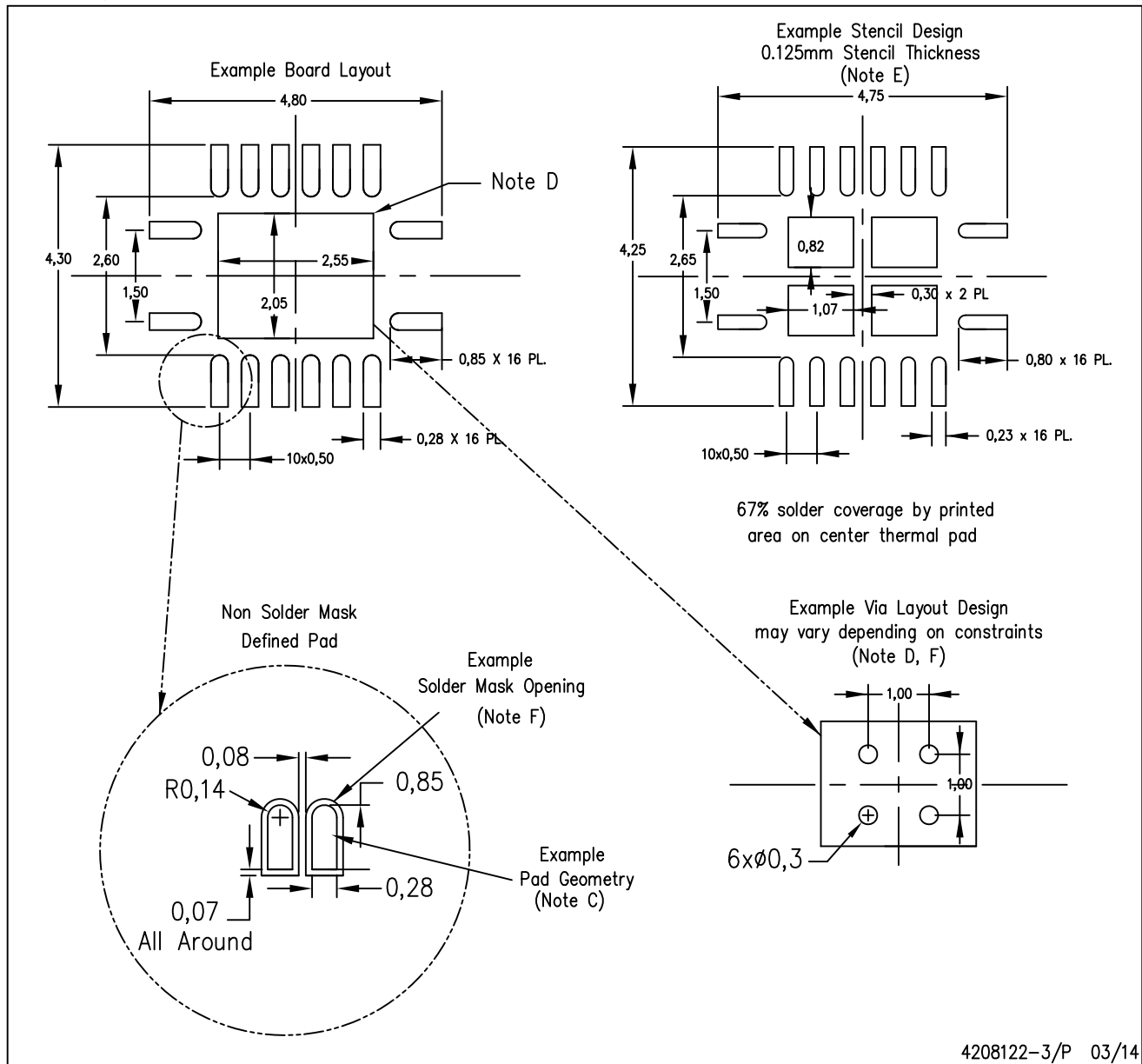
4208122−3/P   03/14

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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