

NHD-5.7-320240WFB-20 Controller Board

TFT Controller Evaluation Board

NHD-	Newhaven Display
5.7-	5.7" Diagonal
320240-	320xRGBx240 pixels
WFB-	Model
20-	20-POS FFC interface (8-bit data) SSD1963 Controller

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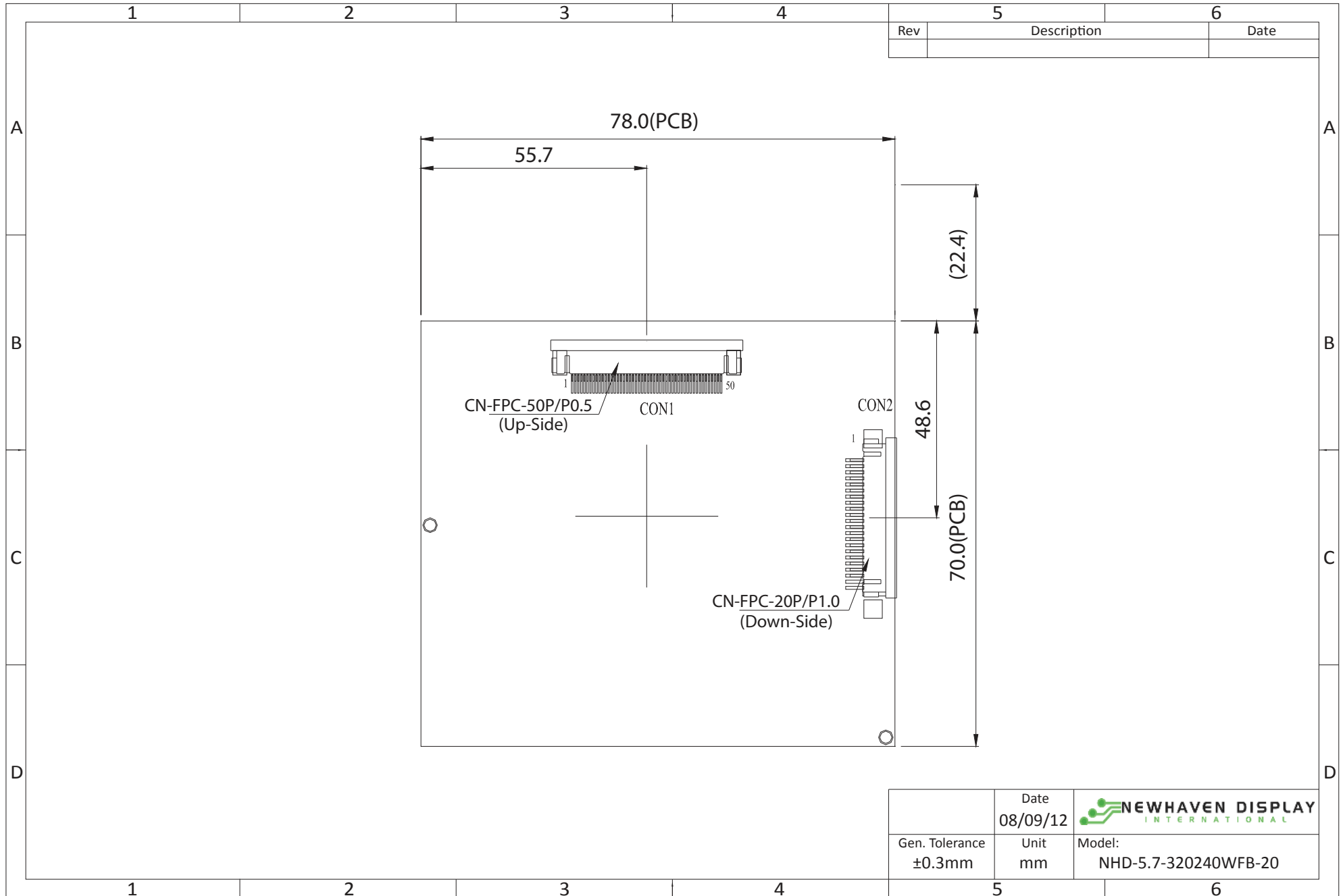
Document Revision History

Revision	Date	Description	Changed by
0	8/9/2012	Initial Release	AK

Functions and Features

- To use for testing, evaluating, or in final production with NHD-5.7-320240WFB displays.

Mechanical Drawing



Pin Description

CON1:

Pin No.	Symbol	I/O	Description	Remark
1	IF1	I	Input data format control (Note1)	Note1
2	IF2	I	Input data format control (Note1)	Note1
3	POL	O	Polarity Signal connect to VCOM driving circuit.	Note3
4	RESET	I	Hardware reset.	
5	SPENA	I	Chip select	Note2
6	SPCL	I	Serial Clock	Note2
7	SPDA	I/O	Serial Data	
8	B0	I	Blue Data bit (LSB)	
9	B1	I	Blue Data bit	
10	B2	I	Blue Data bit	
11	B3	I	Blue Data bit	
12	B4	I	Blue Data bit	
13	B5	I	Blue Data bit	
14	B6	I	Blue Data bit	
15	B7	I	Blue Data bit(MSB)	
16	G0	I	Green Data bit(LSB)	
17	G1	I	Green Data bit	
18	G2	I	Green Data bit	
19	G3	I	Green Data bit	
20	G4	I	Green Data bit	
21	G5	I	Green Data bit	
22	G6	I	Green Data bit	
23	G7	I	Green Data bit(MSB)	
24	R0	I	Red Data bit(LSB)	
25	R1	I	Red Data bit	
26	R2	I	Red Data bit	
27	R3	I	Red Data bit	
28	R4	I	Red Data bit	
29	R5	I	Red Data bit	
30	R6	I	Red Data bit	
31	R7	I	Red Data bit(MSB)	
32	Hsync	I	Horizontal synchronous signal	
33	Vsync	I	Vertical synchronous signal	
34	Data CLK	I	Dot data clock	
35	AVDD(analog)	I	Analog power: 4.5V-5.5V	
36	AVDD(analog)	I	Analog power: 4.5V-5.5V	
37	VDD(digital)	I	Digital power: 3V-3.5V	
38	VDD(digital)	I	Digital power: 3V-3.5V	
39	NPC	O	NTSC/PAL mode Auto detection result H:NTSC/L:PAL	
40	VGL	I	Gate off power	
41	VGL	I	Gate off power	
42	UD	I	Up/Down scan setting. H: Reverse scan / L: Normal scan	
43	VGH	I	Gate on power	
44	LRC	I	Shift direction of device internal shift register control.	
45	GND	I	GROUND	
46	VCOM	I	VCOM driving input	Note3
47	VCOM	I	VCOM driving input	
48	ENB	I	Data enable input. Normally pull low.	Note4
49	GND	I	GROUND	
50	GND	I	GROUND	

Recommended LCD connector: 50-pin, 0.5mm pitch FFC connector. Molex 54132-5097

CON2:

Pin No.	Symbol	External Connection	Function Description
1	GND	Power Supply	Ground
2	VDD	Power Supply	Power supply for LCD and logic (3.3V)
3	NC	-	No Connect
4	D/C#	MPU	Register Select signal: 1= Data, 0=Command
5	WR#	MPU	Active LOW Write signal, 8080 MPU interface
6	RD#	MPU	Active LOW Read signal, 8080 MPU interface
7-14	[DB0-DB7]	MPU	Bi-directional data bus lines
15	CS#	MPU	Active LOW Chip Select signal
16	RES#	MPU	Active LOW Reset signal
17	NC	-	No Connect
18	R/L	-	Scan direction 1: Right (Tied internally)
19	U/D	-	Scan direction 0: Down (Tied internally)
20	NC	-	No Connect

Recommended LCD connector: 1.0mm pitch 20-Conductor FFC. Molex 52271-2079

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-20	-	+70	°C
Storage Temperature Range	Tst	Absolute Max	-30	-	+80	°C
Supply Voltage	VDD		3.0	3.3	3.5	V
Supply Current	IDD	VDD=3.3		130		mA
Input High Voltage	VIH		0.8*VDD	-	VDD	V
Input Low Voltage	VIL		0	-	0.2*VDD	V

Controller Information

Built-in SSD1963 controller

Please download specification at http://www.newhavendisplay.com/app_notes/SSD1963.pdf

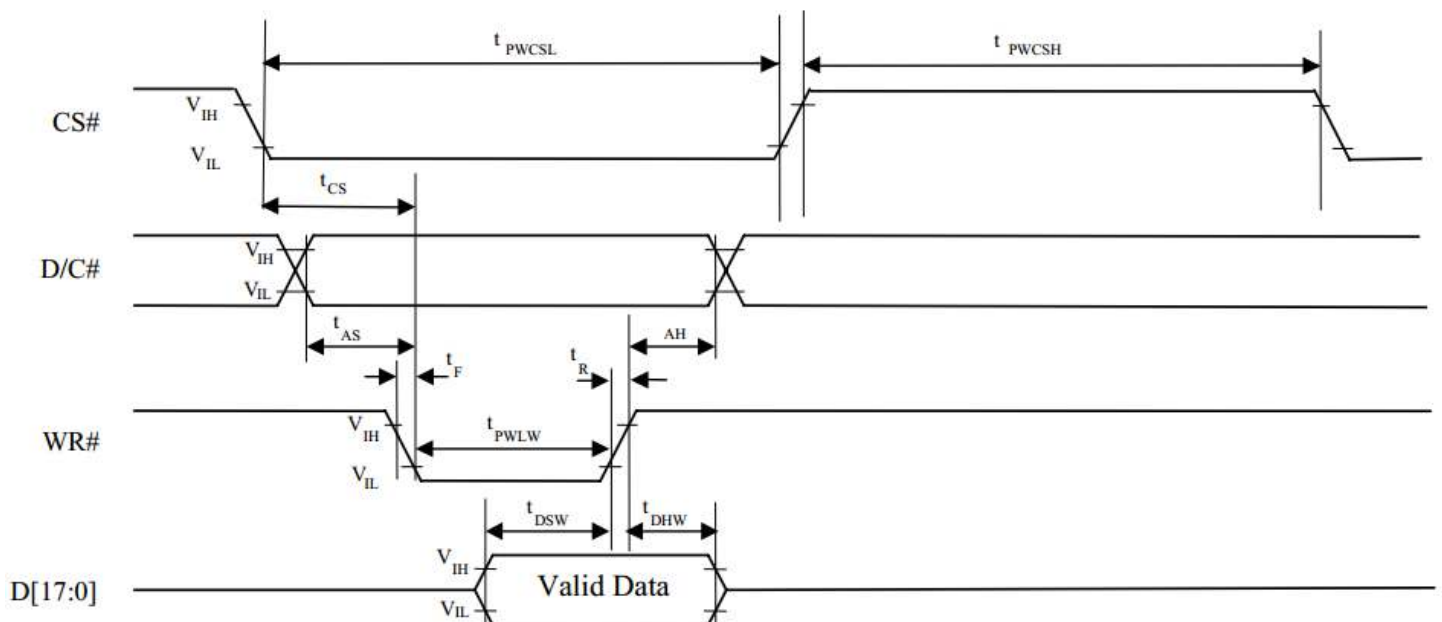
Timing Characteristics

Parallel 8080-series Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{MCLK}	System Clock Frequency*	1	-	110	MHz
t_{MCLK}	System Clock Period*	$1/f_{MCLK}$	-	-	ns
t_{PWCSL}	Control Pulse High Width	13	$1.5 * t_{MCLK}$	-	ns
	Read	30	$3.5 * t_{MCLK}$	-	
t_{PWCSH}	Control Pulse Low Width	13	$1.5 * t_{MCLK}$	-	ns
	Write (next write cycle)	80	$9 * t_{MCLK}$	-	
	Write (next read cycle)	80	$9 * t_{MCLK}$	-	
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	2	-	-	ns
t_{DSW}	Write Data Setup Time	4	-	-	ns
t_{DHW}	Write Data Hold Time	1	-	-	ns
t_{PWLW}	Write Low Time	12	-	-	ns
t_{DHR}	Read Data Hold Time	1	-	-	ns
t_{ACC}	Access Time	32	-	-	ns
t_{PWLR}	Read Low Time	36	-	-	ns
t_R	Rise Time	-	-	0.5	ns
t_F	Fall Time	-	-	0.5	ns
t_{CS}	Chip select setup time	2	-	-	ns
t_{CSH}	Chip select hold time to read signal	3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Parallel 8080-series Interface Timing Diagram (Write Cycle)



Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C 200hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 200hrs	1,2
High Temperature / Humidity Operation	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C , 90% RH , 96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 10 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-55Hz , 15mm amplitude. 60 sec in each of 3 directions X,Y,Z For 15 minutes	3
Static electricity test	Endurance test applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Precautions for using LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms