Development Board EPC90132 Quick Start Guide

40 V Half-bridge with Gate Drive, Using EPC2055

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC90132 is a half bridge development board with onboard gate drives, featuring the 40 V rated EPC2055 GaN field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2055 by including all the critical components on a single board that can be easily connected into the majority of existing converter topologies.

The EPC90132 development board measures 2" x 2" and contains two EPC2055 GaN FET in a half bridge configuration and one EPC2038 GaN FET used to augment the bootstrap supply. The EPC90132 features the uPI Semiconductor uP1966A gate driver. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on EPC2055 please refer to their datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC90132

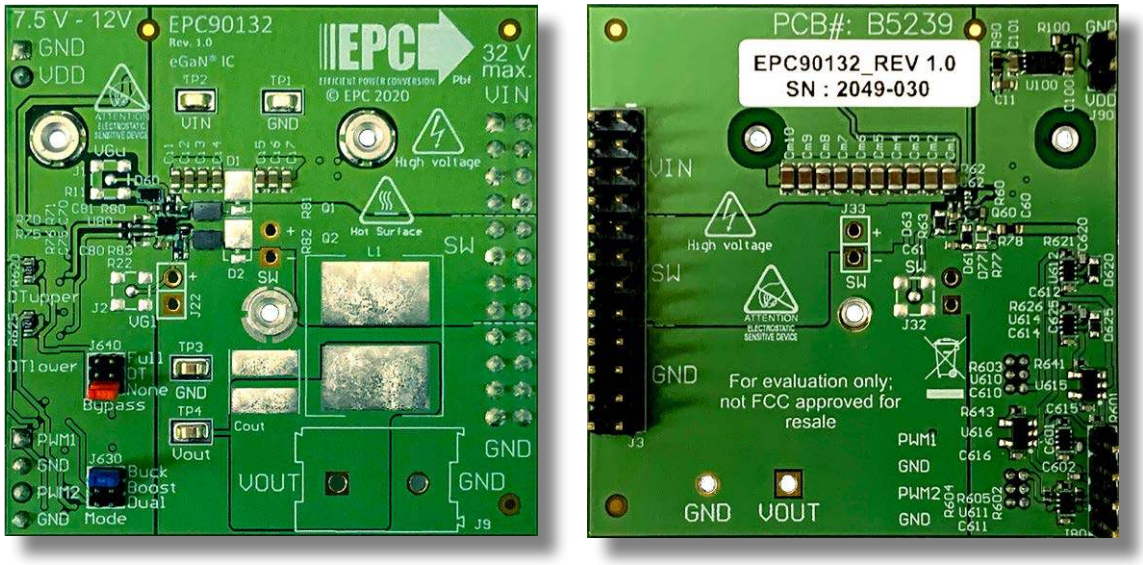
Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Regulator Supply Range		7.5		12	V
V_{IN}	Bus Input Voltage Range(1)				32	V
I_{OUT}	Switch Node Output Current (2)				25	A
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High'	3.5		5.5	V
		Input 'Low'	0		1.5	V
	PWM 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50			ns
	PWM 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10ns	200			ns

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 40 V for EPC2055.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the uP1966A datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view Back view

EPC90132 development board

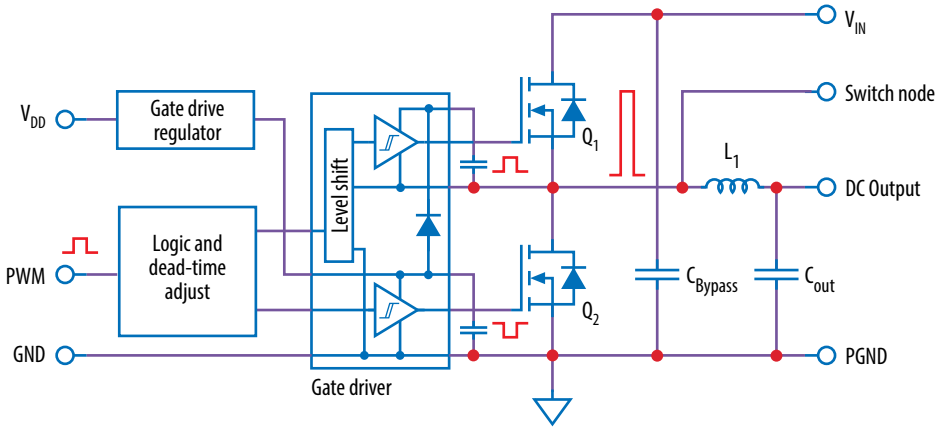


Figure 1: Block diagram of EPC90132 development board default configuration

QUICK START PROCEDURE

The EPC90132 development board is easy to set up as a buck or boost converter to evaluate the performance of two EPC2055 eGaN FETs. This board includes a logic PWM input signal polarity changer used to ensure positive PWM polarity for the switching device when configured in either the buck or boost modes, and can accommodate both single and dual PWM inputs. Furthermore, the board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, this dead time circuit ensures that both the high and low side FETs will not be turned on at the same time thus preventing a shoot-through condition. The dead-time and/or polarity changing circuits can be utilized or bypassed for added versatility.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a single-input buck converter (**blue** jumper across pins 1 & 2 of J630), (b) for a single-input boost converter (**blue** jumpers across pins 3 & 4 of J630), and (c) for a dual-input operation (**blue** jumpers across pins 5 & 6 of J630).

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time.

Dead-time settings

Dead-time is defined as the time between when one FET turns off and the other FET turns on, and for this board is referenced to the input of the gate driver. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET as illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed.

Note: This is the default deadtime and resistor value installed. A minimum dead-time of is 5 ns and maximum of 15 ns is recommended.

Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (Bypass), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.

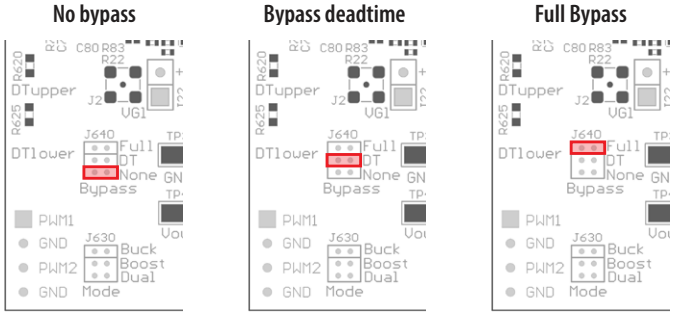


Figure 5: Bypass mode Jumper settings for J640

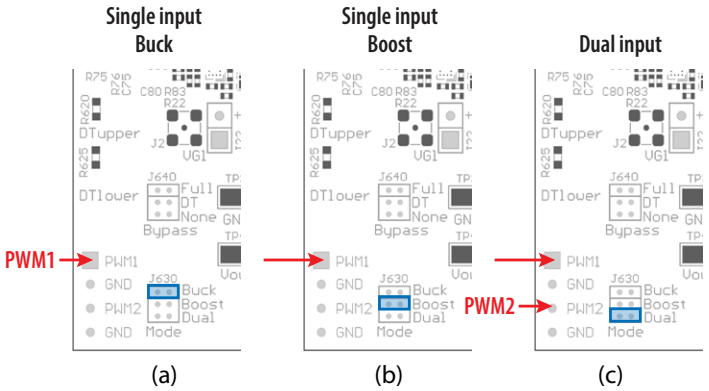


Figure 2: Input mode selection on J630

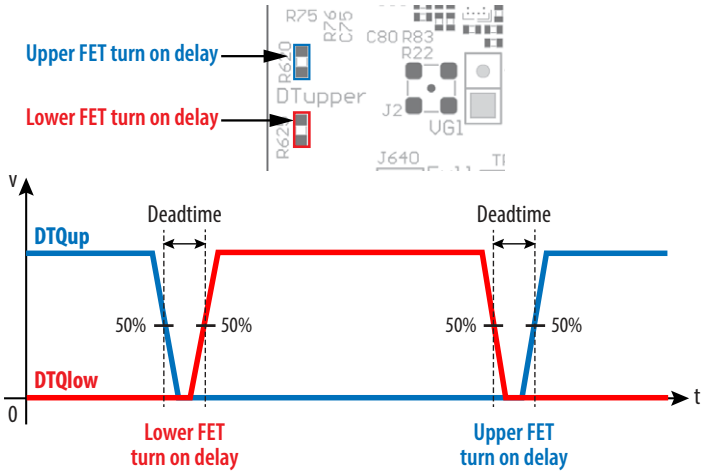


Figure 3: Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)

Figure 4: The required resistance values for R620 or R625 as a function of desired dead-time

In ***no-bypass mode***, figure 5(a) (**red** jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In ***dead-time bypass mode***, figure 5(b) (**red** jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In ***full bypass mode***, Figure 5(c) (**red** jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

Bypass mode warnings

- ***It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.***
- When operating in ***full bypass mode***, the input signal specifications revert to that of the uP1966A gate driver IC. Refer to the uP1966A datasheet for details.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Buck Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the ***buck mode*** J630 ***must*** be selected as shown in figure 6(a).

To select ***Dual Input Buck Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the dual-input mode J630 ***must*** be selected as shown in figure 6(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 6.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is set between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

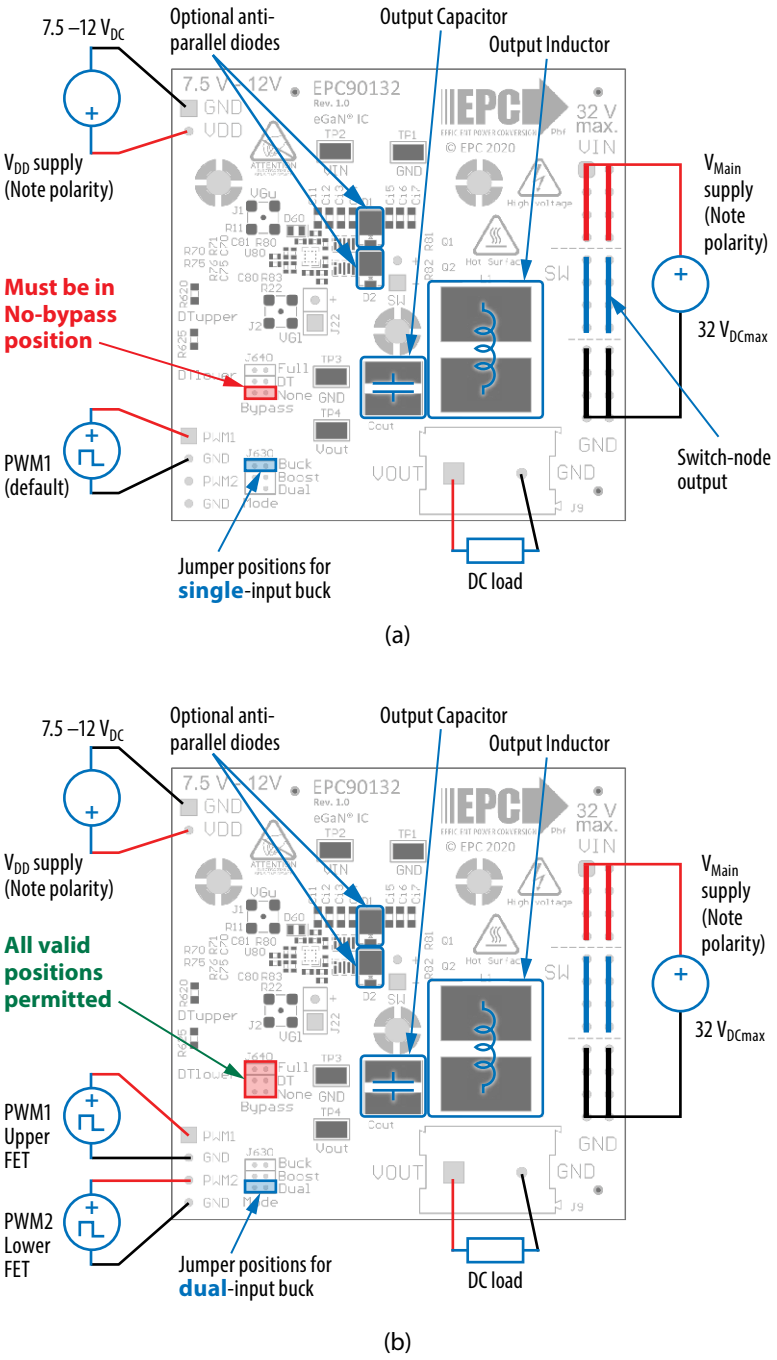


Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Boost Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the boost mode J630 ***must*** be selected as shown in figure.7(a).

To select ***Dual Input Boost Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 7(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the EPC2055 FETs.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (**labeled as VIN**) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to V_{DD} (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. **Making sure the output is not open circuit**, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

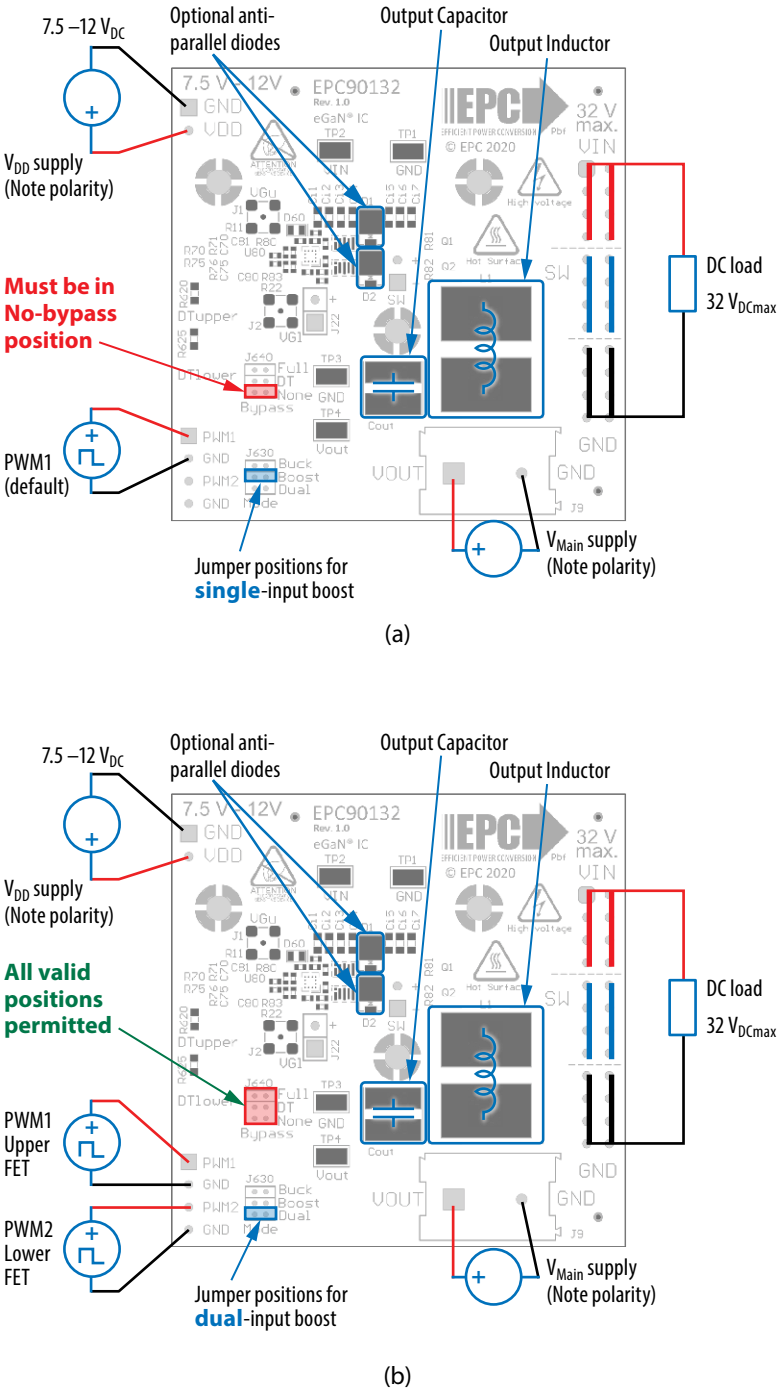


Figure 7: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, output capacitor, PWM, and load connections with corresponding jumper settings.

MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 8. Figure 9 shows an actual switch-node voltage measurement when operating the board as a buck converter.

When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) and an MMCX connector (J32) are provided for switch-node measurement.

A differential probe is recommended for measuring the high-side bootstrap voltage. IsoVu probes from Tektronix has a mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx.

NOTE. For information about measurement techniques, the EPC website offers: "AN023 Accurately Measuring High Speed GaN Transistors" and the How to GaN educational video series, including: HTG09- Measurement

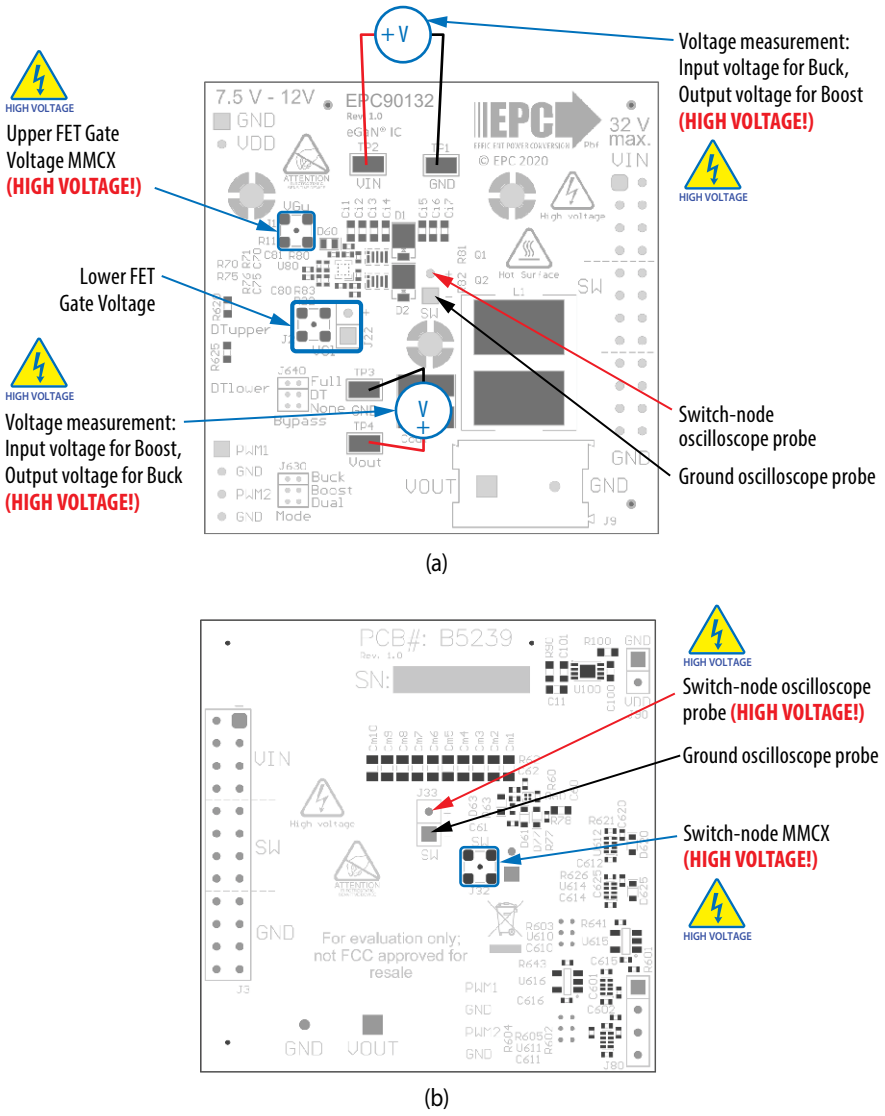
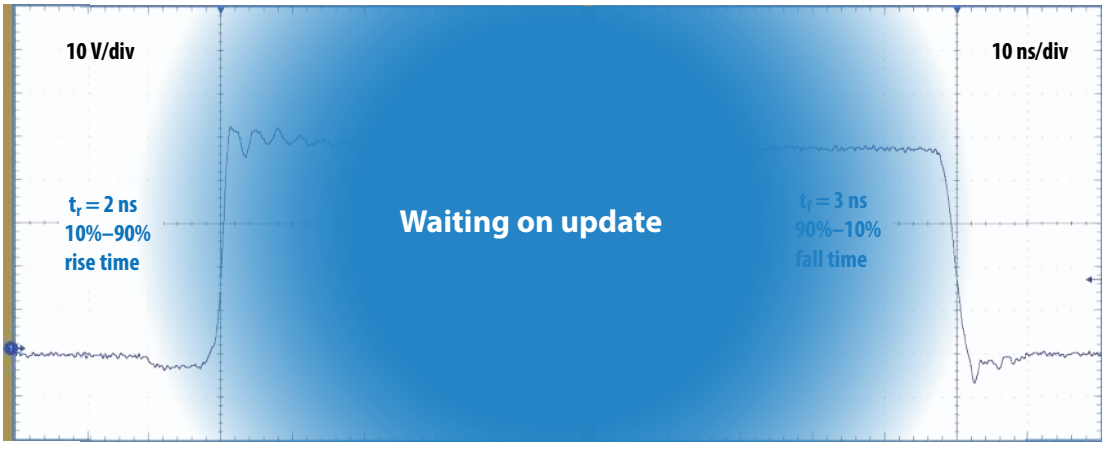


Figure 8: Measurement points (a) top side, (b) bottom side



V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A, f_{sw} = 1 MHz, L = 2.2 µH

Figure 9: Typical switch-node waveform when operated as a buck converter

THERMAL CONSIDERATIONS

The EPC90132 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of a heat-spreader or heatsink and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

The EPC90132 board is equipped with three mechanical spacers that can be used to easily attach a heat-spreader or heatsink as shown in figure 10 (a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/ heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board as shown in figure 10 (b). ***When assembling the heatsink, it may be necessary add a thin insulation layer for components with expose conductors such as capacitors and resistors***.

The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – The TIM becomes compressed during heatsink attached and exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force that maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FETs are substrate that are connected to source and the upper FET will thus be connected to the switch-node. The TIM must therefore provide insulation to prevent short-circuiting the upper FET to the ground.
- **Thermal performance** – The choice of thermal material will affect the thermal performance. Higher thermal conductivity materials will result in higher thermal performance.

EPC recommends t-Global P/N: TG-X 500 µm for the thermal interface material.

The mechanical spacers will accept M2 x 0.4 mm thread screws.

NOTE. The EPC90132 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:

D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

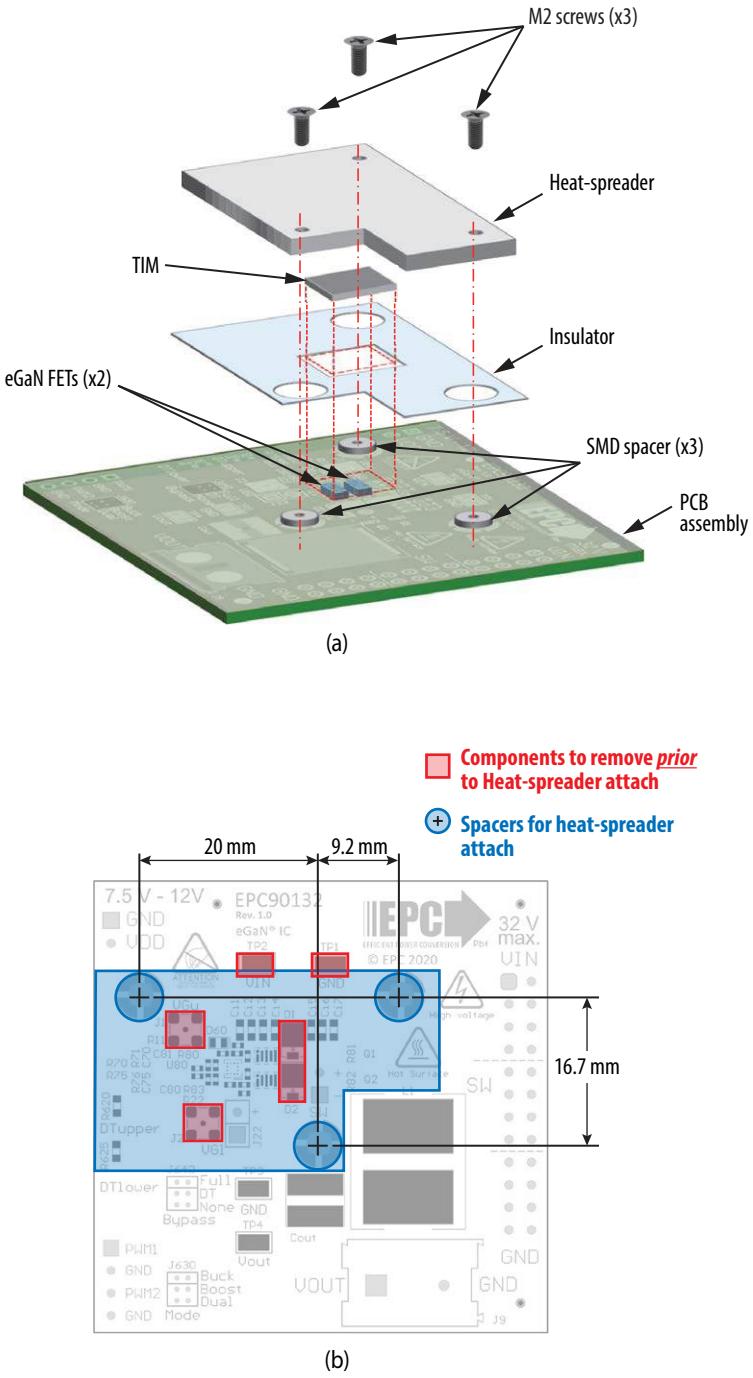


Figure 10: Details for attaching a heatsink to the EPC90132 board. (a) 3D perspective, (b) top view details.

Table 2: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	1	C11	1 µF	TDK	C1608X7R1E105K080AB
2	9	C60, C61, C81, C610, C611, C612, C614, C615, C616	0.1 µF, 25 V	Yageo	CC0402KRX7R8BB104
3	1	C62	22 nF, 25 V	TDK	C1005X7R1E223K050BB
4	1	C80	4.7 µF, 10 V	TDK	C1005X5R1A475K050BC
5	2	C100, C101	1 µF, 25 V	TDK	C1608X7R1E105K
6	2	C601, C602	47 pF, 50 V	Yegeo	CC0402JRNPO9BN470
7	2	C620, C625	100 pF, 50 V	Yegeo	CC0402KRX7R9BB101
8	7	Ci1, Ci2, Ci3, Ci4, Ci5, Ci6, Ci7	1 µF, 50 V	Taiyo Yuden	UMK107AB7105KA-T
9	10	Cm1, Cm2, Cm3, Cm4, Cm5, Cm6, Cm7, Cm8, Cm9, Cm10	4.7 µF, 50 V	TDK	C2012X7R1H475K125AC
10	1	D60	5 V1, 150 mW	Bournes	CD0603-Z5V1
11	4	D61, D63, D620, D625	40 V 30 mA	Diodes Inc.	SDM03U40
12	1	J3	100 mil 2x12 male header	Amphenol	68602-224HLF
13	1	J80	100 mil 1x4 male header	Tyco	4-103185-0-04
14	1	J90	100 mil 1x2 male header	Tyco	4-103185-0-02
15	2	J630, J640	.05" Dual Row Male 3-Pos Vert.	Sullins	GRPB032VWVN-RC
16	1	JP630	50 mil +Handle Blue	Harwin Inc	M50-2030005
17	1	JP640	50 mil +Handle Red	Harwin Inc	M50-2020005
18	2	Q1, Q2	40 V 32 A 3.5 mΩ	EPC	EPC2055
19	1	Q60	100 V 2800 mΩ	EPC	EPC2038
20	1	R62	27 k	Panasonic	ERJ-2GEJ273X
21	1	R63	20 Ω	Stackpole	RMCF0402JT20R0
22	2	R70, R75	2.2 Ω	Panasonic	ERJ-2GEJ2R2X
23	11	R71, R76, R601, R602, R603, R604, R605, R621, R626, R641, R643	10 k	Yageo	RC0402FR-0710KL
24	3	R77, R81, R83	0 Ω	Stackpole	RMCF0402ZT0R00
25	3	R78, R90, R100	0 Ω	Panasonic	ERJ-3GEY0R00V
26	2	R80, R82	1 Ω	Yageo	RC0402FR-071RL
27	2	R620, R625	120 Ω 1%	Yageo	RC0603FR-07120RL
28	3	SO1, SO2, SO3	M2 SMD spacer	Wurth	9774010243R
29	4	TP1, TP2, TP3, TP4	Test point	Keystone	5015
30	1	U80	100 V eGaN Driver	uPI	uP1966A
31	1	U100	5.0 V 250 mA DFN	Microchip	MCP1703T-5002E/MC
32	4	U610, U611, U612, U614	Reconfig Logic	Nexperia	74LVC1G99G
33	2	U615, U616	Bilateral Analog Switch	Texas Instruments	SN74LVC1G66DBV

Optional Components

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	2	C70, C75	100 pF, 50 V	Yegeo	CC0402KRX7R9BB101
2	1	Cout	GenericOutputCap	TBD	TBD
3	2	D1, D2	100 V, 2A	Vishay	SS2PH10-M3
4	1	D77	40 V 300 mA	ST	BAT54KFILM
5	3	J1, J2, J32	MMCX	Molex	734152063
6	1	J9	2 port Euro Block connector	Wurth	691216410002
7	2	J22, J33	100 mil 1x2 male header	Tyco	4-103185-0-02
8	1	L1	GenericOutputInductor	TBD	TBD
9	2	R11, R22	0 Ω	Stackpole	RMCF0402ZT0R00
10	1	R60	4.7 Ω	Panasonic	ERJ-2GEJ4R7X

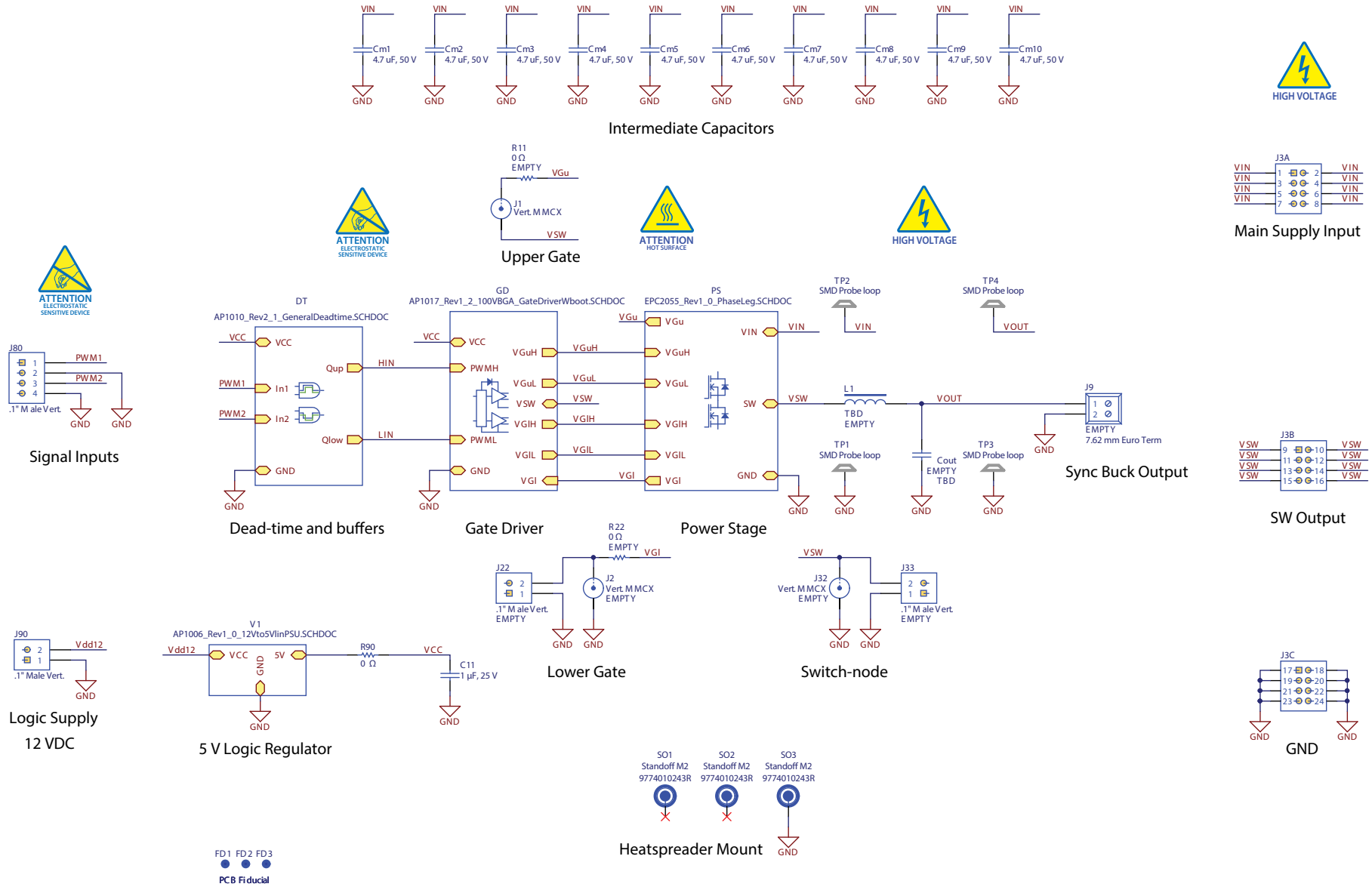


Figure 11: EPC90132 main schematic

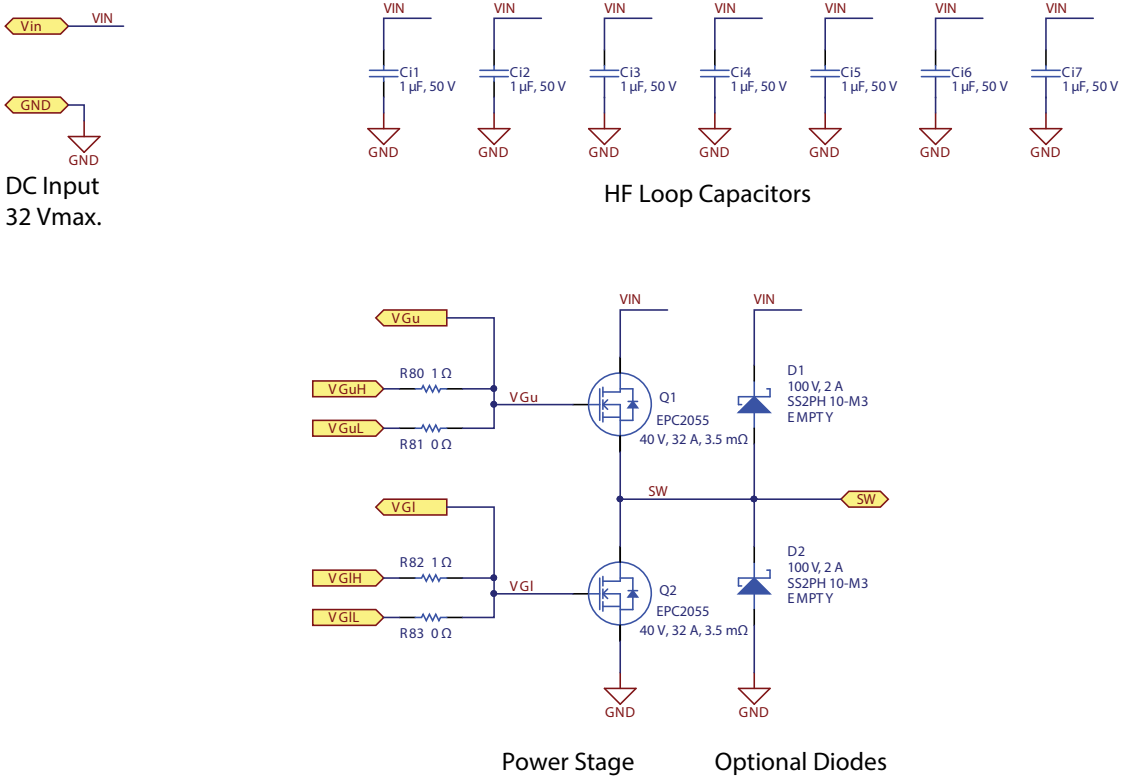


Figure 12: Power Stage schematic using the EPC2055

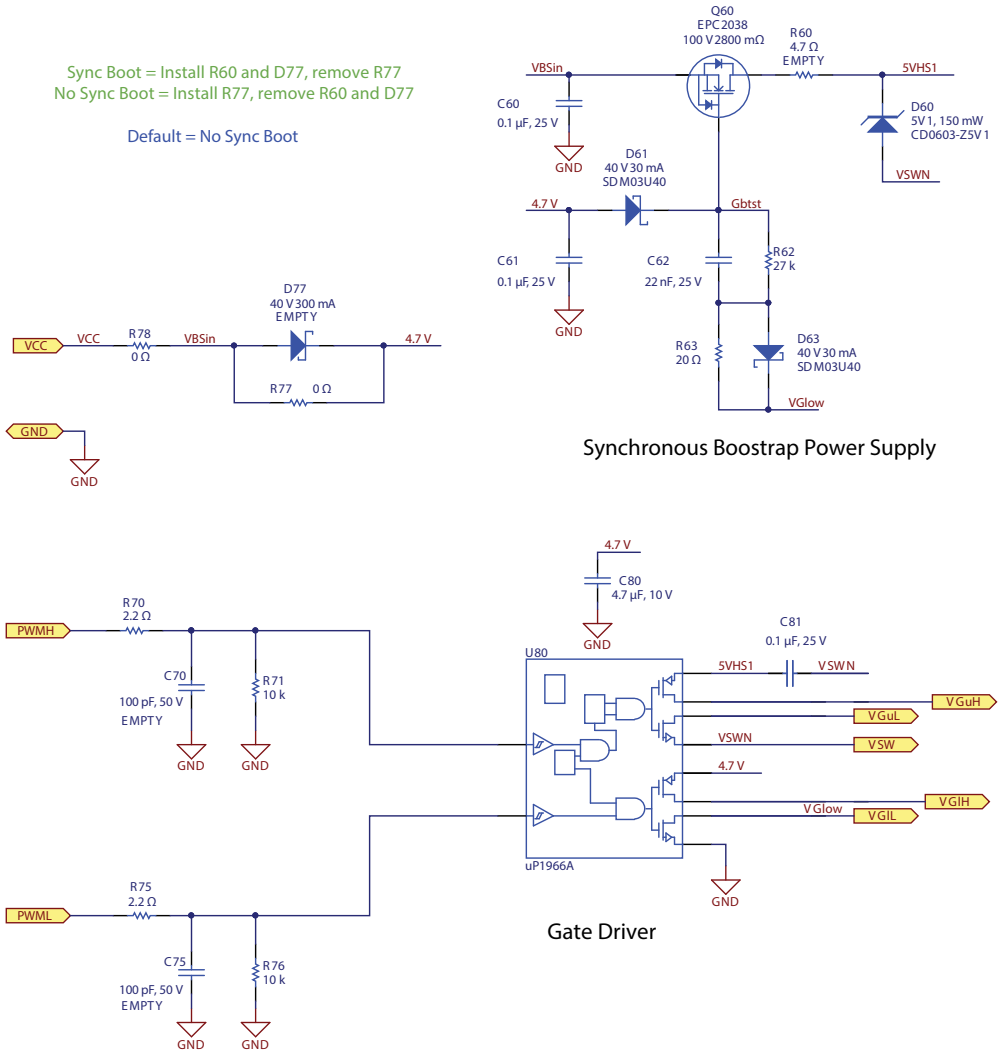


Figure 13: Gate Driver schematic

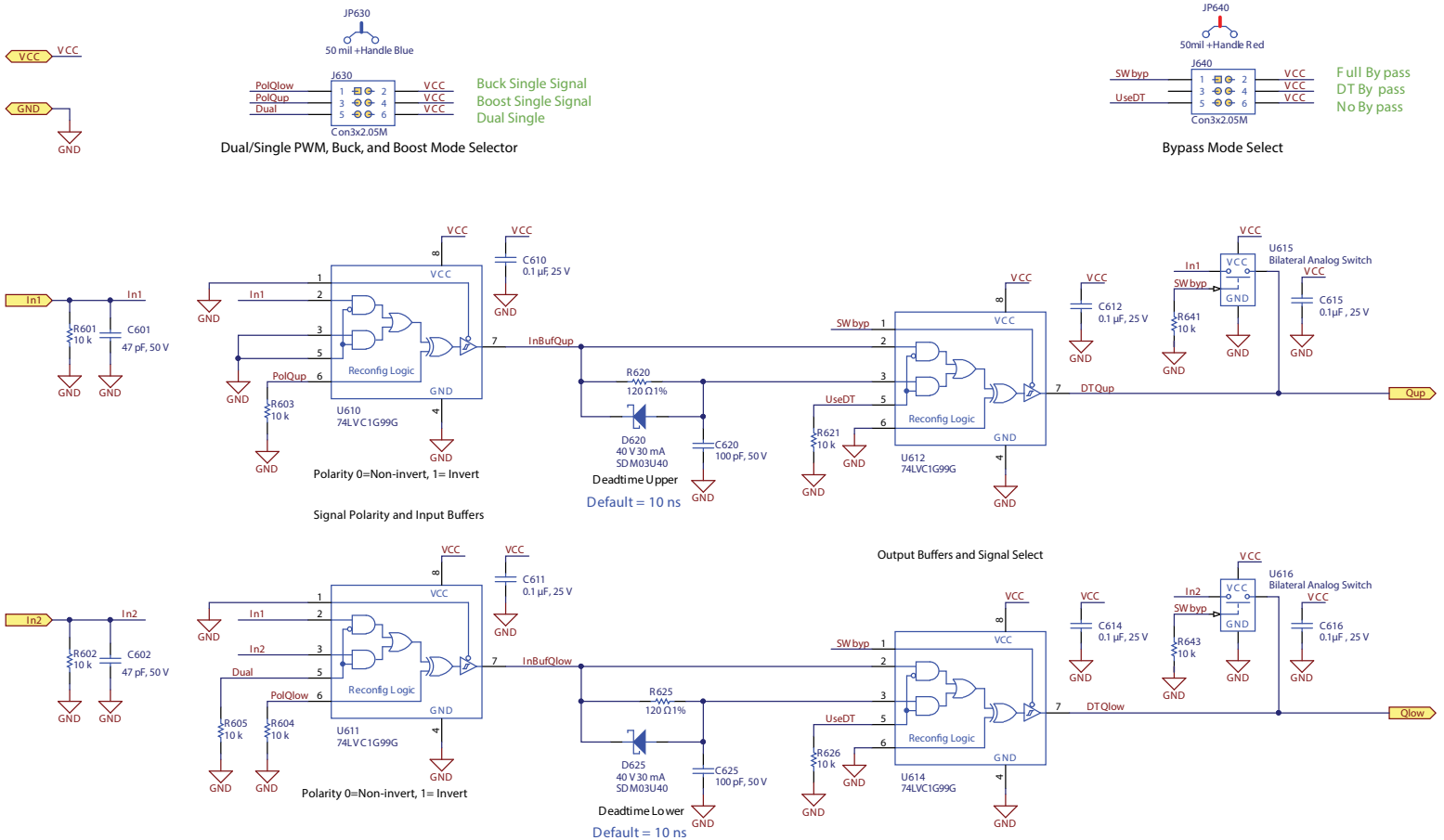


Figure 14: Dead-time and Bypass schematic

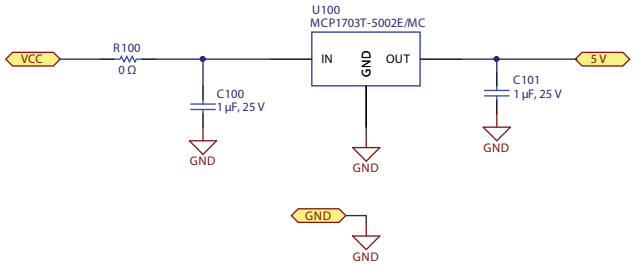


Figure 15: Logic Supply Regulator schematic

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