Simplified Serial Shift Register

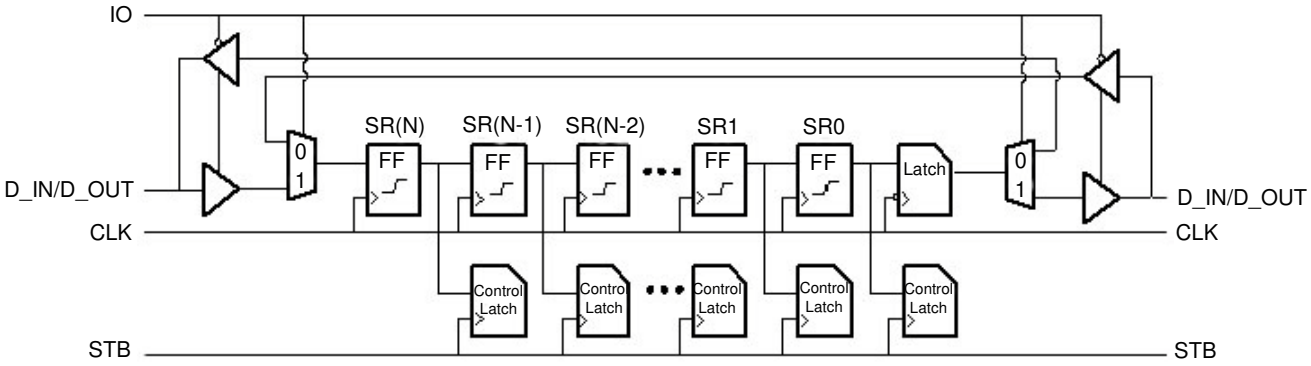

Figure 1

1. INTRODUCTION

TE Connectivity's Optical Driver and Receiver Integrated Circuits (ICs) provide a serial digital interface that allows internal registers to be programmed and monitored. This document describes the protocol used to read and write to the internal registers for ICs featuring the 4-Wire Digital Programming Interface. The customer drawing includes details such as internal register definitions and their default values.

2. DESCRIPTION

The serial interface consists of a four-wire connection to an internal control shift register, as shown in Figure 1. The four control signals are clock (CLK), data in (D_IN), data out (D_OUT), and strobe (STB). Each control signal is intended to be connected to a microcontroller. Some ICs have an IO pad which can control the location of the D_IN and D_OUT pads. If available, the IO pad will be at pad location 1 on the customer drawing.

Data is clocked into the shift register on the rising edge of CLK and is clocked out of the SR on the falling edge of CLK as shown in Figure 2. Asserting STB latches data from the shift registers into control latches. A preamble of 1010 (PREAMBLE [3:0] = 1010) is required for STB to clock data into control latches. If the preamble is incorrect, STB will not write data to the control latches and the wire registers will remain unchanged. Upon power-up of the IC, the shift registers default to a set value which are defined in the customer drawing. The shift register is segmented such that the least significant blocks of registers contain global controls. Shift register bit 0 is the first bit in time to be shifted into the register.

3. REIVISON SUMMARY

- Initial release of document

Serial Interface Timing Diagram

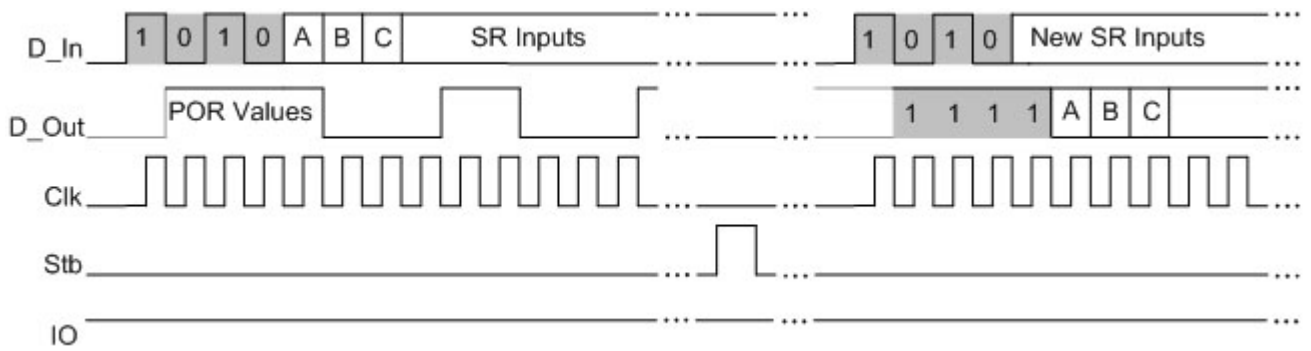

Figure 2

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