



3.3V CMOS 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

IDT74LVCH16373A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in TSSOP package

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

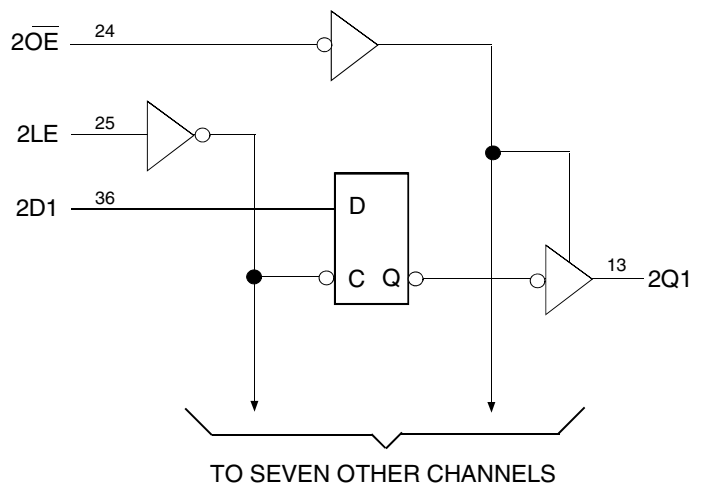
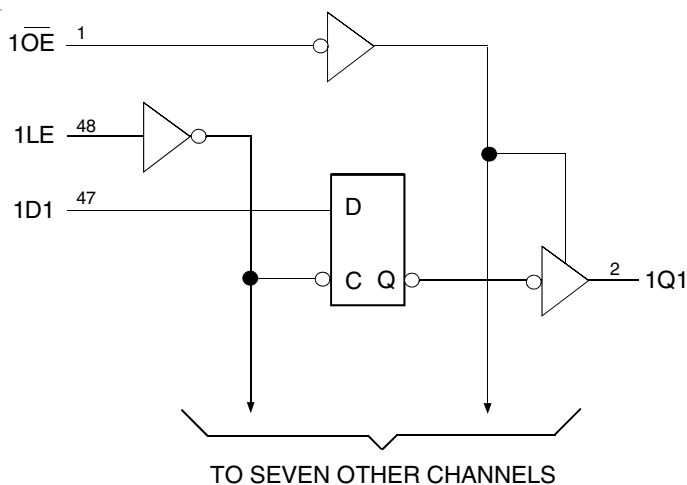
DESCRIPTION

The LVCH16373A 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The LVCH16373A can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

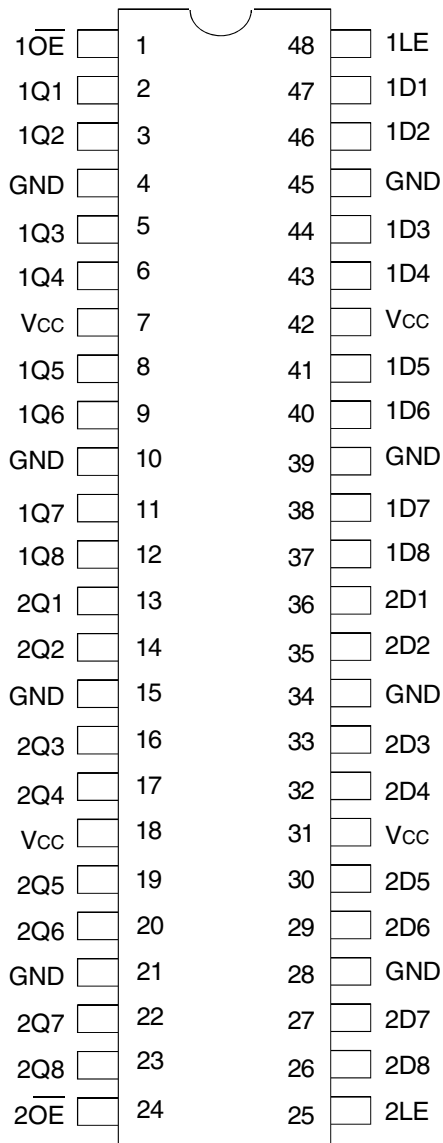
All pins of the LVCH16373A can be driven from either 3.3V or 5V devices. This feature allows the use of the device as a translator in a mixed 3.3V/5V supply system.

The LVCH16373A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|------------------------------------|---|--------------|------|
| VTERM | Terminal Voltage with Respect to GND | -0.5 to +6.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -50 to +50 | mA |
| I _{IK} I _{OK} | Continuous Clamp Current, V _I < 0 or V _O < 0 | -50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ±100 | mA |

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 6.5 | 8 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 6.5 | 8 | pF |

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|-------------------|-----------------------------------|
| xD _x | Data Inputs ⁽¹⁾ |
| xLE | Latch Enable Input |
| x $\overline{O}E$ | Output Enable Inputs (Active LOW) |
| xQ _x | 3-State Outputs |

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

| Inputs | | | Outputs |
|-----------------|-----|-------------------|------------------|
| xD _x | xLE | x $\overline{O}E$ | xQ _x |
| H | H | L | H |
| L | H | L | L |
| X | L | L | Q ⁽²⁾ |
| X | X | H | Z |

NOTES:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|---|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} I _{IL} | Input Leakage Current | V _{CC} = 3.6V | V _I = 0 to 5.5V | — | — | ±5 | μA |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = 0 to 5.5V | — | — | ±10 | μA |
| I _{OFF} | Input/Output Power Off Leakage | V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V | | — | — | ±50 | μA |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V | V _{IN} = GND or V _{CC} | — | — | 10 | μA |
| | | | 3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾ | — | — | 10 | |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 500 | μA |

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|--|----------------------------------|------------------------|----------------------------|------|---------------------|------|------|
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 3V | V _I = 2V | -75 | — | — | μA |
| | | | V _I = 0.8V | 75 | — | — | |
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V | — | — | — | μA |
| | | | V _I = 0.7V | — | — | — | |
| I _{BHHO} I _{BHLO} | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ±500 | μA |

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|--------|---------------------|--------------------------------|---------------|-----------|------|------|
| VOH | Output HIGH Voltage | VCC = 2.3V to 3.6V | IOH = - 0.1mA | VCC - 0.2 | — | V |
| | | VCC = 2.3V | IOH = - 6mA | 2 | — | |
| | | VCC = 2.3V | IOH = - 12mA | 1.7 | — | |
| | | VCC = 2.7V | | 2.2 | — | |
| | | VCC = 3V | | 2.4 | — | |
| | | VCC = 3V | IOH = - 24mA | 2.2 | — | |
| VOL | Output LOW Voltage | VCC = 2.3V to 3.6V | IOL = 0.1mA | — | 0.2 | V |
| | | VCC = 2.3V | IOL = 6mA | — | 0.4 | |
| | | | IOL = 12mA | — | 0.7 | |
| | | VCC = 2.7V | IOL = 12mA | — | 0.4 | |
| | | VCC = 3V | IOL = 24mA | — | 0.55 | |

NOTE:
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|--------|--|---------------------|---------|------|
| CPD | Power Dissipation Capacitance per Latch Outputs enabled | CL = 0pF, f = 10Mhz | 39 | pF |
| CPD | Power Dissipation Capacitance per Latch Outputs disabled | | 6 | |

SWITCHING CHARACTERISTICS⁽¹⁾

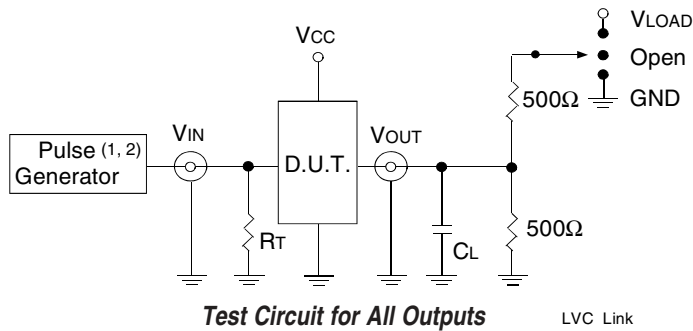
| Symbol | Parameter | VCC = 2.7V | | VCC = 3.3V ± 0.3V | | Unit |
|--------|--|------------|------|-------------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| tPLH | Propagation Delay | — | 4.9 | 1.6 | 4.2 | ns |
| tPHL | xDX to xQx | | | | | |
| tPLH | Propagation Delay | — | 5.3 | 2.1 | 4.6 | ns |
| tPHL | xLE to xQx | | | | | |
| tPZH | Output Enable Time | — | 5.7 | 1.3 | 4.7 | ns |
| tPZL | xOE to xQx | | | | | |
| tPHZ | Output Disable Time | — | 6.3 | 2.5 | 5.9 | ns |
| tPLZ | xOE to xQx | | | | | |
| tsu | Set-up Time, data before LE↓ HIGH or LOW | 1.7 | — | 1.7 | — | ns |
| tH | Hold Time, data after LE↓ HIGH or LOW | 1.2 | — | 1.2 | — | ns |
| tw | Pulse Width xLE HIGH | 3.3 | — | 3.3 | — | ns |
| tsk(o) | Output Skew ⁽²⁾ | — | — | — | 500 | ps |

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} ⁽¹⁾ =3.3V±0.3V | V _{CC} ⁽¹⁾ =2.7V | V _{CC} ⁽²⁾ =2.5V±0.2V | Unit |
|-------------------|---|--------------------------------------|---|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |



DEFINITIONS:

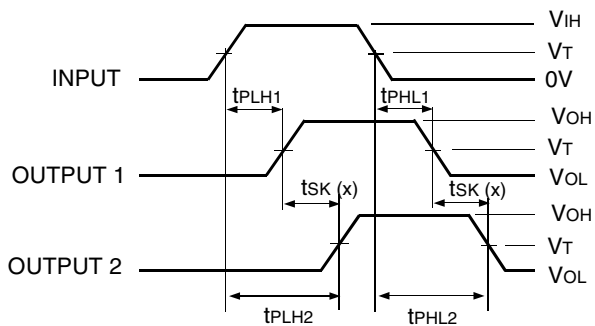
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

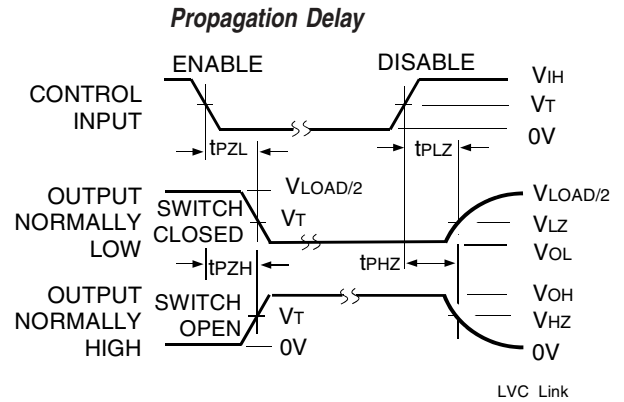
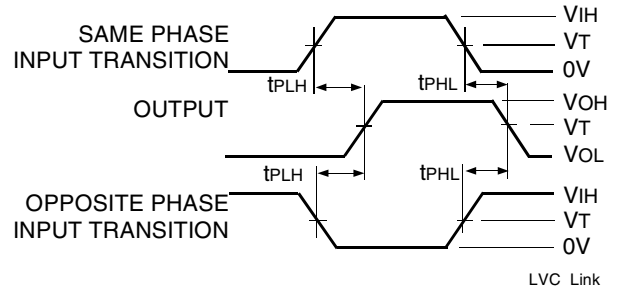
| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other Tests | Open |



$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

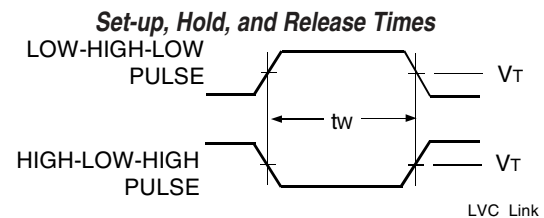
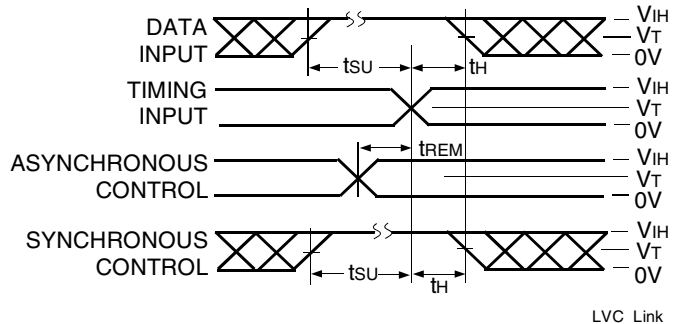
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



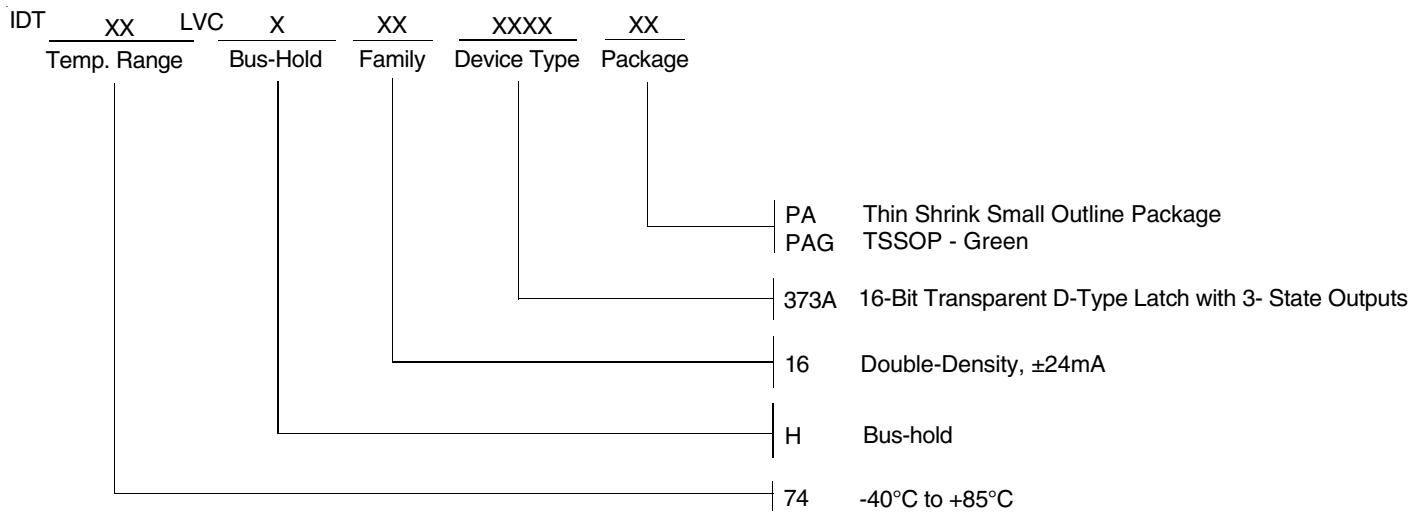
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Pulse Width

ORDERING INFORMATION



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