

## P-Channel Power MOSFET

-30V, -5.3A, 60mΩ

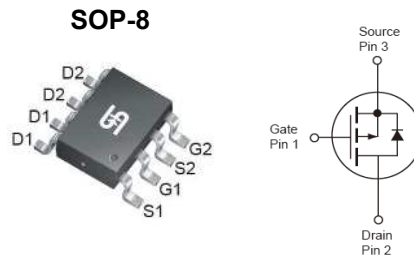
### FEATURES

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance
- Compliant to RoHS Directive 2011/65/EU and WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

### APPLICATION

- Load Switch
- PA Switch

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	60
	$V_{GS} = -4.5V$	90
$Q_g$	9.52	nC



**Notes:** MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current, $V_{GS} @ 4.5V$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	-5.3
		$T_C = 100^\circ\text{C}$	-3.2
Pulsed Drain Current, $V_{GS} @ 4.5V$ (Note 2)	$I_{DM}$	-20	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_{DTOT}$	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	30	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	50	$^\circ\text{C/W}$

**Notes:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 PCB in still air.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 3)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	$BV_{DSS}$	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.0	-1.5	-3.0	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$	$I_{DSS}$	--	--	-1	$\mu A$
Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -5.3A$	$R_{DS(ON)}$	--	50	60	m $\Omega$
	$V_{GS} = -4.5V, I_D = -4.2A$		--	75	90	
<b>Dynamic</b> (Note 4)						
Total Gate Charge	$V_{DS} = -15V, I_D = -5.3A,$ $V_{GS} = -10V$	$Q_g$	--	9.52	--	nC
Gate-Source Charge		$Q_{gs}$	--	3.43	--	
Gate-Drain Charge		$Q_{gd}$	--	1.71	--	
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	$C_{iss}$	--	551.57	--	pF
Output Capacitance		$C_{oss}$	--	90.96	--	
Reverse Transfer Capacitance		$C_{rss}$	--	60.79	--	
<b>Switching</b> (Note 5)						
Turn-On Delay Time	$V_{DD} = -15V, R_{GEN} = 6\Omega,$ $I_D = -1A, V_{GS} = -10V,$	$t_{d(on)}$	--	10.8	--	ns
Turn-On Rise Time		$t_r$	--	2.33	--	
Turn-Off Delay Time		$t_{d(off)}$	--	22.53	--	
Turn-Off Fall Time		$t_f$	--	3.87	--	
<b>Source-Drain Diode</b> (Note 3)						
Forward On Voltage	$I_S = -1.9A, V_{GS} = 0V$	$V_{SD}$	--	--	-1.3	V

**Notes:**

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. Pulse test:  $PW \leq 300\mu s$ , duty cycle  $\leq 2\%$
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

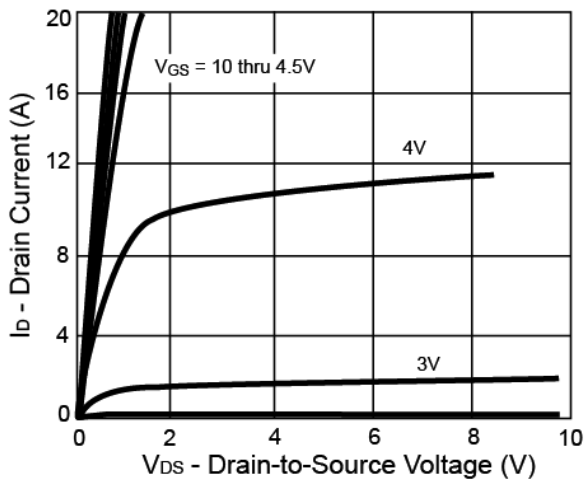
**ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM9435CS RLG	SOP-8	2,500pcs / 13" Reel

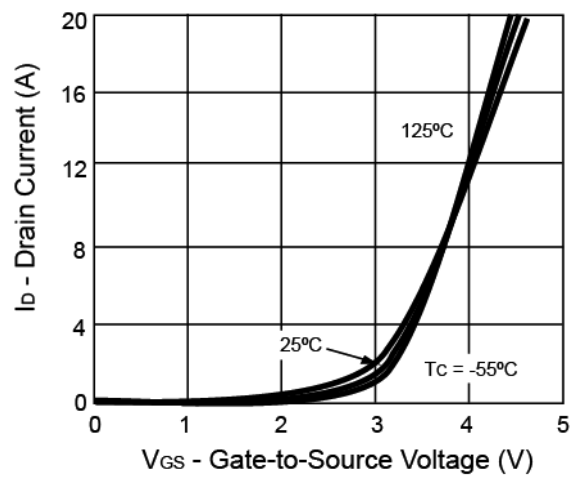
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

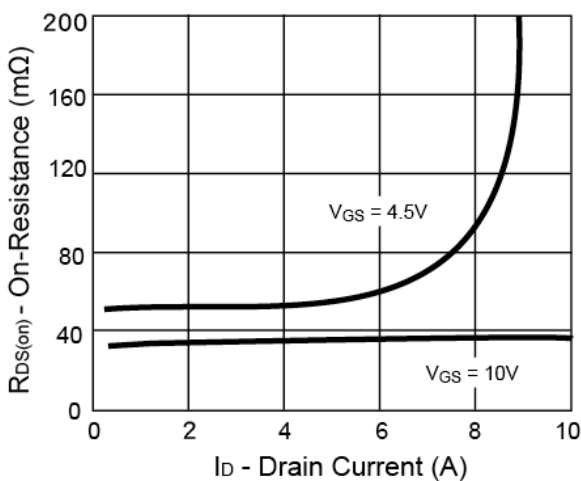
**Output Characteristics**



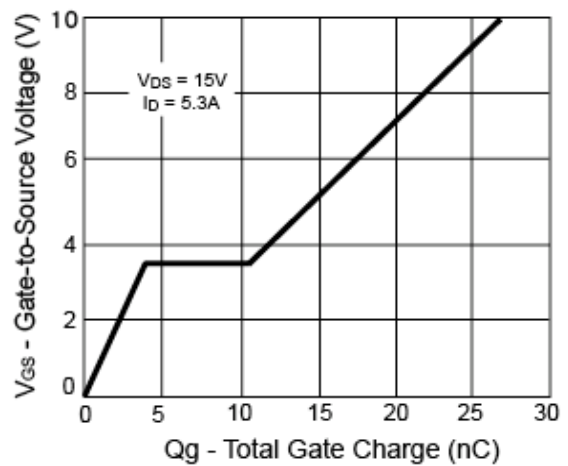
**Transfer Characteristics**



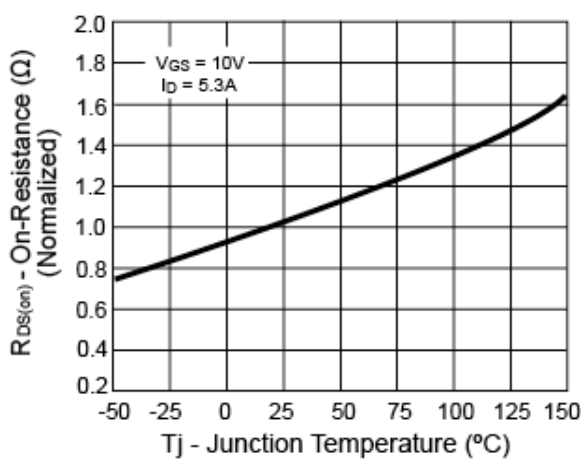
**On-Resistance vs. Drain Current**



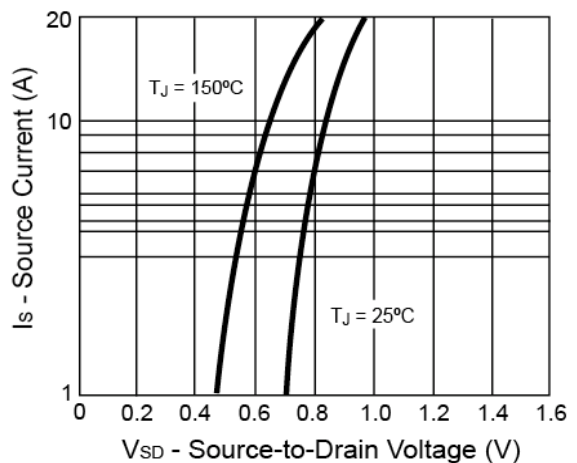
**Gate Charge**



**On-Resistance vs. Junction Temperature**



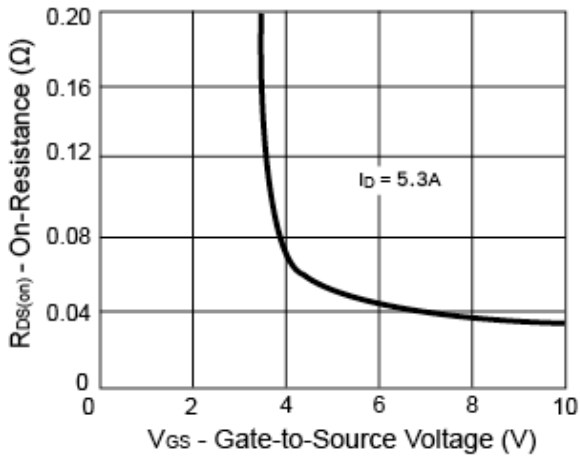
**Source-Drain Diode Forward Voltage**



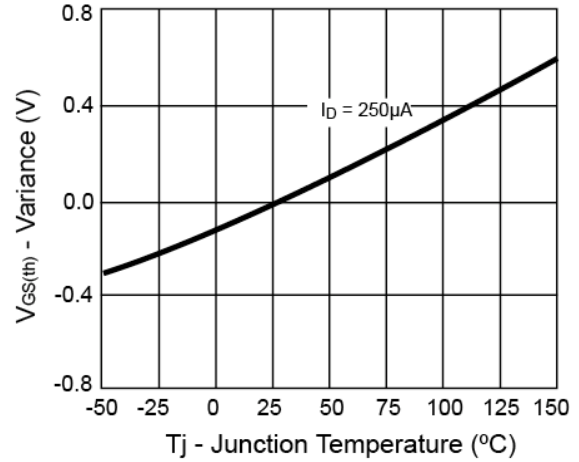
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

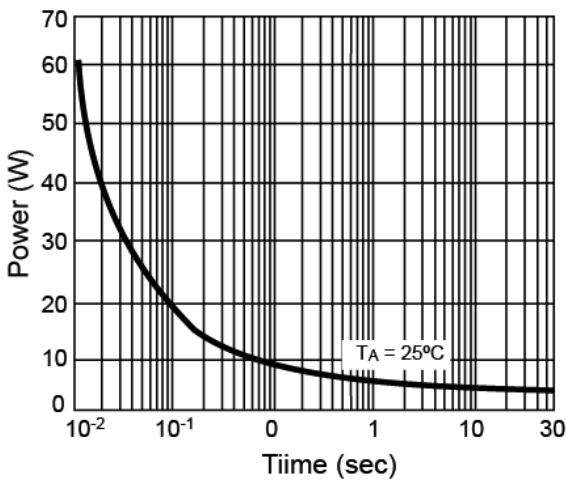
**On-Resistance vs. Gate-Source Voltage**



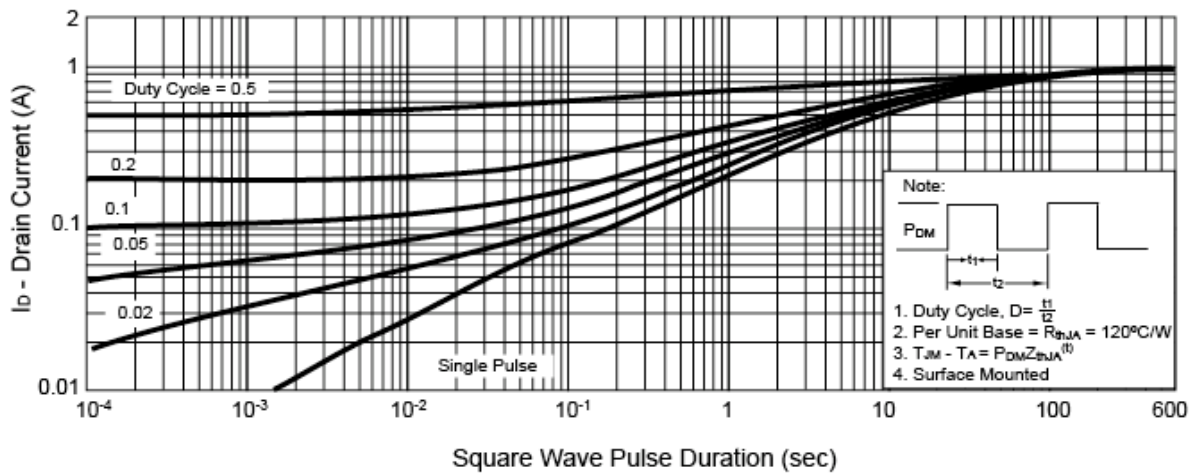
**Threshold Voltage**



**Single Pulse Power**

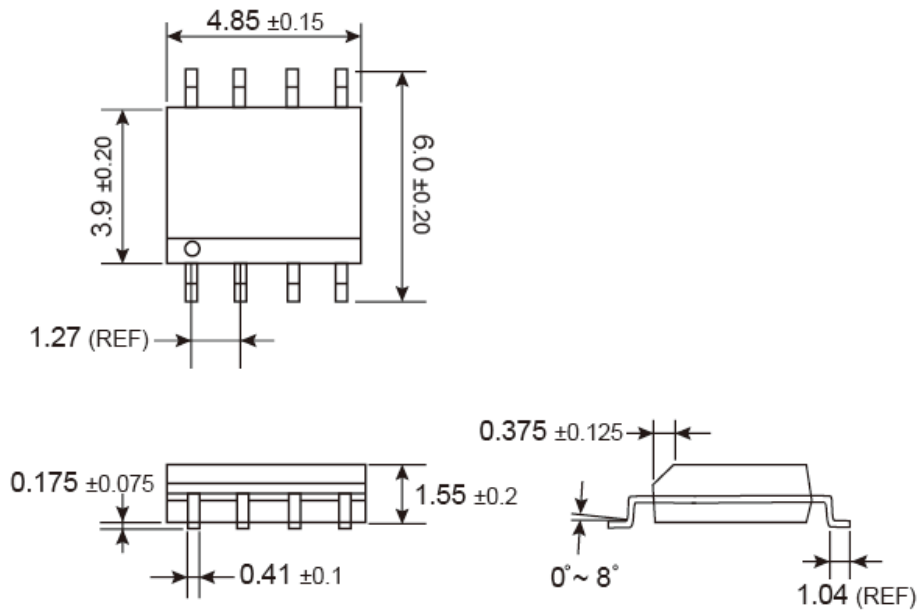


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

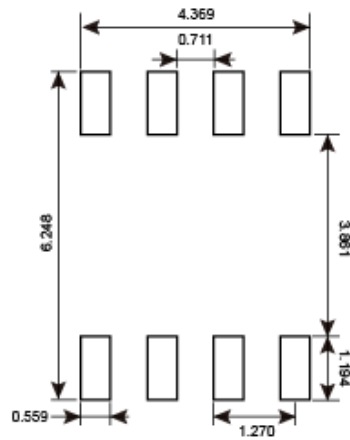


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

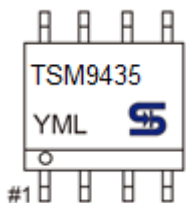
**SOP-8**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



**MARKING DIAGRAM**



- Y** = Year Code
- M** = Month Code for Halogen Free Product
  - O** =Jan    **P** =Feb    **Q** =Mar    **R** =Apr
  - S** =May    **T** =Jun    **U** =Jul    **V** =Aug
  - W** =Sep    **X** =Oct    **Y** =Nov    **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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