VBUS OVP with a PTVS Diode

General Description

The RT9746H is an over-voltage protection devices feature a low 35mΩ (typ) R_{ON} internal FET with PTVS diode. The PTVS also protects the devices from surges up to 100V. When the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected down stream components.

The internal Over-Voltage Protection (OVP) thresholds are preset to 6.8V typical.

The RT9746H is offered in a small WL-CSP-12B (BSC) package provides small PCB area applications.

Ordering Information

RT9746H □

Package Type
WSC : WL-CSP-12B 1.92x1.27

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

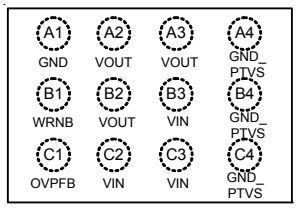
- **PTVS Diode Embedded for VBUS Surge Protection**
- **Warning Indicator for OVP or UVP**
- **28V Maximum Rating for DC Adapter**
- **Integrated Over-Voltage Protection FET on VBUS for Fault Isolation**

Applications

- Cellular Phone
- Smart Handheld Device

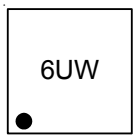
Pin Configuration

(TOP VIEW)



WL-CSP-12B 1.92x1.27 (BSC)

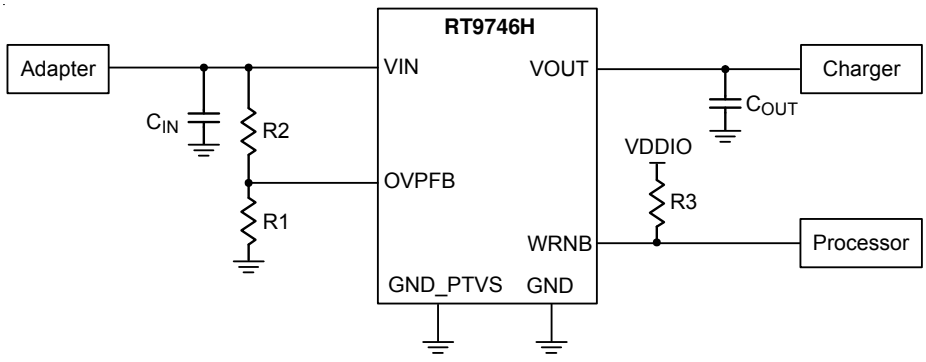
Marking Information



6U : Product Code

W : Date Code

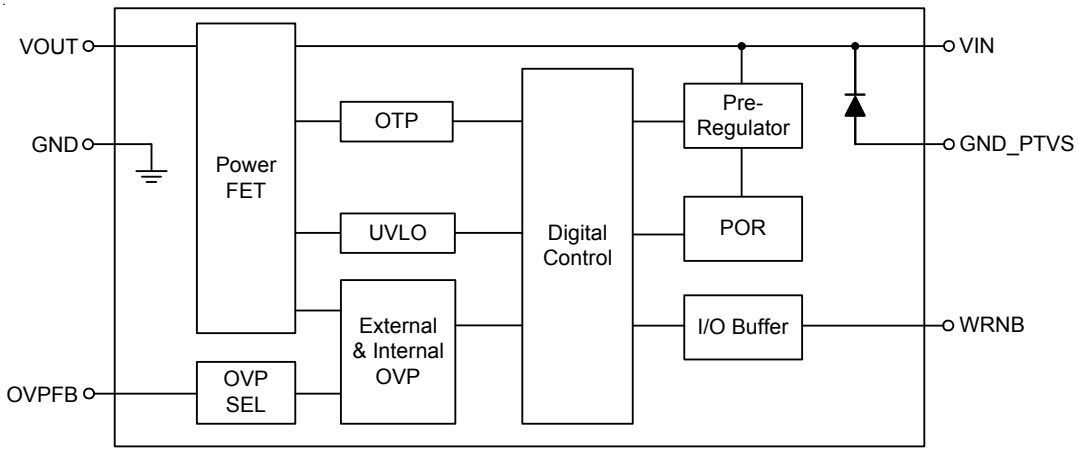
Simplified Application Circuit



Functional Pin Description

Pin No	Pin Name	Pin Function
A1	GND	Common ground of internal circuits.
A2, A3, B2	VOUT	Output from VBUS load-switch.
B1	WRNB	Inverse warning signal (OTP, OVP, UVLO) flag output (open-drain).
A4, B4, C4	GND_PTVS	Common ground of power TVS diode, and pin lay-out place as close as possible VIN capacitor.
B3, C2, C3	VIN	VBUS from power adapter.
C1	OVPFB	External OVP adjustment setting. (If no used, be surely tied to GND)

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN, OVPFB ---------- –0.3V to 28V
- VOUT ---------- –0.3V to 22V
  <10µs ---------- –0.3V to 30V
- WRNB ---------- –0.3V to 6V
- System Level with Air Discharger, VIN, GND ---------- ±15kV
- System Level with Contact Discharger, VIN, GND ---------- ±8kV
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-12B 1.92x1.27 (BSC) ---------- 1.67W
- Package Thermal Resistance (Note 2)
  WL-CSP-12B 1.92x1.27 (BSC), θ_{JA} ---------- 59.6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
- Surge (VIN) ---------- 100V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 3V to 20V
- I/O Supply Voltage (V_{DDIO}) ---------- 1.8V to 3.6V
- VOUT Capacitors ---------- 1µF to 100µF
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
Input Clamp Voltage	V_{IN_CLAMP}	I_{IN} = 10mA	--	31	--	V
VIN Supply Current	I_{VIN_S}	V_{IN} = 5V, I_{OUT} = 0mA	--	90	130	µA
OVP Supply Current	I_{OVP_S}	V_{OVP} = 3V, V_{IN} = 5V, V_{OUT} = 0V	--	63	100	µA
VIN POR Threshold Only for VOUT	V_{POR}	Rising	2.5	2.7	2.9	V
VIN POR Hysteresis Only for VOUT	V_{POR_HYS}		--	100	--	mV
OVP Threshold Voltage	V_{OVP}	Rising	6.6	6.8	7	V
OVP Hysteresis	V_{OVP_HYS}		--	150	--	mV
OVP Propagation Delay to Turn Off VOUT	t_{OVP_PD}	V_{BUS} = 5V to 10V (6V/µs)	--	0.18	0.25	µs
OVP Recover Delay	t_{OVP_RD}	V_{BUS} = 10V to 5V (6V/µs)	--	8	--	ms
OTP Threshold to Turn Off VOUT	T_{OTP_FET}	Rising (Note 5)	--	130	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTP Threshold Hysteresis	$T_{OTP\_FET\_HYS}$	Falling (Note 5)	--	20	--	°C
OTP Recover Delay	t_{OTP_RD}		--	8	--	ms
FET On Resistance	R_{ON_FET}	I_{BUS_OUT} = 1000mA, V_{BUS} = 5V T_A = 25°C	--	35	42	mΩ
External OVP Setting Threshold	V_{REF_EXT}		1.12	1.2	1.24	V
External OVP Adjustment Range	V_{OVP_EXT}		4	--	20	V
External OVP Select Threshold	V_{OVP_SEL}	Rising	--	0.3	--	V
External OVP Select Threshold Hysteresis	V_{OVP_HYS}		--	100	--	mV
WRNB Open-Drain Impedance		V_{BUS} = 5V	--	--	15	Ω
OVP Leakage Current	I_{OVP_LK}		−100	--	100	nA
WRNB Output Low Voltage	V_{OL}	V_{DDIO} = 3.3V, I_{SINK} = 1mA	--	--	0.4	V
WRNB Leakage Current	I_{WRNB_LK}	V_{DDIO} = 3.3V, WRNB deasserted	−0.5	--	0.5	μA
Timing Characteristics						
Debounce Time	t_{DEB}	Time from 2.5V < V_{IN} < V_{IN_OVP} to V_{OUT} = 0.1 x V_{IN}	--	16	--	ms
Soft-Start Time	t_{START}	Time from V_{IN} = V_{IN_MIN} to 0.2 x WRNB, V_{IO} = 1.8V with 10kΩ pull-up resistor	--	30	--	ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_L = 100Ω, V_{OUT} from 0.1 x V_{IN} to 0.9 x V_{IN}, C_{LOAD} = 100μF	--	1.5	--	ms
Switch Turn-Off Time	t_{OFF}	R_L = 100Ω, C_{LOAD} = 0μF, V_{IN} > V_{OVP} to V_{OUT} = 0.8 x V_{IN} (Note 5)	--	125	--	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

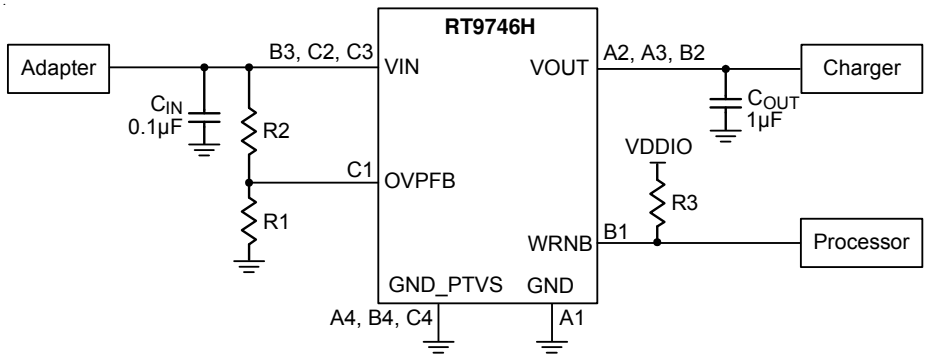
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit



Timing Diagram

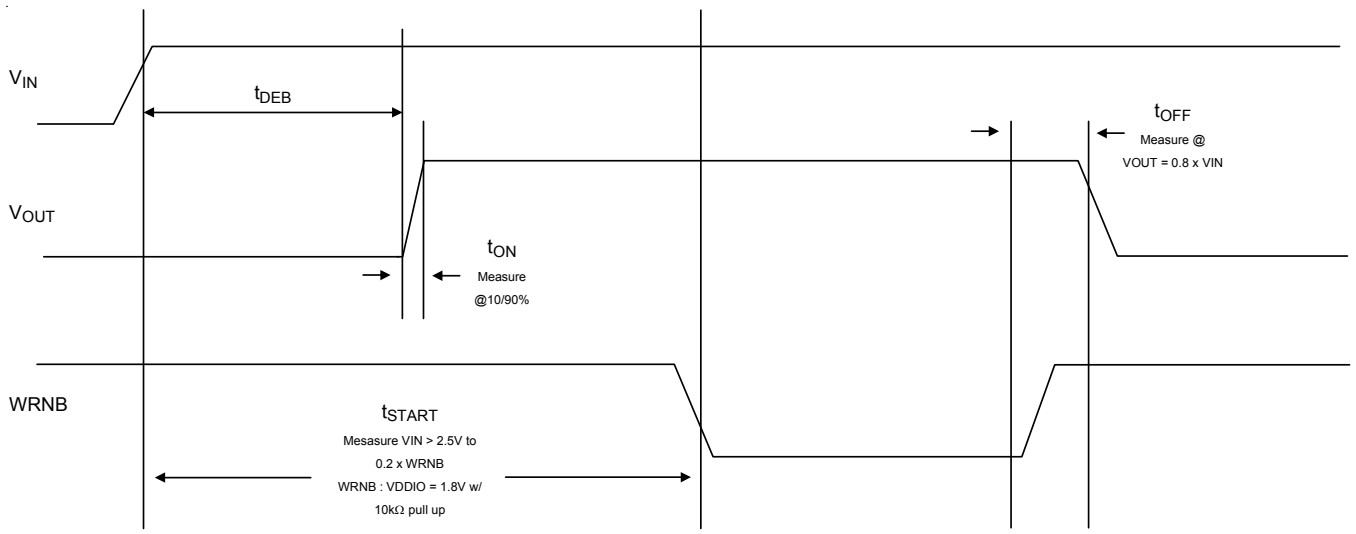


Figure 1. Timing for Power Up and Normal Operation

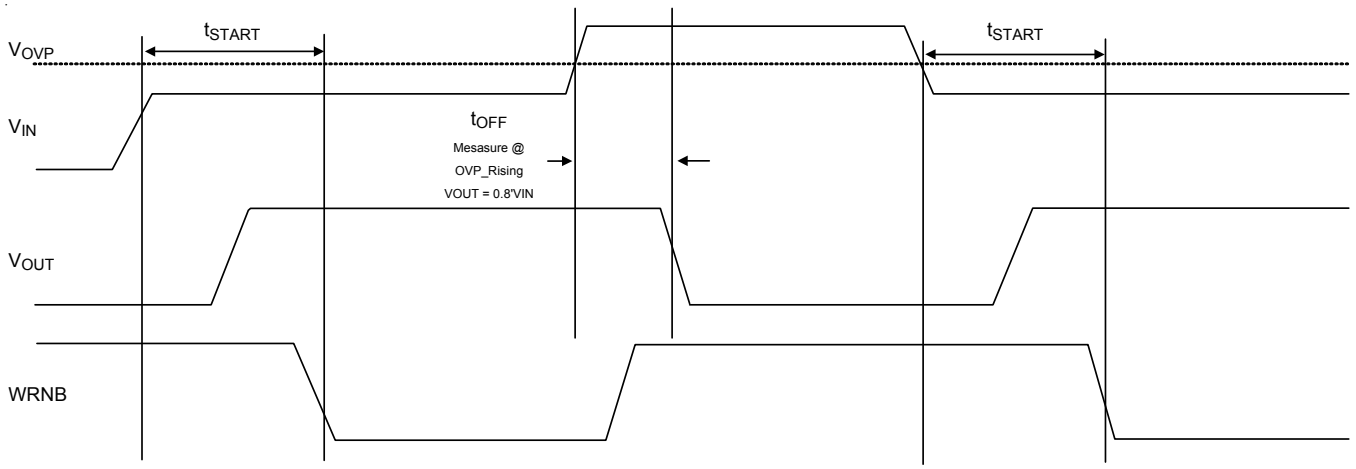
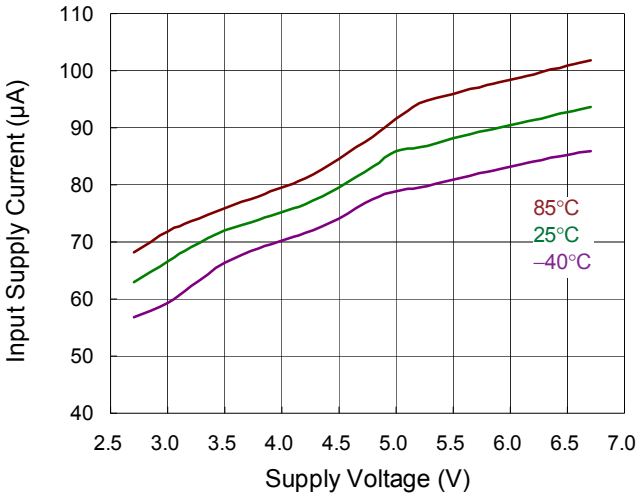


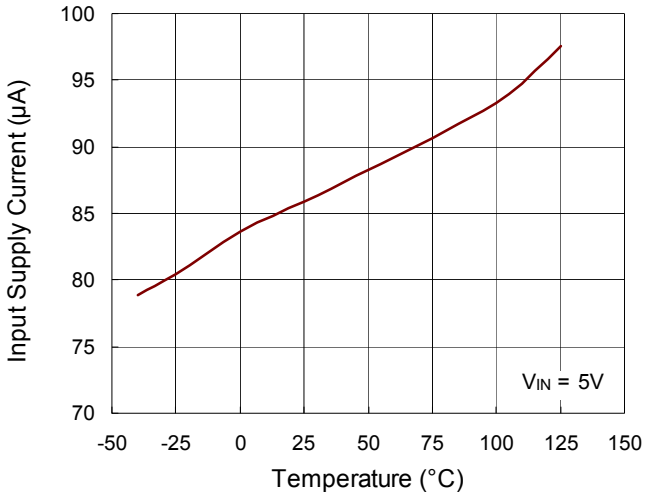
Figure 2. Timing for OVP Trip

Typical Operating Characteristics

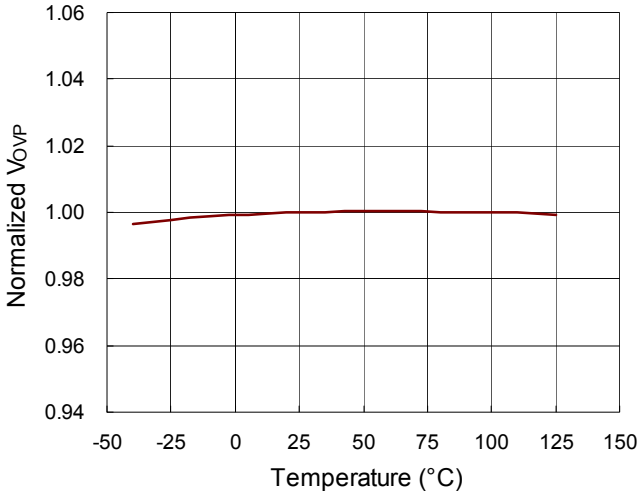
Input Supply Current vs Supply Voltage



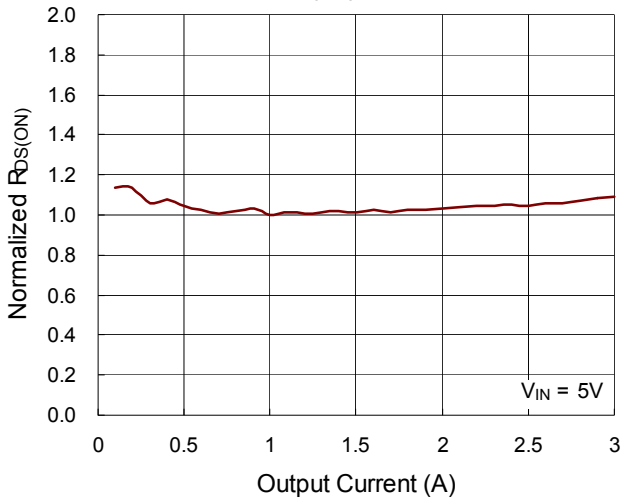
Input Supply Current vs Temperature



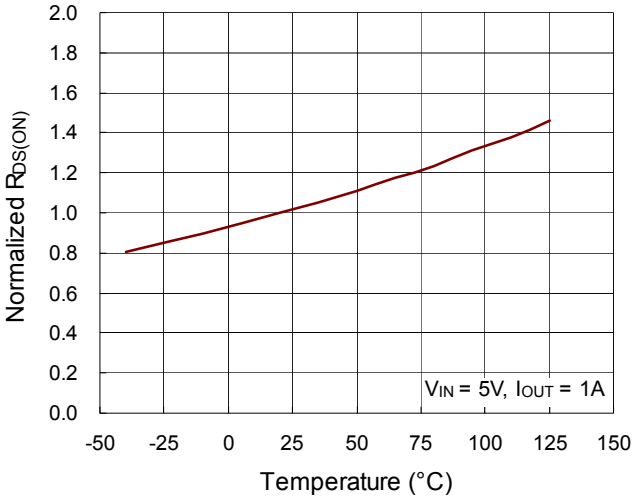
Normalized V_{OVP} vs. Temperature



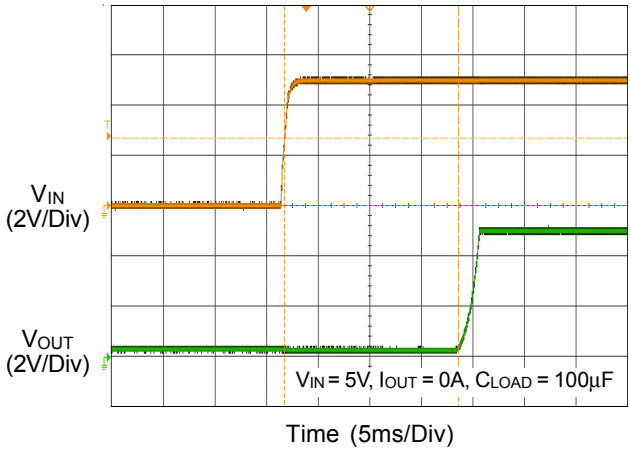
Normalized $R_{DS(ON)}$ vs. Output Current



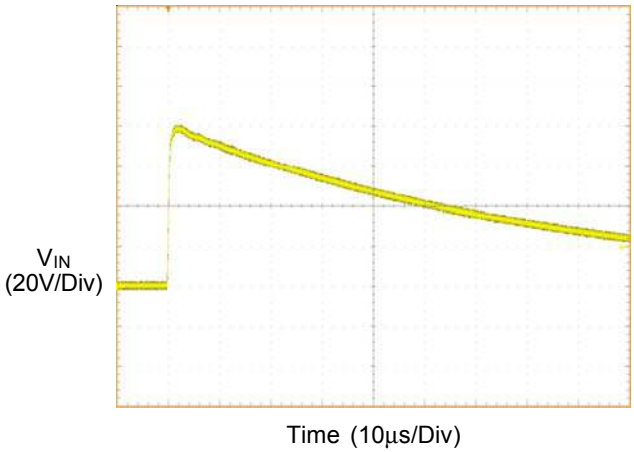
Normalized $R_{DS(ON)}$ vs. Temperature



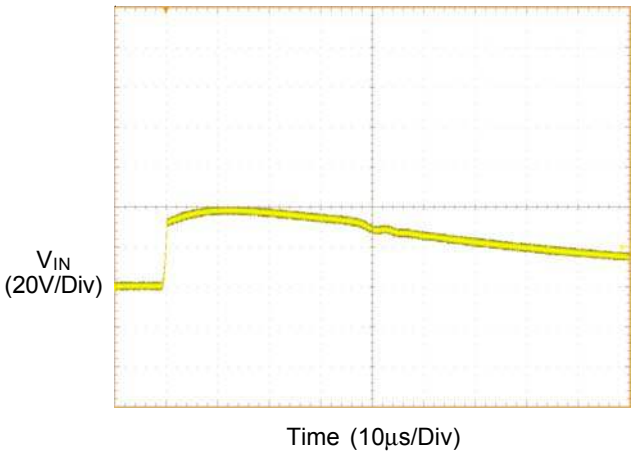
Power Up



80V Surge without RT9746H



80V Surge with RT9746H



Application Information

Power Up

The RT9746H has a threshold of 2.7V power on reset (POR) with a built-in hysteresis of 100mV. Before the input voltage reaches the POR threshold, the RT9746H is off. When the input voltage is over the POR threshold, the VOUT of the RT9746H will delay for 16ms which includes soft-start time of 8ms. The 16ms delay allows the transient at the input during a hot insertion of the power supply to settle down before the IC starts to operate. During the soft-start transition, the RT9746H slowly turns on the internal MOSFET to reduce the inrush current.

Over-Temperature Protection (OTP)

The RT9746H monitors its internal temperature to prevent thermal failures. The chip turns off the MOSFET when the junction temperature reaches 130°C. The IC will resume after the junction temperature is cooled down 20°C.

Input Over-Voltage Protection

The RT9746H provides input over-voltage protection via internal or external resistor to set OVP level. If OVPFB is connected to GND, the RT9746H uses the internal OVP level setting. If an external resistor-divider is connected to OVPFB and V_{OVPFB} exceeds the VOVP_SEL voltage, the RT9746H will adopt external OVP level setting. The OVP level VOVP is set as below.

$$V_{OVP} = V_{REF\_EXT} \times \left(1+\frac{R2}{R1}\right)$$

When the input volatge exceeds the OVP level, the RT9746H will turn off internal MOSFET around 0.18μs to prevent the high input volatge from damaging the end system. When the input volatge returns to normal operation volatge range with hysteresis (internal 150mV, external 100mV), the RT9746H will turn on the MOSFET to re-enable output.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-12B 1.92x1.27 (BSC) package, the thermal resistance, θ_{JA}, is 59.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)} = (125°C - 25°C) / (59.6°C/W) = 1.67W$ for a WL-CSP-12B 1.92x1.27 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

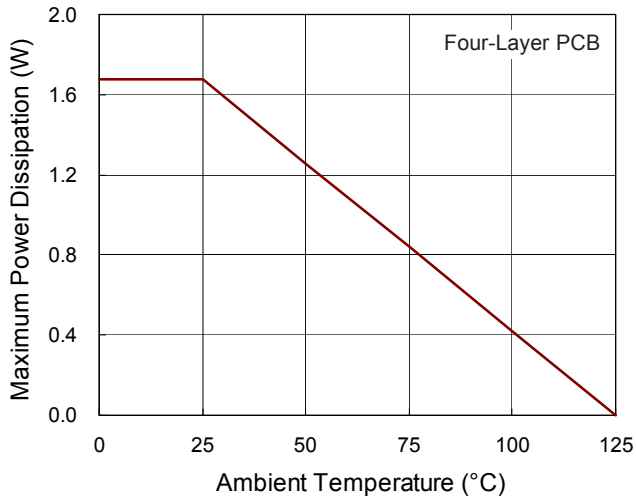
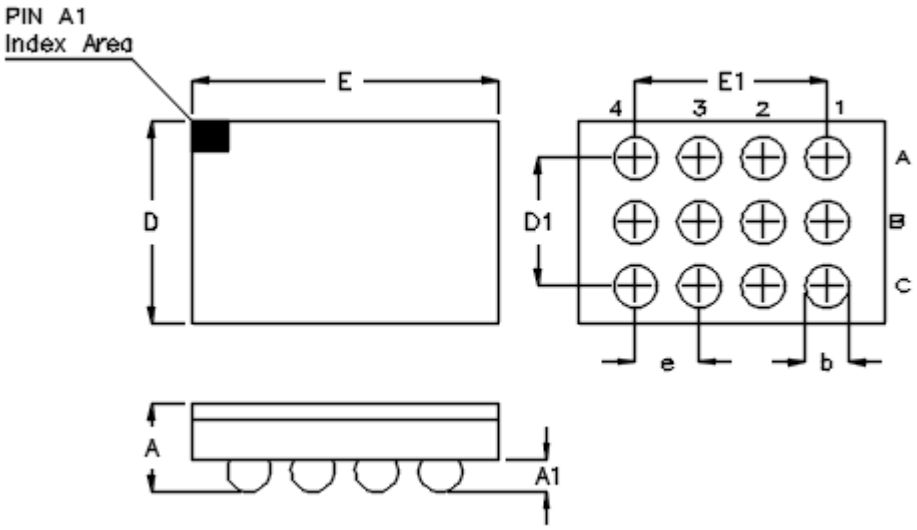


Figure 3. Derating Curve of Maximum Power Dissipation

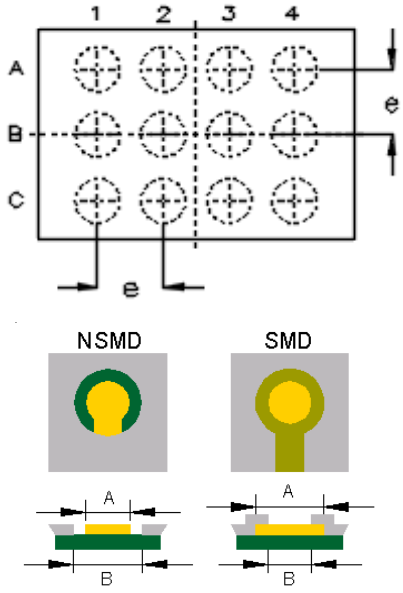
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.220	1.320	0.048	0.052
D1	0.800		0.031	
E	1.870	1.970	0.074	0.078
E1	1.200		0.047	
e	0.400		0.016	

WL-CSP-12B 1.92x1.27 (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.92x1.27-12(BSC)	12	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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