Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages

At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz,1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz

Datasheet

April 2003

Order Number: 298517-006

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Revision History

Date	Revision	Updates
October 2001	298517-001	Initial release
January 2002	298517-002	Updates include: • Added new processor speeds 1.2 GHz, 1.13 GHz, and 1.06 GHz at 1.45V. • Added new Low Voltage 667 MHz • Added new Ultra Low Voltage 650 MHz • Updated Processor Specifications (Tables 9, 12-15, 40) • Added Specification Clarification for VTTPWRGD in Table 25, Figure 21 and Section 4.3.1 • Added note 5 CMOSREF resistor divider recommendations to Table 24. • Updated references
June 2002	298517-003	Updates include: • Targeted processor frequencies updated • Updated Tables 3, 9, 12 - 19, 29, and 44 • Updated/corrected Tables 39 and 40 • Updated Figure 5- Figure 7 • Updated Section 5 • Updated CMOSREF description in Section 8.1 • Added Section 3.2.4
August 2002	298517-004	Updates include: • Added new processor frequencies • Updated Table 11 and Table 48
December 2002	298517-005	Updates include: • Added new processor frequencies • Updated Table 11 and Table 48
April 2003	298517-006	Updates include: • Added new processor frequencies (1.26 GHz) • Updated Table 11 and Table 48

Mobile Intel® Celeron® Processor (0.13 µ) in Micro-FCBGA and Micro-FCPGA Packages

Product Features

- Mobile Intel® Celeron® Processor with the following Processor core/bus speeds:
  - 1.333 GHz/133 MHz at 1.50 V
  - 1.200 GHz/133 MHz at 1.45 V
  - 1.133 GHz/133 MHz at 1.45 V
  - 1.066 GHz/133 MHz at 1.45 V
  - 1.266 GHz/133 MHz at 1.40 V
  - 1.000 GHz/133 MHz at 1.40 V
- Low Voltage Mobile Intel Celeron Processor (0.13 µ) with the following Processor core/bus speeds:
  - 866/133 MHz at 1.15 V
  - 733/133 MHz at 1.15 V
  - 650/100 MHz at 1.15 V
- Ultra Low Voltage Mobile Intel Celeron processor (0.13 µ) with the following Processor core/bus speeds:
  - 800/133 MHz at 1.10V
  - 733/133 MHz at 1.10V
  - 700/100 MHz at 1.10V
  - 650/100 MHz at 1.10 V
- Supports the Intel Architecture with Dynamic Execution
- On-die primary 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level cache (256-Kbyte) with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Integrated AGTL termination
- Integrated math co-processor
- Micro-FCPGA and Micro-FCBGA packaging technologies
  - Supports thin form factor notebook designs
  - Exposed die enables more efficient heat dissipation
  - Mobile ULV and LV Celeron processor (0.13 µ) are available only in Micro-FCBGA package.
  - Mobile Intel Celeron processors at 1.45 V and 1.50 V are available only in Micro-FCPGA package.
- Fully compatible with previous Intel microprocessors
  - Binary compatible with all applications
  - Support for MMX™ technology
  - Support for Streaming SIMD Extensions
- Power Management Features
  - Quick Start and Deep Sleep modes provide low power dissipation
- On-die thermal diode

1. Introduction

Using Intel's advanced 0.13-micron process technology with copper interconnect, the Mobile Intel Celeron Processor offers high-performance and low-power consumption. The Mobile Intel Celeron Processor (0.13µ) in Micro-FCBGA and Micro-FCPGA packages (hereafter referred to as "the Mobile Intel Celeron Processor") is based on the same core as existing mobile Intel® Pentium® III Processor-M. Key performance features include Internet Streaming SIMD instructions, an Advanced Transfer Cache architecture, and a processor system bus speed of 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processors will support both a 133-MHz and 100-MHz bus speed. These features are offered in Micro-FCPGA packages for socketable boards and Micro-FCBGA packages for surface mount boards. The Low Voltage and Ultra Low Voltage Mobile processors will be available only in the Micro-FCBGA package. The Mobile Intel Celeron processors at 1.45 V and at 1.50 V are available only in the Micro-FCPGA package. All of these technologies make outstanding performance possible for mobile PCs in a variety of shapes and sizes.

The 256-KB integrated L2 cache based on the Advanced Transfer Cache architecture runs at full speed and is designed to help improve performance. It complements the system bus by providing critical data faster and reducing total system power consumption. The processor also features Data Prefetch Logic that speculatively fetches data to the L2 cache, resulting in improved performance. The Mobile Intel Celeron Processor's 64-bit wide Assisted Gunning Transceiver Logic (AGTL) system bus provides a glue-less, point-to-point interface for a memory controller hub.

This document covers the electrical, mechanical, and thermal specifications for the following:

- The Mobile Intel Celeron Processor at the following frequencies and voltages: 1.33 GHz at 1.50 V; 1.2 GHz, 1.13 GHz, 1.06 GHz at 1.45 V; and 1.266GHz, 1 GHz at 1.40 V.
- The Low Voltage Mobile Intel Celeron Processor at the following frequencies and voltages: 866 MHz, 733 MHz and 650 MHz at 1.15 V.
- The Ultra Low Voltage Mobile Intel Celeron Processor at the following frequencies and voltages: 800 MHz, 733 MHz, 700 MHz, and 650 MHz at 1.10 V.
- Unless explicitly stated, all references to the Mobile Intel Celeron Processor (0.13 µ) in Micro-FCBGA and Micro-FCPGA packages in this document also apply to the Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processor (0.13 µ) in the Micro-FCBGA package.

1.1 Overview

- Performance features
  - Supports the Intel Architecture with Dynamic Execution
  - Supports the Intel Architecture MMX™ technology
  - Supports Streaming SIMD Extensions for enhanced video, sound, and 3D performance
  - Integrated Intel Floating Point Unit compatible with the IEEE 754 standard
  - Data Prefetch Logic
- On-die primary (L1) instruction and data caches
  - 4-way set associative, 32-byte line size, 1 line per sector
  - 16-Kbyte instruction cache and 16-Kbyte write-back data cache
  - Cacheable range controlled by processor programmable registers

- On-die second level (L2) cache
  - 8-way set associative, 32-byte line size, 1 line per sector
  - Operates at full core speed
  - 256-Kbyte ECC protected cache data array
- AGTL system bus interface
  - 64-bit data bus, 100-MHz and 133-MHz operation
  - Uniprocessor, two loads only (processor and chipset)
  - Integrated termination
- Processor clock control
  - Quick Start for low power, low exit latency clock "throttling"
  - Deep Sleep mode for lower power dissipation
- Thermal diode for measuring processor temperature

1.2 State of the Data

All information in this document is the best available information at the time of publication. Revisions of this document will be provided on an as-required basis until the Mobile Intel Celeron Processor is released for production orders.

1.3 Terminology

Term	Definition
#	A "#" symbol following a signal name indicates that the signal is active low. This means that when the signal is asserted (based on the name of the signal) it is in an electrical low state. Otherwise, signals are driven in an electrical high state when they are asserted. In state machine diagrams, a signal name in a condition indicates the condition of that signal being asserted
!	Indicates the condition of that signal not being asserted. For example, the condition "!STPCLK# and HS" is equivalent to "the active low signal STPCLK# is unasserted (i.e., it is at 1.5V) *and* the HS condition is true."
L	Electrical low signal levels
H	Electrical high signal levels
0	Logical low. For example, BD[3:0] = "1010" = "HLHL" refers to a hexadecimal "A," and D[3:0]# = "1010" = "LHLH" also refers to a hexadecimal "A."
1	Logical high. For example, BD[3:0] = "1010" = "HLHL" refers to a hexadecimal "A," and D[3:0]# = "1010" = "LHLH" also refers to a hexadecimal "A."
TBD	Specifications that are yet to be determined and will be updated in future revisions of the document.
X	Don't care condition

1.4 References

- *P6 Family of Processors Hardware Developer's Manual* (Order Number 244001-001)
- *Intel® Architecture Optimization Reference Manual* (Order Number 245127-001)
- *Intel® Architecture Software Developer's Manual*
  - Volume I: Basic Architecture (Order Number 245470)
  - Volume II: Instruction Set Reference (Order Number 245471)
  - Volume III: System Programming Guide (Order Number 245472)
- *CK-408 (CK-Titan) Clock Synthesizer/Driver Specification* (Contact your Intel Field Sales Representative)
- *Mobile Intel® Pentium® III Processor-M I/O Buffer Models*, IBIS Format (Contact your Intel Field Sales Representative)
- *Intel® 830 Chipset Family: 82830 Graphics and Memory Controller Hub (GMCH-M) Datasheet* (Order Number 298338-003)
- *Intel® 830 Chipset Family: Intel® 830 Chipset Platform Design Guide (Order Number 298339-003)*
- *Intel® 830 Chipset Family: Intel® 82801CAM I/O Controller Hub 3 (ICH3-M) Datasheet* (Order Number 290716-001)
- *Intel® Mobile Voltage Positioning -II (IMVP-II) Design Guide* (Contact your Intel Field Sales Representative)
- *Mobile Intel® Pentium® III Processor-M /440MX Platform Design Guide* (Contact your Intel Field Sales Representative)
- *Intel Processor Identification and the CPUID Instruction Application Note AP-485* (Order Number 241618-020)

2. Mobile Intel Celeron Processor Features

2.1 New Features in the Mobile Intel Celeron Processor

2.1.1 133-MHz PSB With AGTL Signaling

The Mobile Intel Celeron Processor uses Assisted GTL (AGTL) signaling on the PSB interface. The main difference between AGTL and GTL+ used on previous Intel processors is V_{CCT} = 1.25 V for AGTL versus 1.5 V for GTL+. The lower voltage swing enables high performance at lower power. The Low Voltage and Ultra Low Voltage Mobile Celeron Processors will also support a 100-MHz PSB.

2.1.2 256-K On-die Integrated L2 Cache

The 256-K on die integrated L2 cache on the Mobile Intel Celeron Processor is double the L2 cache size on the Mobile Intel Celeron Processor (0.18 µ). The L2 cache runs at the processor core speed and the increased cache size provides superior processing power.

2.1.3 Data Prefetch Logic

The Mobile Intel Celeron Processor features Data Prefetch Logic that speculatively fetches data to the L2 cache before an L1 cache request occurs. This reduces transactions between the cache and system memory reducing or eliminating bus cycle penalties, resulting in improved performance. The processor also includes extensions to memory order and reorder buffers that boost performance.

2.1.4 Differential Clocking

Differential clocking requires the use of two complementary clocks: BCLK and BCLK#. Benefits of differential clocking include easier scaling to lower voltages, reduced EMI, and less jitter. All references to BCLK in this document apply to BCLK# also even if not explicitly stated. The Mobile Intel Celeron Processor will also support Single Ended Clocking. The processor will configure itself for Differential or Single Ended Clocking based on the waveforms detected on the BCLK and BCLK#/CLKREF signal lines.

2.1.5 Signal Differences Between the Mobile Intel Celeron Processor (0.18 µ) (in BGA2 and Micro-PGA2 Packages) and the Mobile Intel Celeron Processor (0.13 µ) (in Micro-FCBGA and Micro-FCPGA Packages)

A list of new and changed signals is shown in Table 1.

Table 1. New and Revised Mobile Intel Celeron Processor (0.13 µ) Signals

Signals	Function
BCLK, BCLK#	Differential host clk signals.
CLKREF	Host Clock reference signal in Single Ended Clocking mode.
BSEL[1:0]	Signals are output only instead of I/O. Please refer to the Appendix for details.
DPSLP#	Deep Sleep pin (replaces SLP# pin on the mobile Celeron processor (0.18 µ))
NCTRL	AGTL output buffer pull down impedance control.
VID[4:0]	Voltage Identification (different implementation from mobile Celeron processor (0.18 µ)). Please refer to Section 3.2.3 for details.
VTTPWRGD	Power Good signal for VCCT, which indicates that, the VID signals are stable. Please refer to Figure 3 for VTTPWRGD system level connections.

2.2 Power Management

2.2.1 Clock Control Architecture

The Mobile Intel Celeron Processor clock control architecture (Figure 1) has been optimized for leading edge mobile computer designs. The clock control architecture consists of six different clock states: Normal, Auto Halt, Quick Start, HALT/Grant Snoop and Deep Sleep states. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power and low exit latency clock state that can be used for hardware controlled “idle” computer states. The Deep Sleep state provides extremely low-power states that can be used for “Power-On-Suspend” computer states, which is an alternative to shutting off the processor’s power. The exit latency of the Deep Sleep state is 30 msec in the Mobile Intel Celeron Processor. Performing state transitions not shown in Figure 1 is neither recommended nor supported. Figure 2 provides the clock state characteristics, which are described in detail in the following sections.

2.2.2 Normal State

The Normal state of the processor is the normal operating mode where the processor’s core clock is running and the processor is actively executing instructions.

2.2.3 Auto Halt State

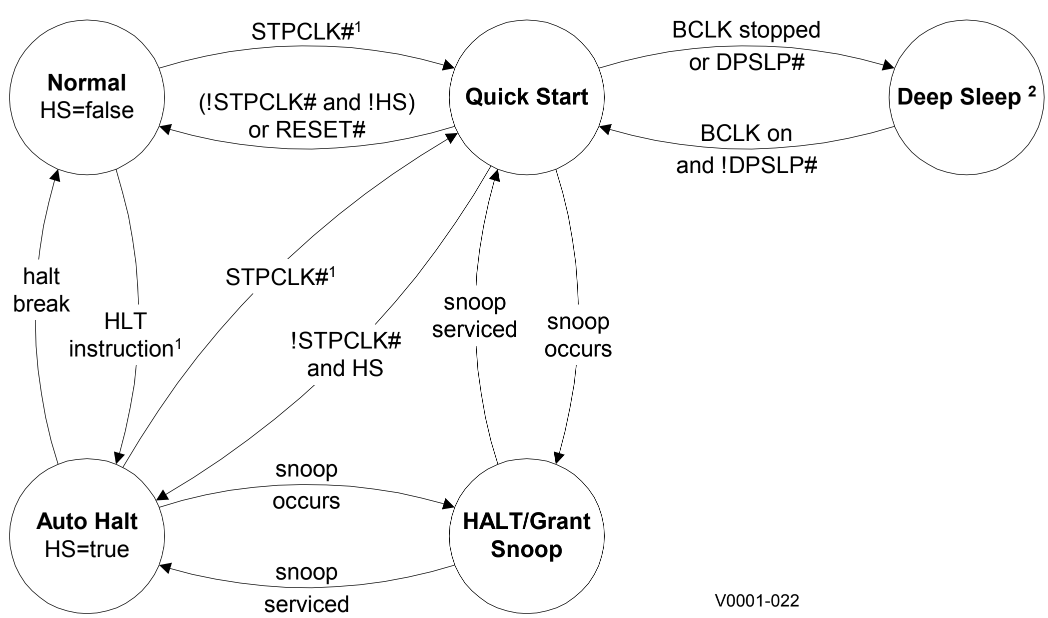
This is a low-power mode entered by the processor through the execution of the HLT instruction. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Quick Start state. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# interrupt is recognized in the Auto Halt state. The return from the System Management Interrupt (SMI) handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from the System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After the on-chip and off-chip caches have been flushed, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

Figure 1. Clock Control States



NOTES:

1. State transition does not occur until the Stop Grant or Auto Halt acknowledge bus cycle completes
   Halt break – A20M#, BINIT#, FLUSH#, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
   HLT – HLT instruction executed
   HS – Processor Halt State
2. Restrictions apply to the use of both methods of entering Deep Sleep. See Deep Sleep state description for details.

2.2.4 Quick Start State

The processor is required to be configured for the Quick Start state by strapping the A15# signal low. In the Quick Start state the processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in a uniprocessor (UP) configuration.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor or asserting the DPSLP# signal. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters, or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

2.2.5 HALT/Grant Snoop State

The processor will respond to snoop transactions on the system bus while in the Auto Halt or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

2.2.6 Deep Sleep State

The Deep Sleep state is a very low power state that the processor can enter while maintaining its context. The Deep Sleep state is entered by stopping the BCLK and BCLK# inputs to the processor or by asserting the DPSLP# signal, while it is in the Quick Start state. Note that either one of the methods can be used to enter Deep Sleep but **not both** at the same time. When BCLK and BCLK# are stopped, they must obey the DC levels specified in Table 38 and Table 39.

The processor will return to the Quick Start state from the Deep Sleep state when the BCLK and BCLK# inputs are restarted or the DPSLP# signal is deasserted. Due to the PLL lock latency, there is a delay of up to 30 µsec after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK and BCLK# turn on or DPSLP# is deasserted when transitioning out of the Deep Sleep state.

Table 2. Clock State Characteristics

Clock State	Exit Latency	Snooping?	System Uses
Normal	N/A	Yes	Normal program execution
Auto Halt	10 µsec	Yes	S/W controlled entry idle mode
Quick Start	Through snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 10 µsec	Yes	H/W controlled entry/exit mobile throttling
HALT/Grant Snoop	A few bus clocks after snoop completion	Yes	Supports snooping in the low power states
Deep Sleep	30 µsec	No	H/W controlled entry/exit mobile powered-on suspend support

2.2.7 Operating System Implications of Low-power States

The time-stamp counter and the performance monitor counters are not guaranteed to count in the Quick Start state. The local APIC timer and performance monitor counter interrupts should be disabled before entering the Deep Sleep state or the resulting behavior will be unpredictable.

2.3 AGTL Signals

The Mobile Intel Celeron Processor system bus signals use a variation of the low-voltage swing GTL signaling technology. The AGTL system bus depends on incident wave switching and uses flight time for timing calculations of the AGTL signals, as opposed to capacitive derating. Intel recommends analog signal simulation of the system bus including trace lengths. Contact your field sales representative to receive the IBIS models for the Mobile Intel Celeron Processor.

The AGTL system bus of the Mobile Intel Celeron Processor is designed to support high-speed data transfers with multiple loads on a long bus that behaves like a transmission line. However, in mobile systems the system bus only has two loads (the processor and the chipset) and the bus traces are short. It is possible to change the layout and termination of the system bus to take advantage of the mobile environment using the same AGTL I/O buffers. This termination is provided on the processor core (except for the RESET# signal).

2.4 Mobile Intel Celeron Processor CPUID

When the CPUID version information is loaded with EAX=01H, the EAX and EBX registers contain the values shown in Table 3. After a power-on RESET, the EDX register contains the processor version information (type, family, model, stepping). Table 4 shows the CPUID Cache and TLB descriptor values after the L2 cache is initialized. See the *Intel Processor Identification* and the *CPUID Instruction Application Note AP-485* for further information.

Table 3. Mobile Intel Celeron Processor CPUID

EAX[31:0]					EBX[7:0]
Reserved [31:14]	**Type [13:12]**	**Family [11:8]**	**Model [7:4]**	**Stepping [3:0]**	**Brand ID**
X	0	6	B	X	07

Table 4. Mobile Intel Celeron Processor CPUID Cache and TLB Descriptors

Cache and TLB Descriptors	01H, 02H, 03H, 04H, 08H, 0CH, 83H

3. Electrical Specifications

3.1 Processor System Signals

Table 5 lists the processor system signals by type. All AGTL signals are synchronous with the BCLK and BCLK# signals. All TAP signals are synchronous with the TCK signal except TRST#. All CMOS input signals can be applied asynchronously.

Table 5. System Signal Groups

Group Name	Signals
AGTL Input	BPRI#, DEFER#, RESET#, RSP#
AGTL Output	PRDY#
AGTL I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BREQ0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#, RS[2:0]#, TRDY#
1.5 V CMOS Input	A20M#, DPSLP#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SMI#, STPCLK#
1.8 V CMOS Input	PWRGOOD
1.5 V Open Drain Output	FERR#, IERR#
3.3 V Open Drain Output	BSEL[1:0], VID[4:0]
1.25 V input	VTTPWRGD
Clock	BCLK, BCLK# (Differential Mode)
2.5 V Clock Input	BCLK (Single Ended Mode)
APIC Clock	PICCLK
APIC I/O	PICD[1:0]
Thermal Diode	THERMDC, THERMDA
TAP Input	TCK, TDI, TMS, TRST#
TAP Output	TDO
Power/Other	CLKREF, CMOSREF, EDGECTRLP, NC, NCTRL, PLL1, PLL2, RTTIMPEDP, V_{CC}, V_{CCT}, V_{REF}, V_{SS},

NOTES:
1. VCC is the power supply for the core logic.
2. PLL1 and PLL2 are power/ground for the PLL analog section. See Section 3.2.2 for details.
3. VCCT is the power supply for the system bus buffers.
4. VREF is the voltage reference for the AGTL input buffers.
5. VSS is system ground.

The APIC data and TAP outputs are Open-drain and should be pulled up to 1.5 V using resistors with the values shown in Table 6. If Open-drain drivers are used for input signals, then they should also be pulled up to the appropriate voltage using resistors with the values shown in Table 6.

Table 6. Recommended Resistors for Mobile Intel Celeron Processor Signals

Recommended Resistor Value (Ω)	Mobile Intel Celeron Processor Signal [1, 2]
10 pull-down	BREQ0#[3]
14 pull-up	NCTRL
39 pull-up	TMS
39 pull-down	TCK
56.2 pull-up	PRDY#, RESET#[4]
56.2 pull-down	RTTIMPEDP
110 pull-down	EDGECTRLP
150 pull-up	PICD[1:0], TDO
200-300 pull-up	PREQ#, TDI
500 pull-down	TRST#
1K pull-up	BSEL[1:0], TESTHI, VID[4:0], VTTPWRGD
1K pull-down	TESTLO
1.5k pull-up	FERR#, IERR#, PWRGOOD
3K pull-up	FLUSH#
Additional Pullup/Pulldown Resistor Recommendations[6]	
270 pull-up	SMI#
680 pull-up	STPCLK#
1.5k pull-up	A20M#, DPSLP#, INIT#, IGNNE#, LINT0/INTR, LINT1/NMI

NOTES:
1. The recommendations above are only for signals that are being used. These recommendations are maximum values only; stronger pull-ups may be used. Pull-ups for the signals driven by the chipset should not violate the chipset specification. Refer to Section 3.1.4 for the required pull-up or pull-down resistors for signals that are not being used.
2. Open-drain signals must never violate the undershoot specification in Section 4.3. Use stronger pull-ups if there is too much undershoot.
3. A pull-down on BREQ0# is an alternative to having the central agent to drive BREQ0# low at reset.
4. A 56.2 Ω 1% terminating resistor connected to V_{CCT} is required.
5. The following signals are actively driven high by the ICH3-M component and do not need external pull up resistors on ICH3-M based platforms: A20M#, DPSLP#, INIT#, IGNNE#, LINT0/INTR, LINT1/NMI, SMI#, STPCLK#.
6. These pull up recommendations apply to systems on which these signals are not actively pulled high such as those utilizing the 82443MX chipset.

3.1.1 Power Sequencing Requirements

Unlike the Mobile Intel Celeron Processor (0.18 µ), the Mobile Intel Celeron Processor (0.13 µ) does have specific power sequencing requirements. The power on sequencing and timings are shown in Figure 15 and Table 31. Power down timing requirements are shown in Figure 16, Figure 17, and Table 31. The V_{CC} power plane must not rise too fast. At least 200 µsec (T_R) must pass from the time that V_{CC} is at 10% of its nominal value until the time that V_{CC} is at 90% of its nominal value. For more details, please refer to the *Intel® Mobile Voltage Positioning -II (IMVP-II) Design Guide* (contact your Field Sales Representative).

3.1.2 Test Access Port (TAP) Connection

The TAP interface is an implementation of the IEEE 1149.1 (“JTAG”) standard. Due to the voltage levels supported by the TAP interface, Intel recommends that the Mobile Intel Celeron Processor and the other 1.5-V JTAG specification compliant devices be last in the JTAG chain after any devices with 3.3-V or 5.0-V JTAG interfaces within the system. A translation buffer should be used to reduce the TDO output voltage of the last 3.3/5.0 V device down to the 1.5-V range that the Mobile Intel Celeron Processor can tolerate. Multiple copies of TMS and TRST# must be provided, one for each voltage level.

A Debug Port and connector may be placed at the start and end of the JTAG chain containing the processor, with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. There are no requirements for placing the Mobile Intel Celeron Processor in the JTAG chain, except for those that are dictated by voltage requirements of the TAP signals.

3.1.3 Catastrophic Thermal Protection

The Mobile Intel Celeron Processor does not support catastrophic thermal protection or the THERMTRIP# signal. An external thermal sensor must be used to protect the processor and the system against excessive temperatures. If the external thermal sensor detects a processor junction temperature of 101 °C (maximum), both the V_{CC} and V_{CCT} supplies to the processor must be reduced to at least 50% of the nominal values within 500 ms and are recommended to be turned off completely within 1 second to prevent damage to the processor. Processor temperature must be monitored in all states including low power states.

3.1.4 Unused Signals

All signals named NC must be unconnected. Unused AGTL inputs, outputs, and bi-directional signals should be unconnected. Unused CMOS active low inputs should be connected to 1.5 V and unused active high inputs should be connected to V_{SS}. Unused Open-drain outputs should be unconnected. When tying any signal to power or ground, a resistor will allow for system testability. For unused signals, Intel suggests that 1.5-kΩ resistors are used for pull-ups and 1.0-kΩ resistors are used for pull-downs.

PICCLK must be driven with a clock that meets specification and the PICD[1:0] signals must be pulled up **separately** to 1.5 V with 150-Ω resistors, even if the local APIC is not used.

If the TAP signals are not used then the inputs should be pulled to ground with 1-kΩ resistors and TDO should be left unconnected.

3.1.5 Signal State in Low-power States

3.1.5.1 System Bus Signals

All of the system bus signals have AGTL input, output, or input/output drivers. Except when servicing snoops, the system bus signals are tri-stated and pulled up by the termination resistors. Snoops are not permitted in the Deep Sleep state.

3.1.5.2 CMOS and Open-drain Signals

The CMOS input signals are allowed to be in either the logic high or low state when the processor is in a low-power state. In the Auto Halt state these signals are allowed to toggle. These input buffers have no internal pull-up or pull-down resistors and system logic can use CMOS or Open-drain drivers to drive them.

The Open-drain output signals have open drain drivers and external pull-up resistors are required. One of the two output signals (IERR#) is a catastrophic error indicator and is tri-stated (and pulled-up) when the processor is functioning normally. The FERR# output can be either tri-stated or driven to V_{SS} when the processor is in a low-power state depending on the condition of the floating-point unit. Since this signal is a DC current path when it is driven to V_{SS}, Intel recommends that the software clears or masks any floating-point error condition before putting the processor into the Deep Sleep state.

3.1.5.3 Other Signals

The system bus clocks (BCLK, BCLK#) must be driven in all of the low-power states except the Deep Sleep state. The APIC clock (PICCLK) must be driven whenever BCLK and BCLK# are driven. Otherwise, it is permitted to turn off PICCLK by holding it at V_{SS}. BCLK and BCLK# should be obey the DC levels in Table 38 (for Differential Clocking) and Table 39 (for Single Ended Clocking).

In the Auto Halt state, the APIC bus data signals (PICD[1:0]) may toggle due to APIC bus messages. These signals are required to be tri-stated and pulled-up when the processor is in the Quick Start or Deep Sleep states.

3.2 Power Supply Requirements

3.2.1 Decoupling Guidelines

The Mobile Intel Celeron Processor in Micro-FCPGA package has twelve 0805IDC, 1-µF surface mount decoupling capacitors. Eight capacitors are on the V_{CC} supply and four capacitors are on $V_{CCT.}$ For the Micro-FCBGA package, there are six 0.68-µF capacitors on V_{CC} and two 0.68-µF capacitors on V_{CCT}. In addition to the package capacitors, sufficient board level capacitors are also necessary for power supply decoupling. The guidelines are as follows:

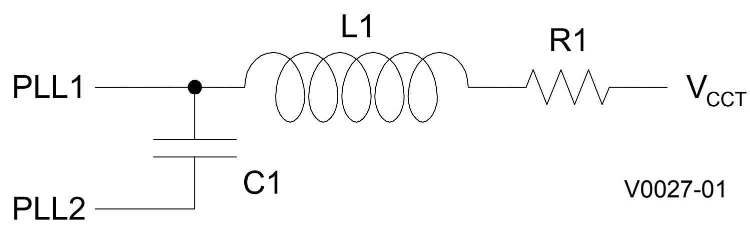
- High and Mid Frequency V_{CC} decoupling – Place twenty-four 0.22-µF 0603 capacitors directly under the package on the solder side of the motherboard using at least two vias per capacitor node. Ten 10-µF X7 6.3V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.
- High and Mid Frequency V_{CCT} decoupling – Place ten 1-µF X7R 0603 ceramic capacitors close to the package. Via and trace guidelines are the same as above.
- Bulk V_{CC} decoupling – Minimum of 1200-µF capacitance with Equivalent Series Resistance (ESR) less than or equal to 3.5 mΩ.
- Bulk V_{CCT} decoupling – Platform dependent but recommendation is minimum of 660 µF with ESR less than or equal to 7 mΩ.

Please refer to the appropriate platform design guidelines for bulk decoupling recommendations.

3.2.2 Voltage Planes

All V_{CC} and V_{SS} pins/balls must be connected to the appropriate voltage plane. All V_{CCT} and V_{REF} pins/balls must be connected to the appropriate traces on the system electronics. In addition to the main V_{CC}, V_{CCT}, and V_{SS} power supply signals, PLL1 and PLL2 provide analog decoupling to the PLL section. PLL1 and PLL2 should be connected according to Figure 2. Do not connect PLL2 directly to V_{SS}. Appendix A contains the RLC filter specification.

Figure 2. PLL RLC Filter



3.2.3 Voltage Identification

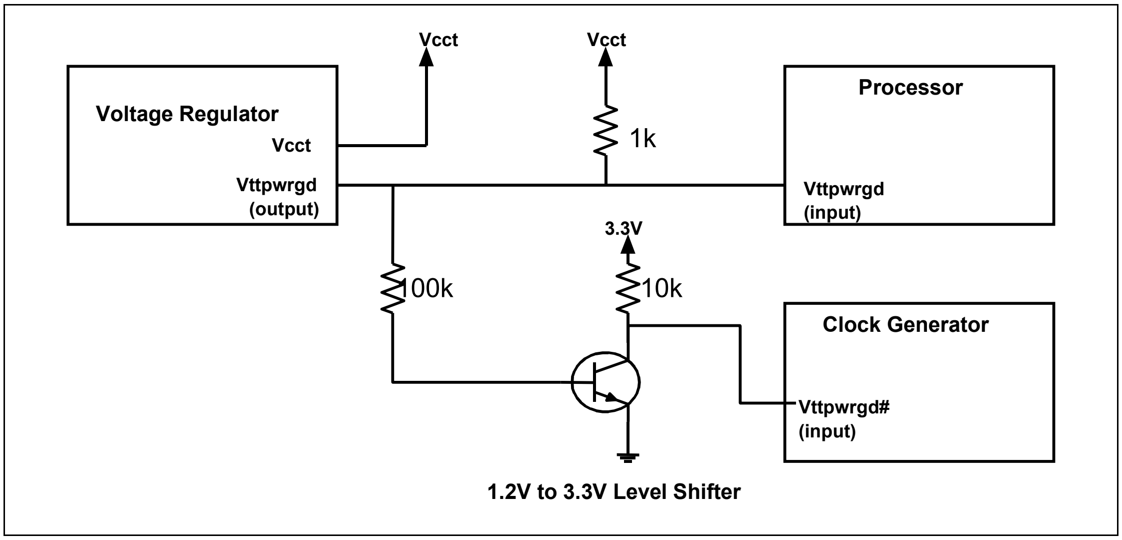
There are five voltage identification balls/pins on the Mobile Intel Celeron Processor. These signals can be used to support automatic selection of V_{CC} voltages. They are needed to cleanly support voltage specification variations on current and future processors. VID[4:0] are defined in Table 7. The voltages specified in the VID table are the Battery Optimized Mode V_{CC} voltages. The VID[4:0] signals are open drain on the processor and need pull-up resistors to 3.3 V on the motherboard. Please refer to the mobile VR guidelines provided by Intel for additional information.

Table 7. Mobile Intel Celeron Processor VID Values

VID[4:0]	V_{CC} (V)	VID[4:0]	V_{CC} (V)	VID[4:0]	V_{CC} (V)	VID[4:0]	V_{CC} (V)
00000	1.750	01000	1.350	10000	0.975	11000	0.775
00001	1.700	01001	1.300	10001	0.950	11001	0.750
00010	1.650	01010	1.250	10010	0.925	11010	0.725
00011	1.600	01011	1.200	10011	0.900	11011	0.700
00100	1.550	01100	1.150	10100	0.875	11100	0.675
00101	1.500	01101	1.100	10101	0.850	11101	0.650
00110	1.450	01110	1.050	10110	0.825	11110	0.625
00111	1.400	01111	1.000	10111	0.800	11111	0.600

Figure 3 shows the system level connections for the VTTPWRGD signal. Please refer to the appropriate VR and system level guidelines provided by Intel for more details.

Figure 3. VTTPWRGD System-Level Connections



3.2.4 VTTPWRGD Signal Quality Specification

The VTTPWRGD signal is an input to the processor used to determine that the VTT power is stable and the VID and BSEL signals should be driven to their final state by the processor. To ensure the processor correctly reads this signal, it must meet the following requirement while the signal is in its transition region of 300 mV to 900 mV. Also, VTTPWRGD should only enter the transition region once, after VTT is at nominal values, for the assertion of the signal.

Table 8. VTTPWRGD Noise Specification

Parameter	Specification
Amount of noise (glitch)	Less than 100 mV

In addition, the VTTPWRGD signal should have reasonable transition time through the transition region. A sharp edge on the signal transition will minimize the chance of noise causing a glitch on this signal. Intel recommends the following transition time for the VTTPWRGD signal.

Table 9. VTTPWRGD Transition Time Specification

Parameter	Recommendation
Transition time (300 mV to 900 mV)	Less than or equal to 100 µs

3.2.4.1 Transition Region

The transition region covered by this requirement is 300 mV to 900 mV. Once the VTTPWRGD signal is in that voltage range, the processor is more sensitive to noise, which may be present on the signal. The transition region when the signal first crosses the 300 mV voltage level and continues until the last time it is below 900 mV.

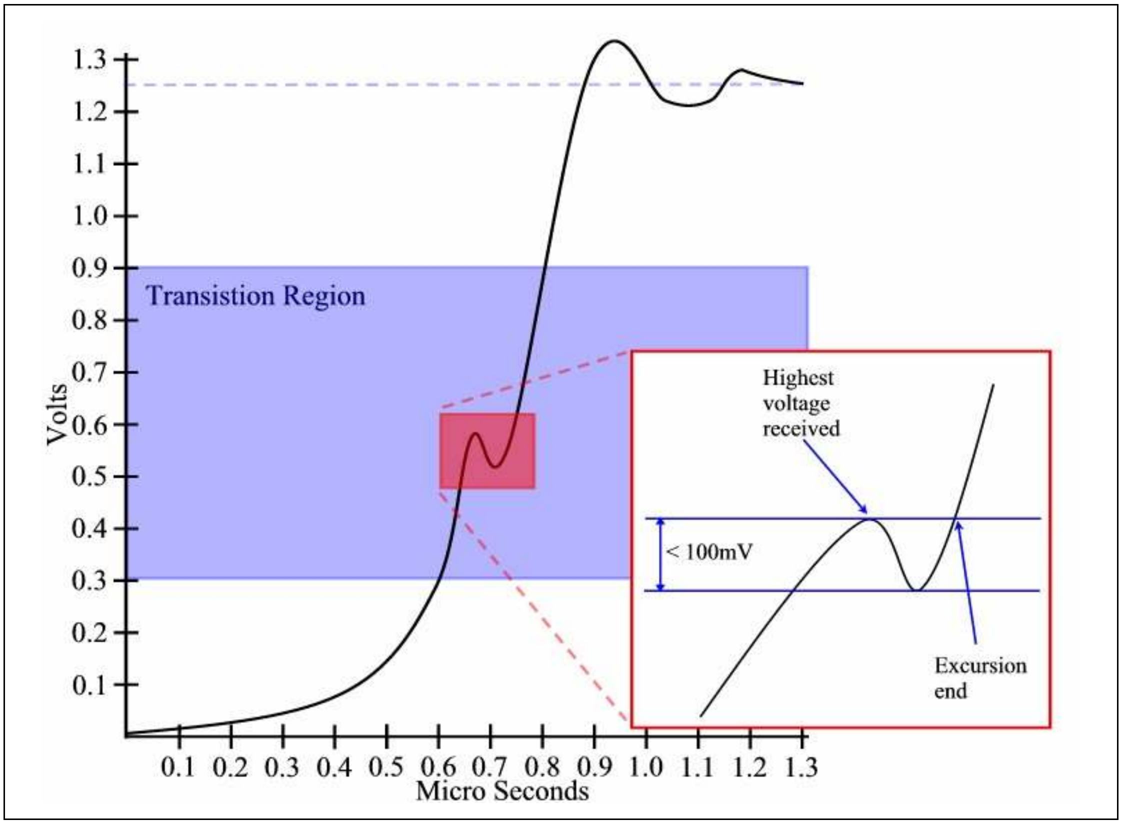
3.2.4.2 Transition Time

The transition time is defined as the time the signal takes to move through the transition region. A 100-µs transition time will ensure that the processor receives a good transition edge.

3.2.4.3 Noise

The signal quality of the VTTPWRGD signal is critical to the correct operation of the processor. Every effort should be made to ensure this signal is monotonic in the transition region. If noise or glitches are present on this signal, it must be kept to less than 100 mV of a voltage drop from the highest voltage level received to that point. This glitch must remain less than 100 mV until the excursion ends by the voltage returning to the highest voltage previously received. Please see Figure 4 for an example graph of this situation and requirements.

Figure 4. Noise Estimation



3.3 System Bus Clock and Processor Clocking

The BCLK and BCLK# clock inputs directly control the operating speed of the system bus interface. All system bus timing parameters are specified with respect to the crossing point of the rising edge of the BCLK input and falling edge of the BCLK# input. The Mobile Intel Celeron Processor core frequency is a multiple of the BCLK frequency. The processor core frequency is configured during manufacturing. The configured bus ratio is visible to software in the Power-on configuration register. See Section 7.2 for details.

Multiplying the bus clock frequency is necessary to increase performance while allowing for easier distribution of signals within the system. Clock multiplication within the processor is provided by the internal Phase Lock Loop (PLL), which requires constant frequency BCLK and BCLK# inputs. During Reset or on exit from the Deep Sleep state, the PLL requires some amount of time to acquire the phase of BCLK and BCLK#. This time is called the PLL lock latency, which is specified in Section 3.6, AC timing parameters T18 and T47.

3.4 Maximum Ratings

Table 10 contains the Mobile Intel Celeron Processor stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are provided in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 10. Mobile Intel Celeron Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{Storage}$	Storage Temperature	–40	85	°C	Note 1
V_{CC}(Abs)	Supply Voltage with respect to V_{SS}	–0.5	1.75	V	
V_{CCT}	System Bus Buffer Voltage with respect to V_{SS}	–0.3	1.75	V	
$V_{IN\ GTL}$	System Bus Buffer DC Input Voltage with respect to V_{SS}	–0.3	1.75	V	Notes 2, 3
V_{IN125}	1.25 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	1.75	V	Note 4
V_{IN15}	1.5 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	2.0	V	Note 5
V_{IN18}	1.8 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	2.0	V	Note 6
V_{IN20}	2.0 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	2.4	V	Note 7
V_{IN25}	2.5 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	3.3	V	Note 9
V_{INVID}	VID ball/pin DC Input Voltage with respect to V_{SS}	—	3.465	V	Note 8
I_{VID}	VID Current	-0.3	3.6	mA	Note 8

NOTES:

1. The shipping container is only rated for 65°C.
2. Parameter applies to the AGTL signal groups only. Compliance with both $V_{IN\ GTL}$ specifications is required.
3. The voltage on the AGTL signals must never be below –0.3 V or above 1.75 V with respect to ground.
4. Parameter applies to CLKREF, TESTHI, VTTPWRGD signals.
5. Parameter applies to CMOS, Open-drain, APIC, TESTLO and TAP bus signal groups only.
6. Parameter applies to PWRGOOD signal.
7. Parameter applies to PICCLK signal.
8. Parameter applies to each VID pin/ball individually.
9. Parameter applies to BCLK signal in Single Ended Clocking Mode.

3.5 DC Specifications

Table 11 through Table 24 list the DC specifications for the Mobile Intel Celeron Processor. Specifications are valid only while meeting specifications for the junction temperature, clock frequency, and input voltages. The junction temperature range for all DC specifications is 0°C to 100°C unless otherwise noted. Care should be taken to read all notes associated with each parameter. Unlike the Mobile Intel Pentium III Processor, the V_{cc} tolerances for the Mobile Intel Celeron Processor are not specified as a percentage of nominal. The tolerances are instead specified in the form of load lines for the static and transient cases in Table 12 through Table 21. Illustration of the load lines is shown in Figure 5 through Figure 8.

Table 11. Power Specifications for Mobile Intel Celeron Processor[1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CC}	Transient V_{CC} for core logic		1.10 1.15 1.40 1.45 1.50		V V V V V	Note 11 Notes 9, 10 Notes 9, 10 Notes 9, 10 Notes 9, 10
$V_{CC,DC}$	Static V_{CC} for core logic		1.10 1.15 1.40 1.45 1.50		V V V V V	Note 11 Notes 9, 10 Notes 9, 10 Notes 9, 10 Notes 9, 10
V_{CCT}	V_{CC} for System Bus Buffers, Transient tolerance	1.138	1.25	1.362	V	± 9%, Notes 7,10
$V_{CCT,DC}$	V_{CC} for System Bus Buffers, Static tolerance	1.188	1.25	1.312	V	±5%, Notes 2,10
I_{CC}	Current for V_{CC} at core frequency 800 MHz & 1.10V 733 MHz & 1.10 V 700 MHz & 1.10 V 650 MHz & 1.10 V 650 MHz & 1.15 V 667 MHz & 1.15 V 733 MHz & 1.15 V 866 MHz & 1.15 V 1.00 GHz & 1.40 V 1.26 GHz & 1.40V 1.06 GHz & 1.45 V 1.13 GHz & 1.45 V 1.20 GHz & 1.45 V 1.33 GHz & 1.50 V			 7.58 7.98 7.89 7.58 10.52 10.68 11.27 10.03 18.27 18.75 18.67 19.14 19.63 15.90	A	 Notes 4, 11 Notes 4, 11 Notes 4, 11 Notes 4, 11 Note 4 Note 4 Note 4 Note 4
I_{CCT}	Current for V_{CCT}			2.7	A	Notes 3, 4
$I_{CC,AH}$	Processor Auto Halt current at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V			 3.09 5.42 8.85 10.20 10.73	A	Note 4 Notes 4, 11
$I_{CC,QS}$	Processor Quick Start current at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V			 2.91 5.16 8.53 9.80 9.90	A	Note 4 Notes 4, 11
$I_{CC,DSLP}$	Processor Deep Sleep Leakage current at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V			 2.65 4.79 8.04 9.20 9.20	A	Note 4 Notes 4, 11
I_{LVID}	VID leakage current			0.5	mA	Note 8
dI_{CC}/dt	V_{CC} power supply current slew rate			400	A/µs	Notes 5, 6

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. Processors will comply with the $I_{CCx,max}$ specification for the current mode of operation.
2. Static voltage regulation includes: DC output initial voltage set point adjust, output ripple and noise, temperature and warm up.
3. I_{CCT} is the current supply for the system bus buffers, including the on-die termination.

4. $I_{CCx,max}$ specifications are specified at V_{CC} static (typical) derived from the tolerances in Table 12 through Table 19, $V_{CCT,max}$, Tjmax, and under maximum signal loading conditions.
5. Based on simulations and averaged over the duration of any change in current. Use to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
6. Maximum values specified by design/characterization at nominal V_{CC} and V_{CCT}.
7. V_{CCx} must be within this range under all operating conditions, including maximum current transients. V_{CCx} must return to within the static voltage specification, $V_{CCx,DC}$, within 100 µs after a transient event.
8. VID leakage current is < 100 µA for VID voltages under 3.0 V.
9. Typical V_{CC} indicates the VID encoded voltage. Voltage supplied must conform to the load line specification shown in Table 12 through Table 19.
10. Voltages are measured at the processor socket pin for the Micro-FCPGA part and at the package ball on the Micro-FCBGA part.
11. This specification applies only to the Ultra Low Voltage Mobile Intel Celeron Processor.

Table 12. V_{CC} Tolerances for the Low Voltage Mobile Intel Celeron Processor: VID = 1.15 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.150	1.125	1.175	1.105	1.195
1.0	1.146	1.121	1.171	1.101	1.191
2.0	1.142	1.117	1.167	1.097	1.187
3.0	1.138	1.113	1.163	1.093	1.183
4.0	1.134	1.109	1.159	1.089	1.179
5.0	1.130	1.105	1.155	1.085	1.175
6.0	1.126	1.101	1.151	1.081	1.171
7.0	1.122	1.097	1.147	1.077	1.167
8.0	1.118	1.093	1.143	1.073	1.163
9.0	1.114	1.089	1.139	1.069	1.159
10.0	1.110	1.085	1.135	1.065	1.155
11.0	1.106	1.081	1.131	1.061	1.151
12.0	1.102	1.077	1.127	1.057	1.147
13.0	1.098	1.073	1.123	1.053	1.143
14.0	1.094	1.069	1.119	1.049	1.139
15.0	1.090	1.065	1.115	1.045	1.135

Table 13. V_{CC} Tolerances for the Low Voltage Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.15 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.114	1.089	1.139	1.069	1.159
1.0	1.110	1.085	1.135	1.065	1.155
2.0	1.106	1.081	1.131	1.061	1.151
3.0	1.102	1.077	1.127	1.057	1.147
4.0	1.098	1.073	1.123	1.053	1.143
5.0	1.094	1.069	1.119	1.049	1.139
6.0	1.090	1.065	1.115	1.045	1.135

Table 14. V_{CC} Tolerances for the Ultra Low Voltage Mobile Intel Celeron Processor: VID = 1.1 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.100	1.075	1.125	1.055	1.145
1.0	1.096	1.071	1.121	1.051	1.141
2.0	1.092	1.067	1.117	1.047	1.137
3.0	1.088	1.063	1.113	1.043	1.133
4.0	1.084	1.059	1.109	1.039	1.129
5.0	1.080	1.055	1.105	1.035	1.125
6.0	1.076	1.051	1.101	1.031	1.121
7.0	1.072	1.047	1.097	1.027	1.117
8.0	1.068	1.043	1.093	1.023	1.113
9.0	1.064	1.039	1.089	1.019	1.109
10.0	1.060	1.035	1.085	1.015	1.105
11.0	1.056	1.031	1.081	1.011	1.101
12.0	1.052	1.027	1.077	1.007	1.097
13.0	1.048	1.023	1.073	1.003	1.093

Table 15. V_{CC} Tolerances for the Ultra Low Voltage Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.1 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.068	1.043	1.093	1.023	1.113
1.0	1.064	1.039	1.089	1.019	1.109
2.0	1.060	1.035	1.085	1.015	1.105
3.0	1.056	1.031	1.081	1.011	1.101
4.0	1.052	1.027	1.077	1.007	1.097
5.0	1.048	1.023	1.073	1.003	1.093

Table 16. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.40 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.400	1.375	1.425	1.355	1.445
1.0	1.396	1.371	1.421	1.351	1.441
2.0	1.392	1.367	1.417	1.347	1.437
3.0	1.388	1.363	1.413	1.343	1.433
4.0	1.384	1.359	1.409	1.339	1.429
5.0	1.380	1.355	1.405	1.335	1.425
6.0	1.376	1.351	1.401	1.331	1.421
7.0	1.372	1.347	1.397	1.327	1.417
8.0	1.368	1.343	1.393	1.323	1.413
9.0	1.364	1.339	1.389	1.319	1.409
10.0	1.360	1.335	1.385	1.315	1.405
11.0	1.356	1.331	1.381	1.311	1.401
12.0	1.352	1.327	1.377	1.307	1.397
13.0	1.348	1.323	1.373	1.303	1.393
14.0	1.344	1.319	1.369	1.299	1.389
15.0	1.340	1.315	1.365	1.295	1.385
16.0	1.336	1.311	1.361	1.291	1.381
17.0	1.332	1.307	1.357	1.287	1.377
18.0	1.328	1.303	1.353	1.283	1.373
19.0	1.324	1.299	1.349	1.279	1.369
20.0	1.320	1.295	1.345	1.275	1.365
21.0	1.316	1.291	1.341	1.271	1.361
22.0	1.312	1.287	1.337	1.267	1.357
23.0	1.308	1.283	1.333	1.263	1.353

Table 17. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.40 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.338	1.313	1.363	1.293	1.383
1.0	1.334	1.309	1.359	1.289	1.379
2.0	1.330	1.305	1.355	1.285	1.375
3.0	1.326	1.301	1.351	1.281	1.371
4.0	1.322	1.297	1.347	1.277	1.367
5.0	1.318	1.293	1.343	1.273	1.363
6.0	1.314	1.289	1.339	1.269	1.359
7.0	1.310	1.285	1.335	1.265	1.355
8.0	1.306	1.281	1.331	1.261	1.351

Table 18. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.45 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.450	1.425	1.475	1.405	1.495
1.0	1.446	1.421	1.471	1.401	1.491
2.0	1.442	1.417	1.467	1.397	1.487
3.0	1.438	1.413	1.463	1.393	1.483
4.0	1.434	1.409	1.459	1.389	1.479
5.0	1.430	1.405	1.455	1.385	1.475
6.0	1.426	1.401	1.451	1.381	1.471
7.0	1.422	1.397	1.447	1.377	1.467
8.0	1.418	1.393	1.443	1.373	1.463
9.0	1.414	1.389	1.439	1.369	1.459
10.0	1.410	1.385	1.435	1.365	1.455
11.0	1.406	1.381	1.431	1.361	1.451
12.0	1.402	1.377	1.427	1.357	1.447
13.0	1.398	1.373	1.423	1.353	1.443
14.0	1.394	1.369	1.419	1.349	1.439
15.0	1.390	1.365	1.415	1.345	1.435
16.0	1.386	1.361	1.411	1.341	1.431
17.0	1.382	1.357	1.407	1.337	1.427
18.0	1.378	1.353	1.403	1.333	1.423
19.0	1.374	1.349	1.399	1.329	1.419
20.0	1.370	1.345	1.395	1.325	1.415
21.0	1.366	1.341	1.391	1.321	1.411
22.0	1.362	1.337	1.387	1.317	1.397
23.0	1.358	1.333	1.383	1.313	1.393

Table 19. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.45 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.388	1.363	1.413	1.343	1.433
1.0	1.384	1.359	1.409	1.339	1.429
2.0	1.380	1.355	1.405	1.335	1.425
3.0	1.376	1.351	1.401	1.331	1.421
4.0	1.372	1.347	1.397	1.327	1.417
5.0	1.368	1.343	1.393	1.323	1.413
6.0	1.364	1.339	1.389	1.319	1.409
7.0	1.360	1.335	1.385	1.315	1.405
8.0	1.356	1.331	1.381	1.31	1.401

Table 20. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.50 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.50	1.475	1.525	1.455	1.545
1.0	1.496	1.471	1.521	1.451	1.541
2.0	1.492	1.467	1.517	1.447	1.537
3.0	1.488	1.463	1.513	1.443	1.533
4.0	1.484	1.459	1.509	1.439	1.529
5.0	1.480	1.455	1.505	1.435	1.525
6.0	1.476	1.451	1.501	1.431	1.521
7.0	1.472	1.447	1.497	1.427	1.517
8.0	1.468	1.443	1.493	1.423	1.513
9.0	1.464	1.439	1.489	1.419	1.509
10.0	1.460	1.435	1.485	1.415	1.505
11.0	1.456	1.431	1.481	1.411	1.501
12.0	1.452	1.427	1.477	1.407	1.497
13.0	1.448	1.423	1.473	1.403	1.493
14.0	1.444	1.419	1.469	1.399	1.489
15.0	1.440	1.415	1.465	1.395	1.485
16.0	1.436	1.411	1.461	1.391	1.481
17.0	1.432	1.407	1.457	1.387	1.477
18.0	1.428	1.403	1.453	1.383	1.473
19.0	1.424	1.399	1.449	1.379	1.469
20.0	1.420	1.395	1.445	1.375	1.465
21.0	1.416	1.391	1.441	1.371	1.461
22.0	1.412	1.387	1.437	1.367	1.457
23.0	1.408	1.383	1.433	1.363	1.453

Table 21. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.50 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.438	1.413	1.463	1.393	1.483
1.0	1.434	1.409	1.459	1.389	1.479
2.0	1.430	1.405	1.455	1.385	1.475
3.0	1.426	1.401	1.451	1.381	1.471
4.0	1.422	1.397	1.447	1.377	1.467
5.0	1.418	1.393	1.443	1.373	1.463
6.0	1.414	1.389	1.439	1.369	1.459
7.0	1.410	1.385	1.435	1.365	1.455
8.0	1.406	1.381	1.431	1.361	1.451

Figure 5. Illustration of V_{CC} Static and Transient Tolerances (VID = 1.15 V)

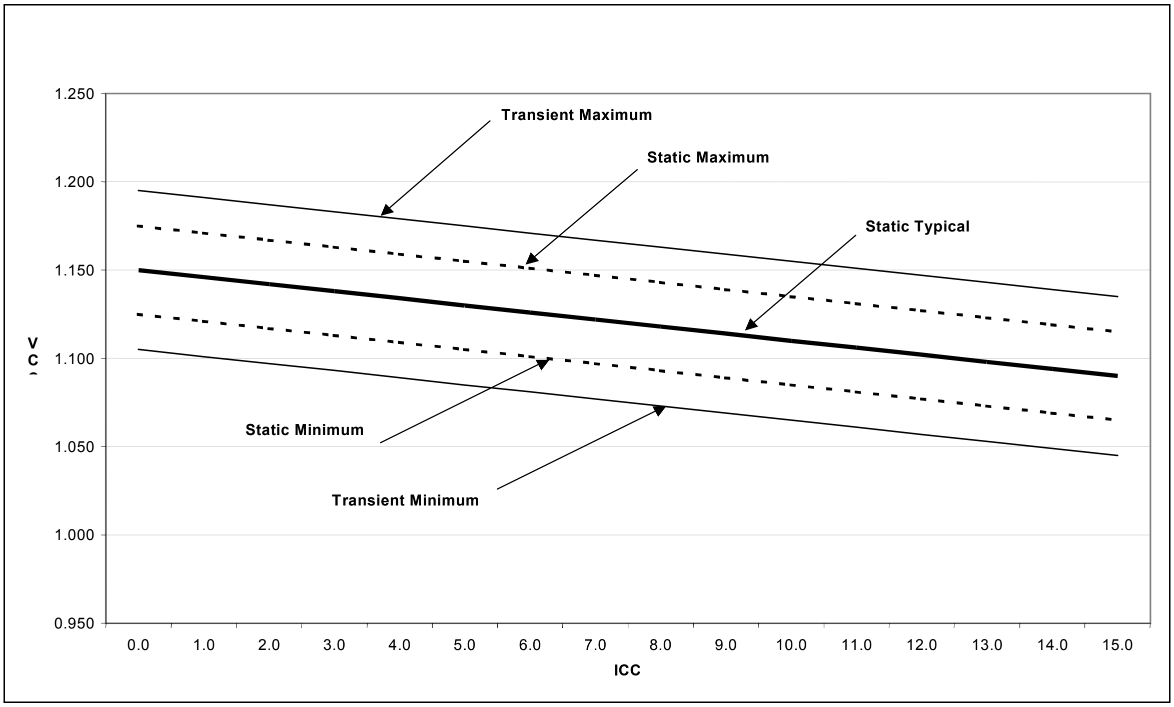


Figure 6. Illustration of Deep Sleep V_{CC} Static and Transient Tolerances (VID Setting = 1.15 V)

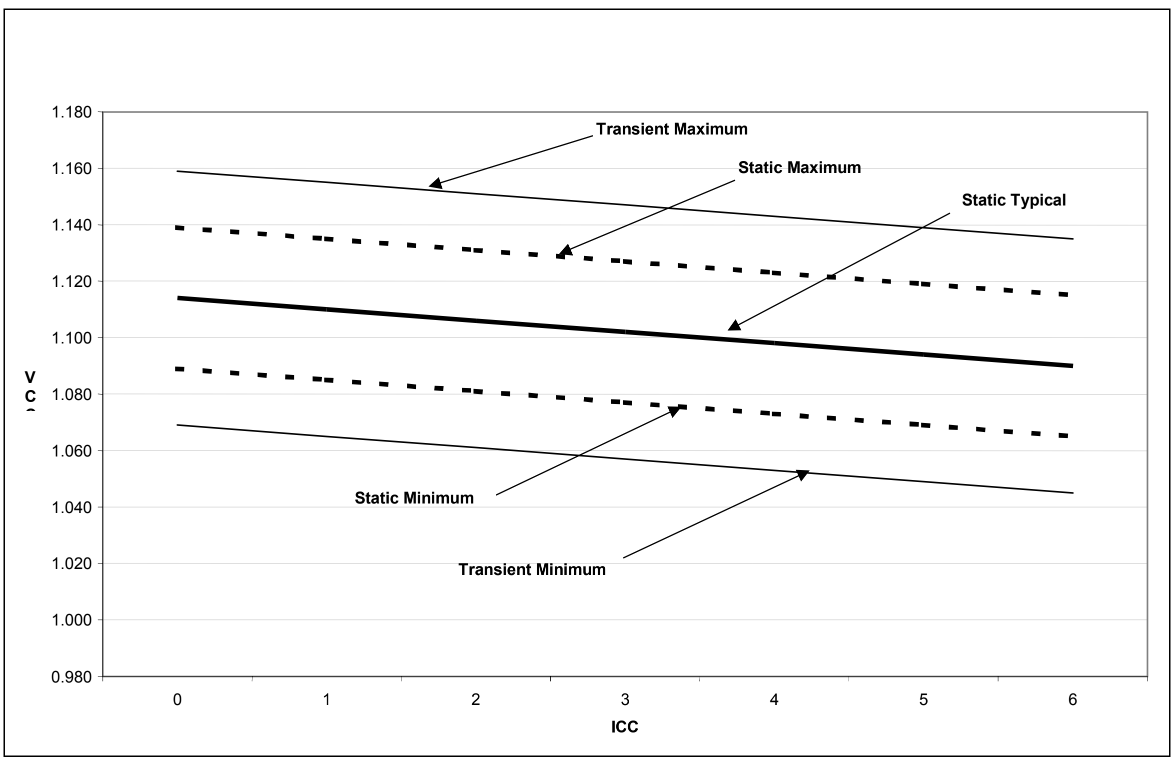


Figure 7. Illustration of V_{CC} Static and Transient Tolerances (VID = 1.40 V)

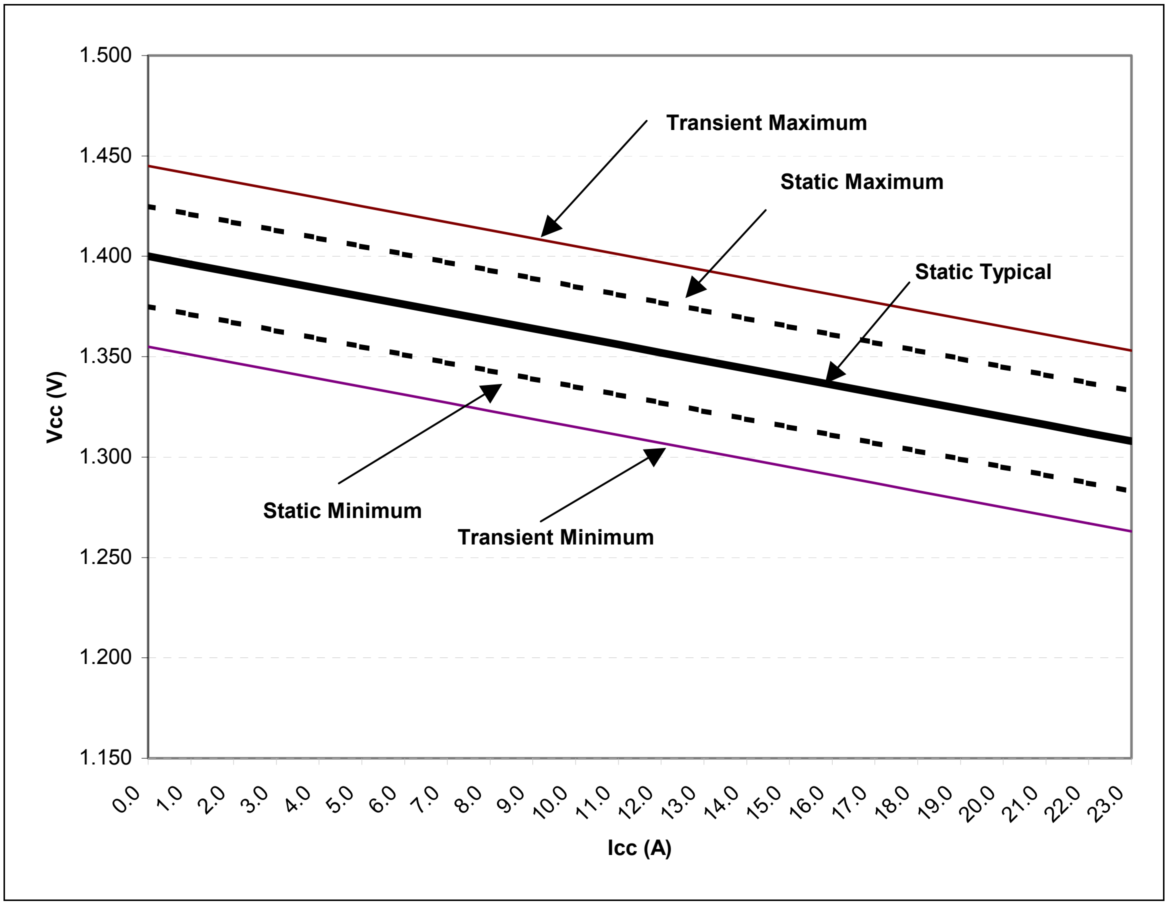


Figure 8. Illustration of Deep Sleep V_{CC} Static and Transient Tolerances (VID Setting = 1.40 V)

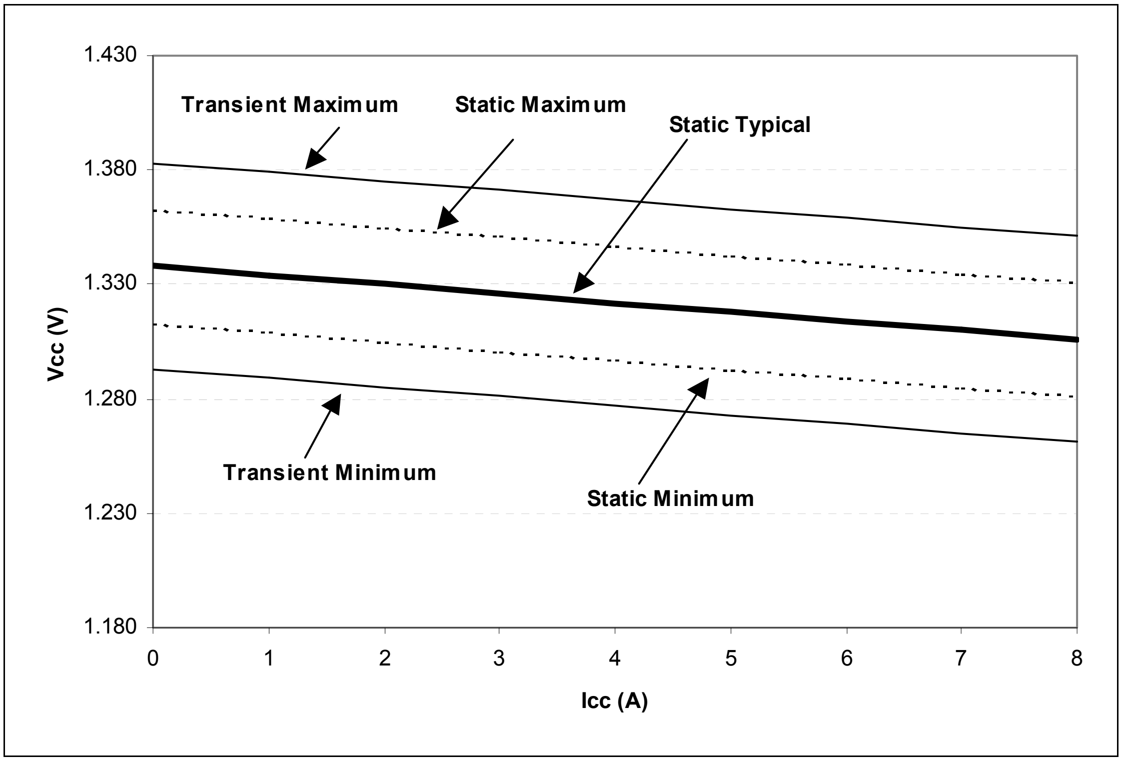


Table 22. AGTL Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.15	V_{REF}-0.2	V	
V_{IH}	Input High Voltage	V_{REF}+0.2	V_{CCT}	V	See $V_{CCT,max}$ in Table 11
V_{OH}	Output High Voltage	—	—	V	See $V_{CCT,max}$ in Table 11
R_{ON}	Output Low Drive Strength		16.67	Ω	Note 2
I_L	Leakage Current for Inputs, Outputs and I/Os		100	μA	Note 1

NOTES:

1. Specification applies to leakage high only, for pins with on die R_{TT}, ($0 < V_{IN/OUT} \leq V_{CCT}$).
2. Refer to IBIS models for I/V characteristics.

Table 23. AGTL Bus DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCT}	Bus Termination Voltage		1.25		V	Note 1
V_{REF}	Input Reference Voltage	$^2/_3 V_{CCT}$ – 2%	$^2/_3 V_{CCT}$	$^2/_3 V_{CCT}$ + 2%	V	±2%, Note 2
R_{TT}	Bus Termination Strength	50	56	65	Ω	On-die R_{TT}, Note 3

NOTES:

1. Please refer to Table 11 for minimum and maximum values.
2. V_{REF} should be created from V_{CCT} by a voltage divider.
3. The RESET# signal does not have an on-die R_{TT}. It requires an off-die 56.2 Ω ±1% terminating resistor connected to V_{CCT}.

Table 24. CLKREF, APIC, TAP, CMOS, and Open-drain Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL15}	Input Low Voltage, 1.5 V CMOS	–0.15	$V_{CMOSREFmin}$ – 300 mV	V	
V_{IL18}	Input Low Voltage, 1.8 V CMOS	–0.36	0.36	V	Notes 1, 2
V_{IH15}	Input High Voltage, 1.5 V CMOS	$V_{CMOSREFmax}$ + 250 mV	2.0	V	Note 10
$V_{IH15PICD}$	Input High Voltage, 1.5 V PICD[1:0]	$V_{CMOSREFmax}$ + 200 mV	2.0	V	Note 11
V_{IH18}	Input High Voltage, 1.8 V CMOS	1.44	2.0	V	Notes 1, 2
V_{OH15}	Output High Voltage, 1.5 V CMOS	N/A	1.615	V	All outputs are Open-drain
V_{OH33}	Output High Voltage, 3.3 V signals	2.0	3.465	V	3.3V + 5%
V_{OL33}	Output Low Voltage, 3.3 V signals		0.8	V	
V_{OL}	Output Low Voltage		0.3	V	Note 8
$V_{CMOSREF}$	CMOSREF Voltage	0.90	1.10	V	Note 4
V_{CLKREF}	CLKREF Voltage	1.187	1.312	V	Note 9
$V_{ILVTTPWR}$	Input Low Voltage, VTTPWRGD		0.4	V	Note 7
$V_{IHVTTPWR}$	Input High Voltage, VTTPWRGD	1.0		V	Note 7
R_{ON}			30	Ω	Note 3
I_{OL}	Output Low Current	10		mA	Note 6
I_L	Leakage Current for Inputs, Outputs and I/Os		±100	µA	Note 5

NOTES:
1. Parameter applies to the PWRGOOD signal only.
2. $V_{Ilx,min}$ and $V_{Ihx,max}$ only apply when BCLK, BCLK# and PICCLK are stopped. PICCLK should be stopped in the low state. See Table 33 and Table 34 for DC levels when BCLK and BCLK# are stopped.
3. Measured at 9 mA.
4. $V_{CMOSREF}$ should be created from a stable 1.5-V supply using a voltage divider. It must track the voltage supply to maintain noise immunity. The same 1.5-V supply should be used to power the chipset CMOS I/O buffers that drive these signals.
5. $(0 \leq _{VIN/OUT} \leq V_{Ihx,max})$.
6. Specified as the minimum amount of current that the output buffer must be able to sink. However, $V_{OL,max}$ cannot be guaranteed if this specification is exceeded.
7. Parameter applies to VTTPWRGD signal only.
8. Applies to non-AGTL signals except BCLK, PWRGOOD, PICCLK, BSEL[1:0], VID[4:0].
9. ±5% DC tolerance. CLKREF must be generated from the 2.5-V supply used to generate the BCLK signal. AC Tolerance must be less than –40 dB @ 1 MHz.
10. Applies to all TAP and CMOS signals (not to APIC signals).
11. Applies to PICD[1:0].

3.6 AC Specifications

3.6.1 System Bus, Clock, APIC, TAP, CMOS, and Open-drain AC Specifications

All system bus AC specifications for the AGTL signal group are relative to the crossing point of the rising edge of the BCLK input and falling edge of the BCLK# input. All AGTL timings are referenced to V_{REF} for both "0" and "1" logic levels unless otherwise specified. All APIC, TAP, CMOS, and Open-drain signals except PWRGOOD are referenced to 1.0 V. All minimum and maximum specifications are at points within the power supply ranges shown in Table 12 through Table 21 and junction temperatures

(Tj) in the range 0°C to 100°C unless otherwise noted. Tj **must** be less than or equal to 100°C (or the otherwise-noted given value) for all functional processor states.

Table 25. System Bus Clock AC Specifications (Differential) [1]

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
	System Bus Frequency		133		MHz		
T1	BCLK Period – average	7.5		7.7	ns	8	Note 2
T1abs	BCLK Period – Instantaneous minimum	7.3			ns	8	Note 2
T2	BCLK Cycle to Cycle Jitter			200	ps	8	Notes 2, 3, 4
T5	BCLK Rise Time	175 175		467 550	ps	8	Notes 2, 6, 8 Notes 2, 6, 9
T6	BCLK Fall Time	175 175		467 550	ps	8	Notes 2, 6, 8 Notes 2, 6, 9
	Vcross for 1-V swing	0.51		0.76	V	7	Note 7
	Rise/Fall Time Matching			325	ps	7	Note 5
	BCLK Duty Cycle	45%		55%		8	Note 2

NOTES:

1. All AC timings for AGTL and CMOS signals are referenced to the BCLK and BCLK# crossing point.
2. Measured on differential waveform: defined as (BCLK – BCLK#).
3. Not 100% tested. Specified by design/characterization.
4. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that the clock driver be designed to meet a period stability specification into a test load of 10 pF to 20 pF. This should be measured on the rising edge of adjacent BCLKs at the BCLK, BCLK# crossing point. The jitter present must be accounted for as a component of BCLK skew between devices. Period difference is measured around 0-V crossing points.
5. Measurement taken from common mode waveform, measure rise/fall time from 0.41 to 0.86 V. Rise/fall time matching is defined as “the instantaneous difference between maximum BCLK rise (fall) and minimum BCLK# fall (rise) time, or minimum BCLK rise (fall) and maximum BCLK# fall (rise) time ”. This parameter is designed to guard waveform symmetry.
6. Rise time is measured from –0.35 V to 0.35 V and fall time is measured from 0.35 V to –0.35 V.
7. Measured on common mode waveform – includes every rise/fall crossing.
8. Measured at the package ball for the Micro-FCBGA package.
9. Measured at the socket pin for the Micro-FCPGA package.

Table 26. System Bus Clock AC Specifications (133 MHz, Single Ended) [1]

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	System Bus Frequency		133		MHz	
T1S	BCLK Period	7.5	7.65	ns	6	Note 2
T1Sabs	BCLK Period – Instantaneous Minimum	7.25				Note 2
T2S	BCLK Period Stability		±250	ps		Notes 2, 3, 4
T3S	BCLK High Time	1.4		ns	6	at>2.0 V
T4S	BCLK Low Time	1.4		ns	6	at<0.5 V
T5S	BCLK Rise Time	0.4	1.6	ns	6	Note 5
T6S	BCLK Fall Time	0.4	1.6	ns	6	Note 5

NOTES:

1. All AC timings for AGTL and CMOS signals are referenced to the BCLK rising edge at 1.25 V.
2. Period, jitter, skew and offset measured at 1.25 V.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5 V and 2.0 V.

Table 27. System Bus Clock AC Specifications (100 MHz, Single Ended)[1]

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
	System Bus Frequency		100		MHz		
T1S1	BCLK Period		10		ns	6	Note 2
T1S1abs	BCLK Period – Instantaneous Minimum	9.75			ns		Note 2
T2S1	BCLK Period Stability			±250	ps		Notes 2, 3, 4
T3S1	BCLK High Time	2.70			ns	6	at>2.0 V
T4S1	BCLK Low Time	2.45			ns	6	at<0.5 V
T5S1	BCLK Rise Time	0.4		1.6	ns	6	Note 5
T6S1	BCLK Fall Time	0.4		1.6	ns	6	Note 5

NOTES:

1. All AC timings for AGTL and CMOS signals are referenced to the BCLK rising edge at 1.25 V.
2. Period, jitter, skew and offset measured at 1.25 V.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5 V and 2.0 V.

Table 28. Valid Mobile Intel Celeron Processor Frequencies

BCLK Frequency (MHz)	Frequency Multiplier	Core Frequency (MHz)	Power-on Configuration bits [27,25:22]
100	6.5	650	0, 1111
133	5.5	733	0, 0100
133	7.5	1000	0, 1101
133	8	1066	0, 1010
133	8.5	1133	1, 0110
133	9	1200	1, 0000
133	10	1333	1, 1011

NOTE: While other combinations of bus and core frequencies are defined, operation at frequencies other than those listed above will not be validated by Intel and are not guaranteed. The frequency multiplier is programmed into the processor when it is manufactured, and it cannot be changed.

Table 29. AGTL Signal Groups AC Specifications[1]

R_{TT} = 56Ω internally terminated to V_{CCT}; V_{REF} = $^2/_3 V_{CCT}$; load = 50 ohms

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T7	AGTL Output Valid Delay	0.40	3.25	ns	9	
T8	AGTL Input Setup Time	0.95 1.30		ns	10	Notes 2, 3, 6 Note 7
T9	AGTL Input Hold Time	1		ns	10	Note 4
T10	RESET# Pulse Width	1		ms	11,12	Note 5

NOTES:

1. All AC timings for AGTL signals are referenced to the crossing point of the BCLK rising edge and the BCLK# falling edge for Differential Clocking and to the BCLK rising edge at 1.25 V for Single Ended Clocking. All AGTL signals are referenced at V_{REF}. Unless other specified, all timings apply to both 100-MHz and 133-MHz bus frequencies.
2. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
3. Specification is for a minimum 0.40-V swing from Vref-200 mV to Vref+200 mV.
4. Specification is for a maximum 0.8-V swing from Vcct-0.8 V to Vcct.
5. After V_{CC}, V_{CCT}, and BCLK, BCLK# become stable and PWRGOOD is asserted.
6. Applies to all processors supporting 133-MHz bus clock frequency except Ultra Low Voltage processors.
7. Applies to all processors supporting 100-MHz bus clock frequency and Ultra Low Voltage processors supporting 133-MHz bus clock frequency.

Table 30. CMOS and Open-drain Signal Groups AC Specifications[1, 2]

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T14	1.5V Input Pulse Width, except PWRGOOD and LINT[1:0]	2		BCLKs	9	Active and inactive states
T14B	LINT[1:0] Input Pulse Width	6		BCLKs	9	Note 3
T15	PWRGOOD Inactive Pulse Width	2		µs	12	Note 4,5

NOTES:

1. All AC timings for CMOS and Open-drain signals are referenced to the crossing point of the BCLK rising edge and BCLK# falling edge for Differential Clocking and to the rising edge of BCLK at 1.25 V for Single Ended Clocking. All CMOS and Open-drain signals are referenced at 1.0 V.
2. Minimum output pulse width on CMOS outputs is 2 BCLKs.
3. This specification only applies when the APIC is enabled and the LINT1 or LINT0 signal is configured as an edge triggered interrupt with fixed delivery, otherwise specification T14 applies.
4. When driven inactive, or after V_{CC}, V_{CCT} and BCLK, BCLK# become stable. PWRGOOD must remain below $V_{IL18,MAX}$ until all the voltage planes meet the voltage tolerance specifications in Table 12 through Table 21 and BCLK, BCLK# have met the BCLK, BCLK# AC specifications in Table 35 and Table 36 for at least 2 µs. PWRGOOD must rise error-free and monotonically to 1.8 V.
5. If the BCLK Settling Time specification (T60) can be guaranteed at power-on reset then the PWRGOOD Inactive Pulse Width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL25,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 31. Reset Configuration AC Specifications and Power On/Power Down Timings

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
T16	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time	4			BCLKs	11	Before deassertion of RESET#
T17	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time	2		20	BCLKs	11	After clock that deasserts RESET#
T18	RESET#/PWRGOOD Setup Time	1			ms	12	Before deassertion of RESET# [1]
T18A	VCCT to VTTPWRGD Setup Time	1			ms	12	
T18B	VCC to PWRGOOD Setup Time		10		ms	12	
T18C	BSEL, VID valid time before VTTPWRGD assertion	1			µs	12	
T18D	RESET# inactive to Valid Outputs	1			BCLK	11	
T18E	RESET# inactive to Drive Signals	4			BCLKs	11	
T19A	Time from VCC(nominal)-12% to PWRGOOD low			0	ns	13	VCC(nominal) is the VID voltage setting
T19B	All outputs valid after PWRGOOD low	0			ns	13	
T19C	All inputs required valid after PWRGOOD low	0			ns	13	
T20A	Time from VCCT-12% to VTTPWRGD low			0	ns	14	
T20B	All outputs valid after VTTPWRGD low	0			ns	14	
T20C	All inputs required valid after VTTPWRGD low	0			ns	14	
T20D	VID, BSEL signals valid after VTTPWRGD low	0			ns	14	
T20E	VTTPWRGD Transition Time			100	µs		Measurement from 300 mV to 900 mV. Amount of noise (glitch) less than 100 mV. See Section 4.3.1 for details

NOTE: At least 1 ms must pass after PWRGOOD rises above $V_{IH18min}$ and BCLK, BCLK# meet their AC timing specification until RESET# may be deasserted.

Table 32. APIC Bus Signal AC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T21	PICCLK Frequency	2	33.3	MHz		Note 2
T22	PICCLK Period	30	500	ns	6	
T23	PICCLK High Time	10.5		ns	6	at>1.6 V
T24	PICCLK Low Time	10.5		ns	6	at<0.4 V
T25	PICCLK Rise Time	0.25	3.0	ns	6	(0.4 V – 1.6 V)
T26	PICCLK Fall Time	0.25	3.0	ns	6	(1.6 V – 0.4 V)
T27	PICD[1:0] Setup Time	8.0		ns	9	Note 3
T28	PICD[1:0] Hold Time	2.5		ns	9	Note 3
T29	PICD[1:0] Valid Delay (Rising Edge) PICD[1:0] Valid Delay (Falling Edge)	1.5 1.5	8.7 12.0	ns	8	Notes 3, 4

NOTES:
1. All AC timings for APIC signals are referenced to the PICCLK rising edge at 1.0 V. All CMOS signals are referenced at 1.0 V.
2. The minimum frequency is 2 MHz when PICD0 is at 1.5 V at reset Referenced to PICCLK Rising Edge.
3. For Open-drain signals, Valid Delay is synonymous with Float Delay.
4. Valid delay timings for these signals are specified into 150 Ω to 1.5 V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.

Table 33. TAP Signal AC Specifications[1]

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T30	TCK Frequency	—	16.67	MHz		
T31	TCK Period	60	—	ns	6	
T32	TCK High Time	25.0		ns	6	≥ $V_{CMOSREF}$+0.2V, Note 2
T33	TCK Low Time	25.0		ns	6	≤ $V_{CMOSREF}$-0.2V, Note 2
T34	TCK Rise Time		5.0	ns	6	($V_{CMOSREF}$-0.2V) – ($V_{CMOSREF}$+0.2V), Notes 2, 3
T35	TCK Fall Time		5.0	ns	6	($V_{CMOSREF}$+0.2V) – ($V_{CMOSREF}$-0.2V) , Notes 2, 3
T36	TRST# Pulse Width	40.0		ns	16	Asynchronous, Note 2
T37	TDI, TMS Setup Time	5.0		ns	15	Note 4
T38	TDI, TMS Hold Time	14.0		ns	15	Note 4
T39	TDO Valid Delay	1.0	10.0	ns	15	Notes 5, 6
T40	TDO Float Delay		25.0	ns	15	Notes 2, 5, 6
T41	All Non-Test Outputs Valid Delay	2.0	25.0	ns	15	Notes 5, 7, 8
T42	All Non-Test Outputs Float Delay		25.0	ns	15	Notes 2, 5, 7, 8
T43	All Non-Test Inputs Setup Time	5.0		ns	15	Notes 4, 7, 8
T44	All Non-Test Inputs Hold Time	13.0		ns	15	Notes 4, 7, 8

NOTES:

1. All AC timings for TAP signals are referenced to the TCK rising edge at 1.0 V. All TAP and CMOS signals are referenced at 1.0 V.
2. Not 100% tested. Specified by design/characterization.
3. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. Valid delay timing for this signal is specified into 150 Ω terminated to 1.5 V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.
7. Non-Test Outputs and Inputs are the normal output or input signals (except TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
8. During Debug Port operation use the normal specified timings rather than the TAP signal timings.

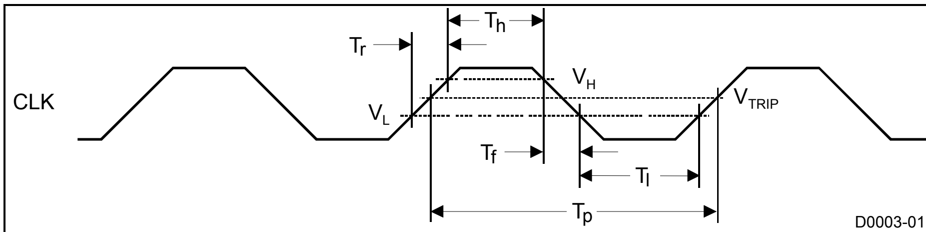
Table 34. Quick Start/Deep Sleep AC Specifications[1]

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T45	Quick Start Cycle Completion to Clock Stop or DPSLP# assertion	100		BCLKs	17, 18	
T46	Quick Start Cycle Completion to Input Signals Stable		0	μs	17, 18	
T47	Deep Sleep PLL Lock Latency	0	30	μs	17, 18	Note 2
T48	STPCLK# Hold Time from PLL Lock	0		ns	17, 18	
T49	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	17, 18	

NOTES:

1. Input signals other than RESET# and BPRI# must be held constant in the Quick Start state.
2. The BCLK, BCLK# Settling Time specification (T60) applies to Deep Sleep state exit under all conditions.

Figure 9. BCLK (Single Ended)/PICCLK/TCK Generic Clock Timing Waveform



NOTES:

T_r=T5S, T5S1, T34, T25 (Rise Time)
T_f=T6S, T6S1, T35, T26 (Fall Time)
T_h=T3S, T3S1, T32, T23 (High Time)
T_l=T4S, T4S1, T33, T24 (Low Time)
T_p=T1S, T1S1, T31, T22 (Period)
V_{TRIP}=1.25V for BCLK (Single Ended);1.0V for PICCLK; 1.0V for TCK
V_L=0.5V for BCLK (Single Ended);0.4V for PICCLK; ($V_{CMOSREF}$-0.2V) for TCK
V_H=2.0V for BCLK (Single Ended);1.6V for PICCLK; ($V_{CMOSREF}$+0.2V) for TCK

Figure 10. Differential BCLK/BCLK# Waveform (Common Mode)

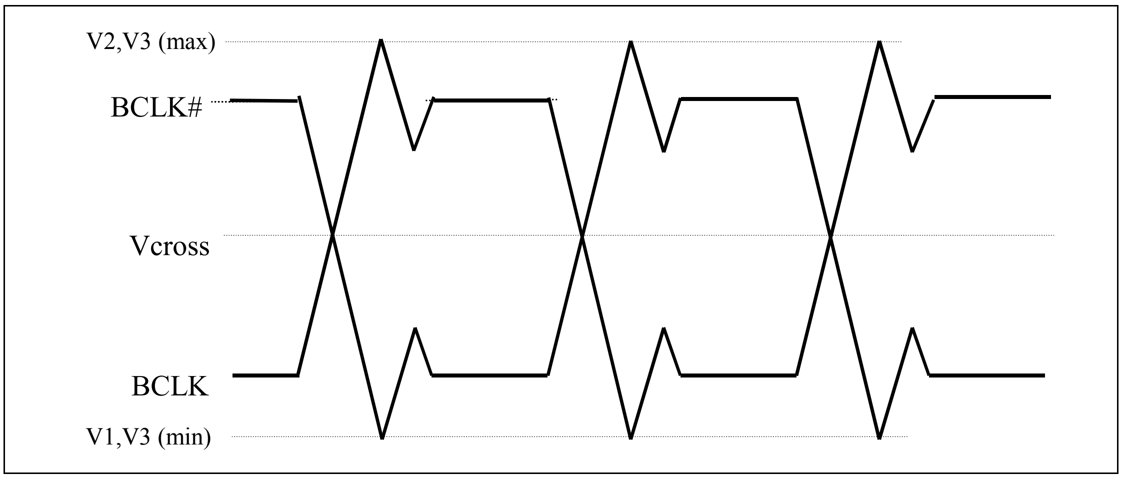


Figure 11. BCLK/BCLK# Waveform (Differential Mode)

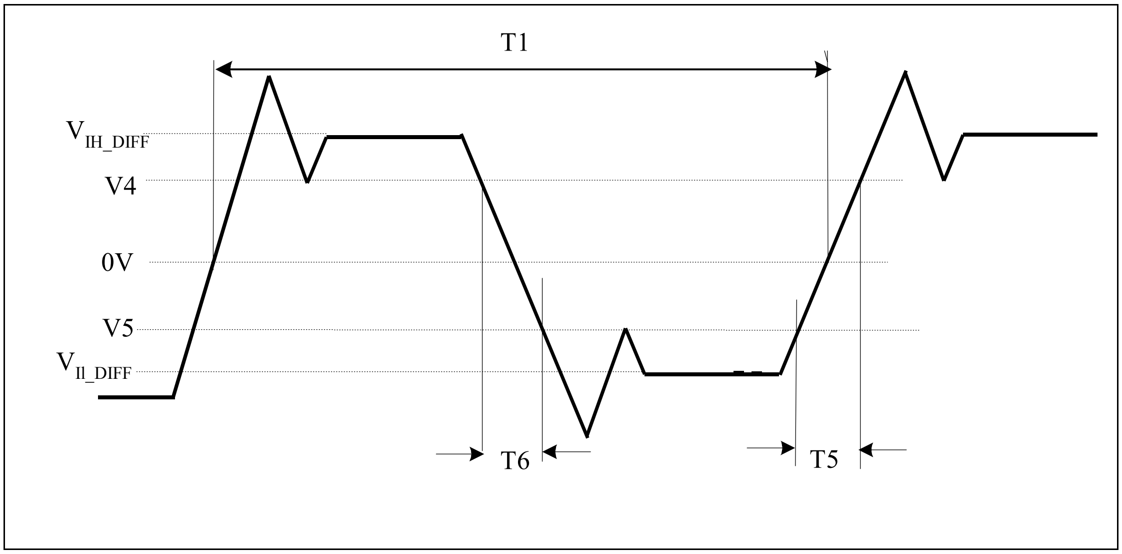
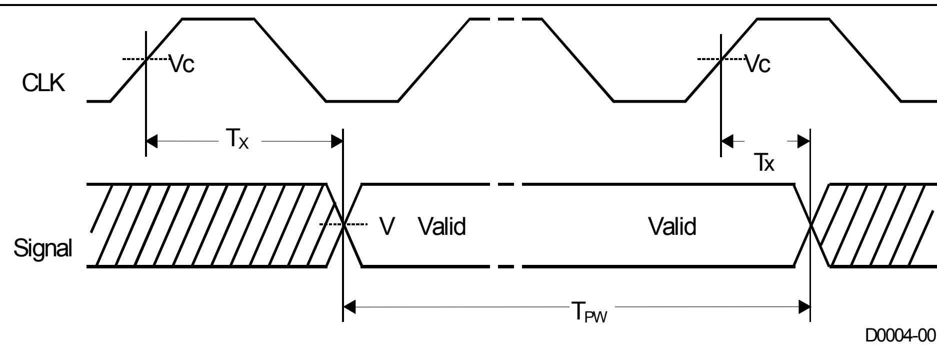


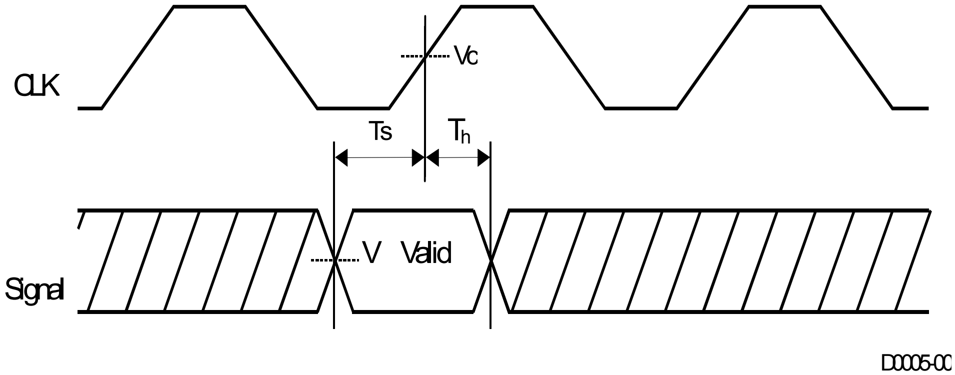
Figure 12. Valid Delay Timings



NOTES:

T_x = T7, T11, T29 (Valid Delay)
T_{pw} = T14, T14B (Pulse Width)
V = V_{REF} for AGTL signal group; 1.0V for CMOS, Open-drain, APIC, and TAP signal groups
Vc = Crossing point of BCLK rising edge and BCLK# falling edge for BCLK references (Differential Clock)
= **1**.25V (Single Ended Clock)

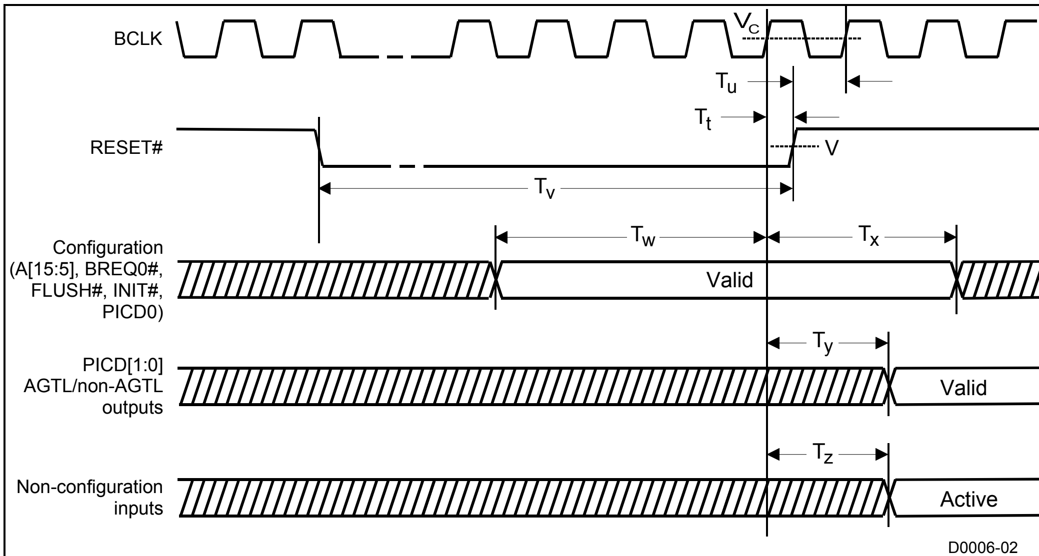
Figure 13. Setup and Hold Timings



NOTES:

T_s = T8, T27 (Setup Time)
T_h = T9, T28 (Hold Time)
V = V_{REF} for AGTL signals; 1.0V for CMOS, APIC, and TAP signals
Vc = Crossing point of BCLK rising edge and BCLK# falling edge for BCLK references (Differential Clock)
= 1.25V (Single Ended Clock)

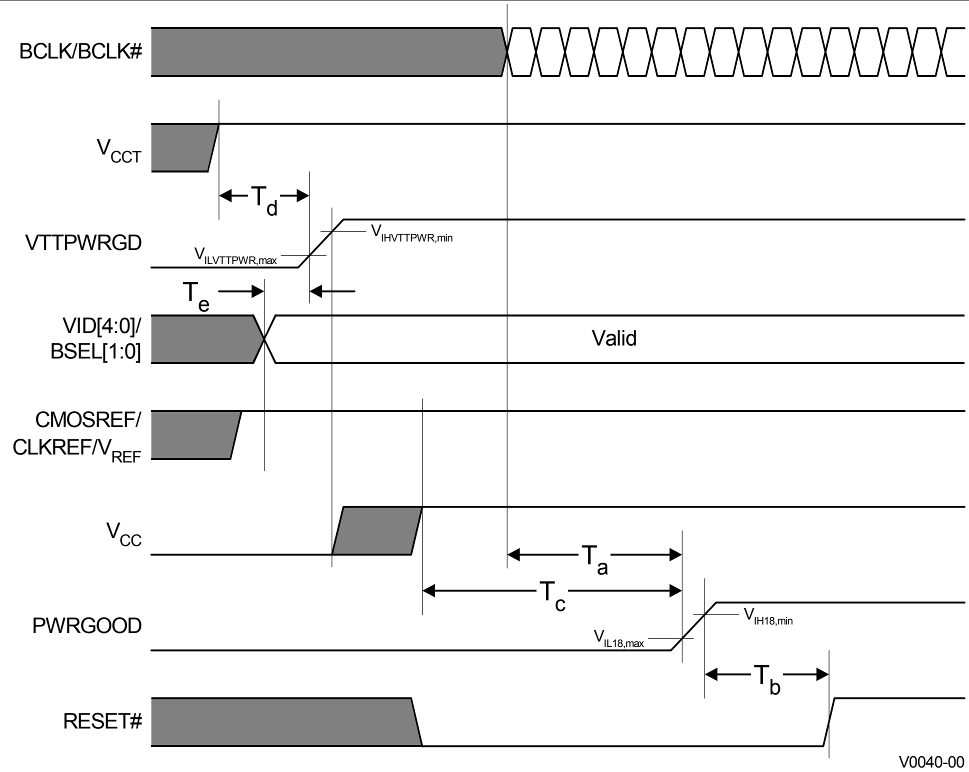
Figure 14. Cold/Warm Reset and Configuration Timings



NOTES:

T_t = T9 (AGTL Input Hold Time)
T_u = T8 (AGTL Input Setup Time)
T_v = T10 (RESET# Pulse Width)
T_w= T16 (Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time)
T_x = T17 (Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time)
Ty = T18D (RESET# inactive to Valid Outputs)
Tz = T18E (RESET# inactive to Drive Signals)
Vc= Crossing point of BCLK rising edge and BCLK# falling edge (Differential Clock)
= 1.25 V (Single Ended Clock)

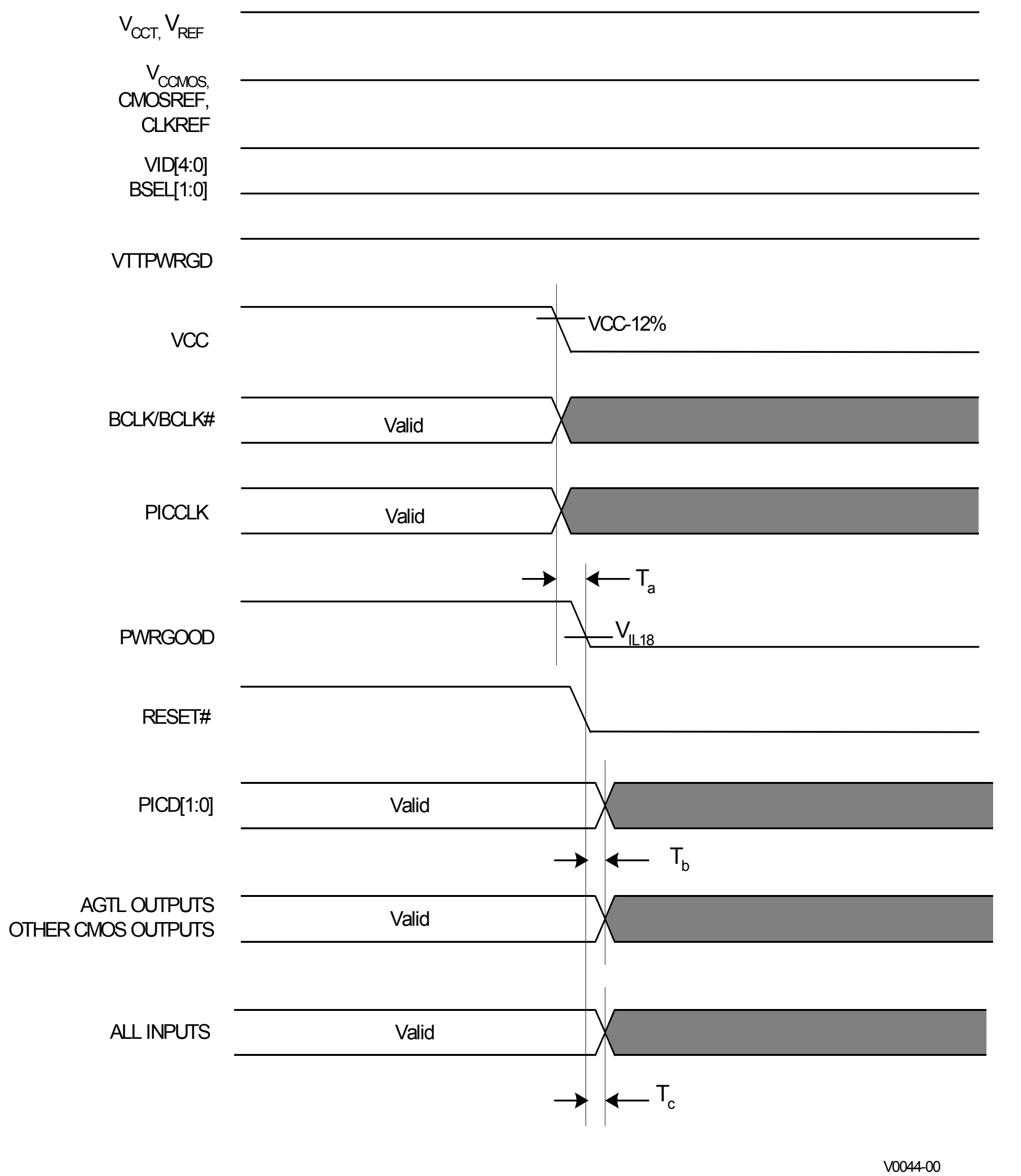
Figure 15. Power-on Sequence and Reset Timings



NOTES:

T_a = T15 (PWRGOOD Inactive Pulse Width)
T_b = T18 (RESET#/PWRGOOD Setup Time)
T_c = T18B (Setup time from V_{CC} valid until PWRGOOD assertion)
T_d = T18A (Setup time from V_{CCT} valid to VTTPWRGD assertion)
T_e = T18C(VID, BSEL valid time before VTTPWRGD assertion)

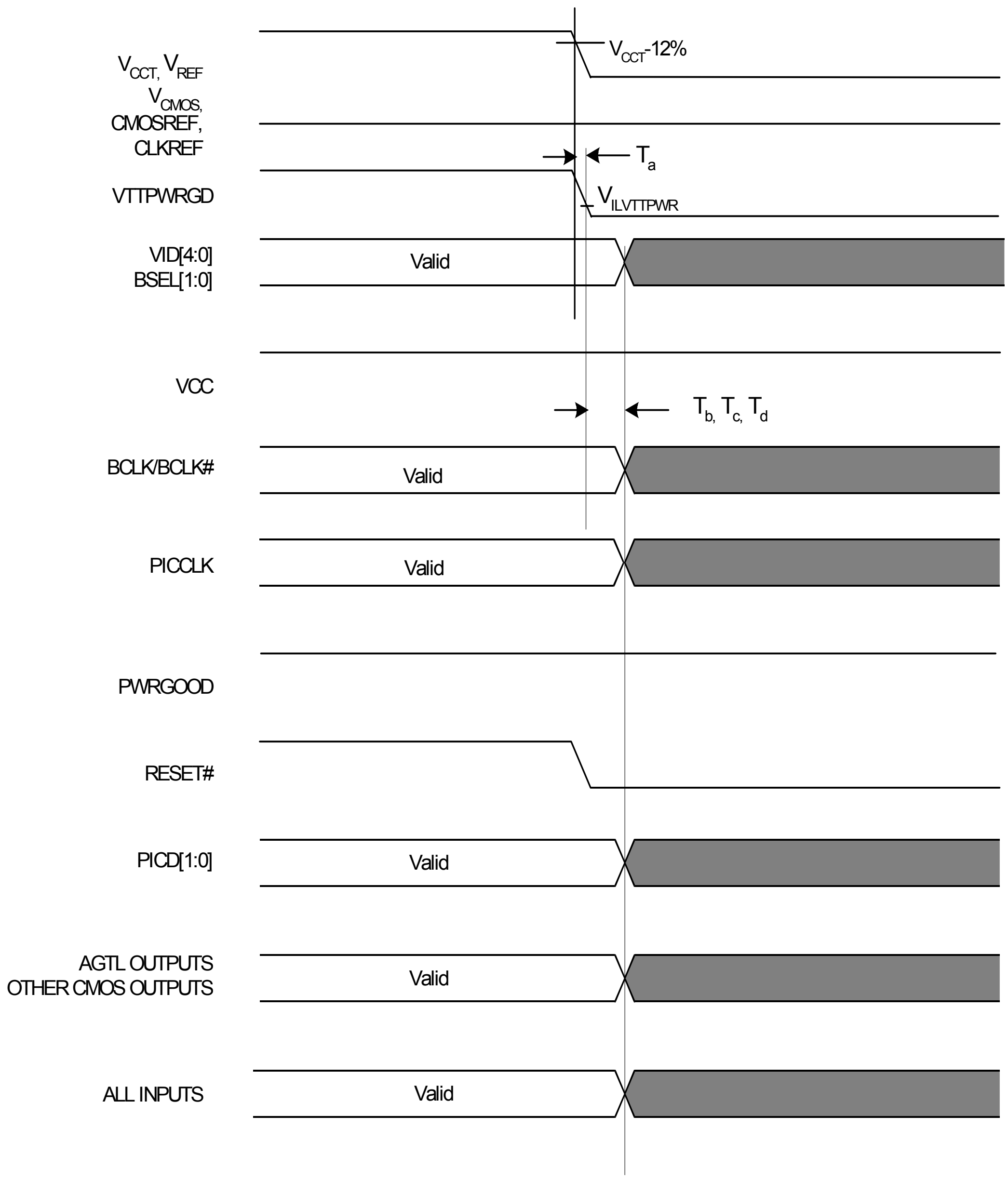
Figure 16. Power Down Sequencing and Timings (VCC Leading)



NOTES:

T_a = T19A (Time from VCC(nominal)-12% to PWRGOOD low)
T_b = T19B (All outputs valid after PWRGOOD low)
T_c = T19C (All inputs required valid after PWRGOOD low)

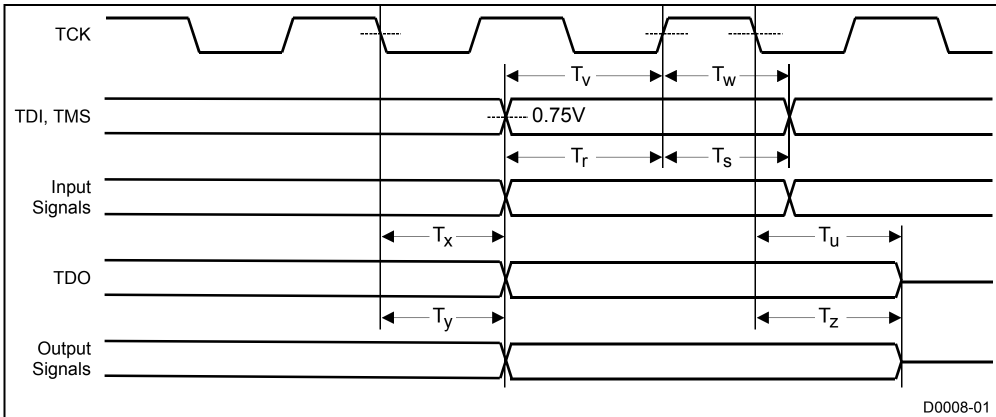
Figure 17. Power Down Sequencing and Timings (V_{CCT} Leading)



NOTES:

T_a = T20A (Time from VCCT-12% to VTTPWRGD low)
T_b = T20B (All outputs valid after VTTPWRGD low)
T_c = T20C (All inputs required valid after VTTPWRGD low)
T_d = T20D (VID, BSEL signals valid after VTTPWRGD low)

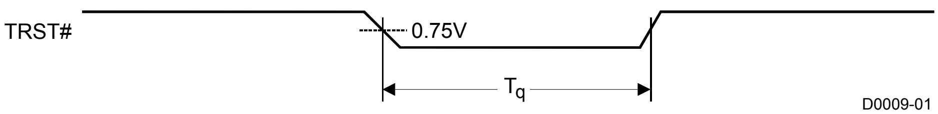
Figure 18.Test Timings (Boundary Scan)



NOTES:

T_r=T43 (All Non-Test Inputs Setup Time)
T_s=T44 (All Non-Test Inputs Hold Time)
T_u=T40 (TDO Float Delay)
T_v=T37 (TDI, TMS Setup Time)
T_w=T38 (TDI, TMS Hold Time)
T_x=T39 (TDO Valid Delay)
T_y=T41 (All Non-Test Outputs Valid Delay)
T_z=T42 (All Non-Test Outputs Float Delay)

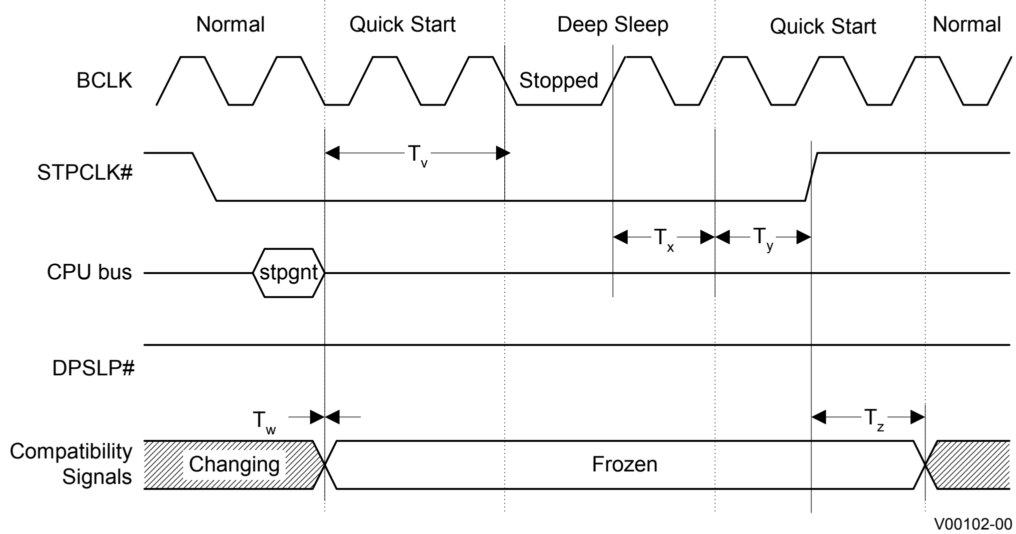
Figure 19. Test Reset Timings



NOTE:

T_q=T36 (TRST# Pulse Width)

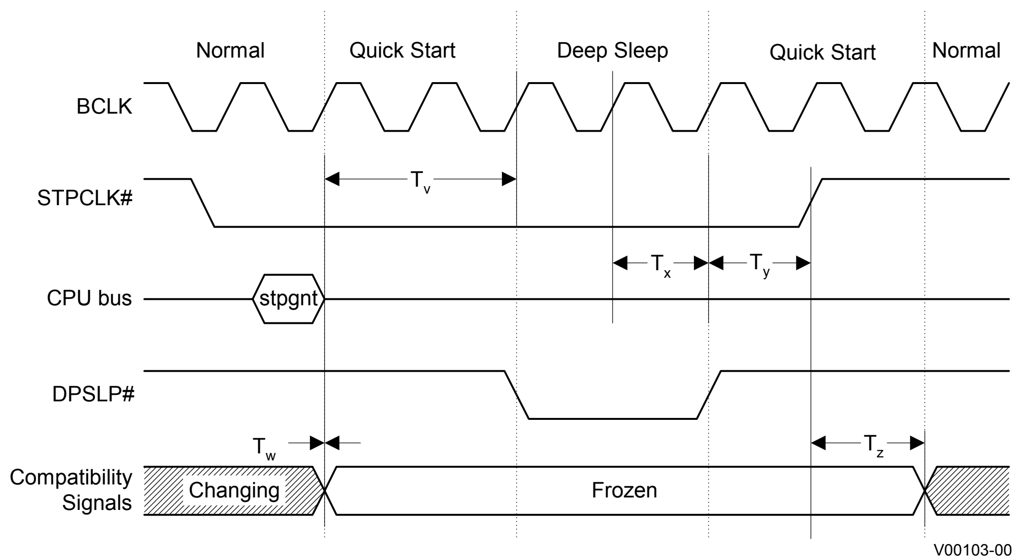
Figure 20. Quick Start/Deep Sleep Timing (BCLK Stopping Method)



NOTES:

T_V=T45 (Stop Grant Acknowledge Bus Cycle Completion to Clock Shut Off Delay)
T_W=T46 (Setup Time to Input Signal Hold Requirement)
T_X=T47 (Deep Sleep PLL Lock Latency)
T_Y=T48 (PLL lock to STPCLK# Hold Time)
T_Z=T49 (Input Signal Hold Time)

Figure 21. Quick Start/Deep Sleep Timing (DPSLP# Assertion Method)



NOTES:

T_V=T45 (Stop Grant Acknowledge Bus Cycle Completion to DPSLP# assertion)
T_W=T46 (Setup Time to Input Signal Hold Requirement)
T_X=T47 (Deep Sleep PLL Lock Latency)
T_Y=T48 (PLL lock to STPCLK# Hold Time)
T_Z=T49 (Input Signal Hold Time)

4. System Signal Simulations

Systems must be simulated using IBIS models to determine if they are compliant with this specification. All references to BCLK signal quality also apply to BCLK# for Differential Clocking.

4.1 System Bus Clock (BCLK) and PICCLK DC Specifications and AC Signal Quality Specifications

Table 35. BCLK (Differential) DC Specifications and AC Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$	-0.2	0.35	V	7	Note 1
V2	$V_{IH,BCLK}$	0.92	1.45	V	7	Note 1
V3	V_{IN} Absolute Voltage Range	-0.2	1.45	V	7	Undershoot/Overshoot, Note 2
V4	BCLK Rising Edge Ringback	0.35		V	8	Note 3
V5	BCLK Falling Edge Ringback		-0.35	V	8	Note 3
V_{BCLK_DPSLP}	BCLK Voltage in Deep Sleep State	0.4	1.45	V		Note 4
$V_{BCLK\#\_DPSLP}$	BCLK# Voltage in Deep Sleep State	0	V_{BCLK_DPSLP} - 0.2 V	V		Note 4

NOTES:

1. The clock must rise/fall monotonically between VIL,BCLK and VIH,BCLK .
2. These specifications apply only when BCLK, BCLK# are running.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) voltage the differential waveform can go to after passing the VIH_DIFF (rising) or VIL_DIFF (falling) levels. VIL_DIFF (max) = -0.57 V, VIH_DIFF (min) = 0.57 V.
4. Applies when BCLK and BCLK# are stopped in Deep Sleep State.

Table 36. BCLK (Single Ended) DC Specifications and AC Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$		0.3	V	20	Note 1
V2	$V_{IH,BCLK}$	2.2		V	20	Note 1
V3	V_{IN} Absolute Voltage Range	-0.5	3.1	V	20	Undershoot/Overshoot, Note 2
V4	BCLK Rising Edge Ringback	2.0		V	20	Absolute Value, Note 3
V5	BCLK Falling Edge Ringback		0.5	V	20	Absolute Value, Note 3

NOTES:

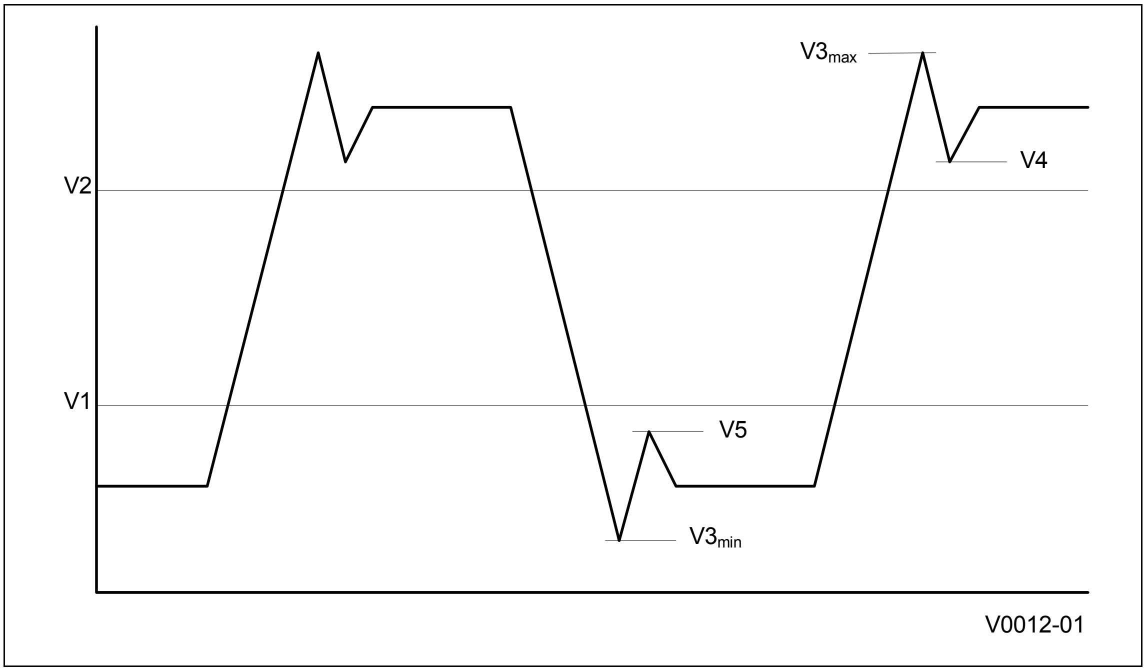
1. The clock must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$. BCLK must be stopped in the low state.
2. These specifications apply only when BCLK is running. BCLK may not be above $V_{IH,BCLK,max}$ or below $V_{IL,BCLK,min}$ for more than 50% of the clock cycle.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can go to after passing the $V_{IH,BCLK}$ (rising) or $V_{IL,BCLK}$ (falling) voltage limits.

Table 37. PICCLK DC Specifications and AC Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	V_{IL20}		0.4	V	20	Note 1
V2	V_{IH20}	1.6		V	20	Note 1
V3	V_{IN} Absolute Voltage Range	-0.5	2.4	V	20	Undershoot, Overshoot, Note 2
V4	PICCLK Rising Edge Ringback	1.6		V	20	Absolute Value, Note 3
V5	PICCLK Falling Edge Ringback		0.4	V	20	Absolute Value, Note 3

NOTES:
1. The clock must rise/fall monotonically between V_{IL20} and V_{IH20}.
2. These specifications apply only when PICCLK is running. See the DC specifications for when PICCLK is stopped. PICCLK may not be above $V_{IH20,max}$ or below $V_{IL20,min}$ for more than 50% of the clock cycle.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the PICCLK signal can go to after passing the V_{IH20} (rising) or V_{IL20} (falling) voltage limits.

Figure 22. BCLK (Single Ended)/PICCLK Generic Clock Waveform



4.2 AGTL AC Signal Quality Specifications

Ringback specifications for the AGTL signals are as follows: Ringback below $V_{REF,max}$ + 200 mV is not authorized during low to high transitions. Ringback above $V_{REF,min}$ – 200 mV is not authorized during high to low transitions.

Overshoot and undershoot specifications are documented in Table 38 and Table 39 and illustrated in Figure 23.

Figure 23. Maximum Acceptable Overshoot/Undershoot Waveform

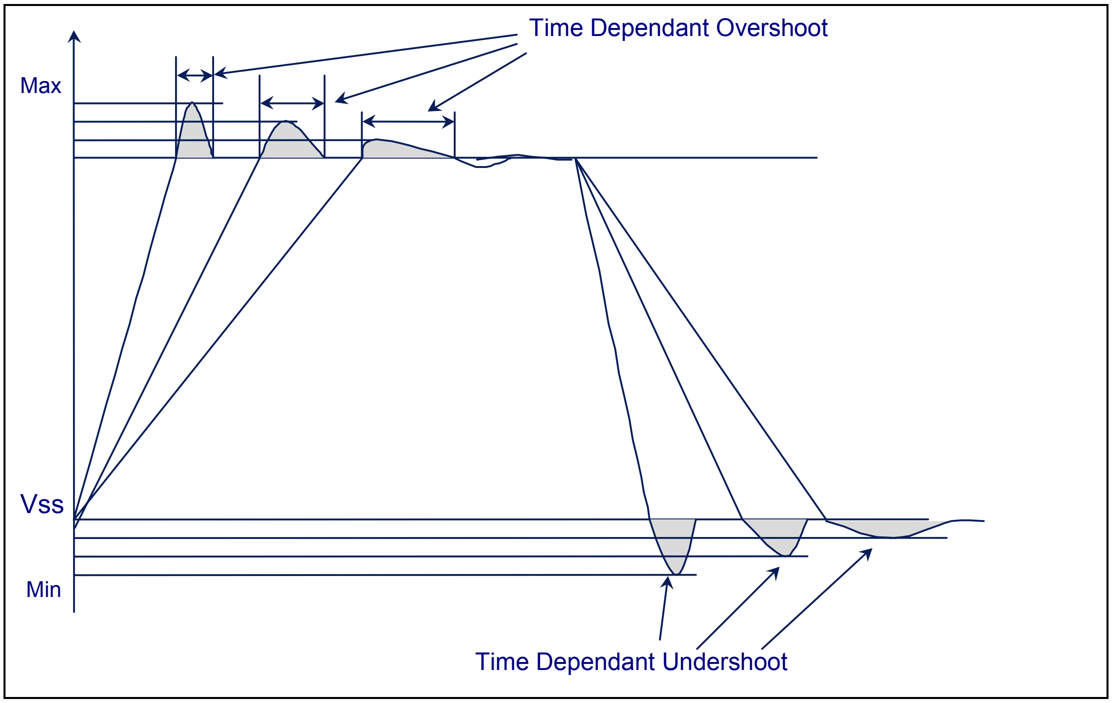


Table 38. 133-MHz AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Max V_{CCT} + Overshoot/Undershoot Magnitude (volts)	Allowed Pulse Duration (ns) [Tj=100C (see Note 7)]		
	Activity Factor = 0.01	Activity Factor = 0.1	Activity Factor = 1
1.78	1.5	0.15	0.015
1.73	3.5	0.35	0.035
1.68	7.2	0.72	0.072
1.63	15	1.5	0.15
1.58	15	3.2	0.32
1.53	15	6.5	0.65
1.48	15	14	1.40

NOTES:

1. Under no circumstances should the sum of the Max V_{CCT} and absolute value of the Overshoot/Undershoot voltage exceed 1.78 V.
2. Activity factor of 1 represents the same toggle rate as the 133-MHz clock.
3. Ringbacks below V_{CCT} cannot be subtracted from overshoots. Lesser undershoot does not allocate longer or larger overshoot.
4. Ringbacks above ground cannot be subtracted from undershoots. Lesser overshoot does not allocate longer or larger undershoot.
5. System designers are encouraged to follow Intel provided AGTL layout guidelines.
6. All values are specified by design characterization and are not tested.
7. Tj = 85°C for 1.33 GHz.

Table 39. 100-MHz AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Max V_{CCT} + Overshoot/Undershoot Magnitude (volts)	Allowed Pulse Duration (ns) [Tj=100C (see Note 7)]		
	Activity Factor = 0.01	Activity Factor = 0.1	Activity Factor = 1
1.78	1.6	0.16	0.016
1.73	4.5	0.45	0.045
1.68	9.5	0.95	0.095
1.63	20	2.0	0.2
1.58	20	4.2	0.42
1.53	20	8.5	0.85
1.48	20	19	1.9

NOTES:

1. Under no circumstances should the sum of the Max V_{CCT} and absolute value of the Overshoot/Undershoot voltage exceed 1.78 V.
2. Activity factor of 1 represents the same toggle rate as the 100-MHz clock.
3. Ringbacks below V_{CCT} cannot be subtracted from overshoots. Lesser undershoot does not allocate longer or larger overshoot.
4. Ringbacks above ground cannot be subtracted from undershoots. Lesser overshoot does not allocate longer or larger undershoot.
5. System designers are encouraged to follow Intel provided AGTL layout guidelines.
6. All values are specified by design characterization and are not tested.
7. Tj = 85°C for 1.33 GHz.

4.3 Non-AGTL Signal Quality Specifications

Signals driven to the Mobile Intel Celeron Processor should meet signal quality specifications to ensure that the processor reads data properly and that incoming signals do not affect the long-term reliability of the processor. The overshoot and undershoot specifications for non-AGTL signals are shown in Table 40. Ringback must not exceed the CMOS V_{IH} and V_{IL} specification levels in Table 24.

Table 40. Non-AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Max V_{Cmos} + Overshoot/Undershoot Magnitude (volts)	Allowed Pulse Duration (ns) [Tj=100C (see note 6)]		
	Activity Factor = 0.01	Activity Factor = 0.1	Activity Factor = 1
2.38	6.5	0.65	0.065
2.33	13	1.3	0.13
2.28	29	2.9	0.29
2.23	60	6	0.6
2.18	60	12	1.2
2.13	60	26	2.6
2.08	60	56	5.6

NOTES:
1. V_{CMOS}(nominal) = 1.5 V.
2. Under no circumstances should the sum of the Max V_{CMOS} and absolute value of the Overshoot/Undershoot voltage exceed 2.38 V.
3. Activity factor of 1 represents a toggle rate of 33 MHz.
4. System designers are encouraged to follow Intel provided non-AGTL layout guidelines.
5. All values are specified by design characterization, and are not tested.
6. Tj = 85°C for 1.33 GHz.

4.3.1 PWRGOOD, VTTPWRGD Signal Quality Specifications

The processor requires PWRGOOD to be a clean indication that clocks and the power supplies (V_{CC}, V_{CCT}, etc.) are stable and within their specifications. Clean implies that the signal will remain below V_{IL18} and without errors from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (1.8 V) state. The VTTPWRGD signal must also transition monotonically.

The VTTPWRGD signal is an input to the processor used to determine that the VTT power is stable and the VID and BSEL signals should be driven to their final state by the processor. To ensure the processor correctly reads this signal, the processor must meet the requirement shown in Table 41 while the signal is in its transition region of 300 mV to 900 mV. Also, VTTPWRGD should only enter the transition region once, after VTT is at nominal values, for the assertion of the signal.

4.3.1.1 VTTPWRGD Noise Parameter Specification

Table 41. VTTPWRGD Noise Parameter Specification

Parameter	Specification
Amount of noise (glitch)	Less than 100 mV

In addition, the VTTPWRGD signal should have reasonable transition time through the transition region. A sharp edge on the signal transition will minimize the chance of noise causing a glitch on this signal. Intel recommends the following transition time for the VTTPWRGD signal.

4.3.1.2 VTTPWRGD Transition Parameter Recommendation

Table 42. VTTPWRGD Transition Parameter Recommendation

Parameter	Recommendation
Transition time (300 mV to 900 mV)	Less than or equal to 100 µs

In addition, the VTT_PWRGD signal should have reasonable transition time through the transition region. A sharp edge on the signal transition will minimize the chance of noise causing a glitch on this signal. Intel recommends the following transition time for the VTT_PWRGD signal.

4.3.1.2.1 Transition Region

The transition region covered by this requirement is 300 mV to 900 mV. Once the VTTPWRGD signal is in that voltage range, the processor is more sensitive to noise, which may be present on the signal. The transition region when the signal first crosses the 300-mV voltage level and continues until the last time it is below 900 mV.

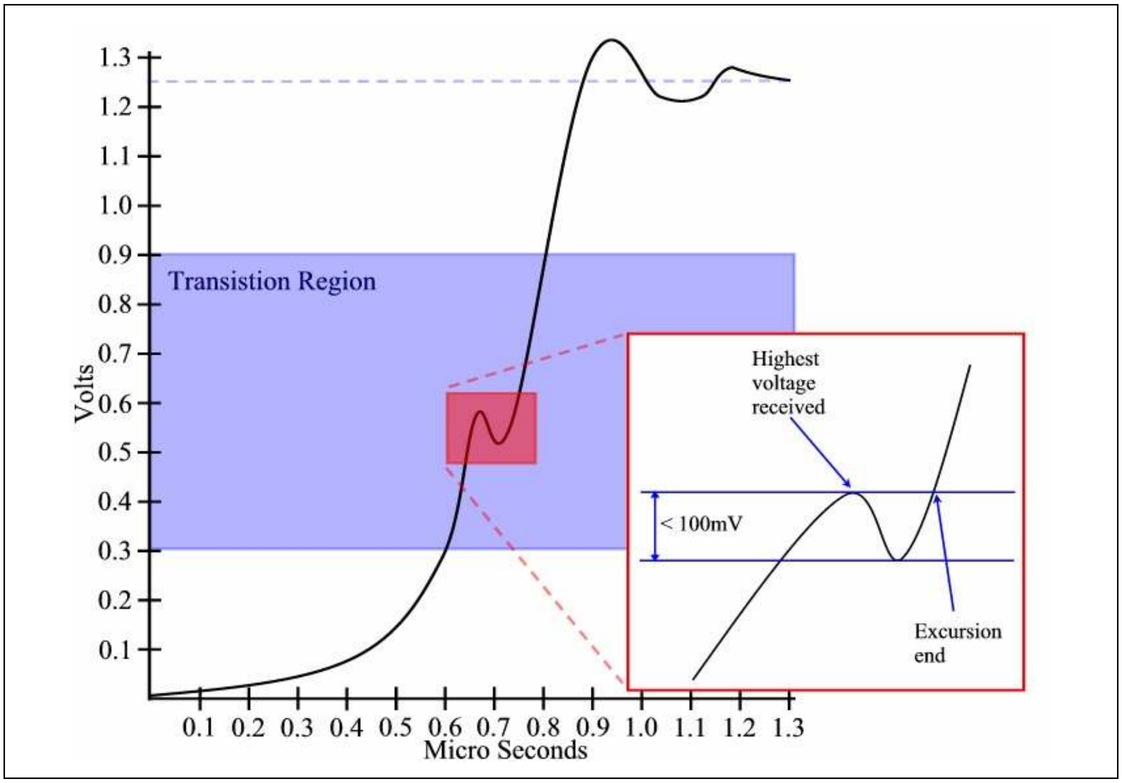
4.3.1.2.2 Transition Time

The transition time is defined as the time the signal takes to move through the transition region. A 100-µs transition time will ensure that the processor receives a good transition edge.

4.3.1.2.3 Noise

The signal quality of the VTTPWRGD signal is critical to the correct operation of the processor. Every effort should be made to ensure this signal is monotonic in the transition region. If noise or glitches are present on this signal, the noise or glitches must be kept to less than 100 mV of a voltage drop from the highest voltage level received to that point. This glitch must remain less than 100 mV until the excursion ends by the voltage returning to the highest voltage previously received. Please see Figure 24 for an example graph of this situation and requirements.

Figure 24. VTTPWRGD Noise Specification



5. Mechanical Specifications

5.1 Socketable Micro-FCPGA Package

The Mobile Intel Celeron Processor is packaged in a 478-pin Micro-FCPGA package. The Low Voltage and Ultra Low Voltage processors will not be available in this package. The mechanical specifications for the socketable package are provided in Table 43. Figure 25 through Figure 27 illustrate different views of the package.

Table 43. Socketable Micro-FCPGA Package Specification

Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to package seating plane	1.81	2.03	mm
-	Overall height, top of die to PCB surface, including socket(1)	4.69	5.15	mm
A1	Pin length	1.95	2.11	mm
A2	Die height	0.854		mm
B	Pin diameter	0.28	0.36	mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18[3] 10.82[4]		mm
E1	Die width	7.20[3] 6.85[4]		mm
e	Pin pitch	1.27		mm
K	Package edge keep-out	5		mm
K1	Package corner keep-out	7		mm
K3	Pin-side capacitor boundary	14		mm
-	Pin tip radial true position	<=0.254		mm
N	Pin count	478		each
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	4.5		g
⏥	Package surface Flatness	0.286		mm

NOTES:

1. All dimensions are subject to change.
2. Overall height with socket is based on design dimensions of the Micro-FCPGA package and socket with no thermal solution attached. Values were based on design specifications and tolerances. This dimension is subject to change based on socket design, OEM motherboard design, or OEM SMT process.
3. Dimension for CPUID = 0x06B1.
4. Dimension for CPUID = 0x06B4.

Figure 25. Socketable Micro-FCPGA Package - Top and Bottom Isometric Views

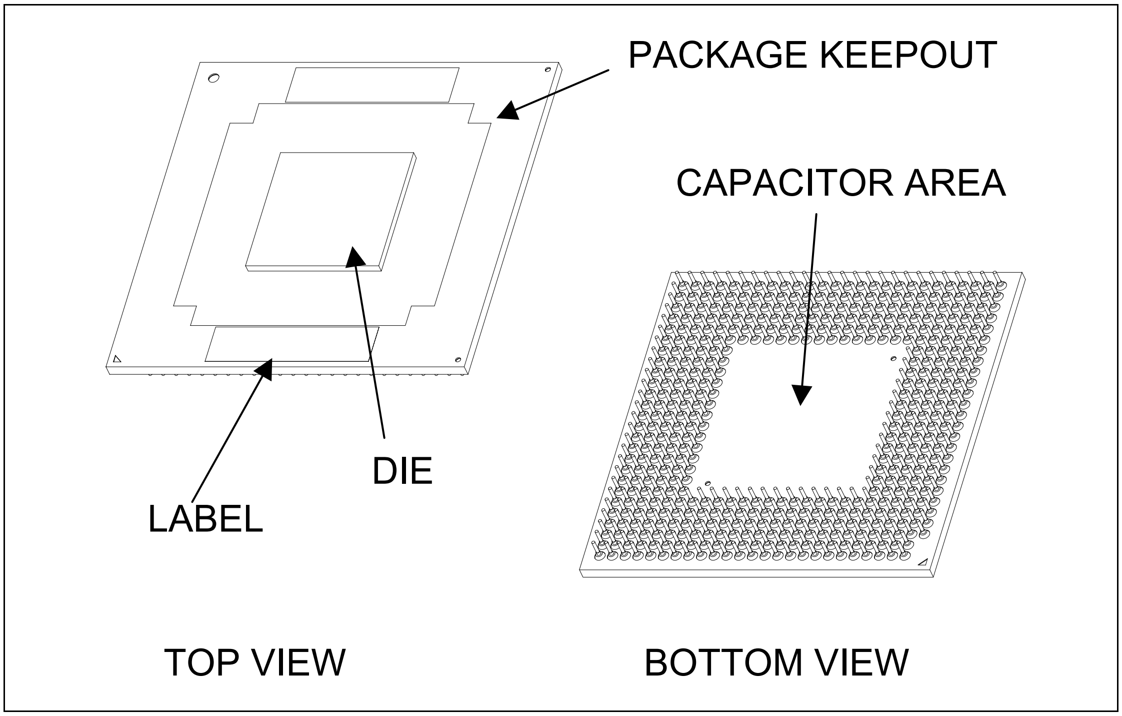
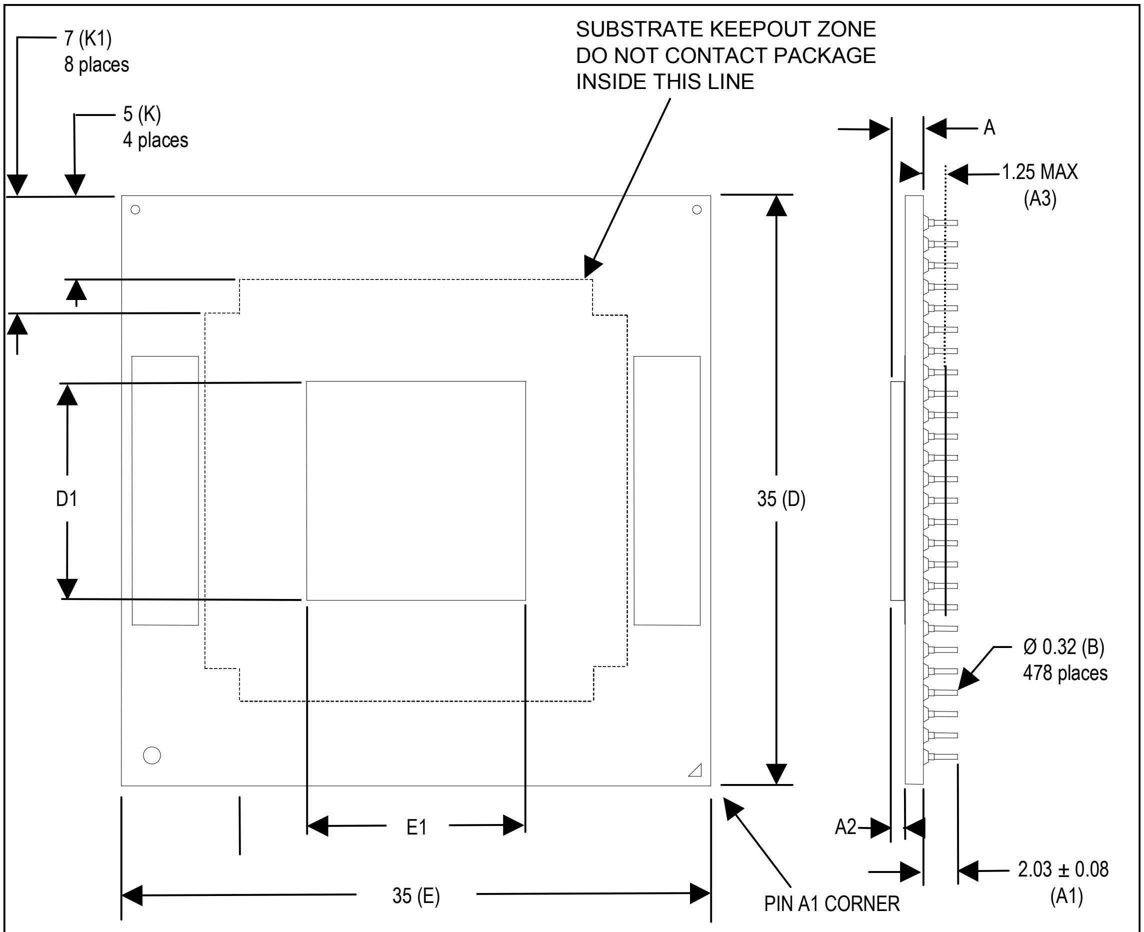
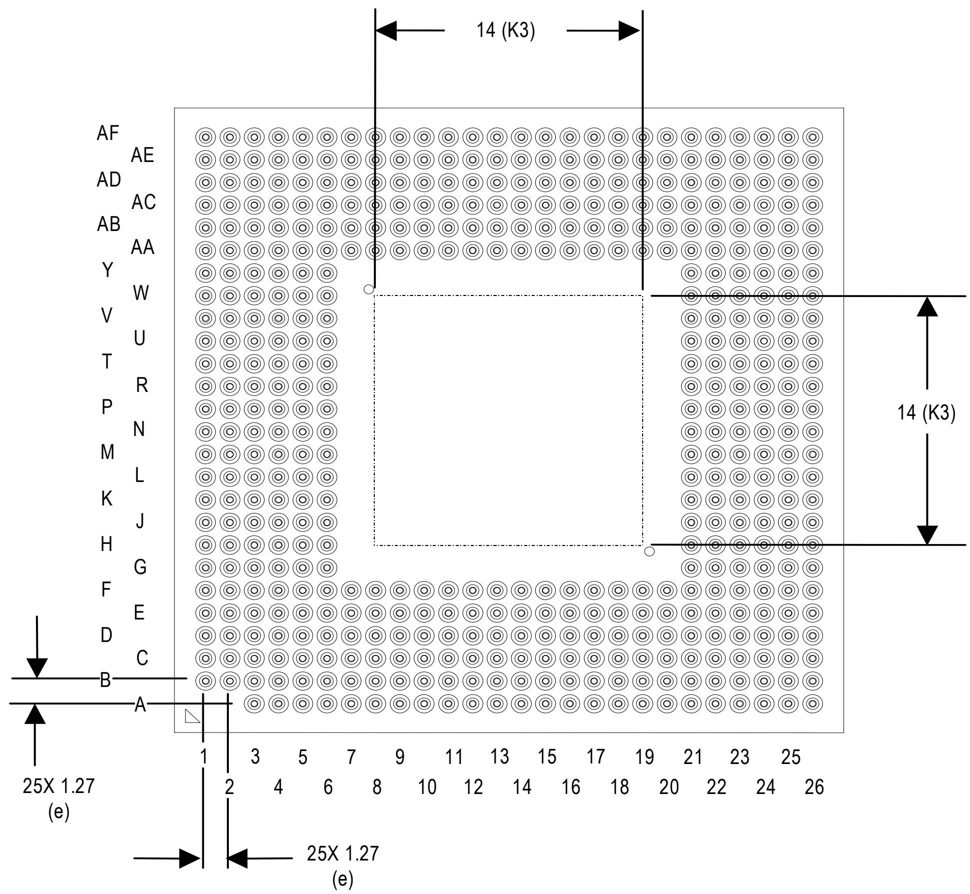


Figure 26. Socketable Micro-FCPGA Package - Top and Side View



NOTE: All dimensions in millimeters. Values shown are for reference only. See Table 36 for specific details

Figure 27. Socketable Micro-FCPGA Package - Bottom View



NOTE: All dimensions in millimeters. Values shown are for reference only. See Table 36 for specific details.

5.2 Surface Mount Micro-FCBGA Package

The Mobile Intel Celeron Processor will also be available in a surface mount, 479-ball Micro-FCBGA package. The Low Voltage and Ultra Low Voltage processors will be available only in this package. The Mobile Intel Celeron processors at 1.45V and 1.5V will not be available in this package. Mechanical specifications are shown in Table 44. Figure 28 through Figure 30 illustrate different views of the package.

The Micro-FCBGA package may have capacitors placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors, and possibly damage the device or render it inactive. The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting.

Table 44. Micro-FCBGA Package Mechanical Specifications

Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (1)	2.27	2.77	mm
A2	Die height	0.854		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18[3] 10.82[4]		mm
E1	Die width	7.20[3] 6.85[4]		mm
e	Ball pitch	1.27		mm
N	Ball count	479		each
K	Keep-out outline from edge of package	5		mm
K1	Keep-out outline at corner of package	7		mm
K2	Capacitor keep-out height	-	0.7	mm
S	Package edge to first ball center	1.625		mm
--	Solder ball coplanarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	4.5		g

NOTES:
1. All dimensions are subject to change.
2. Overall height as delivered. Values were based on design specifications and tolerances. Final height after surface mount depends on OEM motherboard design and SMT process.
3. Dimension for CPUID = 0x06B1.
4. Dimension for CPUID = 0x06B4.

Figure 28. Micro-FCBGA Package – Top and Bottom Isometric Views

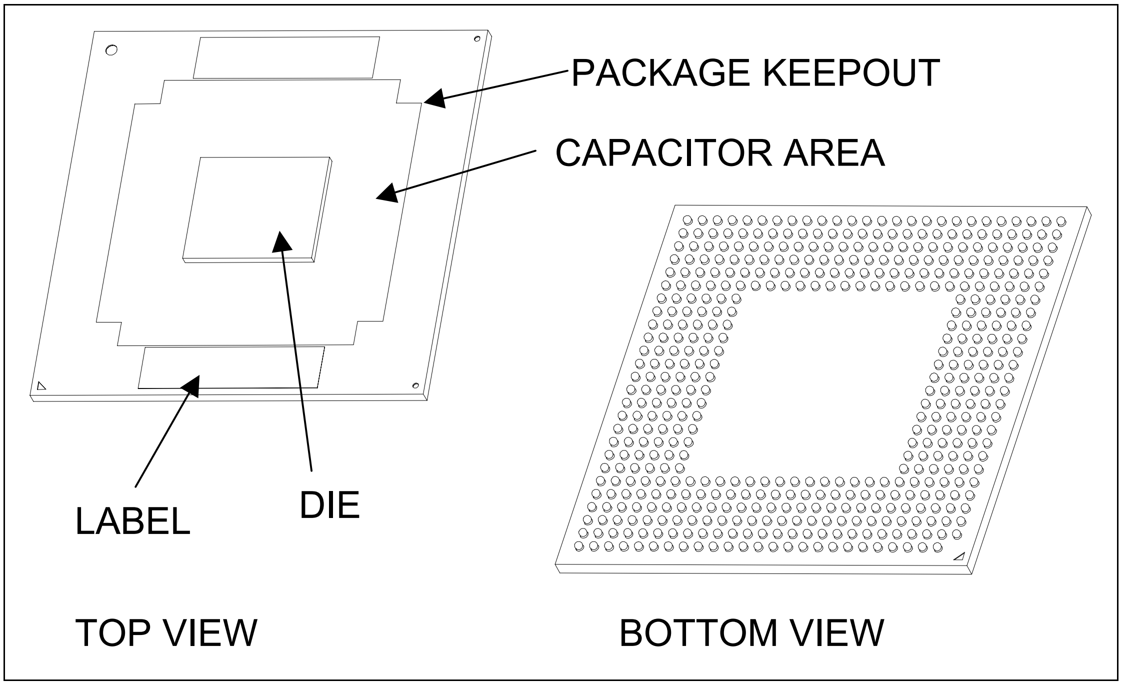
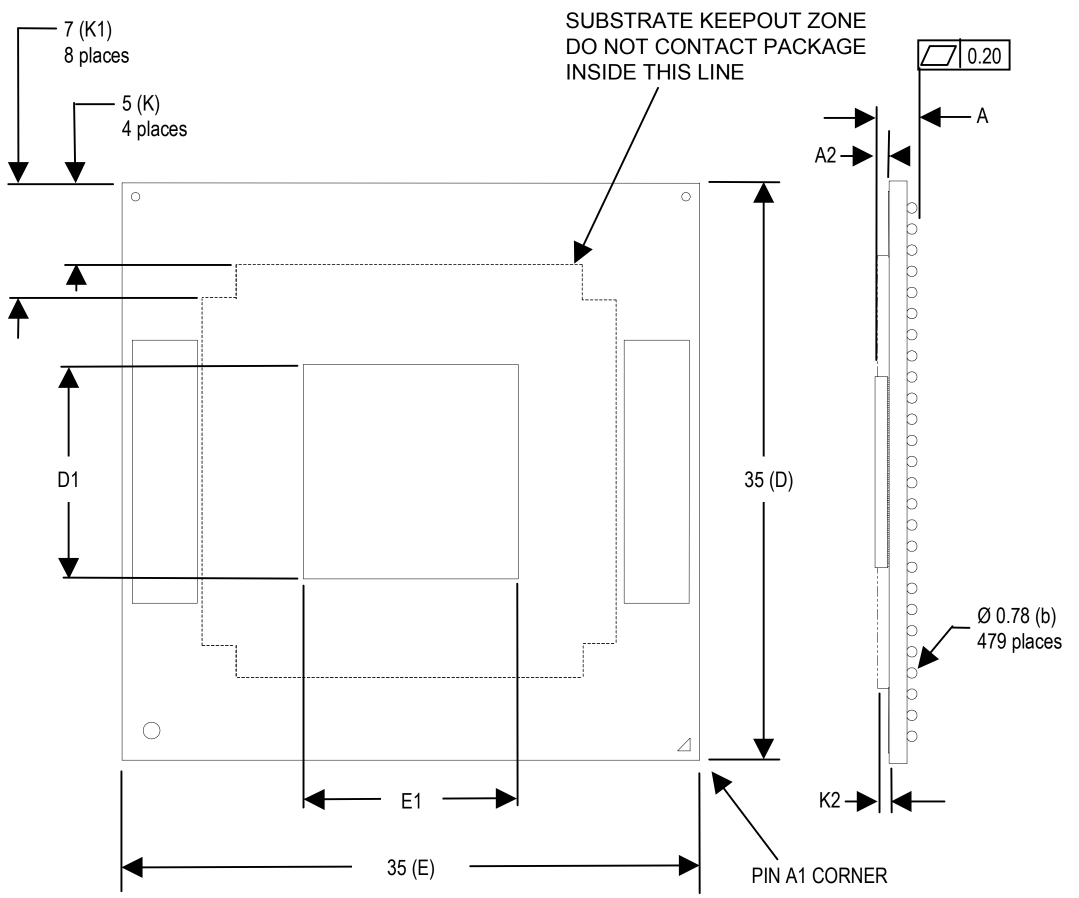
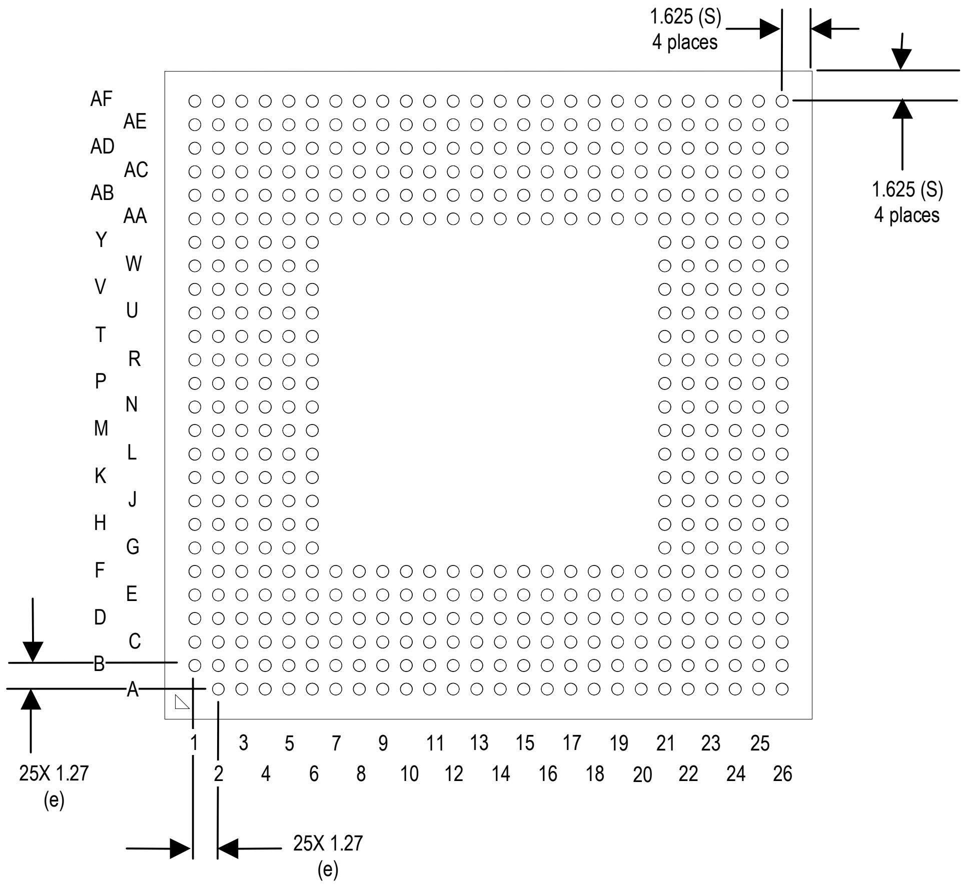


Figure 29. Micro-FCBGA Package – Top and Side Views



NOTE: All dimensions in millimeters. Values shown are for reference only. See Table 37 for specific details.

Figure 30. Micro-FCBGA Package - Bottom View



NOTE: All dimensions in millimeters. Values shown are for reference only. See Table 37 for specific details.

5.3 Signal Listings

Figure 31 is a top-side view of the ball or pin map of the Mobile Intel Celeron Processor with the voltage balls/pins called out. Table 45 lists the signals in ball/pin number order. Table 46 lists the signals in signal name order.

Figure 31. Pin/Ball Map - Top View

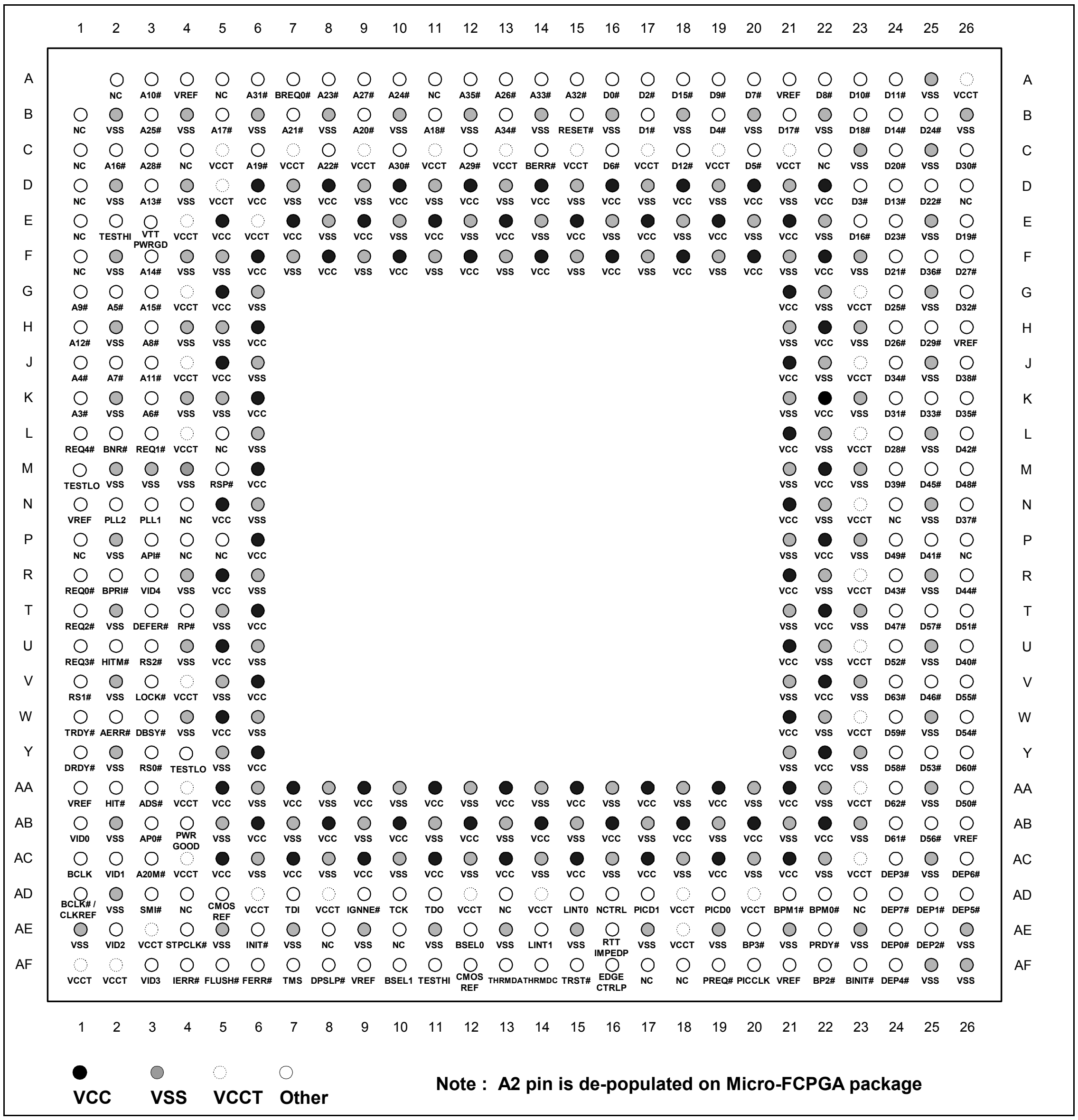


Table 45. Signal Listing in Order by Pin/Ball Number

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
A3	A10#	B18	VSS	D7	VSS	E22	VSS
A4	VREF	B19	D4#	D8	VCC	E23	D16#
A5	NC	B20	VSS	D9	VSS	E24	D23#
A6	A31#	B21	D17#	D10	VCC	E25	VSS
A7	BREQ0#	B22	VSS	D11	VSS	E26	D19#
A8	A23#	B23	D18#	D12	VCC	F1	NC
A9	A27#	B24	D14#	D13	VSS	F2	VSS
A10	A24#	B25	D24#	D14	VCC	F3	A14#
A11	NC	B26	VSS	D15	VSS	F4	VSS
A12	A35#	C1	NC	D16	VCC	F5	VSS
A13	A26#	C2	A16#	D17	VSS	F6	VCC
A14	A33#	C3	A28#	D18	VCC	F7	VSS
A15	A32#	C4	NC	D19	VSS	F8	VCC
A16	D0#	C5	VCCT	D20	VCC	F9	VSS
A17	D2#	C6	A19#	D21	VSS	F10	VCC
A18	D15#	C7	VCCT	D22	VCC	F11	VSS
A19	D9#	C8	A22#	D23	D3#	F12	VCC
A20	D7#	C9	VCCT	D24	D13#	F13	VSS
A21	VREF	C10	A30#	D25	D22#	F14	VCC
A22	D8#	C11	VCCT	D26	NC	F15	VSS
A23	D10#	C12	A29#	E1	NC	F16	VCC
A24	D11#	C13	VCCT	E2	TESTHI	F17	VSS
A25	VSS	C14	BERR#	E3	VTTPWRGD	F18	VCC
A26	VCCT	C15	VCCT	E4	VCCT	F19	VSS
B1	NC	C16	D6#	E5	VCC	F20	VCC
B2	VSS	C17	VCCT	E6	VCCT	F21	VSS
B3	A25#	C18	D12#	E7	VCC	F22	VCC
B4	VSS	C19	VCCT	E8	VSS	F23	VSS
B5	A17#	C20	D5#	E9	VCC	F24	D21#
B6	VSS	C21	VCCT	E10	VSS	F25	D36#
B7	A21#	C22	NC	E11	VCC	F26	D27#
B8	VSS	C23	VSS	E12	VSS	G1	A9#
B9	A20#	C24	D20#	E13	VCC	G2	A5#
B10	VSS	C25	VSS	E14	VSS	G3	A15#
B11	A18#	C26	D30#	E15	VCC	G4	VCCT
B12	VSS	D1	NC	E16	VSS	G5	VCC
B13	A34#	D2	VSS	E17	VCC	G6	VSS
B14	VSS	D3	A13#	E18	VSS	G21	VCC
B15	RESET#	D4	VSS	E19	VCC	G22	VSS
B16	VSS	D5	VCCT	E20	VSS	G23	VCCT
B17	D1#	D6	VCC	E21	VCC	G24	D25#

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
G25	VSS	L4	VCCT	P23	VSS	V2	VSS
G26	D32#	L5	NC	P24	D49#	V3	LOCK#
H1	A12#	L6	VSS	P25	D41#	V4	VCCT
H2	VSS	L21	VCC	P26	NC	V5	VSS
H3	A8#	L22	VSS	R1	REQ0#	V6	VCC
H4	VSS	L23	VCCT	R2	BPRI#	V21	VSS
H5	VSS	L24	D28#	R3	VID4	V22	VCC
H6	VCC	L25	VSS	R4	VSS	V23	VSS
H21	VSS	L26	D42#	R5	VCC	V24	D63#
H22	VCC	M1	TESTLO	R6	VSS	V25	D46#
H23	VSS	M2	VSS	R21	VCC	V26	D55#
H24	D26#	M3	VSS	R22	VSS	W1	TRDY#
H25	D29#	M4	VSS	R23	VCCT	W2	AERR#
H26	VREF	M5	RSP#	R24	D43#	W3	DBSY#
J1	A4#	M6	VCC	R25	VSS	W4	VSS
J2	A7#	M21	VSS	R26	D44#	W5	VCC
J3	A11#	M22	VCC	T1	REQ2#	W6	VSS
J4	VCCT	M23	VSS	T2	VSS	W21	VCC
J5	VCC	M24	D39#	T3	DEFER#	W22	VSS
J6	VSS	M25	D45#	T4	RP#	W23	VCCT
J21	VCC	M26	D48#	T5	VSS	W24	D59#
J22	VSS	N1	VREF	T6	VCC	W25	VSS
J23	VCCT	N2	PLL2	T21	VSS	W26	D54#
J24	D34#	N3	PLL1	T22	VCC	Y1	DRDY#
J25	VSS	N4	NC	T23	VSS	Y2	VSS
J26	D38#	N5	VCC	T24	D47#	Y3	RS0#
K1	A3#	N6	VSS	T25	D57#	Y4	TESTLO
K2	VSS	N21	VCC	T26	D51#	Y5	VSS
K3	A6#	N22	VSS	U1	REQ3#	Y6	VCC
K4	VSS	N23	VCCT	U2	HITM#	Y21	VSS
K5	VSS	N24	NC	U3	RS2#	Y22	VCC
K6	VCC	N25	VSS	U4	VSS	Y23	VSS
K21	VSS	N26	D37#	U5	VCC	Y24	D58#
K22	VCC	P1	NC	U6	VSS	Y25	D53#
K23	VSS	P2	VSS	U21	VCC	Y26	D60#
K24	D31#	P3	API#	U22	VSS	AA1	VREF
K25	D33#	P4	NC	U23	VCCT	AA2	HIT#
K26	D35#	P5	NC	U24	D52#	AA3	ADS#
L1	REQ4#	P6	VCC	U25	VSS	AA4	VCCT
L2	BNR#	P21	VSS	U26	D40#	AA5	VCC
L3	REQ1#	P22	VCC	V1	RS1#	AA6	VSS

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
AA7	VCC	AB22	VCC	AD11	TDO	AE26	VSS
AA8	VSS	AB23	VSS	AD12	VCCT	AF1	VCCT
AA9	VCC	AB24	D61#	AD13	NC	AF2	VCCT
AA10	VSS	AB25	D56#	AD14	VCCT	AF3	VID3
AA11	VCC	AB26	VREF	AD15	LINT0	AF4	IERR#
AA12	VSS	AC1	BCLK	AD16	NCTRL	AF5	FLUSH#
AA13	VCC	AC2	VID1	AD17	PICD1	AF6	FERR#
AA14	VSS	AC3	A20M#	AD18	VCCT	AF7	TMS
AA15	VCC	AC4	VCCT	AD19	PICD0	AF8	DPSLP#
AA16	VSS	AC5	VCC	AD20	VCCT	AF9	VREF
AA17	VCC	AC6	VSS	AD21	BPM1#	AF10	BSEL1
AA18	VSS	AC7	VCC	AD22	BPM0#	AF11	TESTHI
AA19	VCC	AC8	VSS	AD23	NC	AF12	CMOSREF
AA20	VSS	AC9	VCC	AD24	DEP7#	AF13	THRMDA
AA21	VCC	AC10	VSS	AD25	DEP1#	AF14	THRMDC
AA22	VSS	AC11	VCC	AD26	DEP5#	AF15	TRST#
AA23	VCCT	AC12	VSS	AE1	VSS	AF16	EDGECTRLP
AA24	D62#	AC13	VCC	AE2	VID2	AF17	NC
AA25	VSS	AC14	VSS	AE3	VCCT	AF18	NC
AA26	D50#	AC15	VCC	AE4	STPCLK#	AF19	PREQ#
AB1	VID0	AC16	VSS	AE5	VSS	AF20	PICCLK
AB2	VSS	AC17	VCC	AE6	INIT#	AF21	VREF
AB3	AP0#	AC18	VSS	AE7	VSS	AF22	BP2#
AB4	PWRGOOD	AC19	VCC	AE8	NC	AF23	BINIT#
AB5	VSS	AC20	VSS	AE9	VSS	AF24	DEP4#
AB6	VCC	AC21	VCC	AE10	NC	AF25	VSS
AB7	VSS	AC22	VSS	AE11	VSS	AF26	VSS
AB8	VCC	AC23	VCCT	AE12	BSEL0		
AB9	VSS	AC24	DEP3#	AE13	VSS		
AB10	VCC	AC25	VSS	AE14	LINT1		
AB11	VSS	AC26	DEP6#	AE15	VSS		
AB12	VCC	AD1	BCLK#/CLKREF	AE16	RTTIMPEDP		
AB13	VSS	AD2	VSS	AE17	VSS		
AB14	VCC	AD3	SMI#	AE18	VCCT		
AB15	VSS	AD4	NC	AE19	VSS		
AB16	VCC	AD5	CMOSREF	AE20	BP3#		
AB17	VSS	AD6	VCCT	AE21	VSS		
AB18	VCC	AD7	TDI	AE22	PRDY#		
AB19	VSS	AD8	VCCT	AE23	VSS		
AB20	VCC	AD9	IGNNE#	AE24	DEP0#		
AB21	VSS	AD10	TCK	AE25	DEP2#		

Table 46. Signal Listing in Order by Signal Name

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
K1	A3#	AGTL I/O	AF23	BINIT#	AGTL I/O
J1	A4#	AGTL I/O	L2	BNR#	AGTL I/O
G2	A5#	AGTL I/O	AF22	BP2#	AGTL I/O
K3	A6#	AGTL I/O	AE20	BP3#	AGTL I/O
J2	A7#	AGTL I/O	AD22	BPM0#	AGTL I/O
H3	A8#	AGTL I/O	AD21	BPM1#	AGTL I/O
G1	A9#	AGTL I/O	R2	BPRI#	AGTL Input
A3	A10#	AGTL I/O	A7	BREQ0#	AGTL I/O
J3	A11#	AGTL I/O	AE12	BSEL0	3.3 V CMOS Output
H1	A12#	AGTL I/O	AF10	BSEL1	3.3 V CMOS Output
D3	A13#	AGTL I/O	AD5	CMOSREF	CMOS Reference Voltage
F3	A14#	AGTL I/O	AF12	CMOSREF	CMOS Reference Voltage
G3	A15#	AGTL I/O	A16	D0#	AGTL I/O
C2	A16#	AGTL I/O	B17	D1#	AGTL I/O
B5	A17#	AGTL I/O	A17	D2#	AGTL I/O
B11	A18#	AGTL I/O	D23	D3#	AGTL I/O
C6	A19#	AGTL I/O	B19	D4#	AGTL I/O
B9	A20#	AGTL I/O	C20	D5#	AGTL I/O
B7	A21#	AGTL I/O	C16	D6#	AGTL I/O
C8	A22#	AGTL I/O	A20	D7#	AGTL I/O
A8	A23#	AGTL I/O	A22	D8#	AGTL I/O
A10	A24#	AGTL I/O	A19	D9#	AGTL I/O
B3	A25#	AGTL I/O	A23	D10#	AGTL I/O
A13	A26#	AGTL I/O	A24	D11#	AGTL I/O
A9	A27#	AGTL I/O	C18	D12#	AGTL I/O
C3	A28#	AGTL I/O	D24	D13#	AGTL I/O
C12	A29#	AGTL I/O	B24	D14#	AGTL I/O
C10	A30#	AGTL I/O	A18	D15#	AGTL I/O
A6	A31#	AGTL I/O	E23	D16#	AGTL I/O
A15	A32#	AGTL I/O	B21	D17#	AGTL I/O
A14	A33#	AGTL I/O	B23	D18#	AGTL I/O
B13	A34#	AGTL I/O	E26	D19#	AGTL I/O
A12	A35#	AGTL I/O	C24	D20#	AGTL I/O
AC3	A20M#	1.5V CMOS Input	F24	D21#	AGTL I/O
AA3	ADS#	AGTL I/O	D25	D22#	AGTL I/O
W2	AERR#	AGTL I/O	E24	D23#	AGTL I/O
AB3	AP0#	AGTL I/O	B25	D24#	AGTL I/O
P3	AP1#	AGTL I/O	G24	D25#	AGTL I/O
AC1	BCLK	Clock Input	H24	D26#	AGTL I/O
AD1	BCLK#/CLKREF	Clock Input	F26	D27#	AGTL I/O
C14	BERR#	AGTL I/O	L24	D28#	AGTL I/O

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
H25	D29#	AGTL I/O	AF24	DEP4#	AGTL I/O
C26	D30#	AGTL I/O	AD26	DEP5#	AGTL I/O
K24	D31#	AGTL I/O	AC26	DEP6#	AGTL I/O
G26	D32#	AGTL I/O	AD24	DEP7#	AGTL I/O
K25	D33#	AGTL I/O	Y1	DRDY#	AGTL I/O
J24	D34#	AGTL I/O	AF8	DPSLP#	1.5 V CMOS Input
K26	D35#	AGTL I/O	AF16	EDGECTRLP	AGTL Control
F25	D36#	AGTL I/O	AF6	FERR#	1.5 V Open Drain Output
N26	D37#	AGTL I/O	AF5	FLUSH#	1.5 V CMOS Input
J26	D38#	AGTL I/O	AA2	HIT#	AGTL I/O
M24	D39#	AGTL I/O	U2	HITM#	AGTL I/O
U26	D40#	AGTL I/O	AF4	IERR#	1.5 V Open Drain Output
P25	D41#	AGTL I/O	AD9	IGNNE#	1.5 V CMOS Input
L26	D42#	AGTL I/O	AE6	INIT#	1.5 V CMOS Input
R24	D43#	AGTL I/O	AD15	INTR/LINT0	1.5 V CMOS Input
R26	D44#	AGTL I/O	V3	LOCK#	AGTL I/O
M25	D45#	AGTL I/O	AE14	NMI/LINT1	1.5 V CMOS Input
V25	D46#	AGTL I/O	AD16	NCTRL	AGTL impedance control
T24	D47#	AGTL I/O	AF20	PICCLK	1.8 V APIC Clock Input
M26	D48#	AGTL I/O	AD19	PICD0	1.5 V Open Drain I/O
P24	D49#	AGTL I/O	AD17	PICD1	1.5 V Open Drain I/O
AA26	D50#	AGTL I/O	N3	PLL1	PLL Analog Voltage
T26	D51#	AGTL I/O	N2	PLL2	PLL Analog Voltage
U24	D52#	AGTL I/O	AE22	PRDY#	AGTL Output
Y25	D53#	AGTL I/O	AF19	PREQ#	1.5 V CMOS Input
W26	D54#	AGTL I/O	AB4	PWRGOOD	1.8 V CMOS Input
V26	D55#	AGTL I/O	R1	REQ0#	AGTL I/O
AB25	D56#	AGTL I/O	L3	REQ1#	AGTL I/O
T25	D57#	AGTL I/O	T1	REQ2#	AGTL I/O
Y24	D58#	AGTL I/O	U1	REQ3#	AGTL I/O
W24	D59#	AGTL I/O	L1	REQ4#	AGTL I/O
Y26	D60#	AGTL I/O	B15	RESET#	AGTL Input
AB24	D61#	AGTL I/O	T4	RP#	AGTL I/O
AA24	D62#	AGTL I/O	Y3	RS0#	AGTL I/O
V24	D63#	AGTL I/O	V1	RS1#	AGTL I/O
W3	DBSY#	AGTL I/O	U3	RS2#	AGTL I/O
T3	DEFER#	AGTL Input	M5	RSP#	AGTL Input
AE24	DEP0#	AGTL I/O	AE16	RTTIMPEDP	AGTL Pull-up Control
AD25	DEP1#	AGTL I/O	AD3	SMI#	1.5 V CMOS Input
AE25	DEP2#	AGTL I/O	AE4	STPCLK#	1.5 V CMOS Input
AC24	DEP3#	AGTL I/O			

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
AD10	TCK	1.5V JTAG Clock Input	AC2	VID1	Voltage Identification
AD7	TDI	JTAG Input	AE2	VID2	Voltage Identification
AD11	TDO	JTAG Output	AF3	VID3	Voltage Identification
E2	TESTHI	Test Use Only	R3	VID4	Voltage Identification
AF11	TESTHI	Test Use Only	A4	VREF	AGTL Reference Voltage
M1	TESTLO	Test Use Only	A21	VREF	AGTL Reference Voltage
Y4	TESTLO	Test Use Only	N1	VREF	AGTL Reference Voltage
AF13	THERMDA	Thermal Diode Anode	AF9	VREF	AGTL Reference Voltage
AF14	THERMDC	Thermal Diode Cathode	AF21	VREF	AGTL Reference Voltage
AF7	TMS	JTAG Input	AA1	VREF	AGTL Reference Voltage
W1	TRDY#	AGTL I/O	AB26	VREF	AGTL Reference Voltage
AF15	TRST#	JTAG Input	H26	VREF	AGTL Reference Voltage
AB1	VID0	Voltage Identification	E3	VTTPWRGD	VCCT power good signal

Table 47. Voltage and No-Connect Pin/Ball Locations

Signal Name	Pin/Ball Numbers
NC	**A2**, A5, A11, B1, C1, C4, C22, D1, D26, E1, F1, L5, N4, N24, P1, P4, P5, P26, AD4, AD13, AD23, AE8, AE10, AF17, AF18
VCC	D6, D8, D10, D12, D14, D16, D18, D20, D22, E5, E7, E9, E11, E13, E15, E17, E19, E21, F6, F8, F10, F12, F14, F16, F18, F20, F22, G5, G21, H6, H22, J5, J21, K6, K22, L21, M6, M22, N5, N21, P6, P22, R5, R21, T6, T22, U5, U21, V6, V22, W5, W21, Y6, Y22, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AC5, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21
VCCT	A26, C5, C7, C9, C11, C13, C15, C17, C19, C21, D5, E4, E6, G4, G23, J4, J23, L4, L23, N23, R23, U23, V4, W23, AA4, AA23, AC4, AC23, AD6, AD8, AD12, AD14, AD18, AD20, AE3, AE18, AF1, AF2
VSS	A25, B2, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, B26, C23, C25, D2, D4, D7, D9, D11, D13, D15, D17, D19, D21, E8, E10, E12, E14, E16, E18, E20, E22, E25, F2, F4, F5, F7, F9, F11, F13, F15, F17, F19, F21, F23, G6, G22, G25, H2, H4, H5, H21, H23, J6, J22, J25, K2, K4, K5, K21, K23, L6, L22, L25, M2, M3, M4, M21, M23, N6, N22, N25, P2, P21, P23, R4, R6, R22, R25, T2, T5, T21, T23, U4, U6, U22, U25, V2, V5, V21, V23, W4, W6, W22, W25, Y2, Y5, Y21, Y23, AA6, AA8, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AA25, AB2, AB5, AB7, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AB23, AC6, AC8, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC25, AD2, AE1, AE5, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE26, AF25, AF26

NOTE: A2 pin is de-populated on the Micro-FCPGA package.

6. V_{CC} Thermal Specifications

In order to achieve proper cooling of the processor, a thermal solution (e.g., heat spreader, heat pipe, or other heat transfer system) must make firm contact to the exposed processor die. The processor die must be clean before the thermal solution is attached or the processor may be damaged.

Table 48 provides the Thermal Design Power (TDP) dissipation and the minimum and maximum T_J temperatures for the Mobile Intel Celeron Processor. The thermal solution should be designed to ensure the junction temperature never exceeds the specified value while operating at the Thermal Design Power. Additionally, a secondary failsafe mechanism in hardware should be provided to shutdown the processor at 101°C to prevent permanent damage, as described in Section 3.1.3. TDP is a thermal design power specification based on the worst case power dissipation of the processor while executing publicly available software under normal operating conditions at nominal voltages. Contact your Intel Field Sales Representative for further information.

Table 48. Power Specifications for Mobile Intel Celeron Processor

Symbol	Core Frequency/Voltage	Thermal Design Power		Unit	Notes
TDP	650 MHz & 1.10 V 700 MHz & 1.10 V 733 MHz & 1.10 V 800 MHz & 1.10V 650 MHz & 1.15 V 733 MHz & 1.15 V 866 MHz & 1.15 V 1.000 GHz & 1.40 V 1.266 GHz & 1.40 V 1.066 GHz & 1.45 V 1.133 GHz & 1.45 V 1.200 GHz & 1.45 V 1.333 GHz & 1.50 V	7.0 7.0 7.0 7.0 10.6 11.2 9.61 22.0 22.0 23.2 23.8 24.4 19.0		W	At 100°C, Note 1 At 85°C, Note 4
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
P_{AH}	Auto Halt power at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V		1.9 3.6 7.0 8.2 10.1	W	At 50°C, Note 2
P_{QS}	Quick Start power at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V		1.7 3.2 6.5 7.6 8.9	W	At 50°C, Note 2
P_{DSLP}	Deep Sleep power at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V		1.6 2.4 4.8 5.6 6.8	W	At 35°C, Note 2
T_J	Junction Temperature For all processors except 1.33 GHz For 1.33 GHz processor only	0 0	100 85	°C	Note 3 Note 4

NOTES:

1. TDP is defined as the worst case power dissipated by the processor while executing publicly available software under normal operating conditions at nominal voltages that meet the load line specifications. The TDP number shown is a specification based on Icc (maximum) and indirectly tested by Icc (maximum) testing. TDP definition is synonymous with the Thermal Design Power (typical) specification referred to in previous Intel datasheets. The Intel TDP specification is a recommended design point and is not representative of the absolute maximum power the processor may dissipate under worst case conditions.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. T_J is measured with the on-die thermal diode.
4. T_J at 85°C only applies to 1.33 GHz processor. Intel recommends that the notebook thermal management system include full-speed fan activation at no higher than 55°C to provide adequate cooling.

6.1 Thermal Diode

The Mobile Intel Celeron Processor has an on-die thermal diode that should be used to monitor the die temperature (T_J). A thermal sensor located on the motherboard, or a stand-alone measurement kit, should monitor the die temperature of the processor for thermal management or instrumentation purposes. Table 49 and Table 50 provide the diode interface and specifications.

Note: The reading of the thermal sensor connected to the thermal diode will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Table 49. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	AF13	Thermal diode anode
THERMDC	AF14	Thermal diode cathode

Table 50. Thermal Diode Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
n	Diode Ideality Factor (5-150uA)	1.0011	1.0067	1.0122		Notes 1, 2, 3, 4, 6
n	Diode Ideality Factor (5-300uA)	1.0003	1.0091	1.0178		Notes 1, 2, 3, 5, 6

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. Characterized at 100°C.
3. Not 100% tested. Specified by design/characterization.
4. Specified for Forward Bias Current = 5 µA (min) and 150 µA (max).
5. Specified for Forward Bias Current = 5 µA (min) and 300 µA (max).
6. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation: Where I_s = saturation current, q = electronic charge, V_d = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

$$I_{FW} = I_S \cdot \left(e^{qV_D/nkT} - 1 \right)$$

7. Processor Initialization and Configuration

7.1 Description

The Mobile Intel Celeron Processor has some configuration options that are determined by hardware and some that are determined by software. The processor samples its hardware configuration at reset on the active-to-inactive transition of RESET#. The *P6 Family of Processors Developer's Manual* describes these configuration options. Some of the configuration options for the Mobile Intel Celeron Processor are described in the remainder of this section.

7.1.1 Quick Start Enable

Quick Start enabling is mandatory on the Mobile Intel Celeron Processor by strapping A15# low. When the STPCLK# signal is asserted it will enter the Quick Start state when A15# is sampled active on the RESET# signal's active-to-inactive transition. The Quick Start state supports snoops from the bus priority device but it does not support symmetric master snoops nor is the latching of interrupts supported. A "1" in bit position 5 of the Power-on Configuration register indicates that the Quick Start state has been enabled.

7.1.2 System Bus Frequency

The current generation Mobile Intel Celeron Processor will only function with a system bus frequency of 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processors will support both 100-MHz and 133-MHz bus frequencies. Bit positions 18 to 19 of the Power-on Configuration register indicates at which speed a processor will run.

7.1.3 APIC Enable

The processor APIC must be hardware enabled by pulling the PICD[1:0] signals separately up to 1.5 V and supplying an active PICCLK to the processor. Software can be used to disable the APIC if it is not being used, after PICD[1:0] are sampled high when RESET# is deasserted and the processor has started executing instructions.

7.2 Clock Frequencies and Ratios

The Mobile Intel Celeron Processor uses a clock design in which the bus clock is multiplied by a ratio to produce the processor's internal (or "core") clock. The ratio used is programmed into the processor during manufacturing. The bus ratio programmed into the processor is visible in bit positions 22 to 25 and 27 of the Power-on Configuration register. Table 28 shows the 5-bit codes in the Power-on Configuration register and their corresponding bus ratios.

8. Processor Interface

8.1 Alphabetical Signal Reference

A[35:3]# (I/O – AGTL)

The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal.

On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See *P6 Family of Processors Developer's Manual* for details.

A20M# (I - 1.5V Tolerant)

If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.

ADS# (I/O - AGTL)

The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

AERR# (I/O - AGTL)

The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction.

If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.

AP[1:0]# (I/O - AGTL)

The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals is low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.

BCLK, BCLK# (I)

The BCLK and BCLK# signals determines the system bus frequency.

On systems with Differential Clocking, both system bus agents must receive these signals to drive their outputs and latch their inputs on the BCLK rising edge and BCLK# falling edge. All external timing parameters are specified with respect to the crossing point of the BCLK rising edge and BCLK# falling edge.

On systems with Single Ended Clocking, both system bus agents must receive the BCLK signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal. The BCLK# signal functions as the CLKREF input.

BERR# (I/O - AGTL)

The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the Mobile Intel Celeron Processors do not observe assertions of the BERR# signal.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Asserted optionally by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

BINIT# (I/O - AGTL)

The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.

BNR# (I/O - AGTL)

The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.

BP[3:2]# (I/O - AGTL)

The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.

BPM[1:0]# (I/O - AGTL)

The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

BPRI# (I - AGTL)

The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.

BREQ0# (I/O - AGTL)

The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal.

During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#. Optionally, this signal may be grounded with a 10-ohm resistor.

BSEL[1:0] (O – 3.3V Tolerant)

The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. The chipset and system clock generator also uses the BSEL signals. The VTTPWRGD signal informs the processor to output the BSEL signals. During power up the BSEL signals will be indeterminate for a small period of time. The chipset and clock generator should not sample the BSEL signals until the VTTPWRGD signal is asserted. The assertion of the VTTPWRGD signal indicates that the BSEL signals are stable and driven to a final state by the processor. Please refer to Figure 15 for the timing relationship between the BSEL and VTTPWRGD signals.

Table 51 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the Mobile Intel Celeron Processor is 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processors will support both 100-MHz and 133-MHz bus frequencies. If another frequency is used then the processor is not guaranteed to function properly.

Table 51. BSEL[1:0] Encoding

BSEL[1:0]	System Bus Frequency
01	100 MHz
11	133 MHz

CLKREF (Analog)

The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal on platforms supporting Single Ended Clocking. This signal should be connected to a resistor divider to generate 1.25 V from the 2.5-V supply. A minimum of 1-µF decoupling capacitance is recommended on CLKREF. On systems with Differential Clocking, the CLKREF pin functions as the BCLK# input.

CMOSREF (Analog)

The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. CMOSREF must be generated from a stable 1.5V supply (830 chipset family), 2.5 V (440MX chipset family) and must meet the VCMOSREF specification. The same 1.5 V (830 chipset family) or 2.5 V (440MX chipset family) supply should be used to power the chipset CMOS I/O buffers that drive the CMOS signals. The Thevenin equivalent impedance of the VCMOSREF generation circuits must be less than 0.5 KΩ/1 KΩ (i.e., top resistor 500 Ω, bottom resistor 1 KΩ) for the Intel 830 Chipset family. The Thevenin equivalent impedance of the VCMOSREF generation circuits must be less than 0.75 KΩ/0.5 KΩ (i.e., top resistor 750 Ω, bottom resistor 500 Ω) for the Intel 440MX chipset family.

D[63:0]# (I/O - AGTL)

The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

DBSY# (I/O - AGTL)

The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

DEFER# (I - AGTL)

The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

DEP[7:0]# (I/O - AGTL)

The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.

DRDY# (I/O - AGTL)

The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

DPSLP# (I - 1.5 V Tolerant)

The DPSLP# (Deep Sleep) signal, when asserted in the Quick Start state, causes the processor to enter the Deep Sleep state. In order to return to the Quick Start state BCLK, BCLK# must be running and the DPSLP# pin must be deasserted.

EDGCTRLP (I-Analog)

The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the AGTL output buffers. Connect the signal to V_{SS} with a 110-Ω, 1% resistor.

FERR# (O - 1.5 V Tolerant Open-drain)

The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.

FLUSH# (I - 1.5 V Tolerant)

When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted.

On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

HIT# (I/O - AGTL), HITM# (I/O - AGTL)

The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

IERR# (O - 1.5 V Tolerant Open-drain)

The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.

IGNNE# (I - 1.5 V Tolerant)

The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.

INIT# (I - 1.5 V Tolerant)

The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input.

If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self-test (BIST).

INTR (I - 1.5 V Tolerant)

The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.

LINT[1:0] (I - 1.5 V Tolerant)

The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs.

Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.

LOCK# (I/O - AGTL)

The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.

NCTRL (I - Analog)

The NCTRL signal provides the AGTL pull down impedance control. The processor samples this input to determine the N-channel pull-down device strength when it is the driving agent. An external 14 ohm (1% tolerance) pull-up resistor to V_{CCT} is required for this signal. Please refer to platform design guide for implementation details.

NMI (I - 1.5 V Tolerant)

The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

PICCLK (I – 2.0 V Tolerant)

The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.

PICD[1:0] (I/O - 1.5 V Tolerant Open-drain)

The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled. For the Mobile Intel Celeron Processor, the APIC is required to be hardware enabled as described in Section 7.1.3.

PLL1, PLL2 (Analog)

The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.

PRDY# (O - AGTL)

The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.

PREQ# (I - 1.5 V Tolerant)

The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.

PWRGOOD (I – 1.8 V Tolerant)

PWRGOOD (Power Good) is a 1.8-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (V_{CC}, V_{CCT}, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (1.8 V) state. Figure 15 through Figure 17 illustrate the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 30 (Section 3.6) and be followed by a 1 ms RESET# pulse.

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

REQ[4:0]# (I/O - AGTL)

The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.

RESET# (I - AGTL)

Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 ms after V_{CC} and BCLK, BCLK# have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only AGTL signal that does not have on-die AGTL termination. A 56.2 Ω 1% terminating resistor connected to V_{CCT} is required.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *P6 Family of Processors Developer's Manual*.

Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.

RP# (I/O - AGTL)

The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals is low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

RS[2:0]# (I/O - AGTL)

The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

RSP# (I - AGTL)

The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

RTTIMPEDP (I-Analog)

The RTTIMPEDP (R_{TT} Impedance/PMOS) signal is used to configure the on-die AGTL termination. Connect the RTTIMPEDP signal to V_{SS} with a 56.2-Ω, 1% resistor.

SMI# (I - 1.5 V Tolerant)

The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

STPCLK# (I - 1.5 V Tolerant)

The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Quick Start state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Quick Start state. When STPCLK# is deasserted and other conditions in are met, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.

TCK (I - 1.5 V Tolerant)

The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

TDI (I - 1.5 V Tolerant)

The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.

TDO (O - 1.5 V Tolerant Open-drain)

The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.

TESTHI[2:1] (I - 1.25 V Tolerant)

The TESTHI[2:1] (Test input High) signals are used during processor test and need to be pulled high during normal operation.

TESTLO[2:1] (I - 1.5 V Tolerant)

The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.

THERMDA, THERMDC (Analog)

The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.

TMS (I - 1.5 V Tolerant)

The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.

TRDY# (I/O - AGTL)

The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.

TRST# (I - 1.5 V Tolerant)

The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The Mobile Intel Celeron Processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

VID[4:0] (O – Open-drain)

The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. Please refer to Section 3.2.3 for details.

VREF (Analog)

The VREF (AGTL Reference Voltage) signal provides a DC level reference voltage for the AGTL input buffers. A voltage divider should be used to divide V_{CCT} by $^{2}/_{3}$. Resistor values of 1.00 kΩ and 2.00 kΩ are recommended. Decouple the VREF signal with three 0.1-µF high-frequency capacitors close to the processor.

VTTPWRGD (I – 1.25 V)

The VTTPWRGD signal informs the processor to output the VID signals. During power up, the VID signals will be in an indeterminate state for a small period of time. The voltage regulator should not sample and/or latch the VID signals until the VTTPWRGD signal is asserted. The assertion of the VTTPWRGD signal indicates that the VID signals are stable and are driven to the final state by the processor. Please refer to Figure 15 for the power up sequence. (Also see Section 4.3.1.)

8.2 Signal Summaries

Table 52. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS	Always
BCLK	High	—	System Bus	Always
BCLK#	Low	—	System Bus	Always
BPRI#	Low	BCLK	System Bus	Always
DEFER#	Low	BCLK	System Bus	Always
FLUSH#	Low	Asynch	CMOS	Always
IGNNE#	Low	Asynch	CMOS	Always
INIT#	Low	Asynch	System Bus	Always
INTR	High	Asynch	CMOS	APIC disabled mode
LINT[1:0]	High	Asynch	APIC	APIC enabled mode
NMI	High	Asynch	CMOS	APIC disabled mode
NCTRL	High	Asynch		
PICCLK	High	—	APIC	Always
PREQ#	Low	Asynch	Implementation	Always
PWRGOOD	High	Asynch	Implementation	Always
RESET#	Low	BCLK	System Bus	Always
RSP#	Low	BCLK	System Bus	Always
SMI#	Low	Asynch	CMOS	Always
STPCLK#	Low	Asynch	Implementation	Always
TCK	High	—	JTAG	
TDI		TCK	JTAG	
TMS		TCK	JTAG	
TRST#	Low	Asynch	JTAG	
VTTPWRGD	High	Asynch	Power/Other	

Table 53. Output Signals

Name	Active Level	Clock	Signal Group
BSEL[1:0]	High	Asynch	Open-drain
FERR#	Low	Asynch	Open-drain
IERR#	Low	Asynch	Open-drain
PRDY#	Low	BCLK	Implementation
TDO	High	TCK	JTAG
VID[4:0]	High	Asynch	Power/Other

Table 54. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	System Bus	ADS#, ADS#+1
ADS#	Low	BCLK	System Bus	Always
AP[1:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
BREQ0#	Low	BCLK	System Bus	Always
BP[3:2]#	Low	BCLK	System Bus	Always
BPM[1:0]#	Low	BCLK	System Bus	Always
D[63:0]#	Low	BCLK	System Bus	DRDY#
DBSY#	Low	BCLK	System Bus	Always
DEP[7:0]#	Low	BCLK	System Bus	DRDY#
DRDY#	Low	BCLK	System Bus	Always
LOCK#	Low	BCLK	System Bus	Always
REQ[4:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
RP#	Low	BCLK	System Bus	ADS#, ADS#+1
RS[2:0]#	Low	BCLK	System Bus	Always
TRDY#	Low	BCLK	System Bus	Response phase

Table 55. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	System Bus	ADS#+3
BERR#	Low	BCLK	System Bus	Always
BINIT#	Low	BCLK	System Bus	Always
BNR#	Low	BCLK	System Bus	Always
HIT#	Low	BCLK	System Bus	Always
HITM#	Low	BCLK	System Bus	Always
PICD[1:0]	High	PICCLK	APIC	Always

Appendix A. PLL RLC Filter Specification

A1. Introduction

All Mobile Intel Celeron Processors have internal PLL clock generators, which are analog in nature and require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). The PLL RLC filter specifications for the Mobile Intel Celeron Processor are the same as those for the mobile Intel Pentium III Processor-M. The general desired topology is shown in Figure 2. Excluded from the external circuitry are parasitics associated with each component.

A2. Filter Specification

The function of the filter is two fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter.

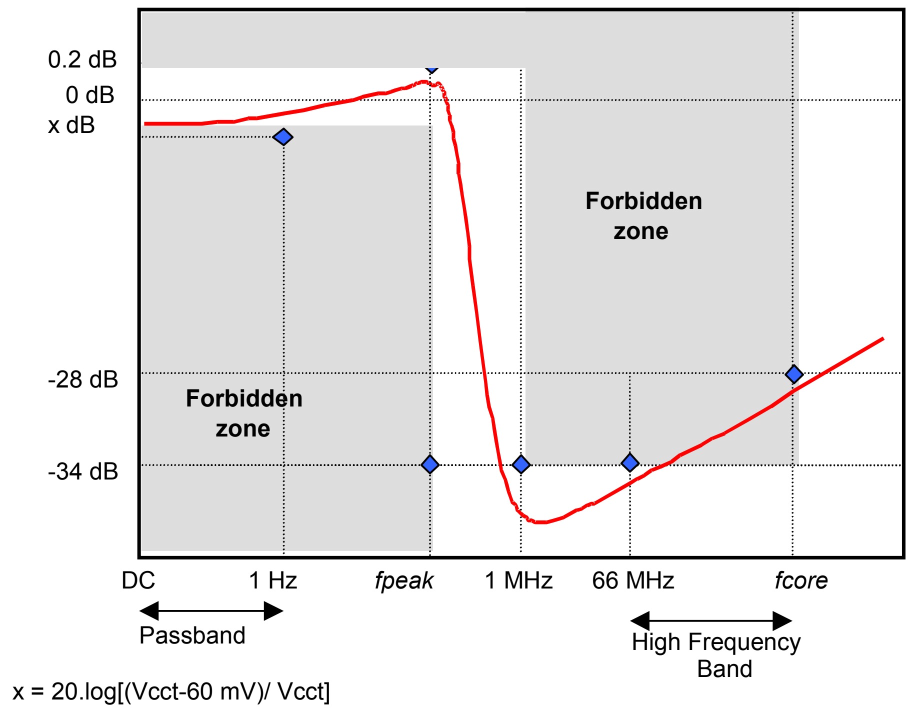
The AC low-pass specification, with input at V_{CCT} and output measured across the capacitor, is as follows:

- < 0.2-dB gain in pass band
- < 0.5-dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34-dB attenuation from 1 MHz to 66 MHz
- 28-dB attenuation from 66 MHz to core frequency
- The filter specification (AC) is graphically shown in Figure 32.

Other requirements:

- Use a shielded type inductor to minimize magnetic pickup
- The filter should support a DC current of at least 30 mA
- The DC voltage drop from V_{CCT} to PLL1 should be less than 60 mV, which in practice implies series resistance of less than 2 Ω. This also means that the pass band (from DC to 1 Hz) attenuation below 0.43 dB for V_{CCT} = 1.25 V.

Figure 32. PLL Filter Specifications



NOTES:
Diagram is not to scale
No specification for frequencies beyond fcore.
Fpeak, if existent, should be less than 0.05 MHz.

A3. Recommendation for Mobile Systems

The following LC components are recommended. The tables will be updated as other suitable components and specifications are identified.

Table 56. PLL Filter Inductor Recommendations

Inductor	Part Number	Value	Tol	SRF	Rated I	DCR	Min Damping R Needed
L1	TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1Ω max)	0Ω
L2	Murata LQG21N4R7K10	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (+/-50%)	0 Ω
L3	Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max	0.2 Ω (assumed)

NOTE: Minimum damping resistance is calculated from 0.35 Ω – DCR_{min}. From vendor provided data, L1 and L2 DCR_{min} is 0.4Ω and 0.5Ω respectively, qualifying them for zero required trace resistance. DCR_{min} for L3 is not known and is assumed to be 0.15Ω. Products with equivalent specifications may also be used.

Table 57. PLL Filter Capacitor Recommendations

Capacitor	Part Number	Value	Tolerance	ESL	ESR
C1	Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
C2	AVX TPSD336M020S0200	33 µF	20%	unknown	0.2 Ω

Table 58. PLL Filter Resistor Recommendations

Resistor	Part Number	Value	Tolerance	Power
R1	Various	1Ω	10%	1/16W

To satisfy damping requirements, total series resistance in the filter (from V_{CCT} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9 Ω, which precludes using L2 and possibly L1.

Other routing requirements include:

- The capacitor should be close to the PLL1 and PLL2 pins, with less than 0.1 Ω per route (These routes do not count towards the minimum damping resistance requirement).
- The PLL2 route should be parallel and next to the PLL1 route (minimize loop area).
- The inductor should be close to the capacitor; any routing resistance should be inserted between VCCT and the inductor.
- Any discrete resistor should be inserted between V_{CCT} and the inductor.

A4. Comments

- A magnetically shielded inductor protects the circuit from picking up external flux noise. This should provide better timing margins than with an unshielded inductor.
- A discrete or routed resistor is required because the LC filter by nature has an under-damped response, which can cause resonance at the LC pole. Noise amplification at this band, although not in the PLL-sensitive spectrum, could cause a fatal headroom reduction for analog circuitry. The resistor serves to dampen the response. Systems with tight space constraints should consider a discrete resistor to provide the required damping resistance. Too large of a damping resistance can cause a large IR drop, which means less analog headroom and lower frequency.
- Ceramic capacitors have very high self-resonance frequencies, but they are not available in large capacitance values. A high self-resonant frequency coupled with low ESL/ESR is crucial for sufficient rejection in the PLL and high frequency band. The recommended tantalum capacitors have acceptably low ESR and ESL.
- The capacitor must be close to the PLL1 and PLL2 pins; otherwise the value of the low ESR tantalum capacitor is wasted. Note the distance constraint should be translated from the 0.1-Ω requirement.