

< IGBT MODULES >

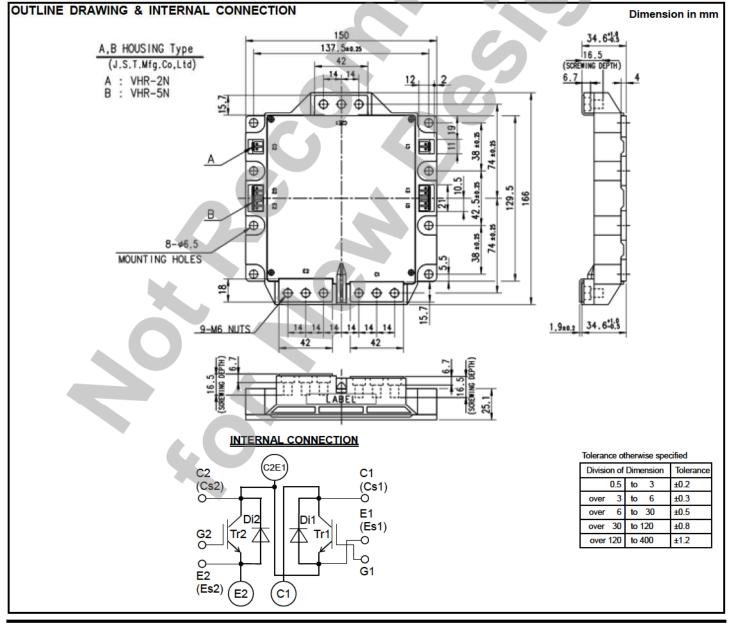
CM900DUC-24NF

HIGH POWER SWITCHING USE **INSULATED TYPE**

	Collector current I _C 900 A
	Collector-emitter voltage V _{CES} 1 2 0 0 V
	Maximum junction temperature Tjmax 150 °C
	•Flat base Type
. 000 000	•Copper base plate (non-plating)
	RoHS Directive compliant
0	Recognized under UL1557, File E323585
Dual switch (Half-Bridge)	

APPLICATION

Wind power, Photovoltaic (Solar) power, AC Motor Control, Motion/Servo Control, Power supply, etc.



MAXIMUM RATINGS (Tj=25 °C, unless otherwise specified)

Symbol	Item	Conditions	Rating	Unit
V _{CES}	Collector-emitter voltage	G-E short-circuited	1200	V
V _{GES}	Gate-emitter voltage	C-E short-circuited	± 20	V
Ic	Collector current	DC, T _C =96 °C ^(Note2, 4)	900	А
ICRM		Pulse, Repetitive (Note3)	1800	
Ptot	Total power dissipation	T _C =25 °C (Note2, 4)	5950	W
IE (Note1)	Emitter current	DC (Note2)	900	А
I _{ERM} (Note1)		Pulse, Repetitive (Note3)	1800	~
Visol	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	2500	V
Tj	Junction temperature	-	-40 ~ +150	°C
Tstg	Storage temperature	(Note7)	-40 ~ +125	

ELECTRICAL CHARACTERISTICS (Ti=25 °C, unless otherwise specified)

Symbol	Item	Conditions			Limits		
Symbol		Conditions		Min.	Тур.	Max.	Unit
I _{CES}	Collector-emitter cut-off current	V _{CE} =V _{CES} , G-E short-circuited		-	-	1.0	mA
I _{GES}	Gate-emitter leakage current	V _{GE} =V _{GES} , C-E short-circuited			-	1.0	μA
$V_{GE(th)}$	Gate-emitter threshold voltage	I _c =90 mA, V _{CE} =10 V		6	7	8	V
	Collector opittor acturation voltage	I _C =900 A, V _{GE} =15 ∨ ^(Note5)	T _j =25 °C		1.8	2.5	v
V _{CEsat}	Collector-emitter saturation voltage	Refer to the figure of test circuit	T _j =125 °C		2.0	-	v
Cies	Input capacitance			-	-	140	
Coes	Output capacitance	V _{CE} =10 V, G-E short-circuited		-	-	16	nF
Cres	Reverse transfer capacitance			-	-	3.0	1
Q _G	Gate charge	V _{cc} =600 V, I _c =900 A, V _{GE} =15 V		-	4800	-	nC
t _{d(on)}	Turn-on delay time			-	-	600	
t,	Rise time	− V _{CC} =600 V, I _C =900 A, V _{GE} =±15 V,		-	-	200	1
t _{d(off)}	Turn-off delay time			-	-	800	ns
t _f	Fall time	R_{g} =0.35 Ω , Inductive load		-	-	300	1
V _{EC} ^(Note.1) Emitter-collector voltage	Emittar collector voltage	I _E =900 A, G-E short-circuited,	T _j =25 °C	-	2.5	3.2	v
V EC	Emitter-collector voltage	Refer to the figure of test circuit (Note5)	T _j =125 °C	-	2.1	-	× ·
t _{rr} ^(Note1)	Reverse recovery time	V _{cc} =600 V, I _E =900 A, V _{GE} =±15 V,		-	-	500	ns
Q _{rr} (Note1)	Reverse recovery charge	$R_{G}=0.35 \Omega$, Inductive load		-	50	-	μC
Eon	Turn-on switching energy per pulse	V _{cc} =600 V, I _c =I _E =900 A,		-	147.5	-	<u> </u>
E _{off}	Turn-off switching energy per pulse	V _{GE} =±15 V, R _G =0.35 Ω, T _i =125 °C,		-	88	-	mJ
Err (Note1)	Reverse recovery energy per pulse	Inductive load		-	91.8	-	mJ
R _{CC'+EE'}	Internal lead resistance	Main terminals-chip, per switch, T _c =25 °C ^(Note4)		-	0.286	-	mΩ
rg	Internal gate resistance	Per switch		-	1.0	-	Ω
4							

THERMAL RESISTANCE CHARACTERISTICS

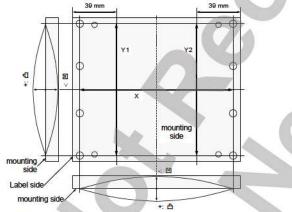
Symbol Item		Que dition o	Limits			1 horis
	Conditions	Min.	Typ.	Max.	Unit	
R _{th(j-c)Q}	Thermal resistance	Junction to case, per Inverter IGBT (Note4)	(2)	-	21	K/kW
R _{th(j-c)D}		Junction to case, per Inverter DIODE (Note4)	1.5		34	
R _{th(c-s)}	Contact thermal resistance	Case to heat sink, per 1/2 module, Thermal grease applied (Note4, 6)	-	12	71	K/kW

MECHANICAL CHARACTERISTICS

Symbol Item	Itom	Conditions	Limits			Linit
	Conditions	Min.	Тур.	Max.	Unit	
Mt	- Mounting torque	Main terminals M 6 screw	3.5	4.0	4.5	N∙m
Ms		Mounting to heat sink M 6 screw	3.5	4.0	4.5	N∙m
d _s Creepage distance	Terminal to terminal	24	-	-		
	Creepage distance	Terminal to base plate	33		-	mm
d		Terminal to terminal	14	-	-	mm
d _a Clearance	Terminal to base plate	33	-	-	mm	
m	mass	-	-	1450	-	g
ec	Flatness of base plate	On the centerline X, Y1, Y2 (Note8)	-50	-	+100	μm

Note1. Represent ratings and characteristics of the anti-parallel, emitter-collector free wheeling diode (DIODE).

- 2. Junction temperature (T_j) should not increase beyond T_{jmax} rating.
- 3. Pulse width and repetition rate should be such that the device junction temperature (T_j) dose not exceed T_{jmax} rating.
- 4. Case temperature (T_c) and heat sink temperature (T_s) are defined on the each surface (mounting side) of base plate and heat sink just under the chips. Refer to the figure of chip location.
- The heat sink thermal resistance should measure just under the chips.
- 5. Pulse width and repetition rate should be such as to cause negligible temperature rise. Refer to the figure of test circuit.
- 6. Typical value is measured by using thermally conductive grease of λ =0.9 W/(m·K).
- 7: The operation temperature is restrained by the permission temperature of female connector housing.
- 8. Base plate (mounting side) flatness measurement points (X, Y1 and Y2) are as follows of the following figure.

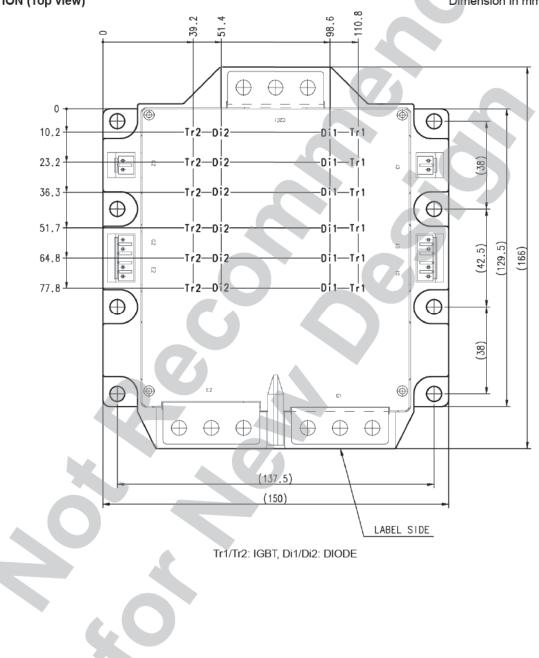


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RECOMMENDED OPERATING CONDITIONS

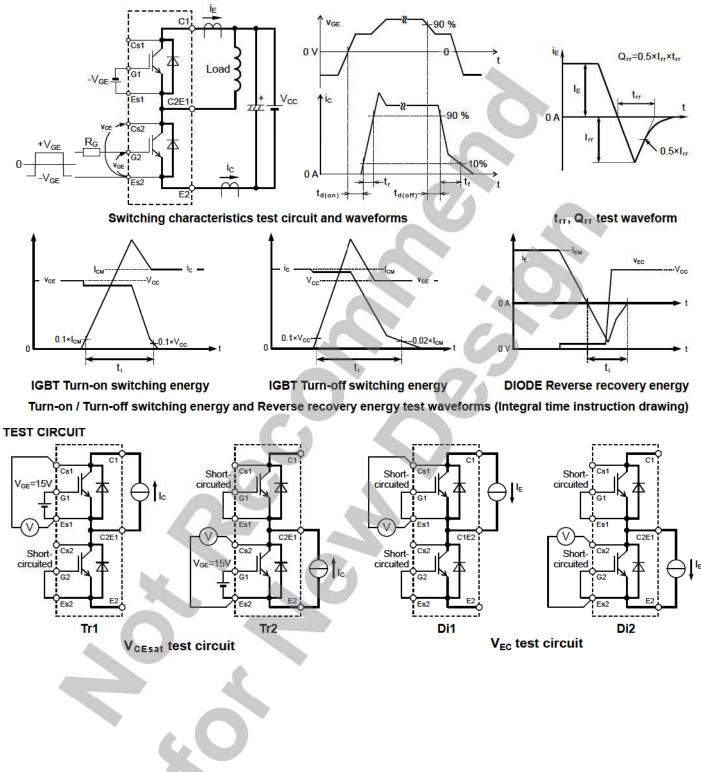
Symbol Item	Itom	Conditions	Limits			Unit
	Conditions	Min.	Тур.	Max.	Unit	
Vcc	(DC) Supply voltage	Applied across C1-E2 terminals	-	600	800	V
V _{GEon}	Gate (-emitter drive) voltage	Applied across G1-Es1/G2-Es2 terminals	13.5	15.0	16.5	V
R _G	External gate resistance	Per switch	0.35	-	2.2	Ω

CHIP LOCATION (Top view)

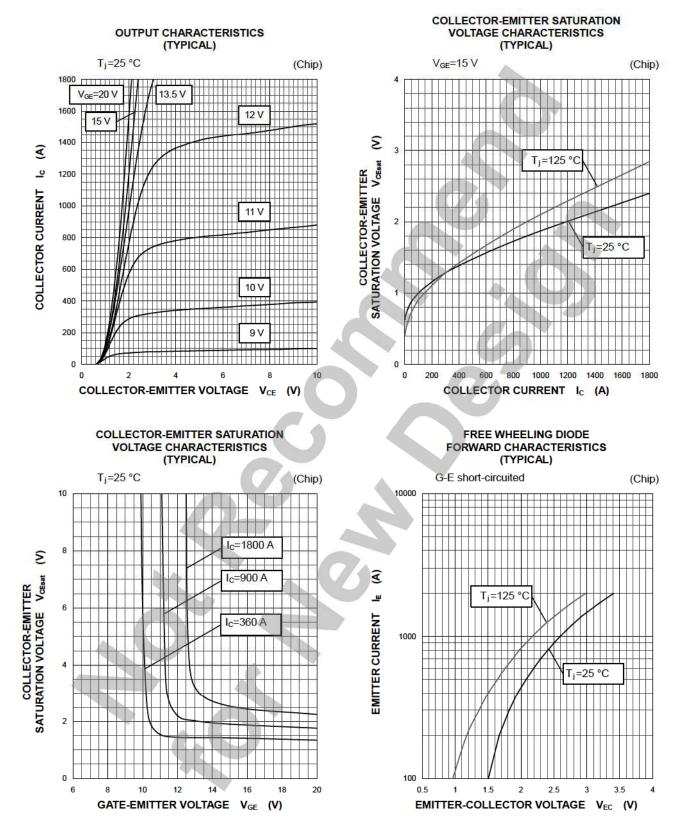


Dimension in mm, tolerance: ±1 mm

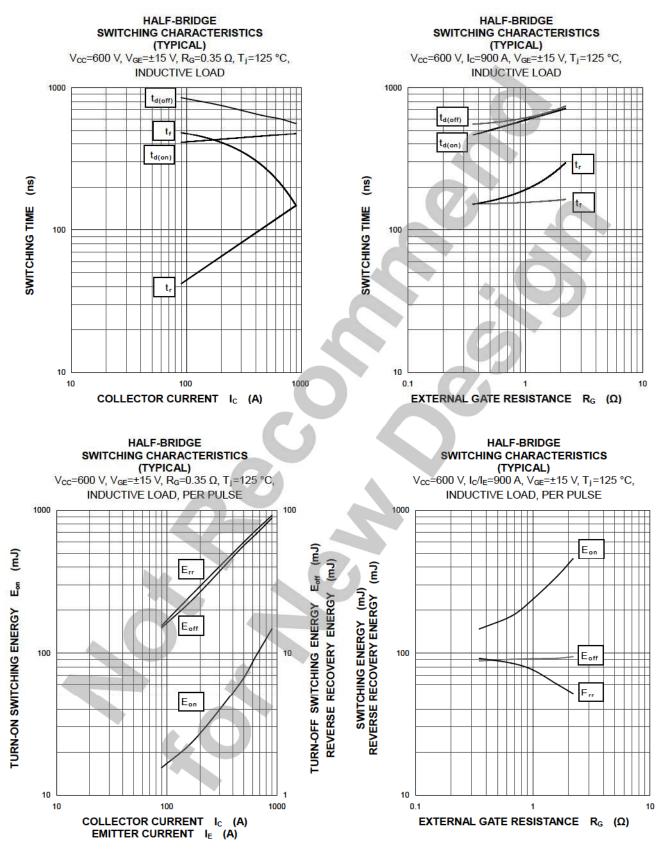




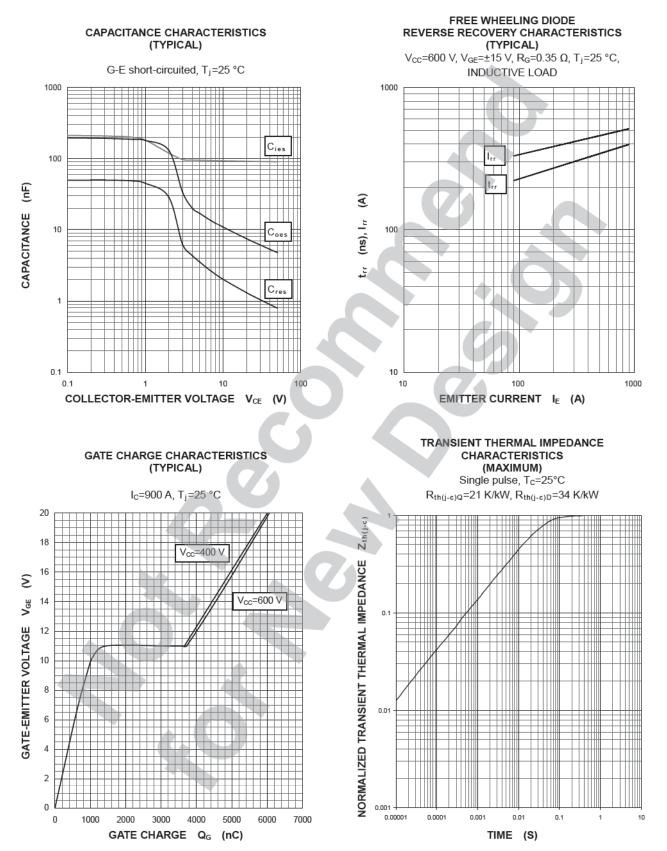
PERFORMANCE CURVES



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PERFORMANCE CURVES



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