Preferred Device

Power MOSFET 12 Amps, 100 Volts

P-Channel TO-220

This Power MOSFET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

Features

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Pb–Free Package is Available*

MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Rating	Symbol	Value	Unit		
Drain-Source Voltage	V _{DSS}	100	Vdc		
Drain–Gate Voltage (R_{GS} = 1.0 M Ω)	V _{DGR}	100	Vdc		
Gate–Source Voltage – Continuous – Non–repetitive ($t_p \le 50 \ \mu$ s)	V _{GS} V _{GSM}	±20 ±40	Vdc Vpk		
Drain Current – Continuous – Pulsed	I _D I _{DM}	12 28	Adc		
Total Power Dissipation Derate above 25°C	P _D	75 0.6	W W/°C		
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C		
Thermal Resistance – Junction–to–Case – Junction–to–Ambient	$R_{ heta JC} \ R_{ heta JA}$	1.67 62.5	°C/W		
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	ΤL	260	°C		

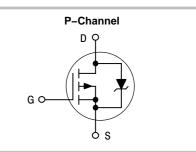
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

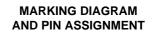


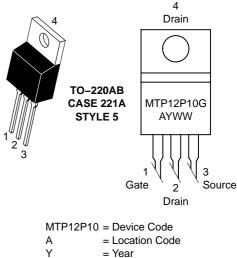
ON Semiconductor®

http://onsemi.com

12 AMPERES, 100 VOLTS R_{DS(on)} = 300 mΩ







Y	= Year
WW	= Work Week
G	= Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping
MTP12P10	TO-220AB	50 Units/Rail
MTP12P10G	TO-220AB (Pb-Free)	50 Units/Rail

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

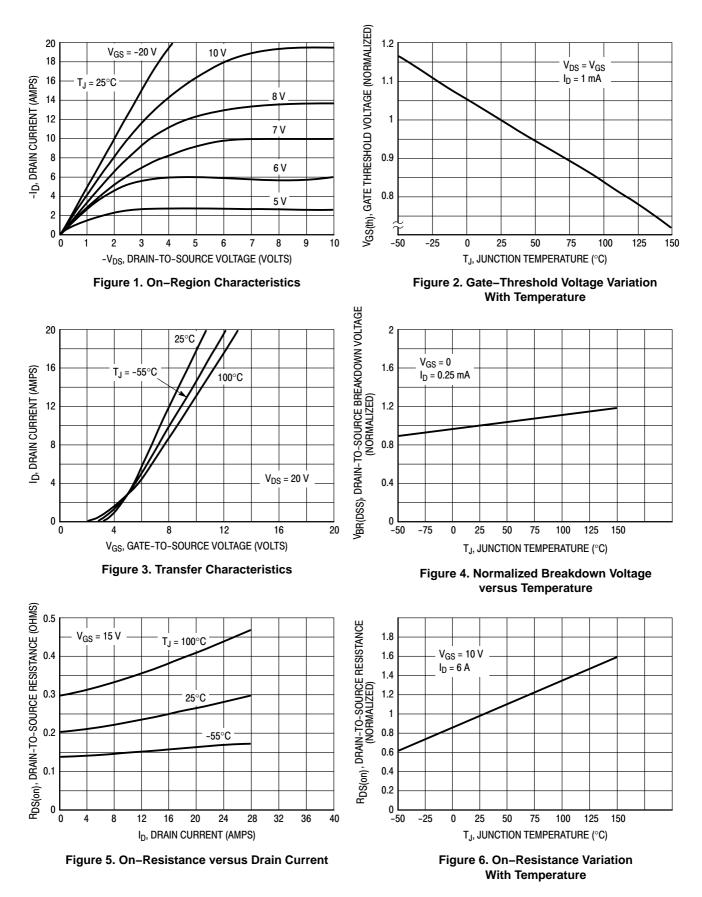
Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

	Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			.		
Drain-Source Breakdown Voltage (\	$I_{\rm GS} = 0, \ {\rm I}_{\rm D} = 0.25 \ {\rm mA})$	V _{(BR)DSS}	100	_	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125^{\circ}C)$		I _{DSS}		10 100	μAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)		I _{GSSF}	-	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)		I _{GSSR}	-	100	nAdc
ON CHARACTERISTICS (Note 1)					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0 mA) T_J = 100°C		V _{GS(th)}	2.0 1.5	4.5 4.0	Vdc
Static Drain–Source On–Resistance	$(V_{GS} = 10 \text{ Vdc}, I_D = 6.0 \text{ Adc})$	R _{DS(on)}	-	0.3	Ω
$ Drain-Source On-Voltage (V_{GS} = 10 V) \\ (I_D = 12 \text{ Adc}) \\ (I_D = 6.0 \text{ Adc}, T_J = 100^{\circ}\text{C}) $		V _{DS(on)}		4.2 3.8	Vdc
Forward Transconductance ($V_{DS} = 2$	15 V, I _D = 6.0 A)	9 _{FS}	2.0	_	mhos
DYNAMIC CHARACTERISTICS			· ·		<u> </u>
Input Capacitance		C _{iss}	-	920	pF
Output Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz) See Figure 10	C _{oss}	-	575	1
Reverse Transfer Capacitance		C _{rss}	-	200	
SWITCHING CHARACTERISTICS (Note 1) (T _J = 100°C)				
Turn-On Delay Time		t _{d(on)}	-	50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, \text{ I}_{D} = 0.5 \text{ Rated I}_{D}, \text{ R}_{G} = 50 \Omega)$	t _r	-	150	-
Turn-Off Delay Time	See Figures 12 and 13	t _{d(off)}	-	150	
Fall Time		t _f	-	150	
Total Gate Charge		Qg	33 (Тур)	50	nC
Gate-Source Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS}, I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V})$ See Figure 11	Q _{gs}	16 (Typ)	_	-
Gate-Drain Charge		Q _{gd}	17 (Тур)	_	
SOURCE-DRAIN DIODE CHARAC	TERISTICS (Note 1)				-
Forward On–Voltage		V _{SD}	4.0 (Typ)	5.5	Vdc
Forward Turn–On Time	$(I_{\rm S} = \text{Rated } I_{\rm D}, V_{\rm GS} = 0)$	t _{on}	Limited by stray inductance		uctance
Reverse Recovery Time	(1S - 1Xaled ID, VGS - 0)	t _{rr}	300 (Typ)	-	ns
INTERNAL PACKAGE INDUCTANO	CE (TO-204)				
Internal Drain Inductance, (Measure source pin and the center of the die)	d from the contact screw on the header closer to the	L _d	5.0 (Typ)	-	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _s	12.5 (Тур)	_	
INTERNAL PACKAGE INDUCTANO	CE (TO-220)		,		
Internal Drain Inductance (Measured from the contact screw o (Measured from the drain lead 0.25"		L _d	3.5 (Typ) 4.5 (Typ)	- -	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)		Ls	7.5 (Тур)	-	1

1. Pulse Test: Pulse Width \leq 300 $\mu s,$ Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS



SAFE OPERATING AREA INFORMATION

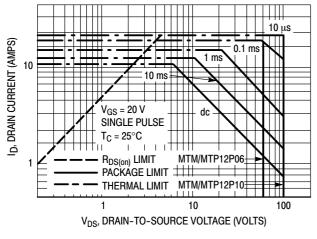
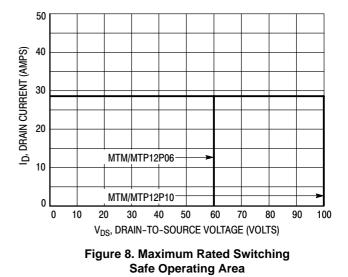


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

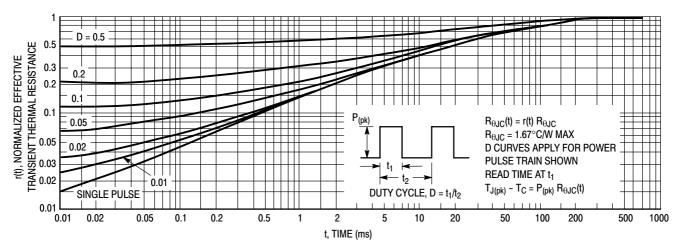
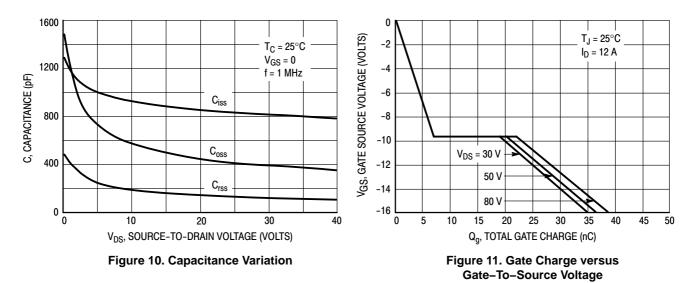
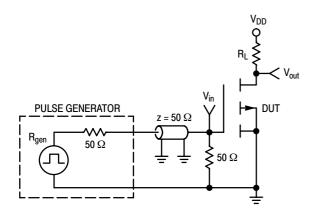


Figure 9. Thermal Response



RESISTIVE SWITCHING





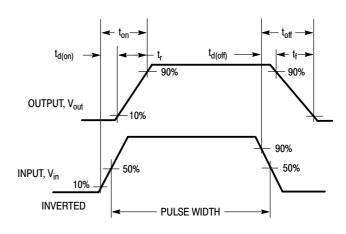


Figure 13. Switching Waveforms

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